AN938
Application note

Designing with L4973, 3.5 A high efficiency DC-DC converter

Introduction

The L4973 family is a 3.5 A monolithic DC-DC converter in step-down topology operating in continuous mode. It uses BCD60 II technology and is available in two plastic packages, power DIP18 (12+3+3) and SO20 (12+4+4).

Two versions of the device are available. The L4973V3.3 sets the output voltage without any voltage divider at 3.3 V and the L4973V5.1 at 5.1 V.

Both the regulators can control higher output voltage values by using an external voltage divider.

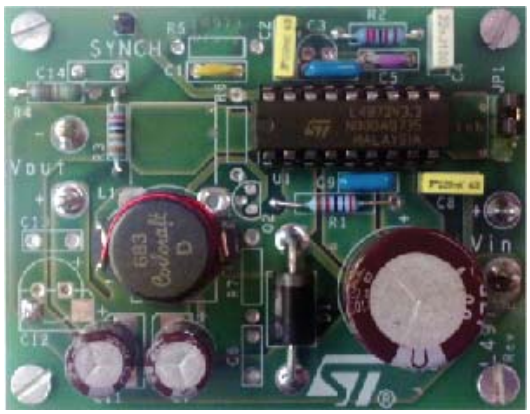
The operating input supply voltage ranges from 8 V to 55 V, while the absolute value with no load is 60 V.

New internal design solutions and superior technological performance have allowed us to develop and produce a device with improved efficiency in all operating conditions and with fewer external components.

While internal current limiting and thermal shutdown are today considered standard protection functions mandatory for a safe load supply, an oscillator with voltage feed-forward improves line regulation and overall control loop. The soft-start function does not allow output overvoltages at turn-on, and the synchronization function can reduce EMI problems in multi-output power supplies. The inhibit function, introduced for power management in equipment having standby features, when active (high), reduces device power consumption by a few tens of µA.

A demonstration board for the L4973 is available through order code EVAL4973 (see *Figure 1*).

Figure 1. EVAL4973 demonstration board



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1 Description

For a better understanding of the device and operation, a short description of the main building blocks is given in *Figure 2* and *3* with packaging options and complete block diagram.

Figure 2. Pin out - power DIP18 and SO20 packages

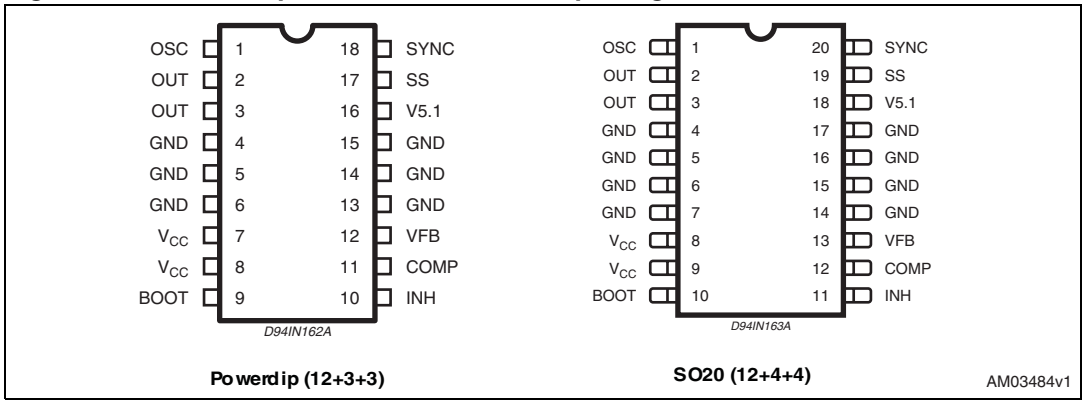
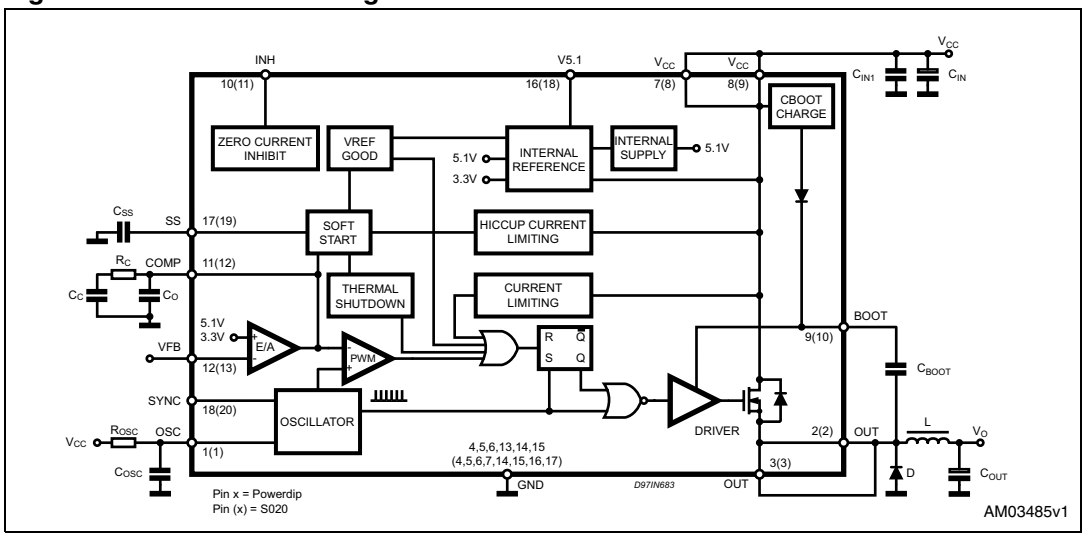


Figure 3. Device block diagram



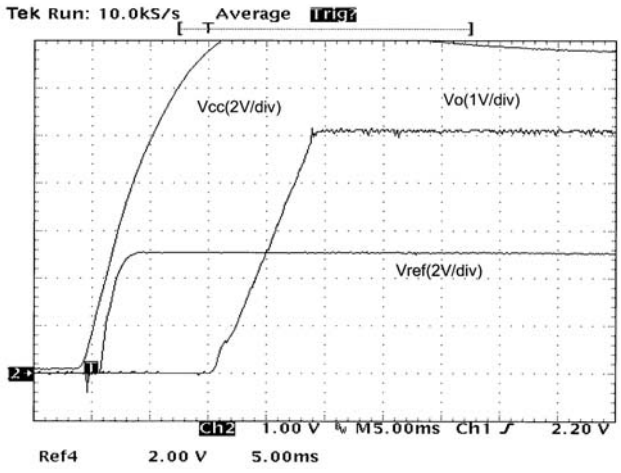
2 Power supply, UVLO and voltage reference

The device is provided with an internal stabilized power supply (of about 12 V typ.) that powers the analog and digital control blocks and the bootstrap section.

Moreover, a safe turn-on sequence is guaranteed by an internal UVLO.

When the supply voltage reaches about 3.8 V, the band gap goes into regulation, while the internal 5.1 V reference starts to increase from zero to its nominal value.

Figure 4. Turn-on sequence



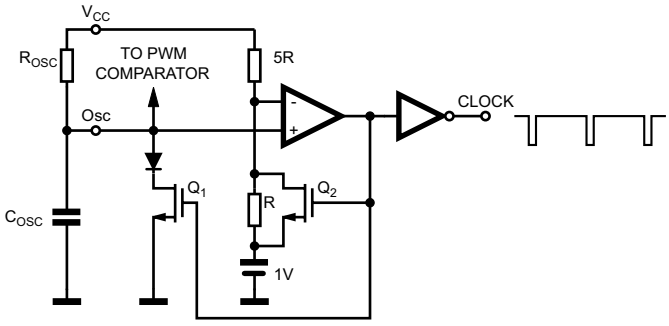
At 6.5 V of V_{CC}, the device begins charging the soft-start capacitor and the power stage generates the first PWM pulses.

The output voltage increases with a slope controlled by the soft-start time. *Figure 4* shows the turn-on sequence of the signals.

From the 12 V pre-regulator, a stable 5.1 V ±2% reference voltage, externally available, is generated, with 10 mA of current capability.

This reference is available on both devices, while the feedback reference is 5.1 V for the L4973V5.1 and 3.3 V for the L4973V3.3.

Figure 5. Oscillator internal circuit



2.1 Oscillator, sync and voltage feed-forward

One pin implements the oscillator function with inherent voltage feed-forward. A second pin is dedicated to in/out synchronization.

A resistor R_{osc} and a capacitor C_{osc}, connected as shown in *Figure 5*, allow the setting of the desired switching frequency given in *Equation 1*:

Equation 1

$$F_{SW} = \frac{1}{(R_{osc} \cdot C_{osc}) \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

where F_{sw} is in kHz, R_{osc} in kΩ and C_{osc} in nF.

The oscillator capacitor C_{osc} is discharged by an internal mos transistor of 100 Ω of $R_{DS(on)}$ (Q1) and during this period the internal threshold is set at 1 V by a second mos, Q2. When the oscillator voltage capacitor reaches the 1 V threshold, the output comparator turns off mos Q1 and turns on mos Q2, charging the external capacitor C_{osc}. The oscillator block, shown in *Figure 5*, generates a sawtooth wave signal that sets the switching frequency of the system.

This signal, compared with the output of the error amplifier, generates the PWM signal that modulates the conduction time of the power output stage.

The design of the oscillator implements the voltage feed-forward function without any additional external components.

Figure 6. Device switching frequency vs. R_{osc} and C_{osc}

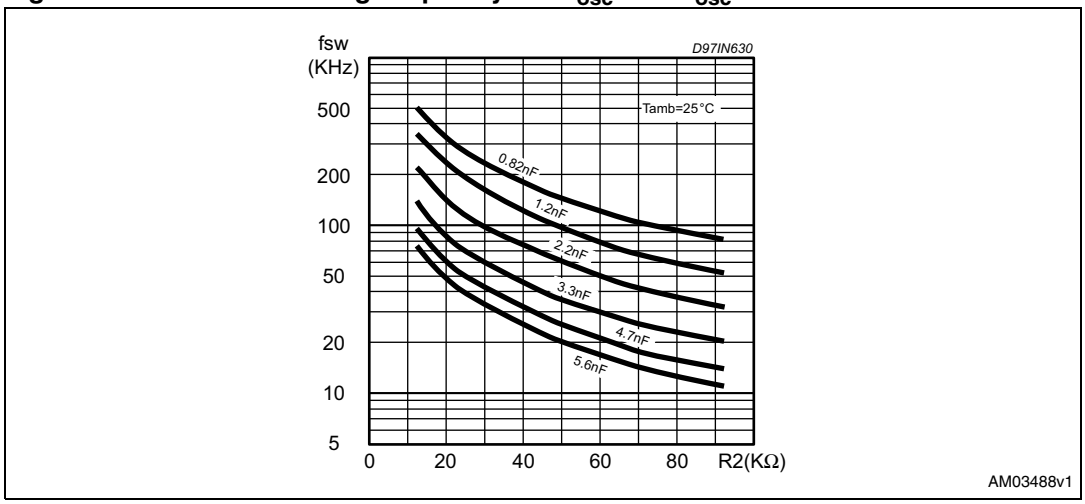
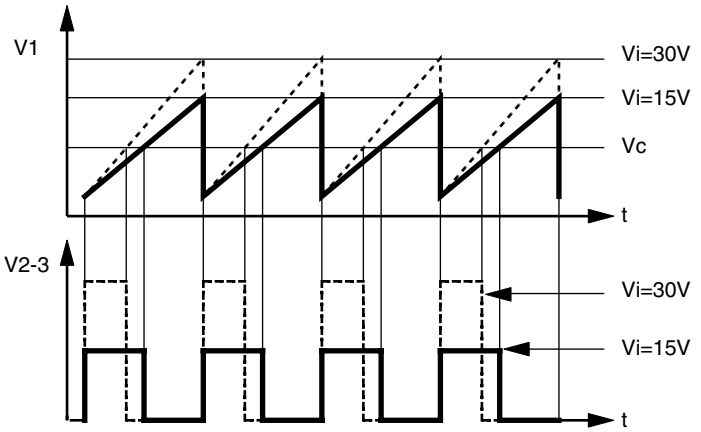


Figure 7. Voltage feed-forward function.



The oscillator peak-to-valley voltage is proportional to the supply voltage, and the voltage feed-forward is operative from 8 V to 55 V of input supply.

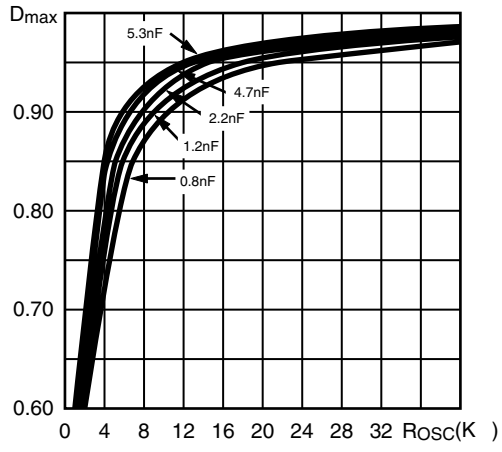
Equation 2

$$\Delta V_{osc} = \frac{V_{CC} - 1}{6}$$

Also the $\Delta V/\Delta t$ of the sawtooth is directly proportional to the supply voltage. As V_{cc} increases, the T_{on} time of the power transistor decreases in such a way to provide to the choke, and finally also the load, the product volt. x sec. as a constant.

Figure 8 shows how the duty cycle varies as a result of the change on the $\Delta V/\Delta t$ of the sawtooth with V_{cc}. The output of the error amplifier doesn't change to maintain the output voltage constant and in regulation. With this function on the board, the output response time is greatly reduced in presence of an abrupt change on the supply voltage, and the output ripple voltage at the mains frequency is greatly reduced too.

Figure 8. Maximum duty cycle vs. R_{osc} and C_{osc} as parameter



In fact, the slope of the ramp is modulated by the input ripple voltage, generally present in the order of some tenths of a volt, for both offline and DC-DC converters using mains transformers.

The charge and discharge time is approximately equal to:

Equation 3

$$Tch = R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right)$$

$$Tdis = 100 \cdot C_{osc}$$

The maximum duty cycle is a function of Tch, Tdis and an internal delay and is represented by the equation below:

Equation 4

$$Dmax = \frac{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) - 80 \cdot 10^{-9}}{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

which is represented in *Figure 9*.

Figure 9. Vo-Io output characteristics - hiccup protection limits output power

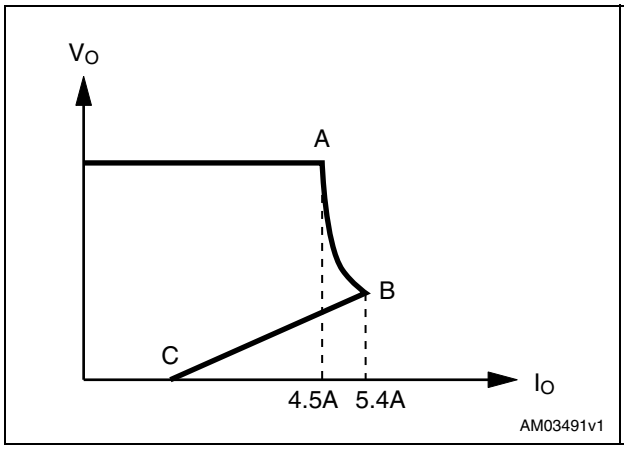
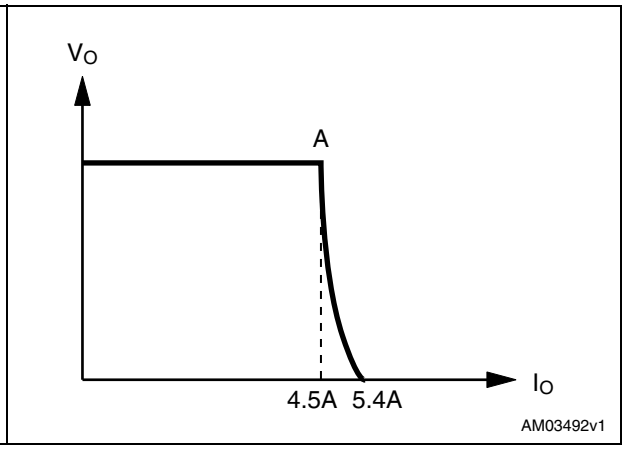


Figure 10. Vo-Io output characteristics - effective pulse-by-pulse protection



2.2 Current protection

The L4973 has two current limiting functions: pulse-by-pulse and hiccup modes.

Increasing the output current to the pulse-by-pulse current limiting threshold (Ith1 typ. value of 4.5 A), the controller reduces the on-time to the value of T_B = 300 ns (the blanking time at which the current limiting protection does not trigger). This minimum time is necessary to avoid undesirable intervention of the protection due to the spike current generated during the recovery time of the freewheeling diode.

In this condition, because of the fixed blanking time, the output current is given by:

Equation 5

$$I_{max} = \frac{[V_{CC} \cdot T_B \cdot F_{SW} - V_f \cdot (1 - T_B \cdot F_{SW})]}{[R_O + (R_D + R_L)(1 - T_B \cdot F_{SW}) + (R_{dson} + R_L)T_B \cdot F_{SW}]}$$

where R_o is the load resistance and V_f is the diode forward voltage. R_D and R_L are the series resistance of, respectively, the freewheeling diode and the choke.

Typical output characteristics are given in *Figure 9* and *10*. In *Figure 10*, the pulse-by-pulse protection is effective in limiting the output current.

In *Figure 9* the pulse-by-pulse protection is no longer effective in limiting the current due to the minimum T_{on} fixed by the blanking time T_B, and the hiccup protection intervenes because the output peak current reaches the relative threshold.

Figure 11. Schematic of internal current limiting

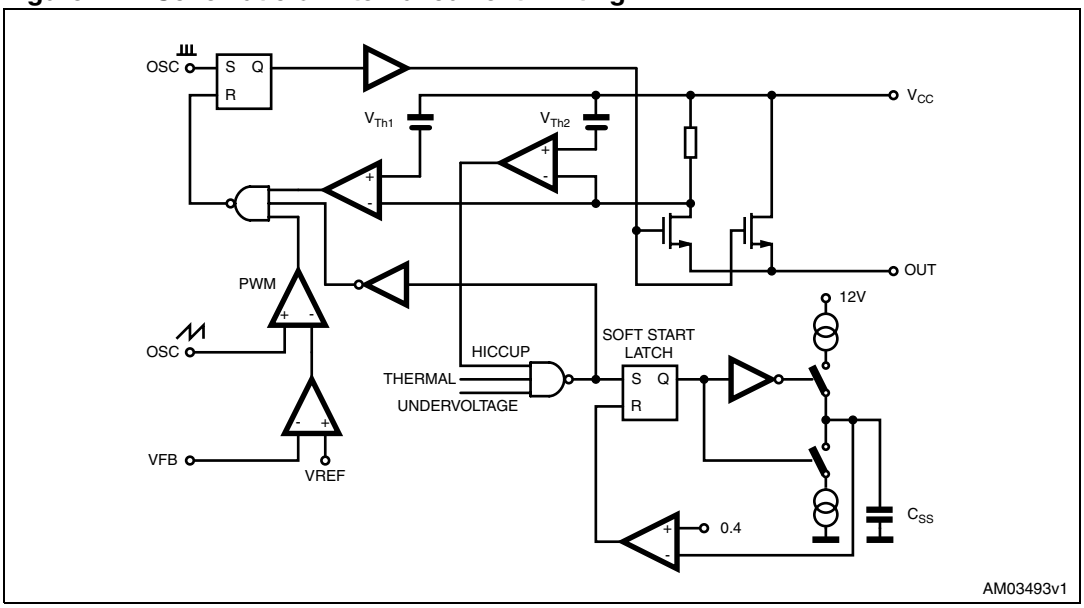
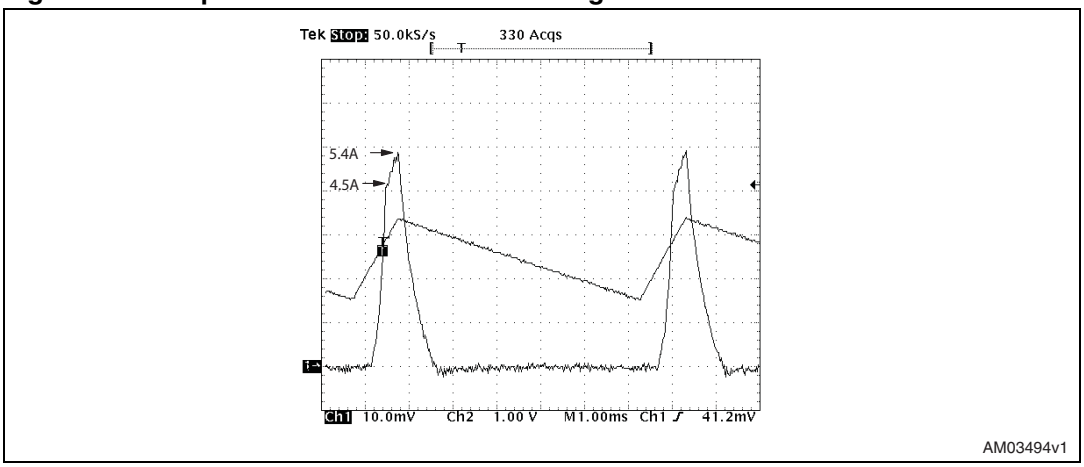


Figure 12. Output current and soft-start voltage



In the pulse-by-pulse intervention (point A) the output voltage drops because of the T_{on} reduction, and the current is almost constant. However, in short-circuit, the current is only limited by the series resistances R_D and R_L (see relation above) and could reach the hiccup threshold (point B), set 20% higher than the pulse-by-pulse. Once the hiccup mode current protection is triggered the output current decreases dramatically at very low values (point C) even in short-circuit.

Figure 11 shows the internal current limiting circuitry. Vth1 is the pulse-by-pulse while Vth2 is the hiccup threshold.

The sense resistor is in series with a small mos implemented as a partition of the main DMOS.

The Vth2 comparator (20% higher than Vth1) sets the soft-start latch, initializing the discharge of the soft-start capacitor at constant current (about 22 µA).

When the valley comparator reaches about 0.4V, it resets the soft-start latch, restarting a new soft-start recharging cycle.

Figure 12 shows the typical waveforms of the current in the output inductor and the soft-start voltage (pin 17).

During the recharging of the soft-start capacitor, T_{on} increases gradually and, if the short-circuit is still present, when $T_{on}>T_B$ and the output peak current reaches the threshold, the hiccup protection intervenes again. So, the value of the soft-start capacitor must not be too high (in this case Ton increases slowly thus taking more time to reach the T_B value) in order to avoid that during the soft-start slope the current exceeds the limit before activation of the protection.

Figure 13 and *14* show the maximum allowed soft-start capacitor value as a function of the input voltage, inductor value and switching frequency.

A minimum value of the soft-start capacitance is necessary to guarantee, in short-circuit, the functionality of the current limiting circuitry. In fact, with an insufficient capacitor, the frequency of the current peaks (see *Figure 11*) is high and the mean current value in short-circuit increases.

Figure 13. Maximum soft-start capacitance with f_{SW} = 100 kHz

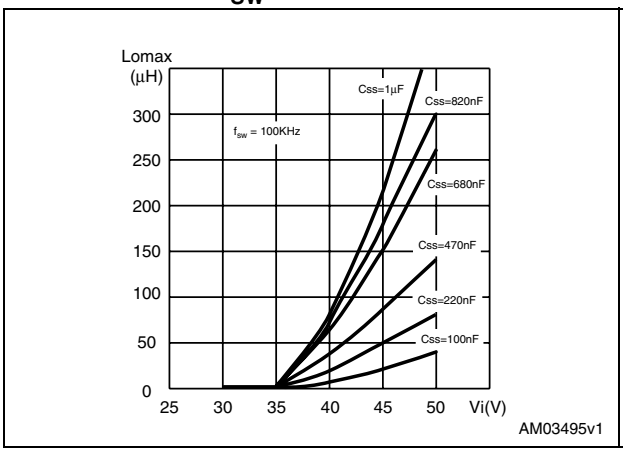
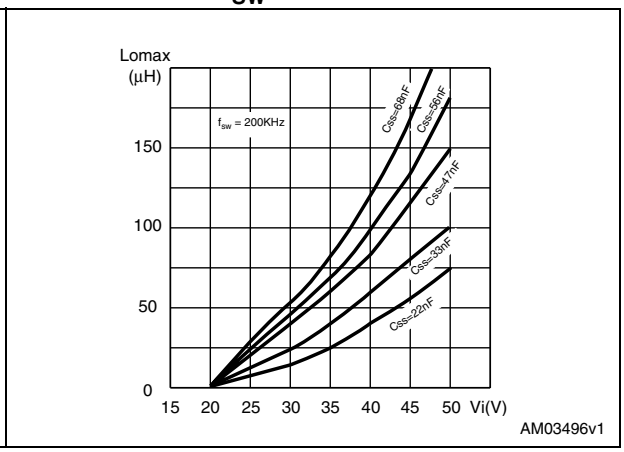
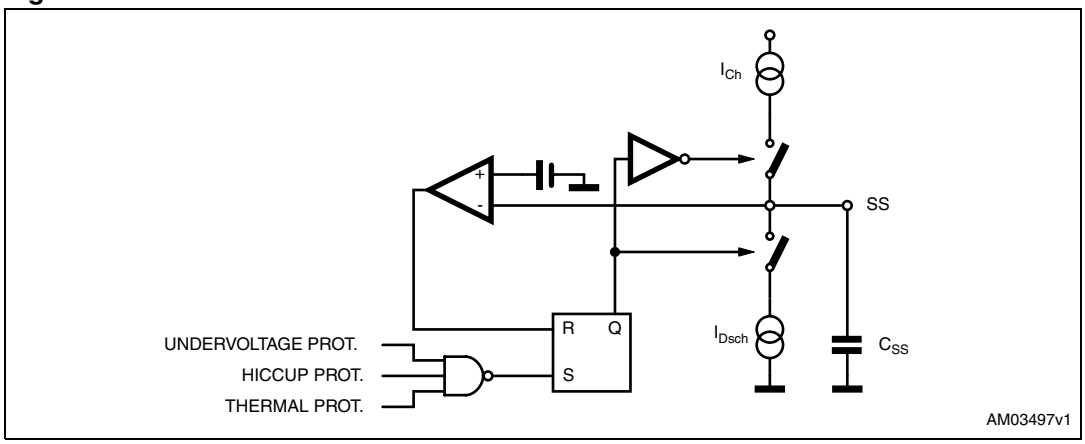


Figure 14. Maximum soft-start capacitance with f_{SW} = 200 kHz



Example: For a maximum V_{cc} of 50 V, at 100 kHz, with an inductor of 140 µH, it is possible to use a soft-start capacitor lower than 470 µF (see *Figure 13*). With such a value, the soft-start time (see *Figure 16*) is about 10 ms for an output voltage of 5 V.

Figure 15. Soft-start internal circuit



2.3 Soft-start

The soft-start function is needed to generate a correct startup of the system without overstressing the power stage, avoiding the intervention of current limiting, and having an output voltage rising smoothly without output overshoots.

The soft-start circuit is shown in *Figure 15*. The soft-start capacitor is charged at 40 µA, and quickly discharged at power-off and in case of thermal shutdown intervention.

The output startup time is calculated using the following formula:

Equation 6

$$Tss = \frac{v_o}{i_{CH} \cdot 6 \cdot D_{max}} \cdot Css$$

where D_{max} is 0.95.

The soft-start time versus output voltage and Css is shown in *Figure 16*. Thanks to the voltage feed-forward the startup time is not affected by the input voltage. *Figure 17* shows the output voltage startup using different soft-start capacitance values.

Figure 16. Soft-start time vs. V_o and Css

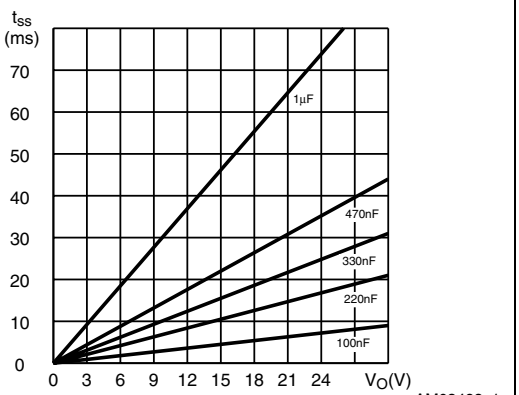
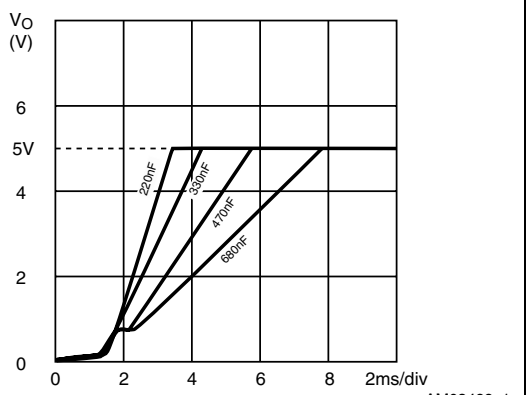


Figure 17. Output rising voltage with Css 680 nF, 470 nF, 330 nF, 220 nF



2.4 Feedback disconnection

In case of feedback disconnection, the duty cycle increases to the maximum allowed value, bringing the output voltage close to the input supply. This condition could destroy the load. To avoid this dangerous condition, the device forces a little current (1.4 µA typical) out of pin 12 (E/A feedback).

If the feedback is disconnected and the impedance at pin 12 is higher than 3.5 MΩ, the voltage at this pin goes higher than the reference voltage of the error amplifier, disabling the embedded power device.

2.5 Zero load

In normal operation, the output regulation is also guaranteed because the bootstrap capacitor is recharged, cycle by cycle, by means of the energy flowing into the choke. Under light load, this topology tends to operate in burst mode, with random repetition rate of the bursts. An internal new function makes this device capable of keeping the output voltage in full regulation with 1 mA of load current only.

Embedded circuitry keeps the output voltage regulated up to 8% above the nominal value at light load (0.5 mA < Iout < 1 mA):

- an internal comparator senses the voltage across the bootstrap capacitor. When this voltage drops below 5 V, it enables the embedded power element for about 300 nsec, recharging the bootstrap capacitor.
- the OVP protection disables the power element when the output voltage is 8% higher than nominal output (see *Section 2.6*).

When the load current is lower than 500 µA, which is also the current consumption of the boostrap section, the output voltage regulaton becomes critical.

A bleeding resistor is suggested to keep the output voltage voltage regulated regardless of the load ($I_{BLEEDING}$ > 0.5 mA).

2.6 Output overvoltage protection (OVP)

The overvoltage protection uses an embedded comparator that monitors the voltage of the FB voltage.

As the reference of the OVP comparator is 8% higher than that of the error amplifier, the protection is triggered when the output voltage is:

Equation 7

$$V_{OVP} = 1.08 \cdot V_{fB} \cdot \frac{(Ra + Rb)}{Rb}$$

where Ra, Rb represent the voltage divider to set the nominal output voltage.

2.7 Power stage

The embedded power element is an N-channel DMOS transistor with a Vdss in excess of 60 V and typ $R_{DS(on)}$ of 150 mΩ (measured at the device pins).

The low $R_{DS(on)}$ value of the power power element minimizes the conduction losses.

2.8 Turn-on

The gate driver circuitry of the L4973D implements solutions to minimize the switching losses.

This is typically done by increasing the rise time of the switching node in order to reduce the crossing losses.

The reverse recovery charge of the external diode (Qrr) which is proportional to the current slew rate does not make it convenient to increase the di/dt in the embedded power element over 100 A/µsec. In fact the extra current at turn-on decreases system efficiency/reliability and increases EMI.

Figure 18. Turn-on and turn-off (pin 2, 3)

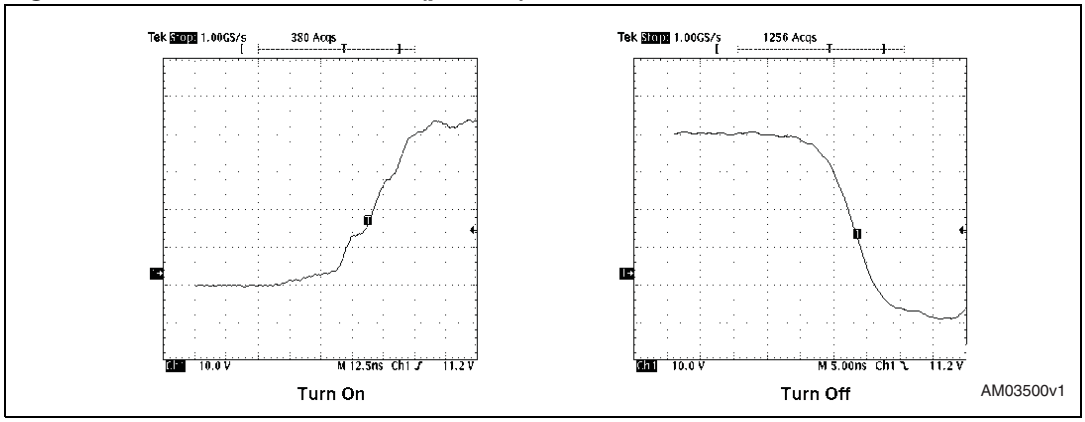
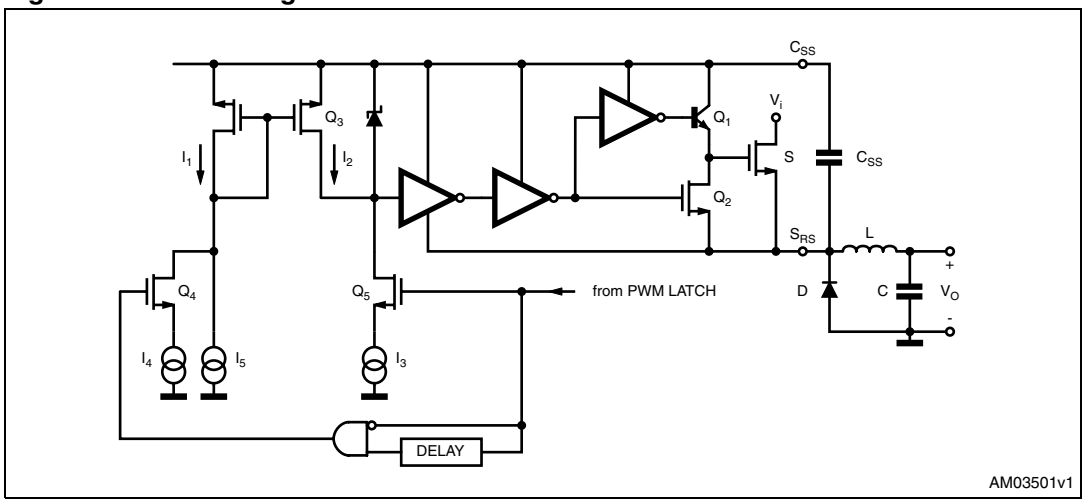


Figure 19. Power stage internal circuit



The L4973 has been developed with a special focus on this dynamic area.

An innovative and proprietary gate driver with two different timings has been introduced.

When the diode reverse voltage reaches about 3 V, the gate is sourced with low current (see *Figure 18*) to assure the complete recovery of the diode without generating unwanted extra peak currents and noise.

After this threshold, the gate drive current is quickly increased, producing a fast rise time to reach a high efficiency.

Figure 20. Sync and oscillator waveforms as slave and as master

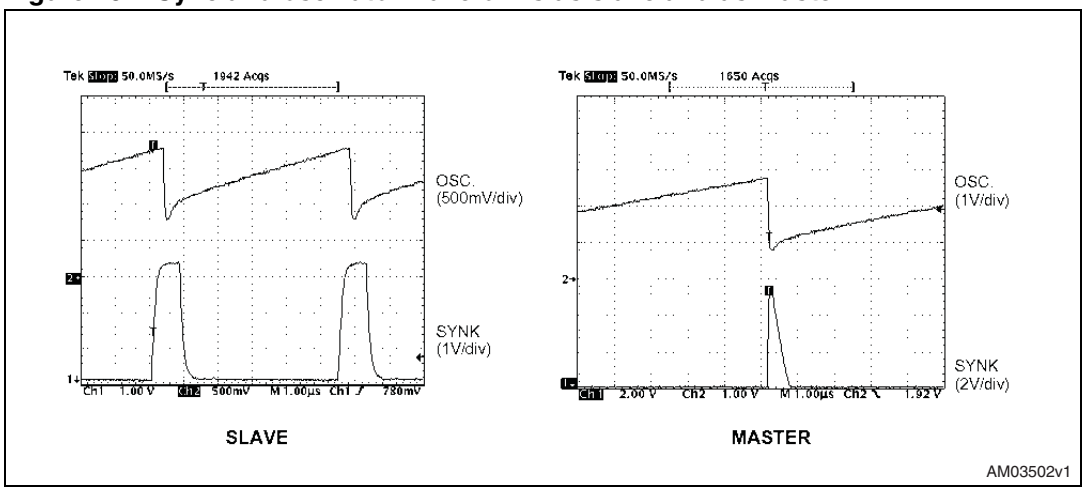
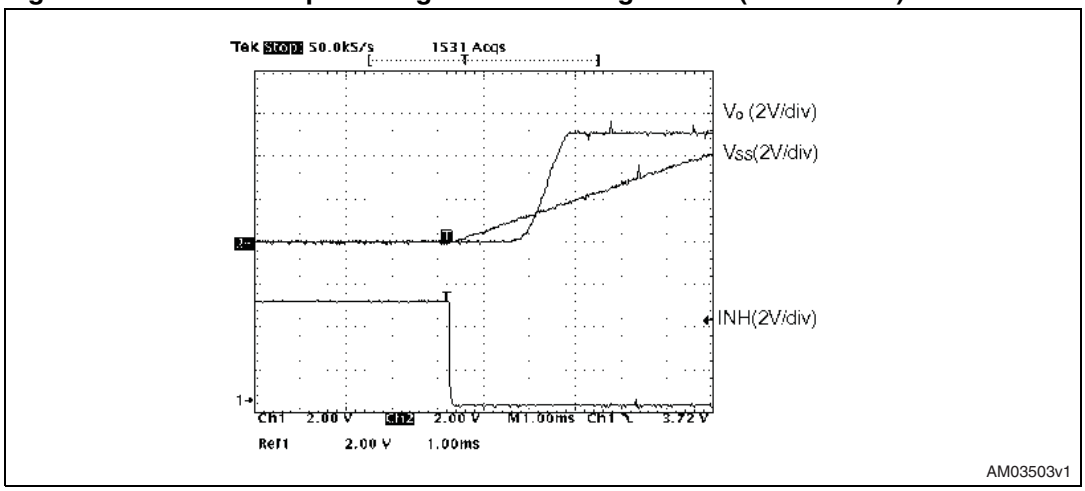


Figure 21. Re-start output voltage when inhibit goes low (Css = 56 nF)



2.9 Turn-off

The turn-off behavior is shown in *Figure 18*.

Figure 19 shows the details of the internal power stage and driver. The request for turn-off of the power switch S occurs at Q2.

2.9.1 Synchronization function

The device is able to synchronize other L4973 devices (up to 6).

Moreover, this function has been implemented to allow the device to operate as a master or slave.

As a master, it's able to source a current of 3 mA min at 4.5 V min. As a slave, it requires a maximum current of 0.45 mA and a minimum pulse width of about 350 ns.
Figure 20 shows the typical synchronization waveforms when the device is used as slave and as master.

2.9.2 Inhibit function

The inhibit pin is active high. An internal current source ties this pin to V_{CC} in case of disconnection, disabling the device.

In disabled state, Vinh = 5 V, the device quickly discharges the soft-start capacitor, also switches off the reference voltage which limits the power consumption to a leakage value only (at 24 V, about 100 µA).

Figure 21 shows the device behavior when the inhibit pin goes low. The soft-start capacitor is linearly recharged, and the output voltage rises until the nominal value.

3 Typical application

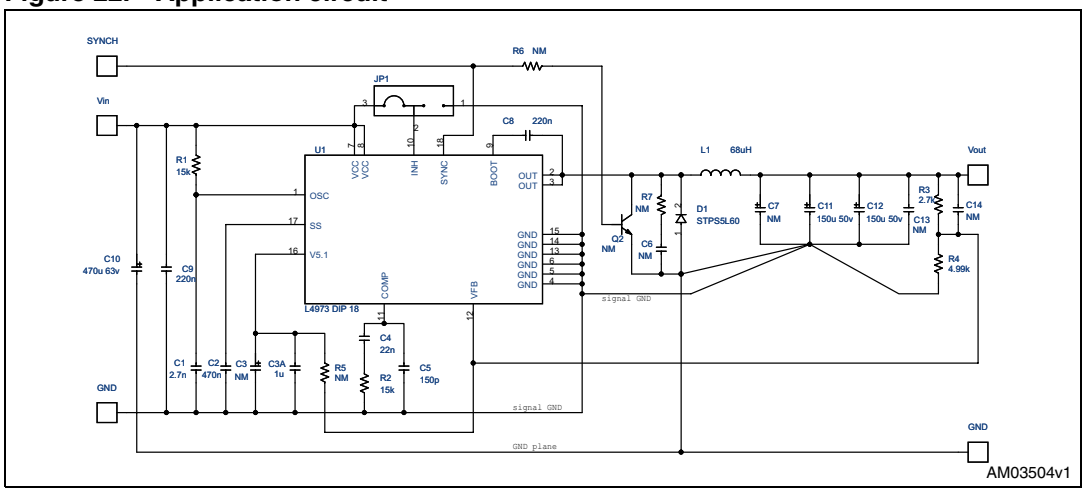
Figure 22 shows the schematic of the L4973 demonstration board.

The selection of the external components allows the device to operate in the entire input voltage range 8 V < V_{IN} < 55 V. The output voltage is limited by the voltage rating of the output capacitor so it can be adjusted in the range 3.3 V < V_{OUT} < 30 V through the voltage divider R3, R4. The input and output capacitors are able to sustain the RMS current in the operating range.

3.1 Electrical specification

- Input voltage range: 8 V - 55 V
- Output voltage: 5.1 V ±3% (line, load and thermal)
- Output ripple: 51 mV
- Output current range: 1 mA - 3.5 A
- Max output ripple current: 30% Iomax
- Current limit: 4.5 A
- Switching frequency: 150 kHz.

Figure 22. Application circuit



3.2 Input capacitor

The input capacitor has to be able to support the maximum input operating voltage of the device and the maximum RMS input current. The input current is squared and the quality of these capacitors has to be very high to minimize its power dissipation generated by the internal ESR, improving the system reliability. Moreover, input capacitors also affect the system efficiency.

The maximum I_{rms} current flowing through the input capacitors is:

Equation 8

$$I_{rms} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle and Io the output DC current.

This function reaches the maximum value at D = 0.5 and the equivalent RMS current is equal to Io/2. The following diagram *Figure 23* is the graphical representation of *Equation 8* with an estimated efficiency of 85% at different output currents.

The maximum and minimum duty cycles are:

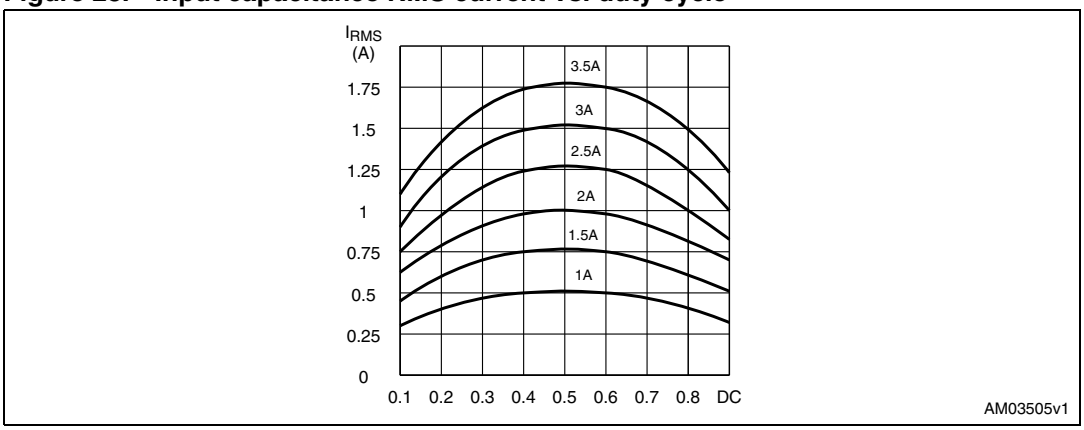
Equation 9

$$D_{max} = \frac{V_O + V_f}{V_{ccmin} + V_f} = 0.66 \qquad D_{max} = \frac{V_O + V_f}{V_{ccmax} + V_f} = 0.1$$

where V_f is the freewheeling diode forward voltage. This formula does not take into account the power MOSFET $R_{DS(on)}$, and considers negligible the inherent voltage drop, with respect to input and output voltages. At full load, 3.5 A, and D=0.5, the RMS capacitor current to be sustained is 1.75 A.

The selected 470 µF/63 V KY, guaranteeing a lifetime of 10000 hours at an ambient temperature of 105°C and switching frequency of 100 kHz, can support 2.3 A RMS current.

Figure 23. Input capacitance RMS current vs. duty cycle



3.3 Output voltage selection

The two available devices can directly regulate the output voltage of 3.3 V for the L4973V3.3 and 5.1 V for the L4973V5.1. Each of the two devices can regulate an output voltage higher than the nominal value, up to 40 V, by adding an external voltage divider.

In case of requested output voltage lower than 3.3 V, it is possible to use the L4973V3.3 with the external connections as shown in *Figure 24* with the function below plotted in *Figure 25*.

Equation 10

$$V_o = V_{fb} - (V_{ref} - V_{fb}) \cdot \frac{R3}{R5}$$

Figure 24. Example of output regulated voltage lower than 3.3 V

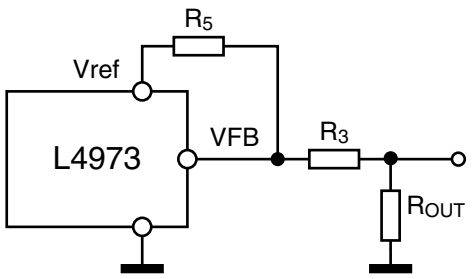
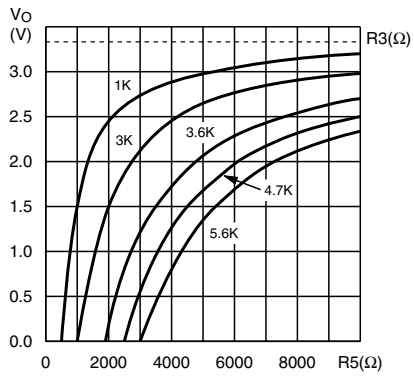


Figure 25. Output voltage vs. R5 using R3 as parameter



Only two resistors are used and no curve intercepts 3.3 V, but all curves have an asymptotic trend to this value.

3.4 Inductor selection

The criteria used in fixing the inductor value have been dictated by the desired output ripple voltage, 50 mV max., performance obtained of course in combination with output capacitors too.

The inductor ripple current, fixed at 30% of Iomax, i.e., 1.05 A, requires an inductor value of:

Equation 11

$$L_O = V_O \cdot \frac{(1 - D_{min})}{\Delta I_L \cdot f_{sw}}$$

It is possible to plot *Equation 11* as a function of Vo and V_{ccmax} at 150 kHz and 200 kHz (see *Figure 26*, *27*).

Figure 26. Ideal inductor value requested for 30% ripple current, as a function of max. input voltage and output (f_{SW}=150 kHz)

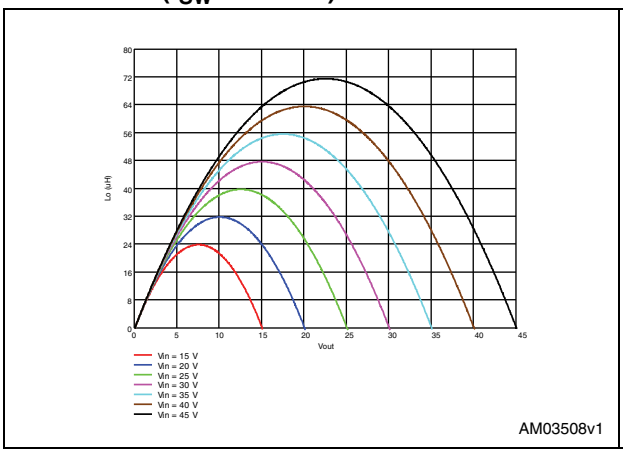
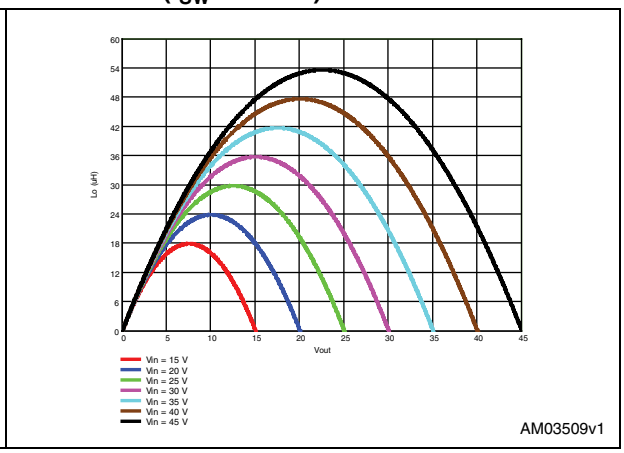


Figure 27. Ideal inductor value requested for 30% ripple current, as a function of max. input voltage and output (f_{SW}=200 kHz)



The 68 µH value of the selected inductor is useful to keep the current ripple below 0.3*I_{LOAD} over the input / output voltage range.

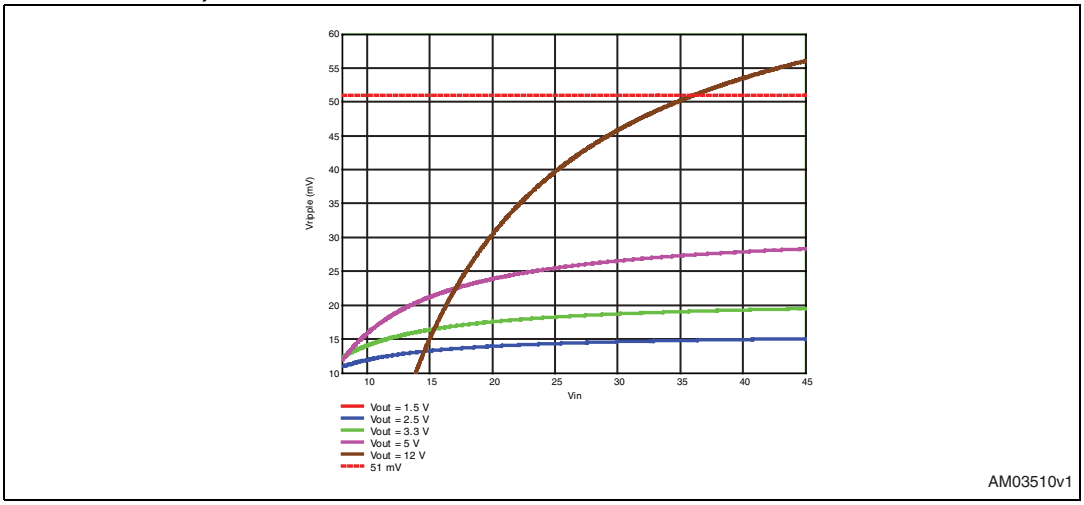
3.5 Output capacitors

The output capacitors selection, Co, is mainly driven by the output ripple voltage that has to be guaranteed, in this case 1% max. of Vo.

The output ripple is defined by the ESR of Co and by the ripple current flowing through it.

The chosen total capacitance is 2 x 150 µF/35 V KY (Nippon Chemi-con), each of which has an ESR of 150 mΩ at 20°C. The ideal ripple voltage over the input voltage range is shown in *Figure 28*.

Figure 28. Ideal ripple voltage as a function of input and output voltage (f_{SW}=150 kHz)



Co also has to support load transients. An idea of the magnitude of the output voltage drop during load transients is given below:

Equation 12

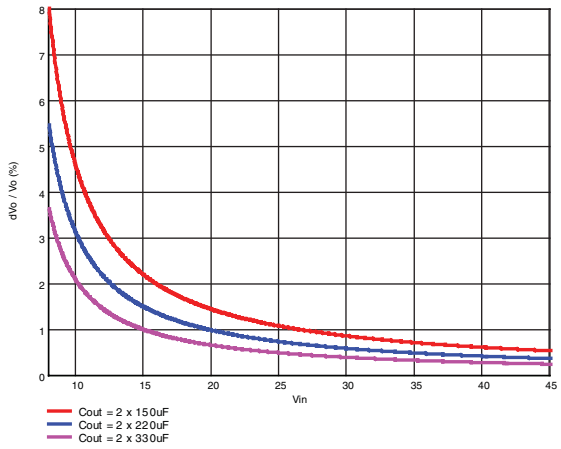
$$\Delta V_O = \frac{(\Delta I_O)^2 \cdot L_O}{2 \cdot C_O \cdot (V_{inmin} \cdot D_{max} - V_O)}$$

where ΔI_o is the load current change from 0.5 A to 3.5 A; D_{max} is the max. duty cycle, 95%; Vo nominal is 5.1 V; and finally L is 68 µH.

Equation 12, normalized at V_o, is represented in *Figure 29* as a function of the minimum input voltage.

These curves are represented for different output capacitors 2x150 µF, 2x220 µF, 2x330 µF all KY, 35 V.

Figure 29. Output drop (%) vs minimum input voltage



3.6 Compensation network

The complete control loop block diagram is shown in *Figure 30*. The error amplifier basic characteristics are:

- gm = 2.5 mS
- Ro = 1.2 MΩ
- Avo = 60 dB
- Isource/sink = 300 µA.

Figure 30. Block diagram compensation loop

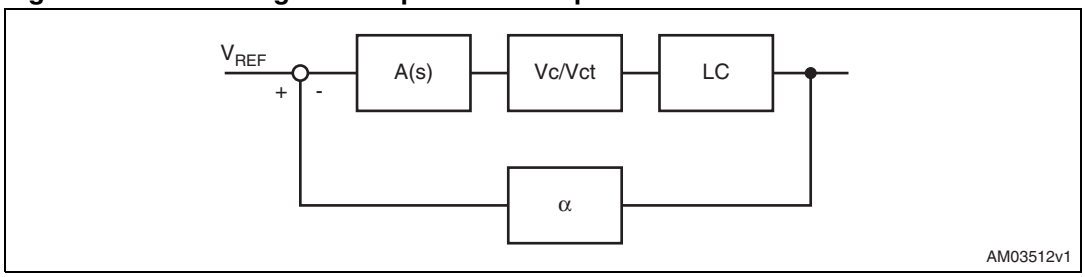


Figure 31. LC output filter

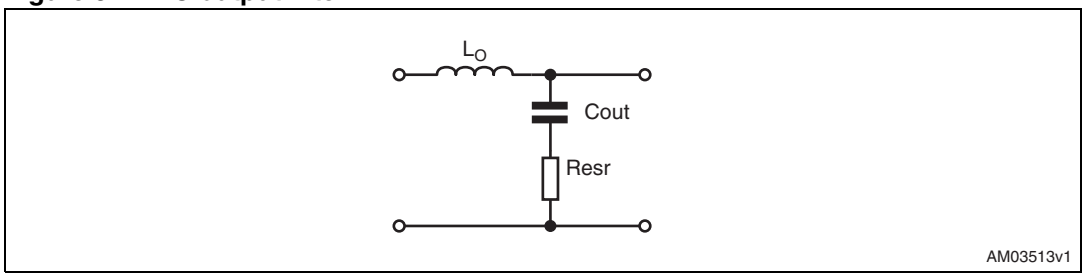
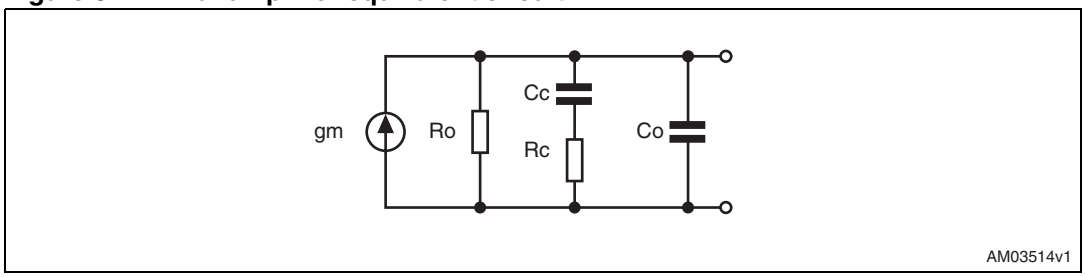


Figure 32. Error amplifier equivalent circuit



3.7 Error amplifier and compensation blocks

The open loop gain is:

Equation 13

$$A(s) = gm \cdot \frac{R_O \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot C_o \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot C_o + R_c \cdot C_c) + 1}$$

where Cout is the parallel between the output and the external capacitance of the error amplifier and R_o is the E/A output impedance. R_c and C_c are the compensation values.

3.8 LC filter

Equation 14

$$A_{o(s)} = \frac{1 + R_{esr} \cdot C_{out} \cdot s}{L \cdot C_{out} \cdot s^2 + R_{esr} \cdot s + 1}$$

3.9 PWM gain

Equation 15

$$\frac{V_{CC}}{V_{ct}} = \frac{V_{CC} \cdot 6}{V_{CC} - 1} \approx 6$$

where V_{ct} is the peak-to-peak sawtooth oscillator.

Pole and zero values are as follows:

Equation 16

$$F_o = \frac{1}{2 \cdot \pi R_{esr} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot 0.065 \cdot 300 \cdot 10^{-6}} = 8.162KHz$$

Equation 17

$$F_p = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{out}}} = \frac{1}{2 \cdot \pi \cdot \sqrt{68 \cdot 10^{-6} \cdot 300 \cdot 10^{-6}}} = 1.087kHz$$

Equation 18

$$F_{ocomp} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 15 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 492Hz$$

Equation 19

$$F_{p1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 1.2 \cdot 10^6 \cdot 22 \cdot 10^{-9}} = 6.029Hz$$

Equation 20

$$F_{p2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o} = \frac{1}{2 \cdot \pi \cdot 15 \cdot 10^3 \cdot 150 \cdot 10^{-12}} = 70KHz$$

The compensation is found by choosing F_{ocomp} close to the frequency of the double pole introduced by the LC filter.

Using a compensation network with R1 = 15 kΩ, C6 = 22 nF and C5 = 150 pF, the gain and phase bode plots are shown in *Figure 32-34*. The cutoff frequency F_c is 22 KHz and the phase margin is 52°C.

Figure 33. Gain bode plot, open loop

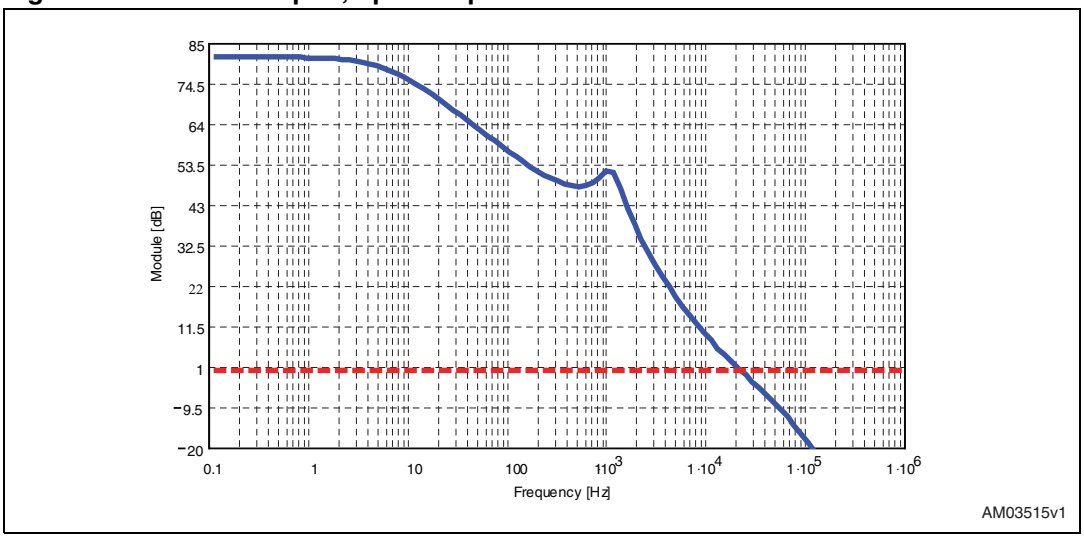


Figure 34. Phase bode plot, open loop

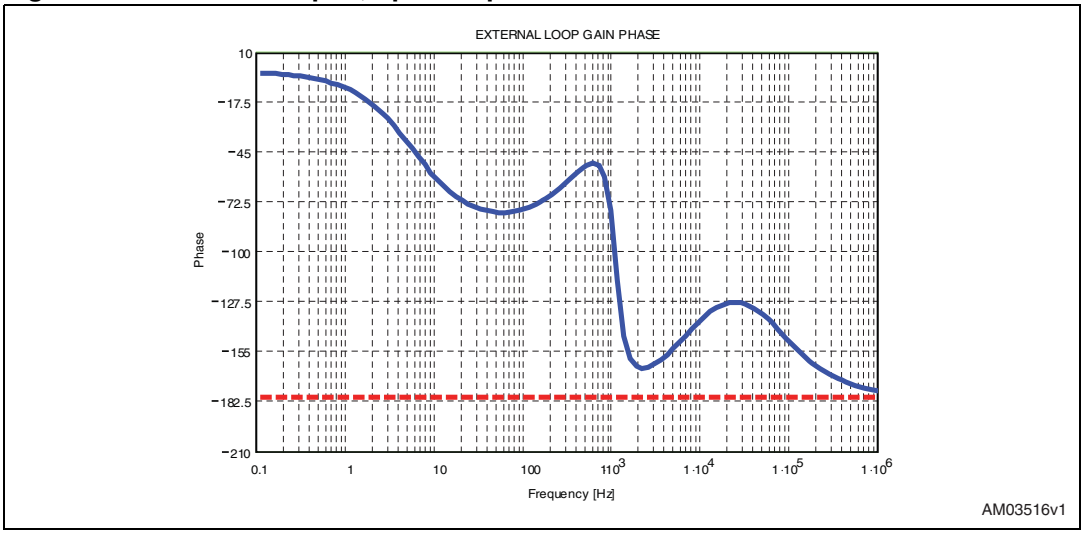


Table 1. Bill of material (f_{SW} = 150 kHz, V_{OUT} = 5 V)

Reference	Description	Part number	Manufacturer
R1	Resistor 15 kΩ 1%		
R2	Resistor 15 kΩ 1%		
R3	Resistor 2.7 kΩ 1%		
R4	Resistor 4.99 kΩ 1%		
R5	Not mounted		
R6	Not mounted		
R7	Not mounted		
C1	Capacitor 2.7 nF 5%		

Table 1. Bill of material (f_{SW} = 150 kHz, V_{OUT} = 5 V) (continued)

Reference	Description	Part number	Manufacturer
C2	Capacitor 470 nF 5%		
C3	Capacitor 1 µF 5%		
C4	Capacitor 22 nF 5%		
C5	Capacitor 150 pF 5%		
C6	Not mounted		
C7	Not mounted		
C8	Capacitor 220 nF 5%		
C9	Capacitor 220 nF 5%		
C10	Capacitor 470 µF 63 V	EKY-630ELL471ML20S	Nippon Chemi-con
C11	Capacitor 150 µF 35 V	EKY-350ELL151MHB5D	Nippon Chemi-con
C11	Capacitor 150 µF 35 V	EKY-350ELL151MHB5D	Nippon Chemi-con
C13	Capacitor 100 nF 5%		
C14	Not mounted		
L1	68 µH I_{rms} = 3.4 A I_{SAT} = 6.7 A	DO5040H-683MLD	Coilcraft
U1		L4973V3.3	STMicroelectronics

Table 2. Resistor divider for V_{OUT} = 12 V

Reference	Description	Part number	Manufacturer
R3	Resistor 2.7 kΩ 1%	-	-
R4	Resistor 1 kΩ 1%	-	-

Figure 35. Demonstration board (component side)

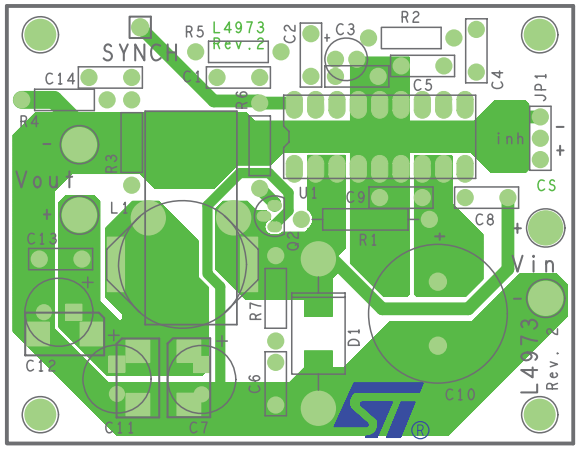


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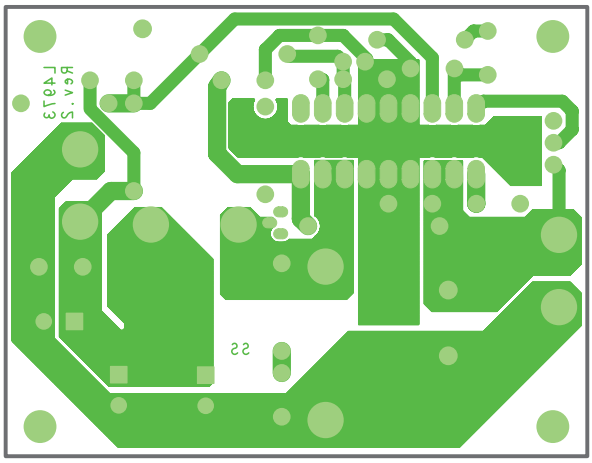
Table 3. Resistor divider for V_{OUT} = 3.3 V

Reference	Description	Part number	Manufacturer
R3	Resistor 2.7 kΩ 1%		
R4	Not mounted		

Figure 36. Demonstration board (solder side)



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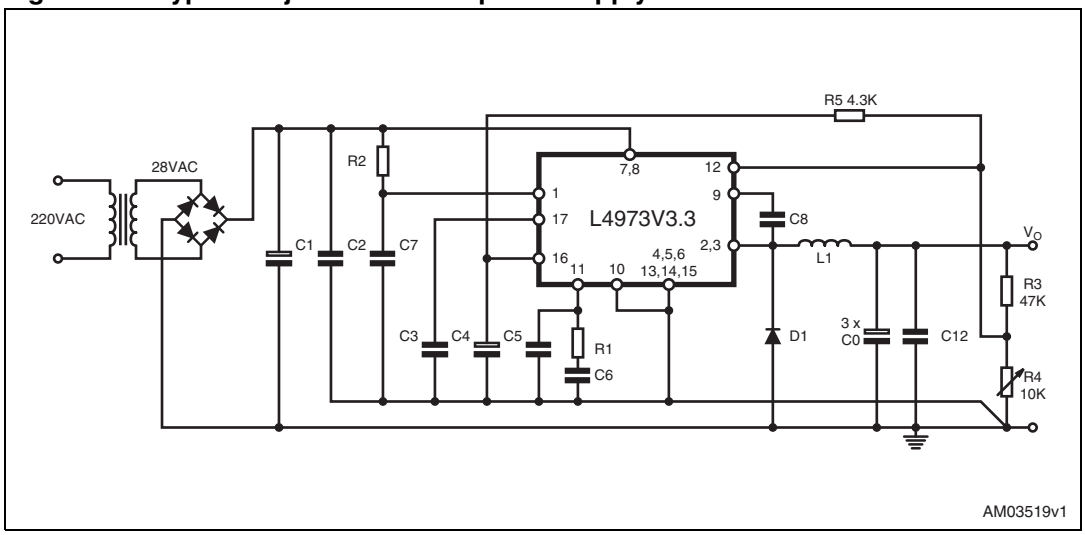
4 Applications

4.1 Mains transformer power supply with output adjustable from 0 V to 24 V

Figure 37 shows a power supply including mains transformer working at 50 Hz 220Vac or 60 Hz 110Vac, bridge rectifier and filtering capacitor. The output voltage is adjustable from 0 to 24 V.

Figure 37. Typical adjustable 0-24 V power supply



The formula to evaluate the output voltage is:

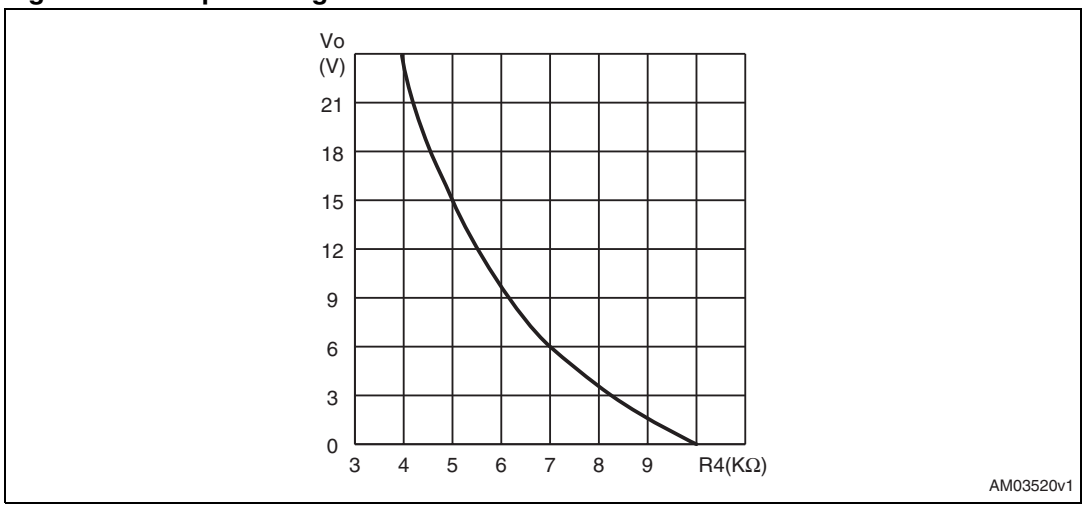
Equation 21

$$V_o = 3.336 + 3.336 \cdot \left(\frac{R3}{R4} + \frac{R3}{R5}\right) - 5.1 \cdot \frac{R3}{R5}$$

Figure 38 shows the formula plot in which it is possible to program the output voltage from 0 V to 24 V using a 10 kΩ potentiometer as R4. R5 is fixed at 4.3 kΩ and R3 is 47 kΩ.

Output capacitors have to be chosen with low ESR to reduce the output ripple voltage and load transients.

Figure 38. Output voltage vs. R4



Particular care has to be taken for input filter capacitors because they have to support high ripple current at mains frequency plus the high frequency current.

Total RMS current is typically heavy, and very low ESR is requested for system reliability.

Input caps can also affect system efficiency.

The transformer could be a single secondary winding with four diodes for rectification or center-tapped with two diodes only, but higher reverse voltage.

Considering a maximum output power close to 100 W, equivalent system efficiency of 93-95%, the mains transformer has to be designed around 200 VA.

A low voltage secondary PFC can reduce the VA need close to the delivered watts (110 W), reducing also the value of the electrolytic capacitors.

Weight and volume of the complete application are also significantly reduced.

4.2 Higher input voltage

Since the max. operating input voltage is 55 V, an input line conditioner is requested. Fixing, for example, the device supply voltage at 50 V, the power dissipation of the pre-regulator is:

Equation 22

$$Pd = Ii \cdot Vce = Ii \cdot (Vi - 50)$$

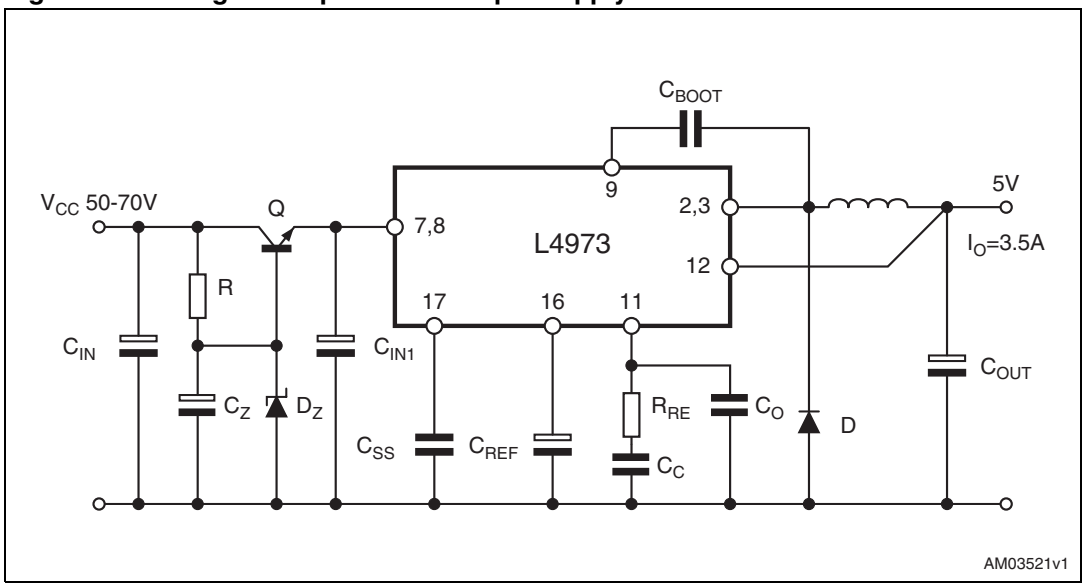
In the buck converter, the average input current is:

Equation 23

$$Ii = Io \cdot \frac{Ton}{T} = Io \cdot \frac{Vo}{Vi}$$

- Vo = 5.1 V; Io = 3.5 A; Po = 17.85 W; Ii = 0.357A; Pd = 3.57 W; (Vi = 60 V)
- Vo = 12 V; Io = 3.5 A; Po = 42 W; Ii = 0.84 A; Pd = 8.4 W (Vi = 60 V)

Figure 39. Design example for 70 V input supply



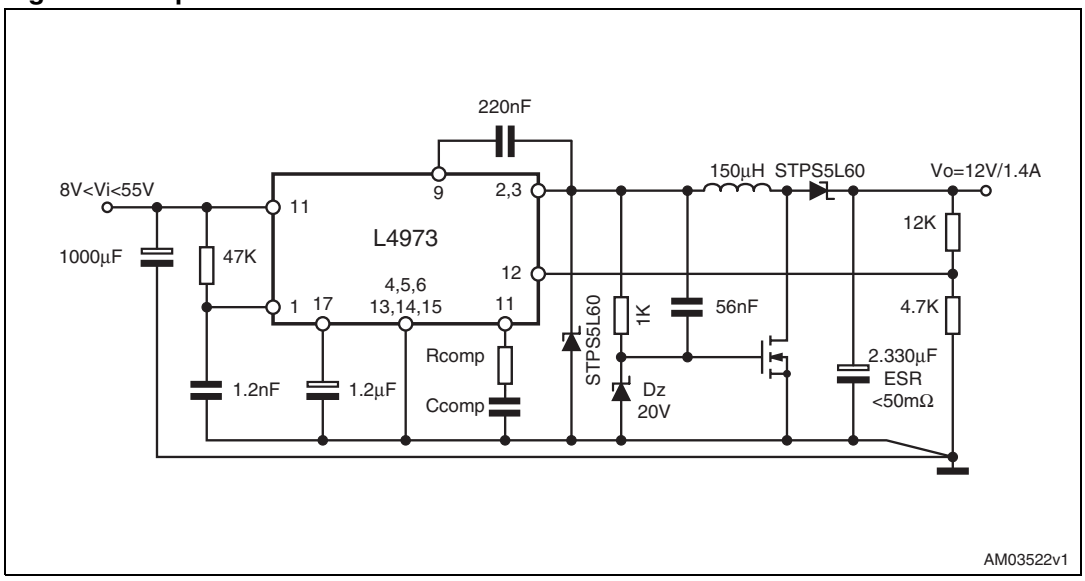
4.3 Buck-boost converter

This topology is useful to stabilize an output voltage higher, equal or lower than the input supply. *Figure 40* shows the schematic diagram of a converter designed for 12 V, $I_{out} = 3.5 \times (1-D)$, with an input supply ranging from 8 V to 55 V.

The 20 V Zener connected to the gate-source of the power MOSFET is for protection purposes when the supply voltage is higher than 20 V.

Such a circuit, asymmetrical half-bridge, is fully protected from output short-circuit, by turning off the on-board floating mos.

Figure 40. Up/down converter



4.4 Current generator

Sometimes the application specifications requires generating constant current, fixed or adjustable, for chemical processes, lamp powering, or battery chargers for lead acids, ni-cd and ni-me-hyd batteries.

We give one suggestion for obtaining an accurate constant current generator.

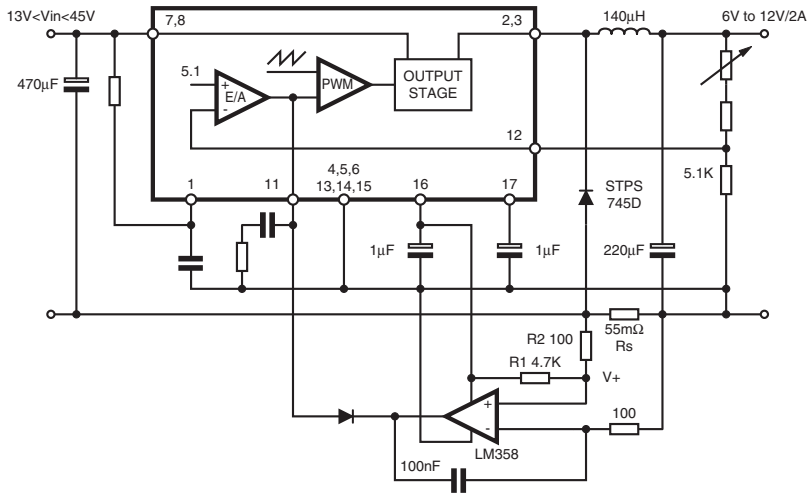
The schematic in *Figure 41* shows a simple solution for constant or variable current generator, with good accuracy of the current, using a simple op/amp supplied by the 5.1 V available reference voltage.The threshold current is fixed by the voltage divider connected to the n.i. input op/amp, at about 100 mV. This is also the maximum voltage dropping on the current sense resistor R_s. Adjusting the 4.7 kΩ, the threshold can be easily changed.

The formula to set the output current is:

Equation 24

$$I_o = \frac{5.1 \cdot R_2}{(R_1 \cdot R_2) \cdot R_s}$$

Figure 41. Constant current generator up to 3.5 A



4.5 From positive input to negative output

Figure 42 shows how to obtain a -12 V, when only a positive supply is available.

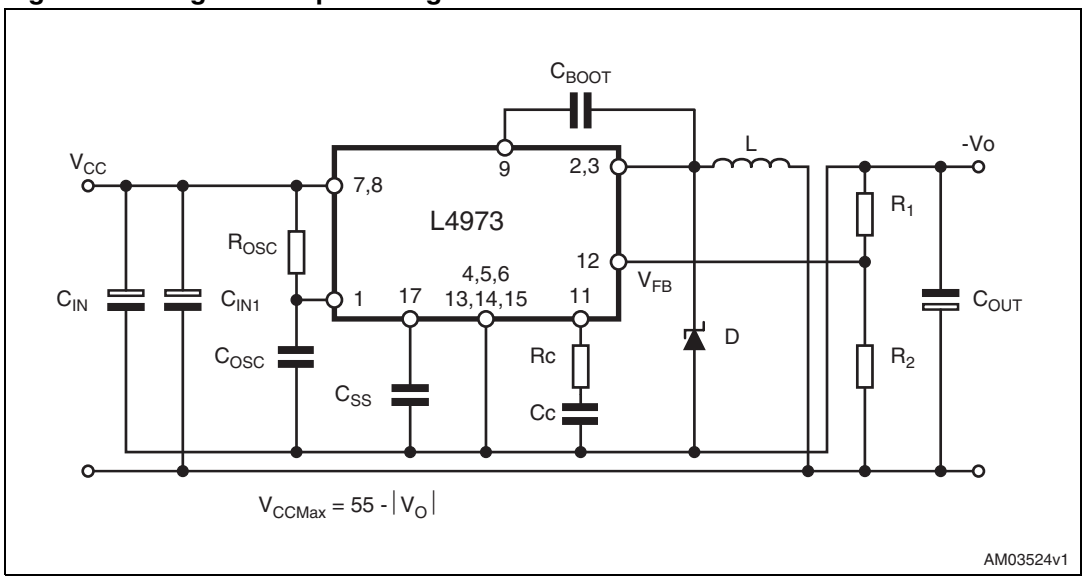
The maximum output current is given by the formula Iout = 3.5 × (1-D) according to the relation for the buck-boost topology.

This negative output has to show good precision, stability and regulation, and it must be protected from output short-circuit.

With the suggested application schematic, one of the aims is to guarantee the performance as specified above and to contribute to the simplification of the power transformer, mains or high frequency.

In inverting buck-boost topology the lower voltage rail of the device floats with the negative output voltage. The voltage applied to the device is equal to (V_{IN} + $|V_{OUT}|$) whose upper limit is given by the maximum input voltage range of the device (55 V).

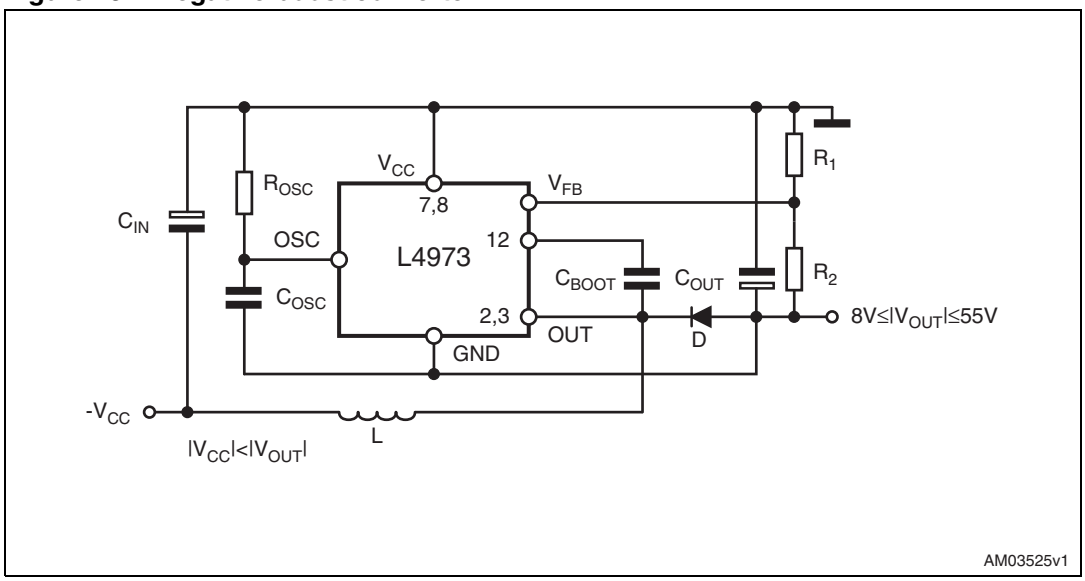
Figure 42. Negative output voltage



4.6 Negative boost converter

Figure 43 shows how to stabilize a negative output voltage higher than negative input voltage.

Figure 43. Negative boost converter.



5 Revision history

Table 4. Document revision history

Date	Revision	Changes
08-Nov-2006	9	Updated the layout.
29-Apr-2009	10	– Modified: *Equation 11*, *16*, *17*, *18*, *19*, *20* – Inserted: *Table 1*, *2*, *3*