AN1513
Application note

VIPower: 30 W SMPS using VIPer50A-E

Introduction

In a growing consumer market, cost effective solutions with good performances and reliability able to meet energy saving international or local standards (Blue Angel) are needed.

STMicroelectronics has, among its wide products portfolio, the VIPer product family offering excellent solutions with all features to design SMPS suitable for consumer applications.

Thanks to the VIPower Technology, these devices combine on the same silicon chip a state-of-the-art PWM control circuit along with an optimized high voltage avalanche rugged Vertical Power MOSFET.

The benefits obtained using these devices are:

- Fewer components compared to a discrete solution
- Less space on PCB
- Simpler design phase
- Automatic burst mode operation in standby for energy savings
- Cost effective solution for SMPS

This document describes the results obtained from an off-line SMPS designed with VIPer50A-E. It has been designed for European mains, providing 30 W on two outputs.

The main target of this application is total power consumption less than 1 W (Blue Angel Norm) in standby mode delivering an output power of 400 mW.

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1 Schematic

The power supply topology is a discontinuous current mode flyback converter, designed with secondary feedback, optocoupler and TL431C. The output voltage regulation is performed on the 6.5 V, so the output voltage 10 V can change according to the load applied on both outputs.

To keep the drain voltage at a safe level and to meet the standby power specification, the clamper used is a Transil 1.5KE220A instead of a classic R-C-D circuit. While the R-C-D circuit dissipates energy in any load condition, the Transil dissipates energy only when the drain voltage spike reaches its breakdown voltage. This consideration is important in order to keep low consumption (<1 W) during standby operation mode.

A Zener diode is also connected to pin Comp for short circuit protection. This diode clamps the voltage on pin Comp under the maximum value (4.5 V), reducing the maximum power delivered by the SMPS.

During short circuit due to the short working time, the V_{DD} voltage drops below the undervoltage lockout threshold and the VIPer starts working in hiccup mode. Even if the peak output current is higher than the nominal one, thanks to the on/off cycles, the average current flowing in the shorted output components is kept under control at a safe value avoiding diodes failure and any other damage to the circuit.

The output rectifiers are Schottky diodes for better efficiency thanks to their lower forward voltage drop and negligible switching losses.

The output capacitors are low ESR type to minimize the output ripple and to manage the RMS output ripple current.

Table 1. Electrical specifications

Parameter	Value
Input voltage	European standard $230V_{ac}$±15%
Output voltage 1	6,5 V±3% at 2.5 A
Output voltage 2	10 V±8% at 1.5 A
Standby consumption	<1 W
Efficiency	>80%
Max working ambient temperature	60°C

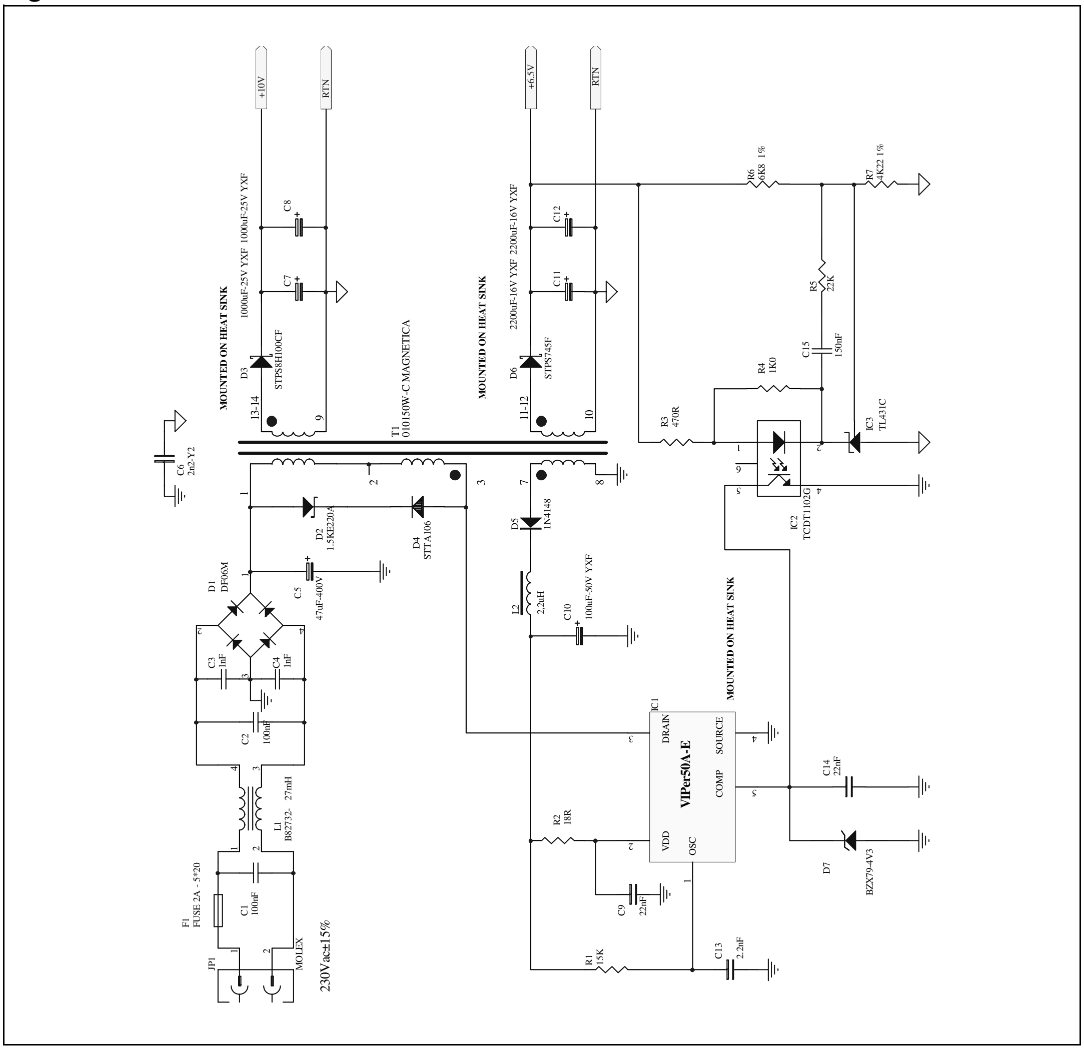
2 Standby

The first test performed is the measure of the power consumption during standby operation mode as the main target of this application is consumption lower than 1 W. For better accuracy, because the power level is very low, the power supply has been tested with a dc voltage source.

Table 2. Standby measurements at 65 mA on output 1

V_{in}	I_{in}	V_{out1} at 65 mA	V_{out2} at 0 mA	P_{out}	P_{in}	Efficiency	Switching frequency
Vdc	mA	Vdc	Vdc	W	W	%	KHz
276	3.33	6.51	16.6	0.42	0.92	46	BURST
325	3.02	6.51	17.5	0.42	0.98	43	BURST
374	2.67	6.51	18.2	0.42	1.0	42	BURST

Figure 1. Electrical schematic



The VIPer50A-E is designed to work in burst mode automatically when the power delivered to the load becomes very low. The burst frequency and its duty-cycle depend on the transformer parameters and the power delivered. The burst mode takes place when the power transferred during the minimum on time is greater than the power required by the load. This should increase the output voltage, but instead the control loop reacts by missing some cycles. It is important to point out that during this working mode, the output voltage is always perfectly under control. The result is a working mode where the effective duty-cycle is much lower than the minimum under normal operation.

To further decrease the consumption during standby operation an additional test has been done. Of course the burst mode has efficiency proportional to its working duty-cycle and to work or not in burst mode is also dependent on the primary inductance of the transformer. Sometimes it is difficult to optimize the primary inductance of the transformer and obtain an efficient burst. The result can be just a few cycles missed and most of the pulses are present at switching frequency. It can be an advantage to work at a lower fixed frequency, giving up the burst operation mode. The network Q1, R8÷R10 decreases the frequency sinking current from R1 (timing resistor) when pin Comp (5) is lower than 1.6 V. In this way the charging current of C13 (timing capacitor) decreases and according to the law

Equation 1

$$T = \frac{C \cdot V}{I}$$

the frequency starts to reduce until the minimum frequency is at standby load. In steady state condition at full load the switching frequency has been set to around 70 KHz, while in standby it is around 30 KHz.

Table 3. Standby measurements at 65 mA on output 1

V_{in}	I_{in}	V_{out1} at 65 mA	V_{out2} at 0 mA	P_{out}	P_{in}	Efficiency	Switching frequency
Vdc	mA	Vdc	Vdc	W	W	%	KHz
276	2.98	6.51	19.5	0.42	0.82	53	30
325	2.69	6.51	19.6	0.42	0.87	48	29
374	2.48	6.51	19.8	0.42	0.93	45	28

3 Full load test

The parameters checked at full load have been the efficiency and main working parameters of the VIPer for system reliability. The minimum voltage has been set at $240V_{dc}$ considering the minimum voltage ripple on the bulk capacitor when the power supply is connected to the ac mains.

The drain voltage spike reaches its maximum value at full load and maximum input voltage. This spike is caused at turn-off by the energy stored in the primary leakage inductance of the transformer during the T_{on}. This is the reason why it is recommended to design the power transformer with a primary leakage inductance as low as possible. In addition a good coupling between primary and secondaries improves total regulation, especially in SMPS with more than one output.

Figure 2. Adjustment for frequency reduction

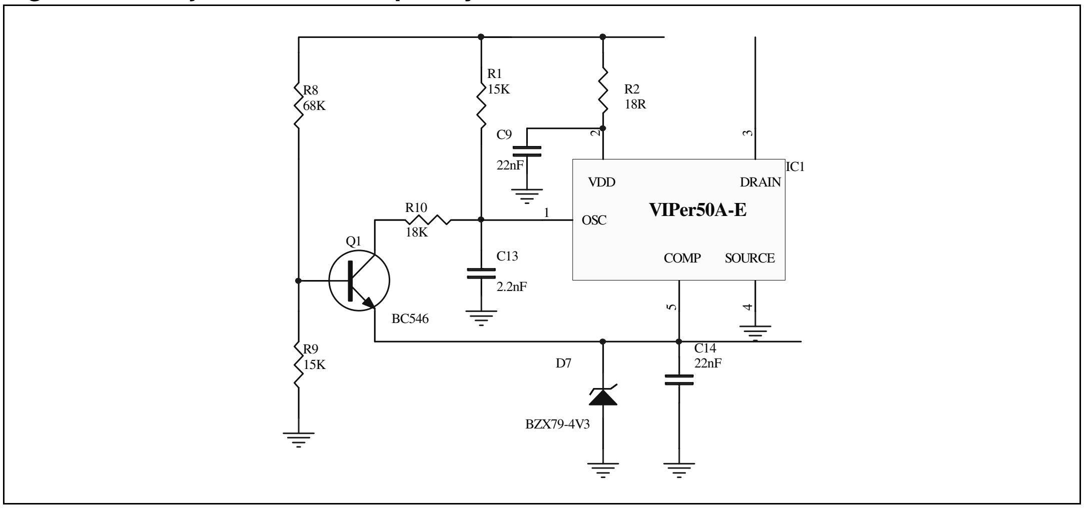


Figure 3. Drain current at full load

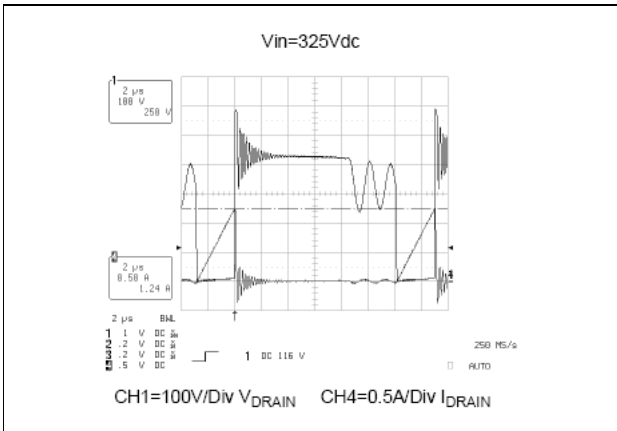
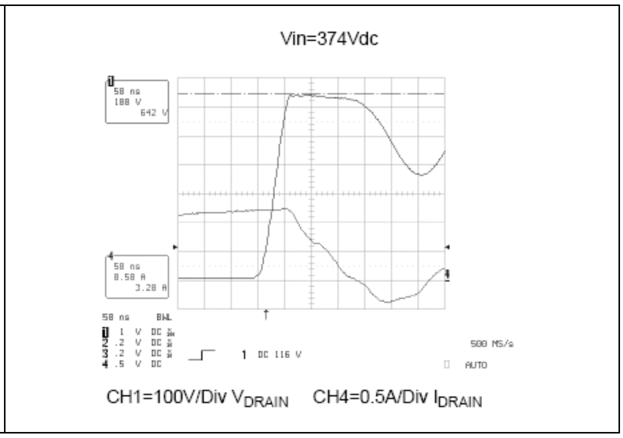


Figure 4. Voltage current at full load



The maximum peak voltage measured on the drain is 642 V, thanks to the clamp 1.5KE220A. This value guarantees a reliable operation of VIPer with a good margin with respect to the maximum B_{VDSS}, which is 700 V. The VIPer is an avalanche rugged device able to withstand a momentary energy peak caused by voltage greater than 700 V.

The SMPS meets the specification with efficiency better than 80% at any input voltage value, as shown in *Table 4*.

Table 4. Full load measurements

Full load						
V_{in}	I_{in}	V_{out1} at 2.5 A	V_{out2} at 1.5 A	P_{out}	P_{in}	Efficiency
Vdc	mA	Vdc	Vdc	W	W	%
240	160	6.50	10.26	31.6	38.4	82.3
325	118	6.50	10.25	31.6	38.3	82.5
374	102	6.50	10.25	31.6	38.1	82.9

4 Load step

This SMPS has been designed to operate under two conditions: standby and full load. In *Figure 5* and *Figure 6* show the outputs voltages during load steps from standby and full load and vice versa. CHA is the resampling of V_{out1} highlighting that no undershoot or overshoot is present during load transient. The same test has been done to show the behavior of the voltage on pins V_{DD} and Comp.

Figure 5. Load transient (V_{out1}, V_{out2})

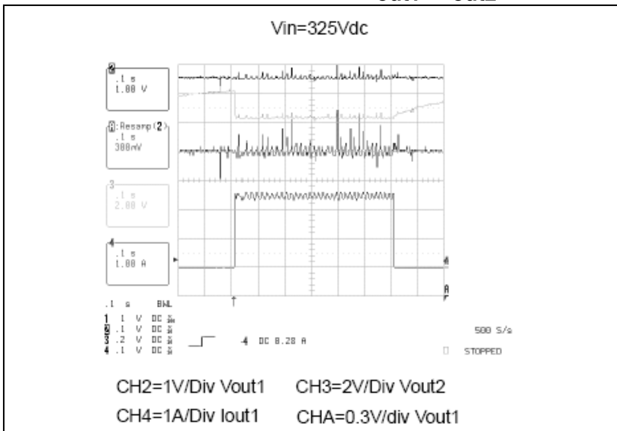
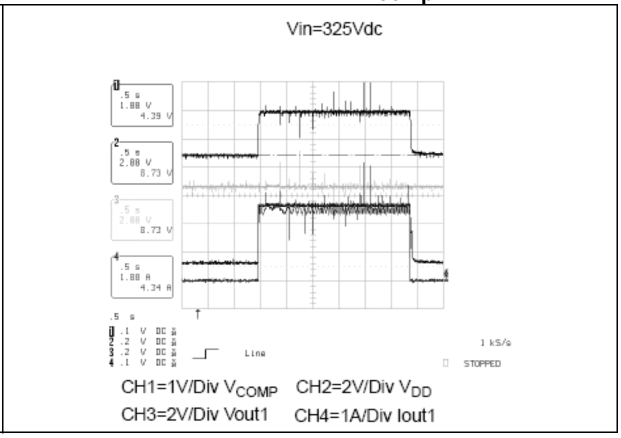


Figure 6. Load transient (V_{comp}, V_{DD})



5 Short circuit protection

The SMPS is protected against short circuit on both outputs. The short circuit test has been done with an active load for the complete input voltage range. As shown in *Figure 7* and *Figure 8*, taken at worst case at 374 V_{dc}, during short circuit on output1 or output 2, the SMPS works in “hiccup” mode keeping the mean output current at a safe value for the rectifiers, respectively at 3.3 A for output 1 and 2.2 A for output 2. Also the drain voltage remains at a safe level during short circuit. To achieve these results a Zener diode has been connected between pin Comp and Source of the VIPer. This Zener clamps the voltage on pin Comp, limiting the maximum primary peak current. During short circuit the auxiliary voltage is low because it is proportional to the output voltage. V_{DD} drops under the low threshold (8 V) blocking the VIPer and beginning the start up cycle. When C12 is charged at 11 V, the VIPer turns on again. It works as long as C12 is discharged to 8 V because the auxiliary voltage, thanks to the reduced duty-cycle, is not capable of supplying the VIPer.

Figure 7. Short circuit (V_{out1})

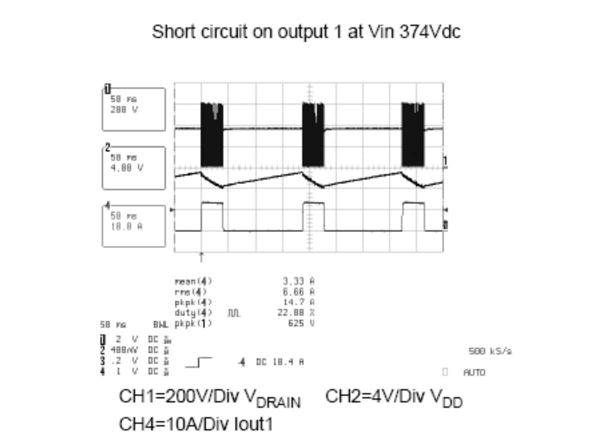
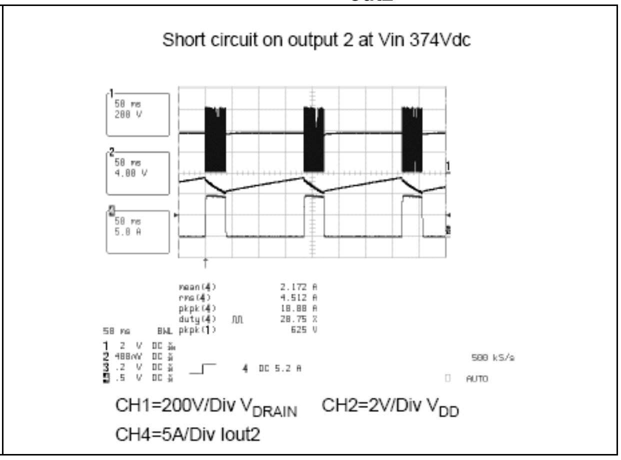


Figure 8. Short circuit (V_{out2})



6 Overvoltage protection

Thanks to the V_{DD} regulation capability, this SMPS is protected against secondary feedback failure. If the secondary feedback loses control, the voltages increase. As the auxiliary voltage is proportional to the outputs, V_{DD} increases up to 13 V, which is the typical regulation value for VIPer50A-E, so the VIPer takes control avoiding any damage to the output capacitors and rectifiers. *Table 5* gives the measurements in standby and at full load with R6 removed from the board to simulate secondary feedback failure.

Table 5. Overvoltage measurements

Operation mode	V_{out1}	V_{out2}
Standby	9.5V	22.5 V
Full load	7.2V	11.2 V

7 Thermal test

For system reliability it is important to keep device temperature at a safe level, considering the maximum ambient temperature especially when the board is inside a chassis. In *Table 6* shows the temperatures measured on the SMPS after 4 hours of warm-up at full load at nominal input voltage $230V_{ac}$: the results are compatible with robust design rules.

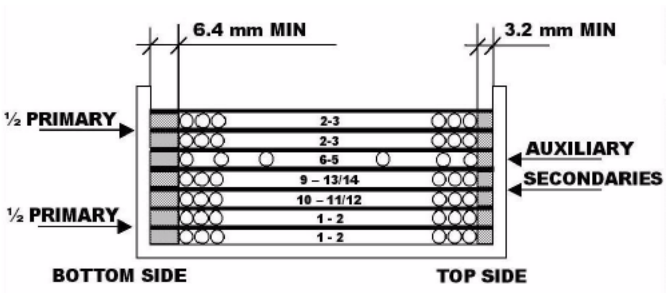
Table 6. Thermal measurements

Measure point	Temperature (°C)
Ambient	25
VIPer50A-E	47
STPS8H100F	53
STPS745	58
1.5KE220A	84
STTA106	55
DFO6M	52
T1 Ferrite	53

Table 7. Transformer specification and construction

Parameter	Value	
Primary inductance	670 µH ±8%	58 TURNS
Winding output1		4 TURNS
Winding output2		6 TURNS
Auxiliary winding		6 TURNS
Primary leakage inductance	12 µH	1.8% of Lp
Core	EPCOS ETD29-N67	
Code	B66358-G500-X67	

Figure 9. Transformer cross section



8 Conclusion

The main specification requirements of this application have been reached and thanks to the VIPer features, it also has been demonstrated that a quite difficult task such as attaining very low power consumption in standby is easily achievable.

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
04-Jan-2005	1	First issue
27-Sep-2007	2	– The document has been reformatted – VIPer50A becomes VIPer50A-E

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