



AN1673 APPLICATION NOTE

L6598 OFF-LINE CONTROLLER FOR RESONANT CONVERTERS

INTRODUCTION

Because of the much high efficiency that can be achieved (higher than the traditional PWM) and the reduction of the high frequency electromagnetic interference (thanks to the utilization of parasitic parameters of the circuit), the interest for resonant topologies is recently growing in power conversion market. In fact this kind of topologies allows high power/weight ratio and low power dissipation of the power parts.

Several power supply application segments such as Adapters, Television, Monitor, Telecom and Car Radio can benefit by using converters based on the topology.

The L6598 is designed for half bridge configuration.

This paper deals on how to use this device. At the end, it will be discussed concerning some design criteria and application tips.

FEATURED DEVICE DESCRIPTION

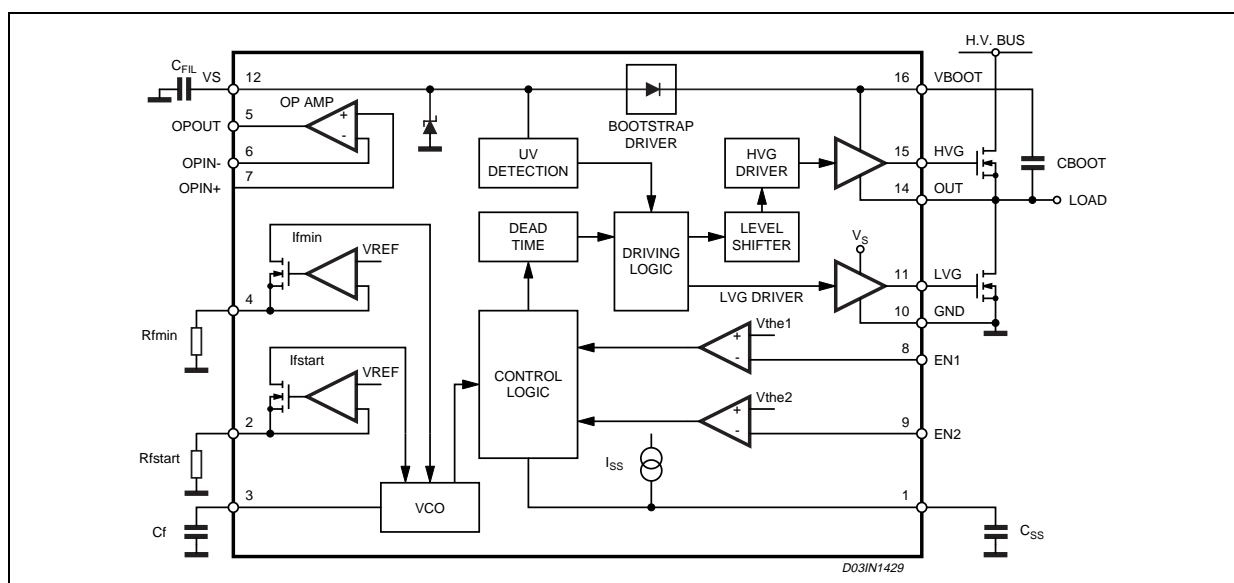
The device, whose internal block diagram is shown in fig.1, is an integrated circuit realized in Off-Line technology. Able to drive Powermos or IGBT, in half bridge topology, it is provided with all the features (such as VCO, Soft-Start, OP-Amp and Enables) needed to implement and control properly a resonant SMPS with the minimum components count.

Even though the device is able to withstand high voltage, it can operate at low voltage starting from its operative supply. It is available in DIP16 and SO16N packages.

The most significant peculiarities are:

- High voltage rail (up to 600V) and $\frac{dv}{dt}$ immunity (± 50 V/ns) at full temperature range.
- 250 mA (source) / 450 mA (sink) driver current capability.
- Under voltage lockout.
- Precise current controlled oscillator and frequency shift for soft-star function.
- Integrated bootstrap driver for C-boot charging.

Figure 1. Internal Block diagram



AN1673 APPLICATION NOTE

DEVICE PINS FUNCTION

Pin #	Name	Description
1	C _{SS}	Soft Start Timing Capacitor. The device is provided with Soft Start features. The capacitor C _{SS} sets the soft start time, according to the relations: T _{SS} = k _{SS} · C _{SS} (typ. k _{SS} = 0.15 s/μF). In steady state the voltage at pin1 is 5V. During T _{SS} a current I _{SS} , function of I _{fstart} , charges the capacitor. Anyway T _{SS} , set at k _{SS} · C _{SS} depends only on C _{SS} value. See pin-2 and timing description in the data-sheet.
2	R _{fstart}	Maximum Oscillation Frequency Setting. A resistance connected between this pin and ground sets the f _{start} value, fixing the difference between f _{start} and f _{min} (f _{start} > f _{min}). The voltage at this pin is fixed at V _{REF} = 2V, so R _{fstart} programs the I _{fstart} current = V _{REF} /R _{fstart} . The R _{fstart} value is recommended to be not less than 18 - 20 kOhm.
3	C _f	Oscillator Frequency Setting. The C _F capacitor, with R _{fstart} and R _{fmin} , sets f _{start} and f _{min} . In normal operation this pin shows a triangular wave. See timing and oscillator section in the data-sheet.
4	R _{fmin}	Minimum Oscillation Frequency Setting. A resistance connected between this pin and ground sets the f _{min} value. The voltage at this pin is fixed at V _{REF} = 2V, so R _{fmin} sets the I _{fmin} current equal to V _{REF} /R _{fmin} . To set precise frequency, the R _{fmin} value is recommended not to be less than 20 kOhm.
5	OP _{out}	Out of the operational amplifier. Characterized with 1M-gain bandwidth product, this Op Amp is a free feature for any need. To implement a feedback control loop this pin can be connected to the Remind pin by means of an appropriate circuitry.
6	OP _{IN-}	Inverting Input of the operational amplifier.
7	OP _{IN+}	Non Inverting Input of the operational amplifier.
8	EN1	Enable 1. This pin forces the device in latched shutdown state (The same as in under voltage conditions). Active high, the typical threshold level is 0.6V. There are two ways to resume normal operation. The first is to reduce the supply voltage below the under voltage threshold and then increase it again until the valid supply is recognized. The second is activating EN2 input. The enable-1 is especially designed for strong fault (e.g. in case of short circuit or open load).
9	EN2	Enable 2. Enable input (active high at 1.2V threshold level). When activated, this function forces the soft-start sequence to be executed. The EN2 is prevalent on EN1 and so; it is possible to cancel the latched enable (EN1).
10	GND	Ground
11	LVG	Low Side Driver Output. This pin must be connected to the low side power MOSFET gate of the half bridge. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
12	V _s	Supply Voltage. This pin will be connected to the supply filter capacitor. An internal clamp (15.6V typical) limits the supply voltage.
13	N.C.	Not Connected. This pin is not internally connected thus increasing the distance between the high voltage and low voltage circuitry. The increased distance gives benefit for insulation.
14	OUT	High Side Driver Floating Reference. This pin must be connected close to the source of the high side power MOS or IGBT.
15	HVG	High Side Driver Output. This pin must be connected to the high side power MOSFET gate of the half bridge. A resistor connected between this pin and the power MOS gate can be used to reduce the peak current.
16	V _{boot}	Bootstrapped Supply Voltage. The bootstrap capacitor must be connected between this pin and V _s . A patented integrated circuitry replaces the high voltage external diode. This feature is achieved by means of a high voltage DMOS, synchronously driven with the low side power MOSFET. See Bootstrap section in the data-sheet for details.

DEVICE OPERATION.

The device will start its function as the supply voltage reaches the UVLO threshold.

Before the supply threshold is O.K., both the external half bridge's Powermos are cut off thank to the low impedance of the drivers. As the supply is valid, the circuit starts to run; the low side driver is active during the first half period so that the boost capacitor will be fully charged.

The oscillator is based on a current controlled oscillator. Choosing the appropriate biasing at R_{fmin} and R_{fstart} we can define the minimum and maximum frequency operation limits. The device is provided with soft start function (ss); connecting a delay capacitor at C_{SS} , it can be controlled ss time. At start up the frequency is set to the maximum value (F_{max}) and will gradually decrease to the operative one during the startup time.

The oscillator controls the power stage circuit by the Low and High side gate drivers, connected to the external Power MOS . The control of the frequency can be done acting on the R_{fmin} in closed loop controlled condition.

The significant current capability of both, the high and low side drivers (typically 450mA source and 250mA sink), allows many different power MOS size to be driven maintaining fast switching transition. The internal logic ensures a dead time between the gate turn off of the high/low side and the low/high side gate turn on. This important feature allows to easily operating in zero voltage-switching mode, minimizing the transistor switching losses and the electromagnetic interference (see below in the soft switching section). The built-in dead time is typical 300ns; the transition will be completed within this time.

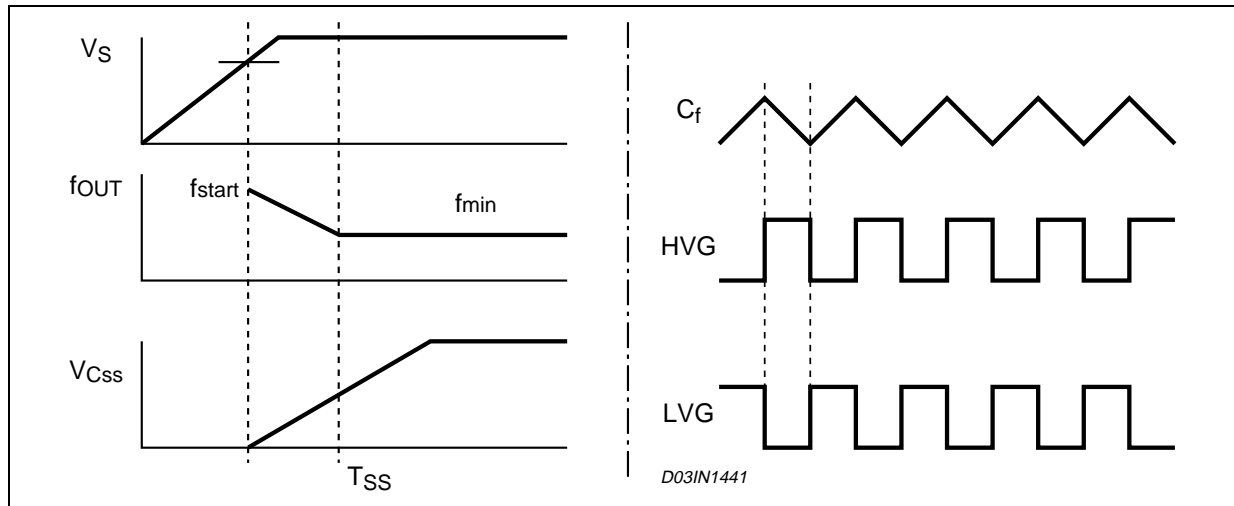
The integrated Bootstrap function, allows avoiding the need of the external fast diode for charge the bootstrap capacitor (required to supply the floating driver).

The internal operational amplifier can be useful in closed loop control or protection function.

SOFT START AND OSCILLATOR.

The soft start function consists in a period of time, T_{SS} , in which the switching frequency shifts from f_{start} to f_{min} . This feature is detailed explained below (ref. to fig.2).

Figure 2. Soft start timing and Oscillator to drivers phase.



During the soft start time the current I_{SS} charges the capacitor C_{SS} , generating a voltage ramp which is delivered to a trans conductive amplifier, as shown in fig. 2. Thus this voltage signal is converted in a growing current, which is subtracted to I_{fstart} . Therefore the current, which drives the oscillator to set the frequency during the soft start, is equal to:

$$[1] \quad I_{osc} = I_{fmin} + (I_{fstart} - gm \cdot V_{CCS(t)}) = I_{fmin} + \left(I_{fstart} - \frac{gm \cdot I_{SS} t}{C_{SS}} \right)$$

AN1673 APPLICATION NOTE

Where:

$$[2] \quad I_{f_{\min}} = \frac{V_{REF}}{R_{f_{\min}}}; \quad I_{f_{\text{start}}} = \frac{V_{REF}}{R_{f_{\text{start}}}}; \quad V_{REF} = 2V$$

At the start-up ($t=0$) the L6598 oscillates (see also fig3 and relation [7]) at f_{start} :

$$[3] \quad f_{\text{start}} = \frac{1}{t} = \frac{I_{OSC}}{2 \cdot C_f \cdot \Delta V_C} \quad \text{set by:}$$

$$[3b] \quad I_{osc0} = I_{f_{\min}} + I_{f_{\text{start}}} = V_{ref} \left(\frac{1}{R_{f_{\min}}} + \frac{1}{R_{f_{\text{start}}}} \right)$$

At the end of soft start ($t = T_{SS}$) the second term of eq.1 decreases to zero and the switching frequency is set only by I_{\min} (i.e. $R_{f_{\min}}$):

$$[4] \quad I_{OSC}(T_{SS}) = I_{f_{\min}} = \frac{V_{REF}}{R_{f_{\min}}}$$

Since the second term of eq.1 is equal to zero, we have:

$$[5] \quad I_{f_{\text{start}}} - \frac{g_m \cdot I_{SS}}{C_{SS}} \cdot T_{SS} = 0 \Rightarrow T_{SS} = \frac{C_{SS} \cdot I_{f_{\text{start}}}}{g_m \cdot I_{SS}}$$

Note: there is not a fixed threshold of the voltage on C_{SS} in which the soft start finishes (i.e. the end of the frequency shifting), and T_{SS} depends on C_{SS} , $I_{f_{\text{start}}}$, g_m , and I_{SS} (eq. 5). Making T_{SS} independent of $I_{f_{\text{start}}}$, the I_{SS} current has been designed to be a fraction of $I_{f_{\text{start}}}$, so:

$$[6] \quad I_{SS} = \frac{I_{f_{\text{start}}}}{K} \Rightarrow T_{SS} = \frac{C_{SS} \cdot I_{f_{\text{start}}}}{g_m \cdot I_{SS}} \Rightarrow T_{SS} = \frac{C_{SS}}{g_m \cdot K} \Rightarrow T_{SS} = k_{SS} \cdot C_{SS}$$

In this way the soft_start time depends only on the capacitor C_{SS} . The typical value of the k_{SS} constant (Soft Start Timing Constant) is 0.15 s/ μ F.

The current I_{OSC} is fed to the oscillator as shown in fig. 3. It is twice mirrored (x4 and x8) generating the triangular wave on the oscillator capacitor C_f . Referring to the internal structure of the oscillator (fig.3):

$$[7] \quad f_{\min} = \frac{1}{t} = 2 \frac{I_{OSC}}{C_f \cdot \Delta V_C}$$

Where: $I_{OSC} = 4 \cdot I_{R_{f_{\min}}}$; ΔV_C is the peak to valley oscillator value ($\approx 2.84V$).

A good relationship to compute an approximate value of the oscillator frequency in normal operation is:

$$[7b] \quad f_{\min} = \frac{1.41}{R_{f_{\min}} \cdot C_{f_t}}$$

The degree of approximation depends on the frequency value, but it remains much good in the range from 30kHz to 100kHz (fig.4).

Figure 3. Oscillator Block

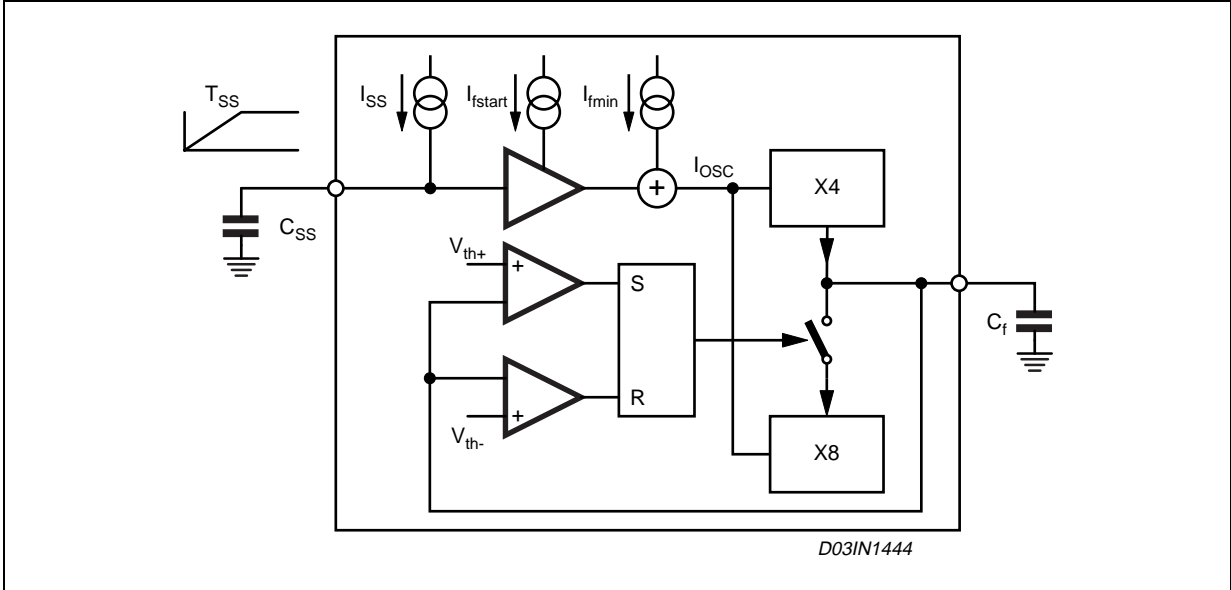
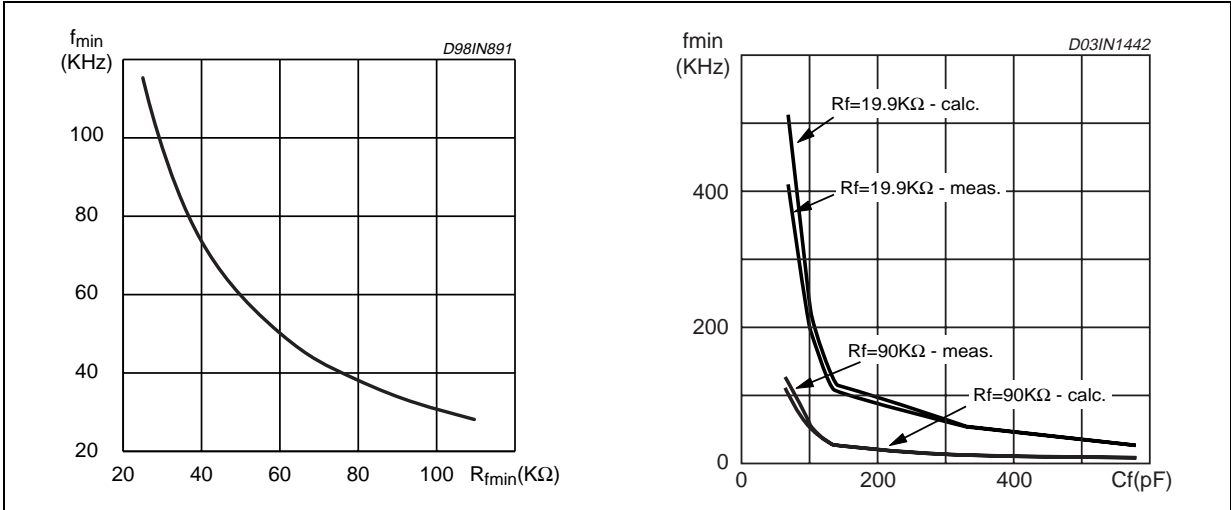


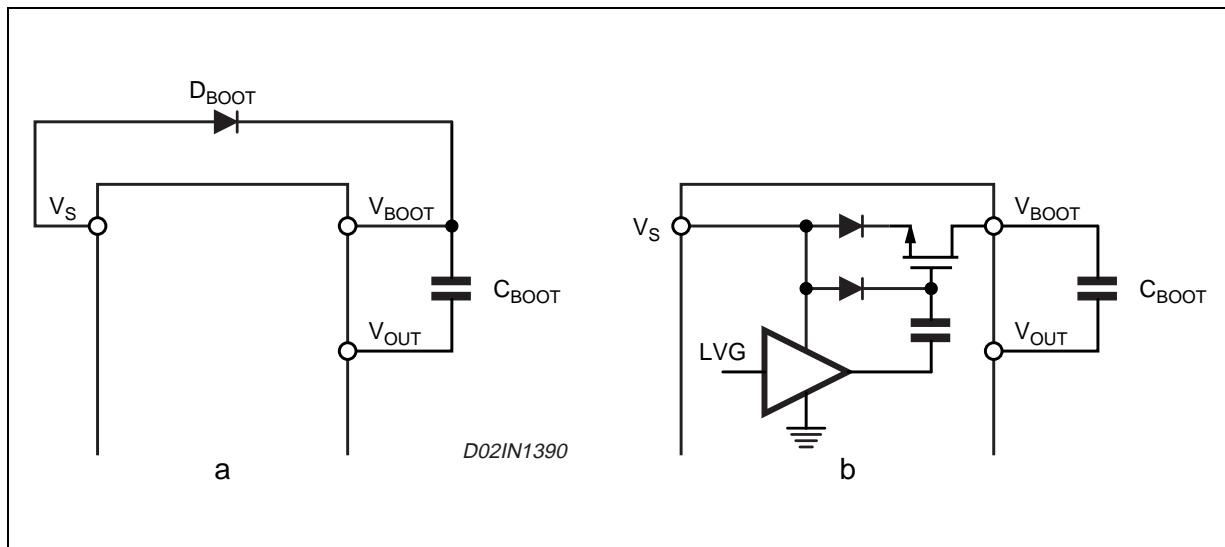
Figure 4. Frequency Diagrams



BOOTSTRAP SECTION.

The supply of the high voltage section is obtained by means of a bootstrap circuitry. This solution normally requires a high voltage fast recovery diode for charging the bootstrap capacitor (fig. 5a). In the device a patented integrated structure, replaces this external diode. It is realised by means of a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in fig. 5b.

Figure 5. Bootstrap driver.



To drive the synchronised DMOS it is necessary a voltage higher than the supply voltage V_S . This voltage is obtained by means of an internal charge pump.

The diode connected in series to the DMOS has been added to avoid undesirable turn on of it. The introduction of the diode prevents any current can flow from the V_{boot} pin to the V_S one in case that the supply is quickly turned off when the internal capacitor of the pump is not fully discharged.

The bootstrap driver introduces a voltage drop during the recharging time of the capacitor C_{boot} (when the low side driver is on), which increases with the frequency and with the size of the external power MOS. It is the sum of the drop across the R_{DSON} and of the diode threshold voltage. At low frequency this drop is very small and can be neglected. Anyway increasing the frequency it must be taken in to account. In fact the drop, reducing the amplitude of the driving signal, can significantly increase the R_{DSON} of the external power MOS (and so the dissipation).

To be considered that in resonant power supplies the current, which flows in the power, MOS decreases increasing the switching frequency and generally the increases of R_{DSON} are not a problem because power dissipation is negligible. The following equation is useful to compute the drop on the bootstrap driver:

$$[8] \quad V_{drop} = I_{charge} \cdot R_{dson} + V_{diod} \Rightarrow V_{drop} \cdot \frac{Q_g}{T_{charge}} \cdot R_{dson} + V_{diode}$$

Where Q_g is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the time in which the bootstrap driver remains on (about the semi period of the switching frequency minus the dead time). The typical resistance value of the bootstrap DMOS is 150 Ohm. For example using a power MOS with a total gate charge of 30nC the drop on the bootstrap driver is about 2.5V, at a switching frequency of 200kHz. In fact:

$$[9] \quad V_{drop} = \frac{130nQ}{2.3\mu s} \cdot 150\Omega + 0.6V \cong 2.6V$$

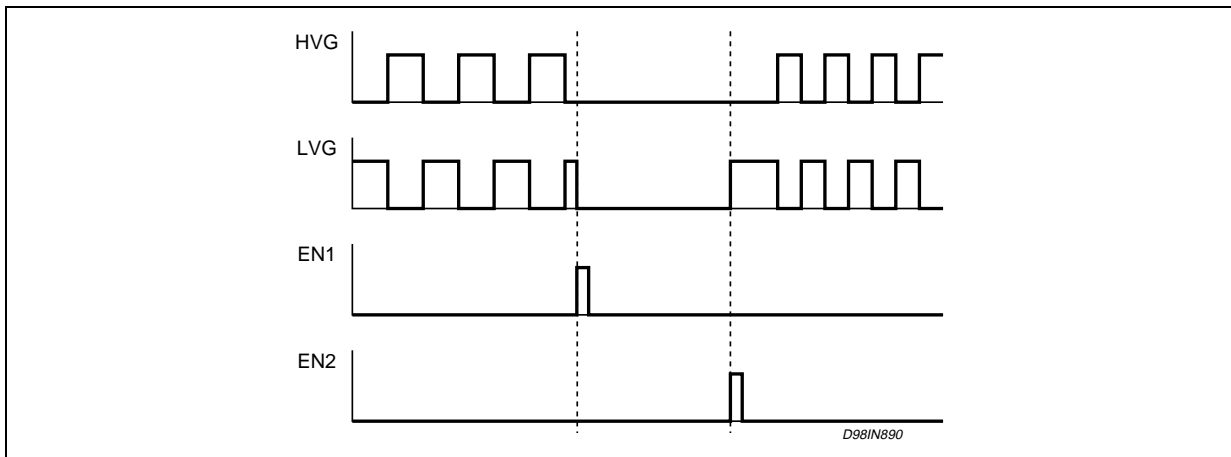
In practice, if a significant drop on the bootstrap driver (at high switching frequency when large power MOS are used) represents a problem, an external diode can be used, avoiding the voltage reduction on the C_{boot} .

ENABLE FUNCTIONS.

The L6598 is provided with two different enable inputs, EN1 (pin8) and EN2 (pin 9), suitable for a flexible control of the application.

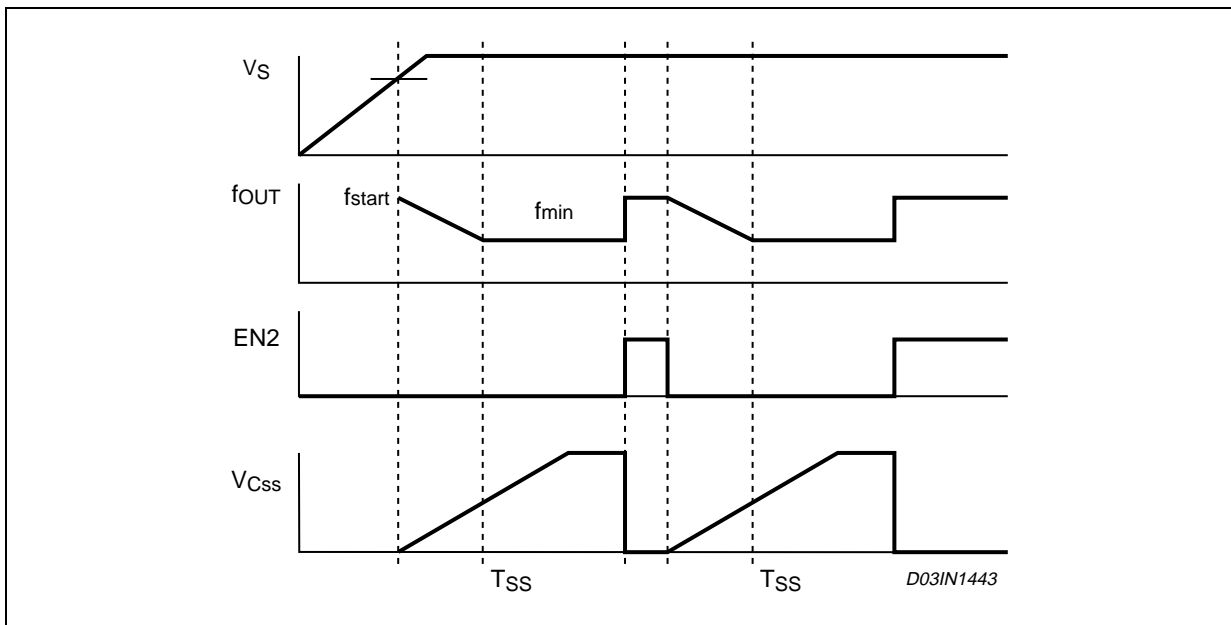
The Enable 1 (active high) threshold is typically 0.6V. When activated, it forces the device in a latched shut down state in which the oscillator is stopped and both HVG and LVG are cut off, like in the under voltage condition. In this state the device sinks from the supply a low quiescent current (250µA max.). There are two ways to restart the device: one is reducing the supply voltage below the turn off threshold (then turning it on again). The second is activating Enable 2 input (fig.6). Latched O.V.P function can be achieved using this function.

Figure 6. Enable 1 timing diagrams



The En2, active high, has a typical threshold of 1.2V. It restarts the start up sequence and, if the En1 has been previously activated, it resumes from the latched condition (fig.7).

Figure 7. Enable 2 timing diagrams



RESONANT APPLICATIONS.

In the switched mode power conversion, the resonant converters can be distinguished from the non-resonant ones observing the waveforms, specifically seen by the power switches and parasitic elements within the converter. In practice, in contrast to a traditional PWM (typically rectangular/trapezoidal shaped), the resonant converters waveforms contain pieces of sinusoidal ringing waveforms.

The resonant conversion technique can be applied for all the converter topologies (buck, boost, fly-back). It is possible to classify this kind of converters in different classes:

- **Series** or **parallel load** of the resonant circuit.
- **Fixed** or **variable frequency** operation.
- **Continuous** or **discontinuous** resonance.
- **Full resonant, half resonant** (resonant switches) converters.

This technical paper can't discuss about the variety of many different topologies.

We can define resonant the converters that takes advantage of the L-C network resonance and the concerning possibility to switching in zero-voltage or zero-current condition.

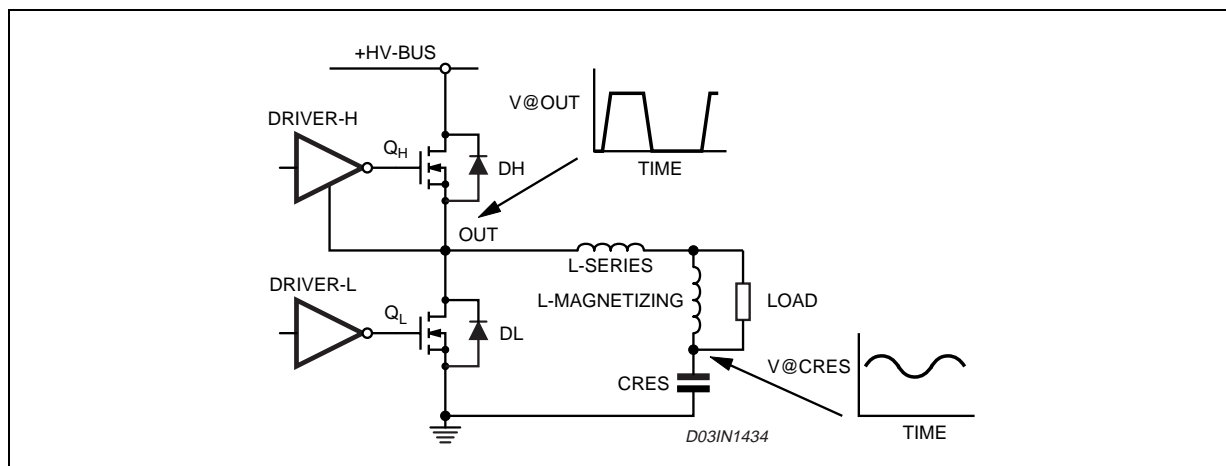
Zero voltage switching is generally considered essential in high frequency-high voltage applications because of the parasitic capacitors of the power devices.

The ZVS topology can suffer from high voltage stresses related to the ringing switch voltage waveform, but the recent efficient way to realize the half bridge connection of the power switches, offers the soft switching features in both, "ON" and "OFF" edges of commutation and so, the full resonant converters to be easy realized.

The device is designed for the applications based on half-bridge topology, working with 50% duty cycle at variable frequency. In this type of converters the control of the output parameters will be accomplished by varying the switching frequency.

The most popular Load Resonant Converters (SR series resonant, PR parallel resonant, LCL type series resonant and so on) can be implemented using this configuration (See fig. 8).

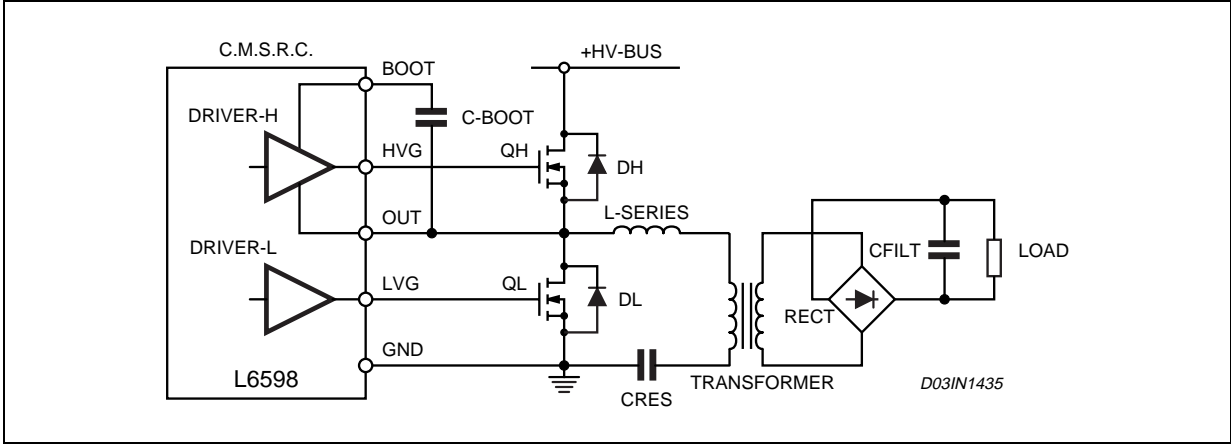
Figure 8. Half Bridge Connection.



In the present discussion (for highest interest on it), we will normally refer to applications realized by using a transformer (T) in charge of to separate the load from the mains.

Moreover, because of the device operation mode, the continuous mode resonant converter is the configuration of our interest (Ref fig.9). In particular, we will refer to the LCL.

Figure 9. Insulated LCL converter



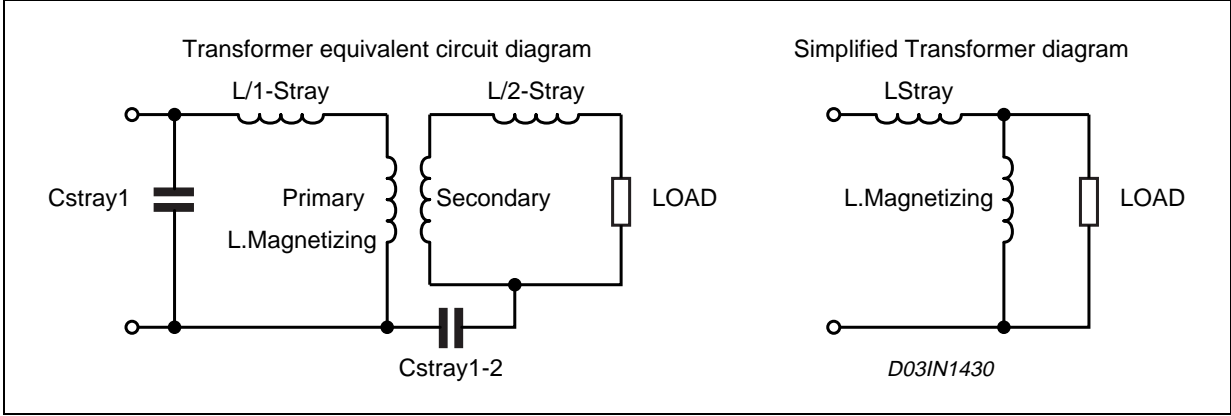
Resonant circuits.

Any resonant circuit includes capacitors and inductors. Since we deal about applications using the transformer, it can be useful to recall the equivalent scheme of the transformer (fig.10), with its simplification and parameters.

The stray inductance is the one that can be measured from the primary side with the secondary winding in short circuit connection. The magnetizing inductance is the one that can be measured from the primary opening the secondary. The parasitic capacitors will not be considered.

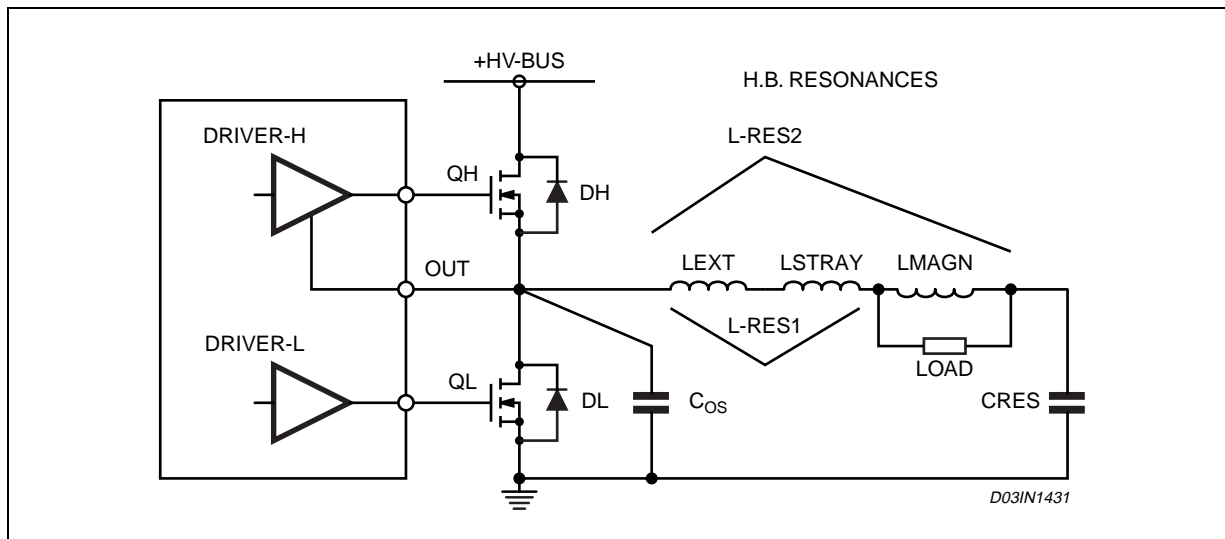
The simplified diagram of the transformer is acceptable for the present circuits discussion.

Figure 10. Transformer equivalent circuit



We can now define some basic resonance circuits and their inherent impact on the application, (ref. to fig.11).

Figure 11. Resonance's LCL-Resonant Converter



In the diagram at Fig.11, it can be observed the net circuit (seen from the OUT node) driven by the half bridge totem pole. The circuit path consists in the series of a determine inductors (L_{RES1}), the primary of the transformer ($L_{Mag.} // Load$) and the resonant capacitor (C_{RES}). We call the series of the L_{RES1} and the Magnetizing inductance ($L_{Mag.}$) L_{RES2} .

The C_{OS} , placed between OUT and ground, is the equivalent capacitance seen at the driving node (related to the power switches and to the circuit's distributed capacitors).

Let's start calling basic resonance the one concerning the circuit path net $C_{OS} + L_{RES} + C_{RES}$.

Where L_{RES} can range between L_{RES1} and L_{RES2} depending on the Load value.

Assuming the C_{RES} (tens or hundreds nF) value much higher than the C_{OS} one (C_{OS} is normally in the range of nF or lower values), we can just consider the series $C_{OS} + L_{RES}$.

This basic resonance concerns the soft switching operation.

Soft switching.

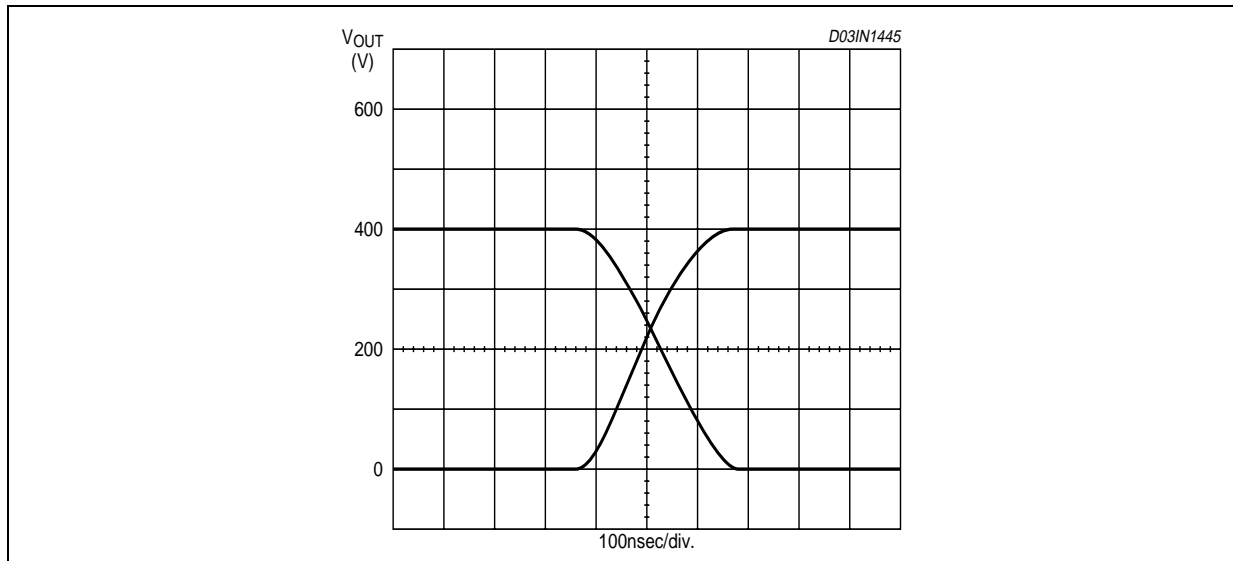
Still referring to figure 10: The external active switch (Q_H) is cut off before the current across the inductance reaches its zero (the active time is less than half period), the current is so forced to flow from the node OUT; initially discharging C_{OS} then, as the voltage cross the voltage threshold, throw the free wheeling diode D_L .

After a short time ($\approx 300ns$), when the Drain-Source voltage of Q_L is close to zero, the inherent gate driver will be activated confirming its "ON" state.

The same will arises at the second half period: Driving off the active Q_L produces the commutation of the node Out thanks to the energy transferred from the coil L_{RES} to the capacitance C_{ox} and the resulting activation of the opposite diode D_H .

Both the rising and the falling edges of the commutation can be considered as portions of the "above defined basic resonance. In Fig.12 it can be observed the portion of sine shaped of the Out node commutations.

Figure 12. Soft switching



This way to operate allows the "zero-voltage switching" thus dramatically reducing the switching losses and improving the noise immunity of the system.

To operate in soft switching, it has to be ensured that the gate cut-off is forced before the current, flowing in the load, reaches the zero or its polarity is reversed. As can be easily realized, care will be taken in order to do not disconnect the OUT node.

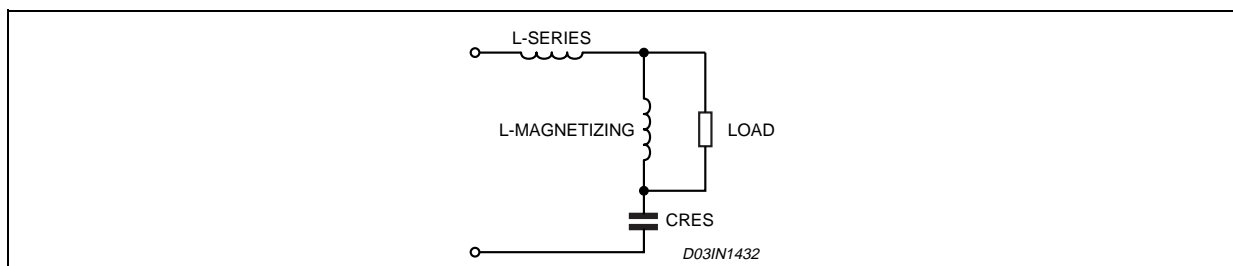
The basic resonance and its consistent soft switching operation, is essential for resonant converters even if it is not involved in the energy regulation.

Varying the frequency for the regulation.

As the soft switching condition can be ensured, let us proceed describing the resonant circuitry that allows controlling the output by varying the switching frequency.

The resonant path is inherent to the circuit $L_{RES} + L_{MAGNETIZING} // L_{LOAD} + C_{RES}$ (see fig. 13) and its resonance is applicable to modulate the energy transferred to the output (Load), varying the frequency.

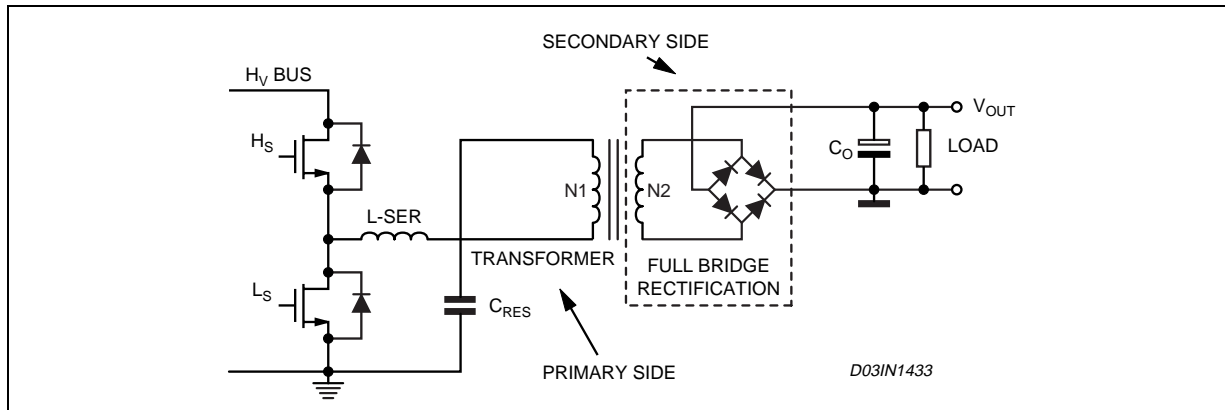
Figure 13. LCL resonant path



The Load block (connected in parallel to the magnetizing inductor) includes the load "seen at the secondary" reflected back to the primary.

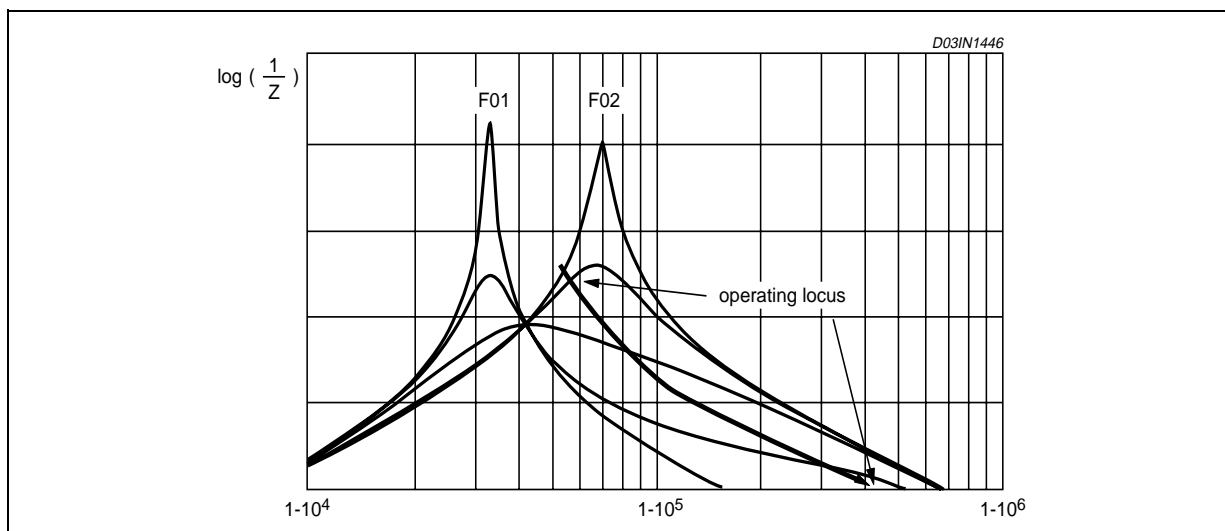
Now, we must consider that the load could vary much (the extreme limits are the short circuit and the open load). Moreover, in the real converter (see fig14), the load includes a rectifier section and the output filter. Therefore, even in the limits of the single cycle, the load changes much and the $L_{MAGNETIZING}$ can be seen in parallel to a very low impedance during the diode conduction (charging C_o) and to very high impedance as the diode is cut off (i.e. as the instantaneous voltage at the anode drops down lower than the output one).

Figure 14. Simplified real converter



Consistent with the above consideration, we can see the circuit as a multiple resonant path. E.g. in the family of curves depicted in fig.15, it can be observed the trend of the admittance as a function of the frequency, for different resistive load.

Figure 15. Multiple Resonance



We have two separate peak of resonance:

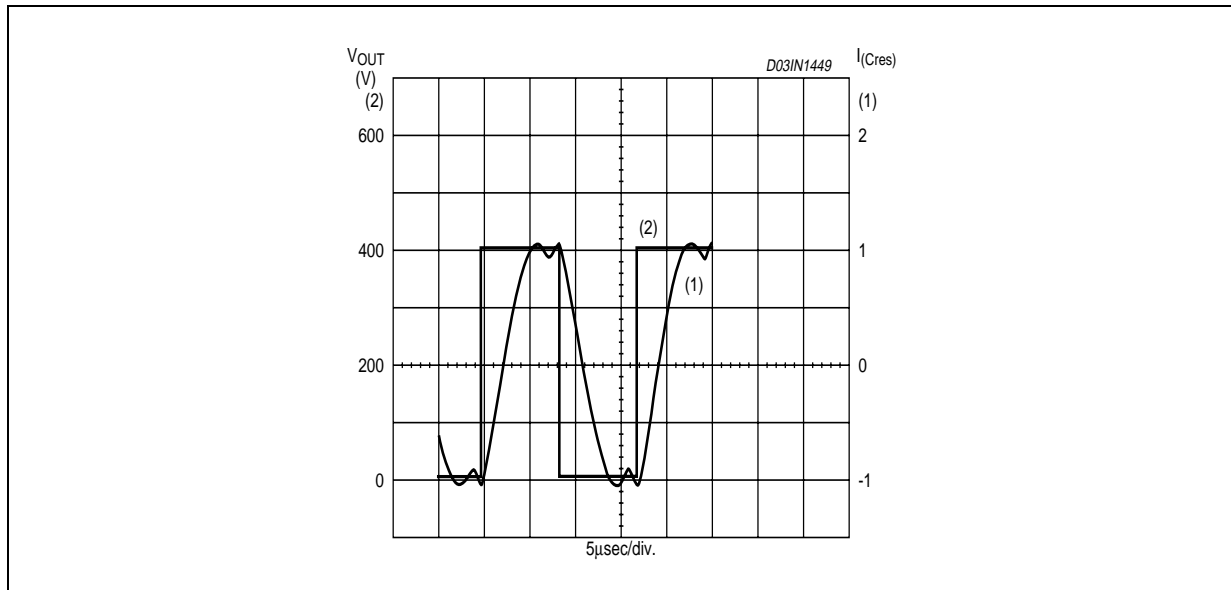
The first peak (F01, lower in frequency) is inherent to the magnetizing inductance (in series with the L.Ext. if one is connected) it is the case with the load open. The second resonance (F02) depends on the series inductance L_{SERIES} (case in which the load is much heavy or during the rectifier's conduction phase).

Both the resonance play a role in the energy transferred to the load and its control.

We can start to discuss assuming the value of the magnetizing inductance (L-MAGNETIZING) is so high that its current is negligible for the frequency range of our interest.

In this hypothesis, it is evident that the maximum current will occurs at the peak of F02 resonance; it should not be reasonable to operate at frequency lower than F02 in order do not loosing the zero-voltage switching and also because the energy transferred to the load should not longer be increased reducing the frequency.

In the practice, for the real transformer, the magnetizing inductance can't be negligible (its value will not be so high). Anyway it should be possible to control its value making so it possible to operate at switching frequency lower than the F02 (See fig16).

Figure 16. $V_{out} + I_{(Cres)}$ characteristics.

The control of magnetizing inductance (in the LCL topology) can play an important role in the energy management; its value (and its ratio with L-SERIES) will affect more than one behavior of the application.

Assuming the load is disconnected, the maximum current occurs at the peak of F01 resonance that concerns the path $L_{MAGNETIZING} + C_{RES}$.

The value of the magnetizing inductance will be (usually) significantly higher than the series inductance, consistently; the "lowest" resonance (F01) is mainly dependant on its values.

We can define F01 "lowest" resonance to well remind that the switching frequency must not be lower than its value.

In fact, forcing the half bridge working at lower frequency (F01), the series circuit represents a capacitive load. This condition cannot be accepted in the application for the following reasons:

- In capacitive load the "zero voltage switch operation" is lost with resulting significant power dissipation (hard switching).
- In closed loop, the transfer function should be reversed (when going in below resonance) and the control should be lost.

To summarize:

It is needed to operate in the "inductive region" of the curve. In this way, the higher frequency applied to the resonant net, the lower is the resulting power.

It is remarkable that, working in the deep inductive mode (far from the peak of resonance), the current moves from sinusoidal shape to triangular and wide frequency change is requested to control the regulation.

On the contrary, working as close as possible to the resonance, for a given load change, the frequency variation will be minimized.

If the application is designed to operate between to the "lowest" resonance (F01) and the second resonance (F02), it will be verified that the primary current (at the switch off time of one of the two Powermos), should not be too low in order to ensure the energy needed for soft switching in all condition.

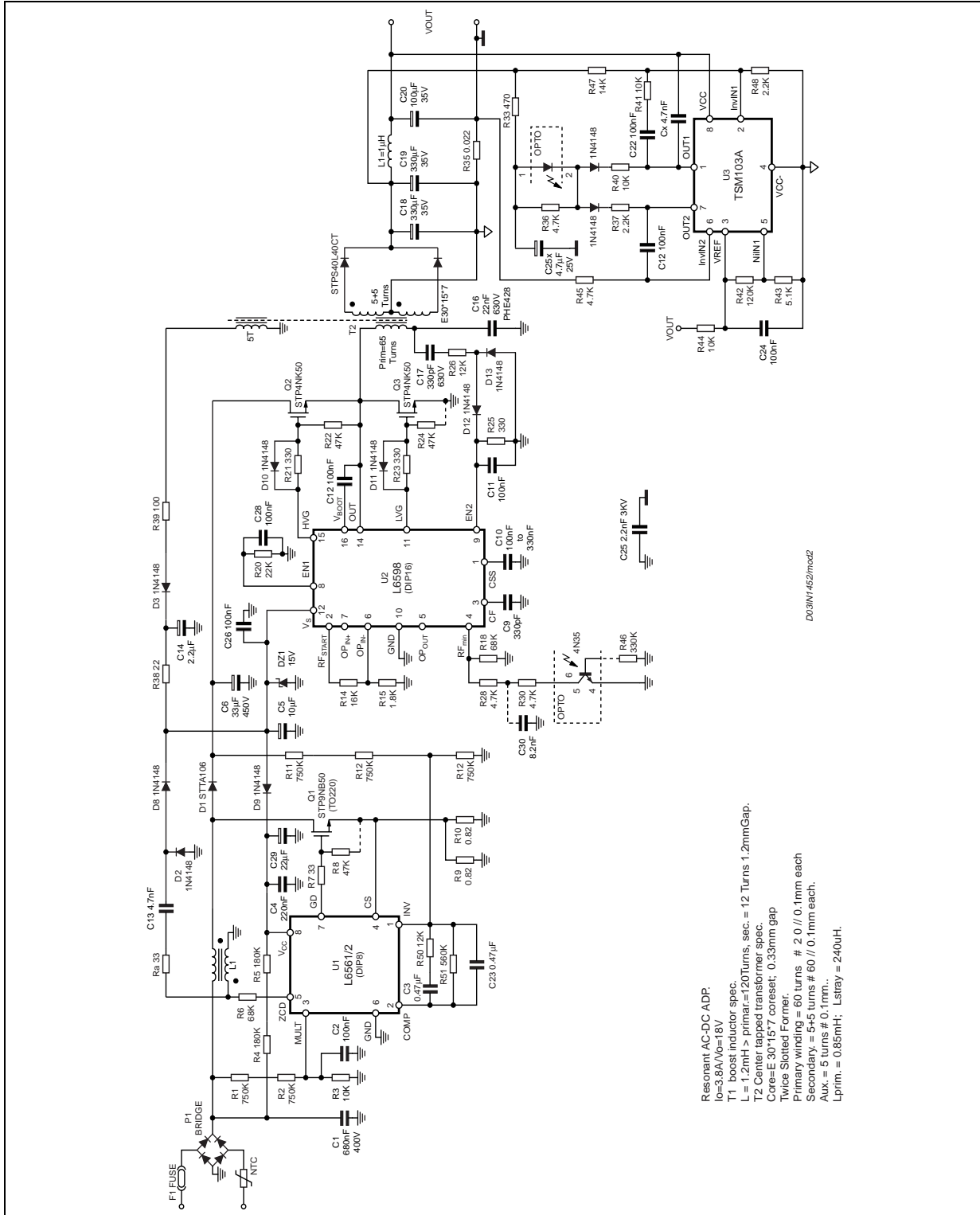
The L6598 function and the resonance's effects in the regulation have been discussed. Now we can start to describe some design criteria.

AN1673 APPLICATION NOTE

DESIGN CRITERIA AND APPLICATION TIPS.

The description of design flow is referred to the implementation of the demo-board prototype used for evaluation. The whole schematic that comes from the design process below described is shown in fig. 17.

Figure 17. Diagram of the application



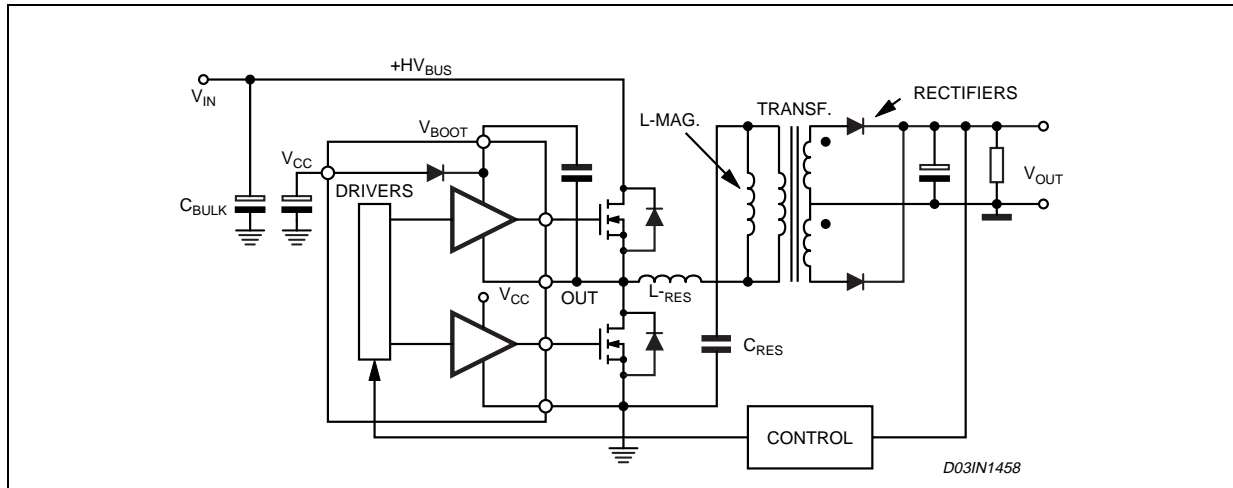
For the PFC portion of the entire application, it will be dedicated a small section with a concise description and a reference for the specific application note.

The following design discussion will be limited to the resonant converter.

Design process:

The converter block diagram can be separate in some basic blocks as in fig.18.

Figure 18. LCL. Resonant converter



Output rectification and filtering; Transformer and resonant parts (Lres-Cres); Half Bridge; Driver Controls
 The target specification is given for 70W AC Adapter, here follows the parameters and requirements: -
 – Output voltage VO=18V and maximum rated current controlled at IO=3.8 to 4A.
 – Wide range mains input 85V to 264 V.
 – High power factor required (P.F.C. needed); +Vbus should be 360V to 420V

Based on these values we can start designing the output stage filter:

– The current relations at the secondary side ("contiguous sine shaped" hypothesis):

$$[10] \quad I_{opk} = I_o \cdot \frac{\pi}{2} = 6.28A; \quad I_{orms} = \frac{I_{opk}}{\sqrt{2}} = 4.44A; \quad I_{crms} = \sqrt{I_{orms}^2 - I_o^2} = 1.93A$$

Output filter and rectification.

Need to be used good quality electrolytic capacitors; the output voltage ripple is function of the equivalent series resistor (ESR) (the contribution of the capacitance is negligible).

Set the limit to <1% using:

$$[11] \quad ESR \leq \frac{\partial V_o}{I_{opk}} = \frac{180mV}{6.28A} \leq 29m\Omega$$

This is obtained using two capacitors (330µF with ESR=75 mΩ each). The power dissipated inside the capacitors will results 140mW at the maximum rated output current. [12/13] the voltage ripple should around 240mV.

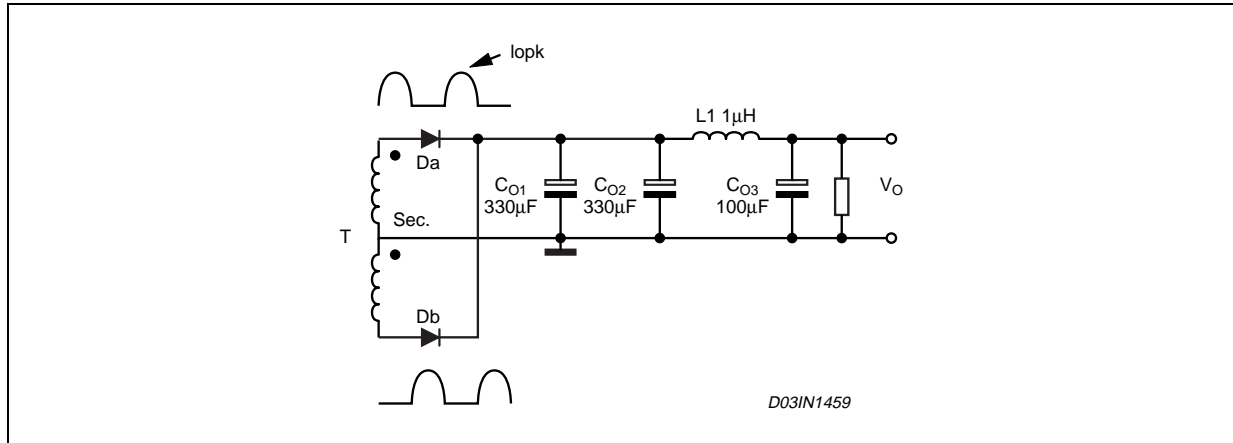
$$[12] \quad PC_o = I_{Corms}^2 \cdot ESR = 140mW; \quad \partial V_o = \sqrt{ESR^2 + XC_o} \cdot 1 - pk = 240mV$$

AN1673 APPLICATION NOTE

The connection of a second L*C filter's cell can be much effective to limit the output voltage ripple, without exceeding a reasonable high quality capacitor number.

In our case, a low price inductance ($L1=1\mu\text{H}$) and a $100\mu\text{F}$ - $180\text{ m}\Omega$ ESR, reduces the high frequency voltage ripple down to 80mV (See fig.19)

Figure 19. Output rectification and filtering



Because of the output Current/Voltage ratio, the output rectification stage can represent most of the power dissipated in this kind of application.

For the present application, the efficiency is significantly improved choosing the center-tapped connection; this allows to half the power dissipated on the output rectifiers. Using this solution, care will be taken in winding up the secondary in order to get a good coupling between the two secondary and for a good symmetry in the current waveforms.

For our design, choose the STPS40L40CT that is a low drop power schottky diode in TO220AB package ($V_{th} = 0.28\text{V}$; $R_d = 0.0105\Omega$; $B_V = 40\text{V}$).

The power dissipated on the rectifier can be estimated using the sinusoidal model:

– @ $I_o = 4\text{A}$

The peak current of secondary diode $I_{dp} = \frac{I_o \cdot \pi}{2}$ $I_{dp} = 6.3\text{A}$; $I_{rms} = \frac{I_{dp}}{\sqrt{2}}$ $I_{rms} = 4.45\text{A}$;

$$[13] \quad P_D = V_{th} \cdot I_o + R_d \cdot I_{orms}^2 \quad P_D = 1.35\text{W}$$

– The reverse peak-voltage of Diode $\geq V_o \cdot 2 \geq 36\text{V}$

Transformer design:

The LCL resonant configuration requires a resonant inductor ($L_{ser.}$) placed in series to the transformer's primary and to the resonant capacitor ($C_{res.}$). This inductor plays an important role and its value controls the current peak during the energy-transferred phase (or in extreme heavy load conditions).

Since the primary path will be submitted to high frequency alternate current (with a significant large flux density swing ΔB), a high quality resonant inductor should be needed in order to limit the coil's power dissipation.

In much real design, the stray inductance of the transformer can efficiently replace any external resonant inductor (or minimize its value).

We adopt this solution that allows saving the part and limits the magnetic power dissipation.

The leakage inductance (L_{stray}) parameter is not easy to be design and usually it requires some mechanical tricks for obtaining a significant value. Anyway, as soon as the transformer is defined, the stray inductance value will be constant enough and its spread limited.

Apart of this, the first step is to choose the size of the magnetic set.

Using the "Product Area" (AP) criterion, we can get a first approximation of the core area product. The required AP can be found using the equations Ap1 and Ap2 (we use the same formulas as for the standard half bridge forward converter).

AP (=AW*Ae) is the winding area (AW, associated to the former) time the magnetic cross section (Ae, associated to the ferrite).

N.B. For choosing the resonant elements (inductance and capacitor) and its relation with the frequency to be set, one can have an easy task referring to the convention described in appendix A.

– Start choosing the minimum operative frequency (corresponding to full load) at 65kHz.

$$[14] \quad \text{Ap1) } AP1 = \left(\frac{41.7 \cdot \text{Pin}}{K \cdot f_{sw}} \right)^{1.58} \cdot (K_h \cdot ft + K_e \cdot ft^2)^{0.66} \quad \# \text{ related to core losses limit}$$

Where: $K_h = 4 \cdot 10^{-5}$; $K_e = 4 \cdot 10^{-10}$; $f_{sw} = 65\text{kHz}$

For the present design, $AP1 = 0.38\text{cm}^4$

$$[15] \quad \text{Ap2) } AP2 = \left(\frac{11.1 \cdot \text{Pin}}{K \cdot \Delta B_{max} \cdot f_{sw}} \right)^{1.31} \quad \# \text{ related to saturation limit}$$

Where:

$K = 0.165$ related to the Half Bridge connection; $\Delta B_{max} 0.4\text{T}$; Pin is the power handled by the transformer.

In the present design, should be $AP2 = 0.17\text{cm}^4$

The needed AP will be the larger of the two resulting values.

To met the current target specification, we need $AP = AP1 = 0.38\text{cm}^4$.

Select the ferrite's set EE30 (E30 · 15 · 7) in high frequency (e.g. B2 or F1) material.

($V_e = 3.9\text{cm}^3$; $A_w = 0.8 \text{cm}^2$; $A_e = 0.6\text{cm}^2$) $\Rightarrow AP = A_w \cdot A_e = 0.48 \text{cm}^4$.

Transformer's Winding

To define the winding, first it must be fixed the input DC Bus value.

Since in the discussed design the pre regulator stage (see later in Power Factor section) is requested, let's start fixing the voltage bus range at 360V to 420V.

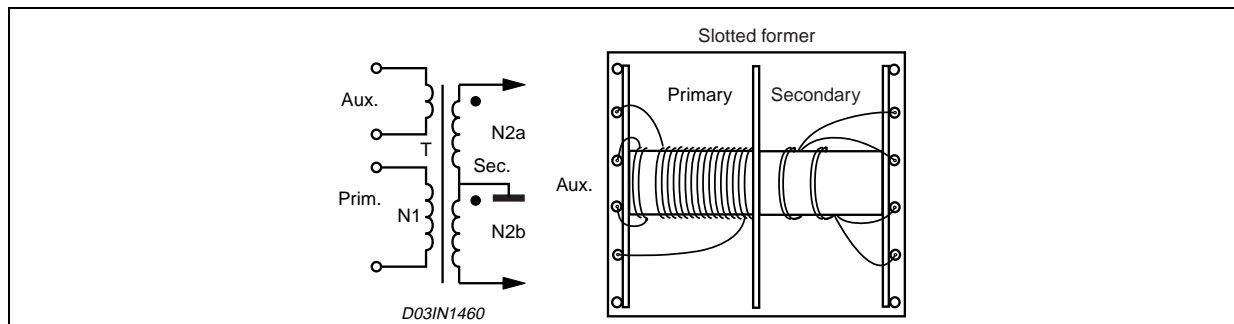
The second resonant inductor of the LCL resonant converter can be achieved managing the proper value of primary inductance of Transformer.

This second inductance allows to properly operating in light load condition holding in the same time the higher efficiency for the entire load range. In our experience, to take advantage by using the primary inductance as second inductor, a good ratio between its value and the stray inductance (L_{mag}/L_{stray}) is in the range of 3.5 to 7.

The relation between the primary and the stray inductances can be adjusted using the slotted bobbin (that increases the stray inductance) and introducing an air gap in the transformer's ferrite set (that reduces the magnetizing inductance).

We choose a two layer slotted former (split the primary and secondary sides). See fig.20.

Figure 20. Transformer



AN1673 APPLICATION NOTE

The design of the winding starts calculating the minimum requested primary turns number.
For turns number calculation:

$$[16] \quad N_P = \frac{V_{in(min)} \cdot 10^4}{8 \cdot \Delta B \cdot f_{sw} \cdot A_e}; N_P \geq 50$$

Where: $V_{in(min)} = 360V$; $\Delta B = 0.230T$ (*); $A_e = 0.6cm^2$

(*) In the case AP is defined by the AP1, ΔB is calculated by the formula [17].

$$[17] \quad \Delta B = \left(\frac{P_{cv}}{kh \cdot f_{sw} + Ke \cdot f_{sw}^2} \right)^{\frac{1}{2.4}} = 0.230T$$

where: $P_{cv} = \frac{P_t}{2 \cdot V_e}$; $P_t = 1.3 \cdot AP1^{0.37}$

Instead, in the case that AP should be AP2, ΔB_{max} will be fixed by the designer (up to 0.400Tesla).

Choose primary turns number $N_p = 60$

The turn's ($n = N_p/N_s$) ratio will define the secondary winding turns number.

$$[18] \quad n = \frac{V_{in(min)} \cdot \text{duty}}{V_o + V_f}; n = 10$$

Where: $\text{duty} = 0.5$;

Choose $n = 12^*$; Secondary turns $N_s = 5^{**}$

* The ratio n can be significantly higher than [18] because of the L_{mag} effect

** The secondary winding is realized with $N_s = 5+5$ turns because of the center-tapped solution.

In order to limit skin effect (and the inherent power losses), the Litz wire solution has been adopted for the windings:

- 20 wires 0.1mm each for the primary winding ($\Rightarrow 0.157 \text{ mm}^2$ cross section)
- 60 wires 0.1mm each at the secondary winding ($\Rightarrow 0.47 \text{ mm}^2$ cross section)

As the primary and secondary windings have been defined, we need fix the inductances of the transformer. The formula [19] allows calculating, with good approximation, the value of the primary inductance in function of ferrite set and the gap length, the ferrite's set parameters and the primary turns number.

$$[19] \quad L = \left\{ \frac{10^{-1}}{\mu_0} \cdot \left(\frac{l_e}{\mu_r \cdot A_e} \cdot \frac{0.1 \cdot l_{gap}}{\left(\sqrt{A_e} + 0.2 \cdot l_{gap} \cdot \frac{\pi}{4} \right)^2} \right) \right\}^{-1} \cdot N_p^2$$

Where: $\mu_0 = 4 \cdot \pi \cdot 10^{-7}$ is the absolute permeability. μ_r is the relative permeability (e.g. 2000)

l_e is the magnetic path length, (in cm). A_e is the effective area (in cm^2).

l_{gap} is the gap size (in mm).

The calculated primary inductance will be in mH. In our case the $L = 0.85 \text{ mH}$.

Concerning the stray inductance, the models used in the standard forward application's transformers are not precise (mainly because the mechanical position). The approximate value can be foreseen using the formula:

$$[20] \quad L_{\text{leak}} \approx \frac{1.3 \cdot lw \cdot Np^2}{bw} \cdot \frac{hw}{3} \cdot 10^{-8} \quad \text{In our case the calculated } L_{\text{leak}} \text{ is } 270\mu\text{H.}$$

Where: $lw = 5.6\text{cm}$; $bw = 0.5\text{cm}$; $hw = 1.55\text{cm}$.

In the real transformer of the present example, the stray inductance (tested at the primary when one of the secondary sections is shorted) is about $240\mu\text{H}$.

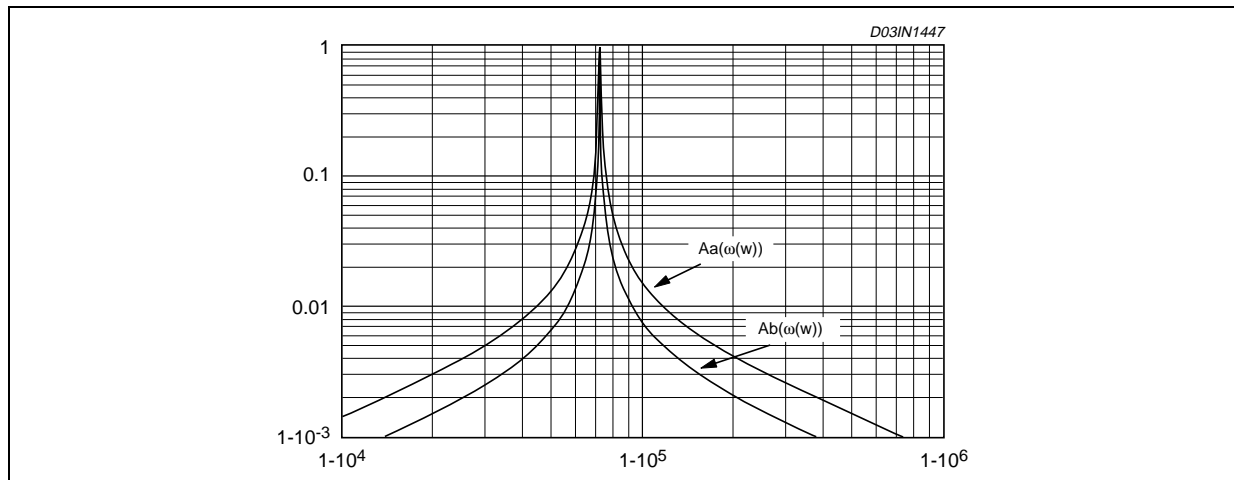
As already told, introducing an air gap in the ferrite set can control the ratio between the primary and the stray inductance. Chose the air gap 0.33mm to get the ratio $Lm/Ls=3.5$,

Resonant capacitor (Cres).

For the resonant capacitor selection, it must be consider its rated current; in fact the current can be an important limit, in particular for low capacitor values. In the polypropylene series capacitor it is usually possible to find the suitable one. On the other side the value of the Cres, for a given resonance's value (see fig.21), profiles the sloop of the resonant curve (Q factor that is function of $\sqrt{L_{\text{res}}/C_{\text{res}}}$), thus changing the impedance change versus the frequency variations.

In our design it has been chosen the $22\text{nF}/630\text{V}$ PHE- (100°C).

Figure 21. Q factor.



Powermos.

Concerning the Powermos to be used in the half bridge, the required class of blocking voltage (Bvdss) is 500V .

Choose STP4NB50 or the equivalent STP4NK50)

The relations and parameters that can be used for calculation:

$$[21] \quad R_{\text{in}} = \frac{8 \cdot V_o}{\pi^2 \cdot I_o} \cdot n^2 = \frac{8 \cdot 18\text{V}}{3.14 \cdot 3.14 \cdot 4\text{A}} \cdot 144 = 525$$

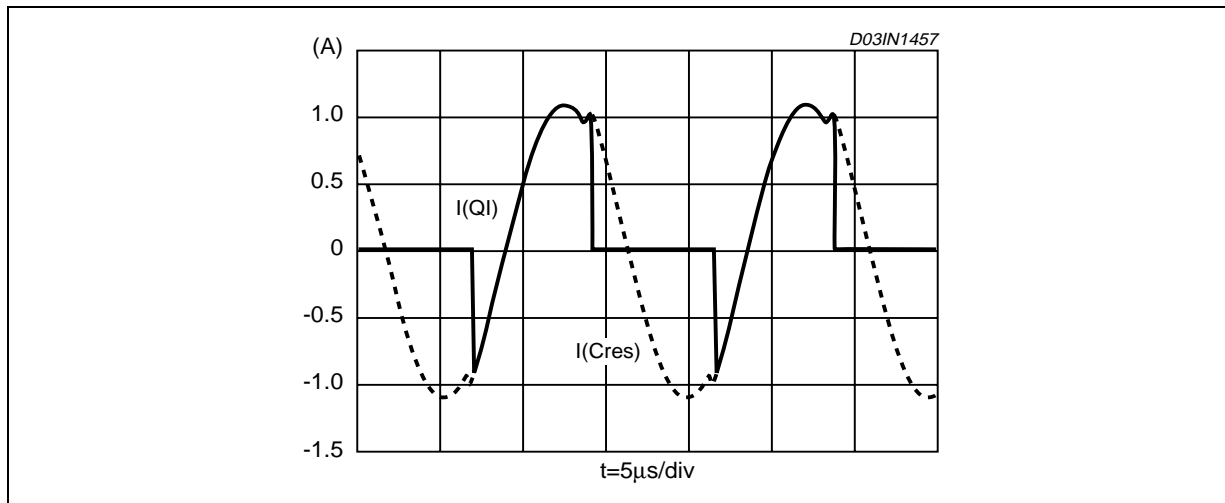
R_{in} : equivalent input resistance (seen at the primary side).

$$[22] \quad I_{\text{Qpk}} \geq \frac{I_o \cdot \pi}{2 \cdot n} \geq \frac{4 \cdot \pi}{24} \geq 0.525$$

AN1673 APPLICATION NOTE

Where: I_{Qpk} : peak of current at the primary side #.

Figure 22. $I(Q) + I(Cres)$ characteristics.



Because the L_m/L_s ratio, a not negligible portion of current managed in the transformer's primary should not be transferred to the load. For this reason, using the formulas for calculate the primary side current (21 & 22), the results will be significantly lower than the tested one see fig 22.

Bulk capacitor C-Bulk.

The relations for design:

$$[23] \quad C_{Bulk} = \frac{P_o}{2 \cdot \pi \cdot 2f \cdot \Delta V_o \cdot V_o}$$

Where ΔV_o is the accepted voltage ripple

$$[24] \quad C_{Bulk} \geq \frac{2 \cdot P_o \cdot t_{Hold}}{V_o^2 - V_{o(min)}^2}$$

Where t_{Hold} is the requested hold-up time and $V_{o(min)}$ the minimum voltage for correct operating.

The key points for selecting the bulk capacitor are in sequence: the rated voltage, the capacitance related to the 100Hz ripple and the Holdup time (on request) see also PFC documentation.

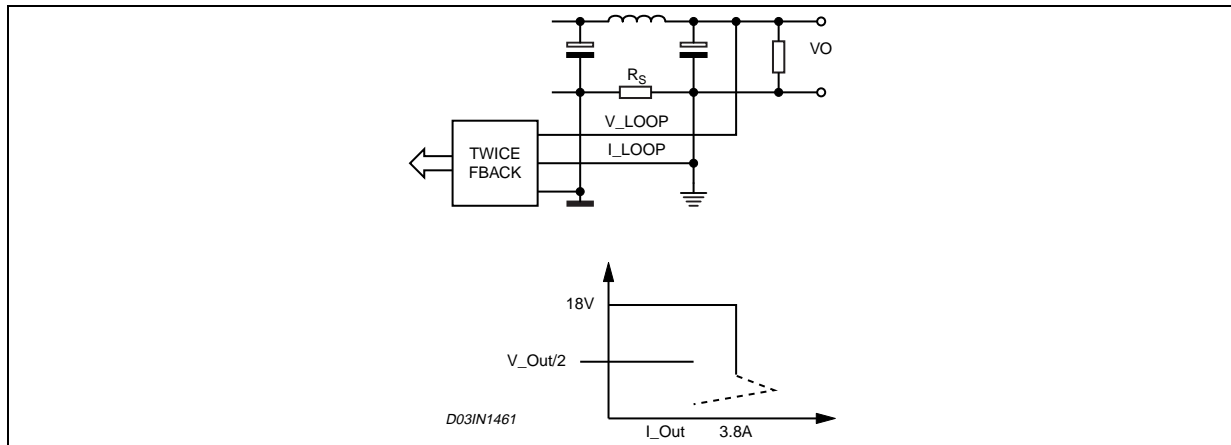
Choose C-bulk (6) = 33µF-450V that involve $\pm 9V$ voltage ripple without fixing any hold-up time.

Control circuits.

The control of the output voltage and current has been realized with twice loop using the TSM103 (Dual amplifier and voltage reference). This component, in addition to an Optic Coupler, allows profiling a full control of the output both of the voltage and the current profile (see fig.23). The control's parameter for the frequency variation is the current drawn from R_{fmin} (pin4). See also Device Operation page 3.

Since the control of the output could not be longer ensured in case of a heavy load (because of very low output voltage e.g. < 5V), at the primary side the current is sensed (by the C17, R26, D12+D13) and as the signal, filtered and feed to the EN2 of the L6598, exceeds the threshold limit the soft start is reactivated.

Figure 23. Output V/I Characteristics.



Miscellaneous.

Few critical points to be considered in design and debugging phases are:

- The frequency accuracy; the actual frequency can be affected by external components (e.g. the precision of C_{osc} and its thermal variation). Moreover, when the C_{osc} is much low, the stray effects must be considered (the pin and PCBs capacitance). The oscillator accuracy can be affected if the current drawn from the references (Pin2_Rfstar and pin4-Rfmin) exceeds $100\mu A$.
- The layout of Pcb and coupled noises: a good criterion for checking the noises is to test the signal at the Cf(pin3) that should be a symmetric triangular waveform in order to ensure the correct drivers duty. Another point to be tested is the voltage at Out(pin14) that, during the freewheeling, should not be too much below ground (few volt).

Power Factor section.

In spite of the PFC stage should not be strictly necessary for the resonant application, in our design it has been introduced for the following reasons.

The front-end stage of conventional off-line converters, consists of a full wave rectifier bridge with a capacitor filter, gets an unregulated DC bus from the AC mains. Therefore the instantaneous line voltage is below the voltage on the capacitor most of the time, thus the rectifiers conduct only for a small portion of each line half-cycle. The current drawn from the mains is then a series of narrow pulses whose amplitude is 5-10 times higher than the resulting DC value.

Lots of drawbacks result from that: much higher peak and RMS current drawn from the line, distortion of the AC line voltage, over currents in the neutral line of the three-phase systems and, after all, a poor utilization of the power system's energy capability.

This can be measured in terms of either Total Harmonic Distortion (THD), as norms provides for, or Power Factor (PF), intended as the ratio between the real power (the one transferred to the output) and the apparent power (RMS line voltage times RMS line current) drawn from the mains, which is more immediate. A traditional input stage with capacitive filter has a low PF (0.5-0.7) and a high THD ($> 100\%$).

The International norms and standard requirements have spurred the design of high power factor.

For these reasons power factor corrector (PFC) is now diffusing in off-line power management. With a high power factor switching pre regulator, interposed between the input rectifier bridge and the bulk filter capacitor, the power factor will be improved (up to 0.99). The current capability is increased; the bulk capacitor peak current and the harmonic disturbances are reduced.

Moreover, the PFC with its pre regulated high voltage bus, provides an important advantage, because operating at fixed DC input, it makes much easier the resonant converter to be controlled.

The L6561 is an integrated controller dedicated to PFC stage by using the transition mode technique and is optimized for low to medium power applications.

AN1673 APPLICATION NOTE

The PFC section of the present application has been designed to pre regulate 400V and to deliver 80W. The AC mains voltage can range from 85V to 264 V.

For a detailed description of the L6561 operation, refer to AN966.

Evaluation result.

The demo board has been evaluated in two different modes. The first evaluation (see table_01) has been done for the resonant converter section (not included the PFC pre regulator circuit) at two different output power levels.

In practice the resonant converter has been supplied using a 400V DC power supply and it has been evaluated its efficiency.

Table 1.

Input supply Voltage = +400 VDC

Pin=72W	Vo=17.8V	Io=3.8A	Po=67.64	n=93.9%
Pin=39W	Vo=17.8V	Io=2A	Po=35.6	n=91.3%

The second evaluation (see Table 2) has been done for the entire application circuit, including the PFC. The load has been changed as in the first evaluation (3.8A and 2A), moreover it have been set four significant values of the mains voltage according to the requested wide range.

Table 2a.

Output loaded @ 3.8A.

Vin=88Vac	Pin=77.5W	Vo=17.8V	Io=3.8A	Po=67.64	n=87.3%
Vin=110Vac	Pin=76.35W	Vo=17.8V	Io=3.8A	Po=67.64	n=88.6%
Vin=220Vac	Pin=74.7W	Vo=17.8V	Io=3.8A	Po=67.64	n=90.5%
Vin=255 Vac	Pin=74.4W	Vo=17.8V	Io=3.8A	Po=67.64	n=91%

Table 2b.

Half load (@ 2A).

Vin=88Vac	Pin=41W	Vo=17.82V	Io=2A	Po=35.64	n=86.93%
Vin=110Vac	Pin=40.5W	Vo=17.82V	Io=2A	Po=35.64	n=88%
Vin=220Vac	Pin=40.3W	Vo=17.82V	Io=2A	Po=35.64	n=88.4%
Vin=255 Vac	Pin=40.3W	Vo=17.82V	Io=2A	Po=35.64	n=88.4%

APPENDIX A.

A practical way to handle the resonant components is to adopt the normalized voltage and current. The minimum operative frequency has been set at 65kHz. This frequency can be considered a good compromise for holding the transformer's magnetic set low size and to avoid the high frequency problems (e.g. skin effect, switching losses and so on).

Let us fix the normalized out put voltage $M = 0.98$ $\left\{ M \cong \frac{V_o \cdot n}{\frac{V_{in(max)}}{2}} \right\}$

Assume normalized operating current as $J = 0.2$ $\left\{ J \cong \frac{I_o \cdot R_o}{n \cdot \frac{V_{in(max)}}{2}} \right\}$

Where: R_o is characteristic impedance = $\sqrt{\frac{L_r}{C_r}}$

The resonant Z_o can be calculated as $Z_o = \frac{\left(\frac{V_{in}}{2}\right)^2 \cdot J \cdot M}{V_o \cdot I_o}$ $Z_o = 120$

– The resonant capacitor will be: $C_r \cong \frac{1}{Z_o \cdot \omega}$ $C_r \cong \frac{1}{110 \cdot 2\pi \cdot 65 \cdot 10^3} \cong 20\text{nF}$

– The resonant Inductance $L_r \cong \frac{Z_o}{\omega}$ $L_r \cong \frac{110}{2\pi \cdot 65 \cdot 10^3} \cong 295\mu\text{H}$

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