AN2030
APPLICATION NOTE

BACK EMF DETECTION DURING PWM ON TIME BY ST7MC

INTRODUCTION

The direct back EMF sensing scheme used by ST72141 synchronously samples the motor back EMF during PWM “off” time without the need to sense or re-construct the motor neutral in a sensorless BLDC motor drive system. Since this direct back EMF sensing scheme requires minimum PWM “off” time to sample the back EMF signal, the duty cycle can't reach 100%. Also in some applications, i.e. HVAC using high inductance motors, we see the zero crossing detection is unsymmetrical in the ST72141 sensorless drive system at high speed. It is found that the long settling time of a parasitic resonant between the motor inductance and the parasitic capacitance of power devices causes false zero crossing detection of back EMF. This application note provides an analysis of the resonant transient during PWM “off” time. As a result, the back EMF detection during PWM “on” time is used in ST7MC to solve the problem.

1 TRANSIENT ANALYSIS DURING PWM OFF TIME

Generally, a brushless dc motor is driven by a three-phase inverter with what is called six-step commutation. The conducting interval for each phase is 120° by electrical angle. Therefore, only two phases conduct current at any time, leaving the third phase floating. This opens a window to detect the back EMF in the floating winding.

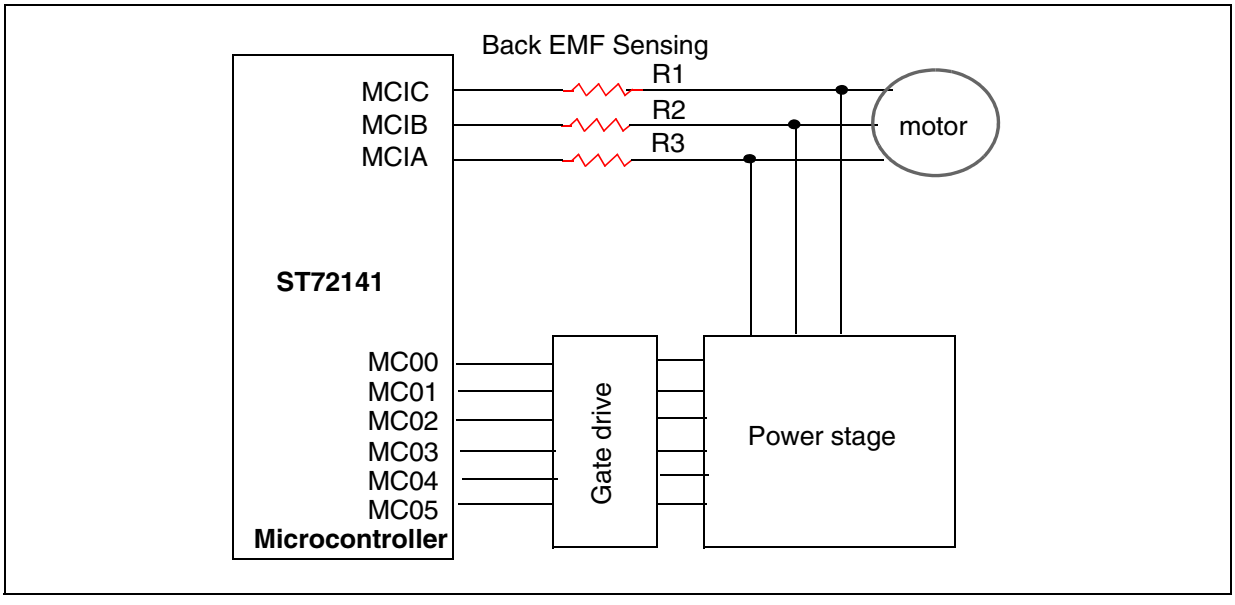
For the direct back EMF sensing scheme, the PWM signal is applied on high side switches only, and the back EMF signal is synchronously sampled during the PWM off time. The low side switches are only switched to commutate the phases of the motor. The true back EMF can be detected during off time of PWM because the terminal voltage of the motor is directly proportional to the phase back EMF during this interval. Also, the back EMF information is referenced to ground, which eliminates the common mode noise; and the synchronous sampling rejects the high-frequency switching noise. Only three resistors are required to detect the back EMF, as shown in Figure 1.

Ideally, the terminal voltage for the floating phase is directly proportional to the back EMF signal in steady state during PWM off time [1]. The equation is as following:

$$v_{a,b,c} = \frac{3}{2} e_{a,b,c} \qquad (1)$$

Where Vx is the terminal voltage, ex is the back EMF of the floating phase.

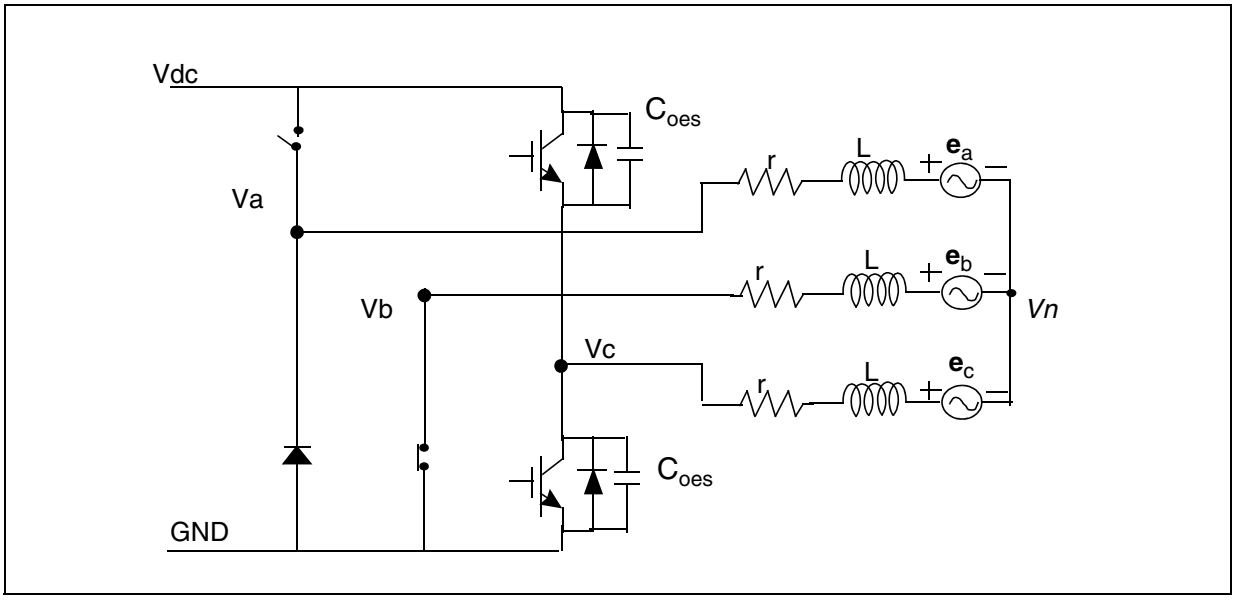
Figure 1. Direct Back EMF Sensing block diagram



The equation (1) is valid only in steady state.

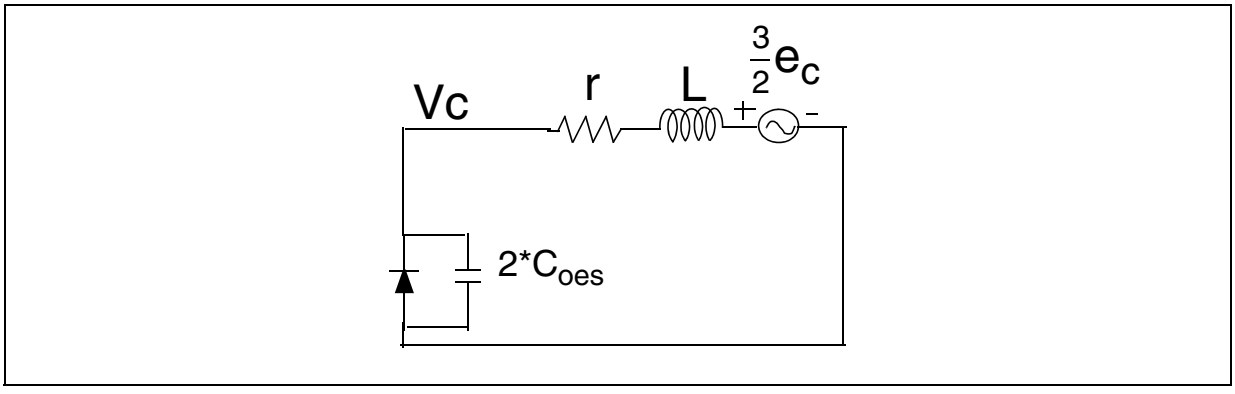
Considering the parasitic capacitance C_{oes} in the switches, the voltage in the floating phase will have some transition time during PWM off time. Figure 2 shows the circuit where the PWM is applied to phases A and B while phase C is floating.

Figure 2. Phase C is floating



We can simplify the circuit by using the neutral voltage Vn=1/2 * ec during PWM off time [1] and during PWM on time (see next chapter) to get the equivalent circuit in Figure 3.

Figure 3. Simplified equivalent circuit when phase C is floating



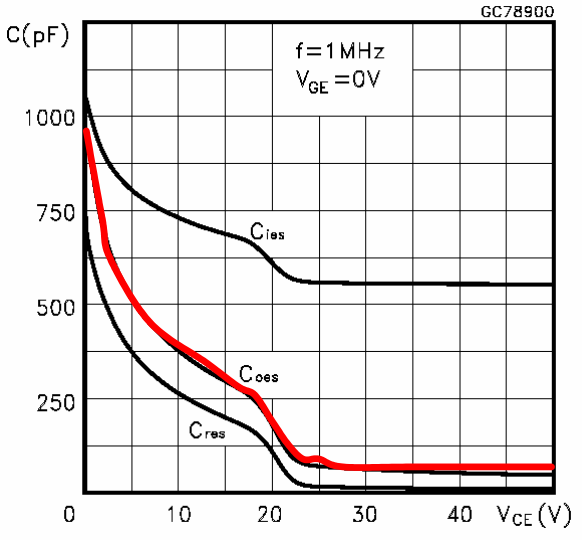
When PWM is on in phase A and B, the terminal voltage in steady state will be:

$$v_c = \frac{1}{2}v_{dc} + \frac{3}{2}e_c \qquad (2)$$

which is the initial condition in the capacitor during PWM off time.

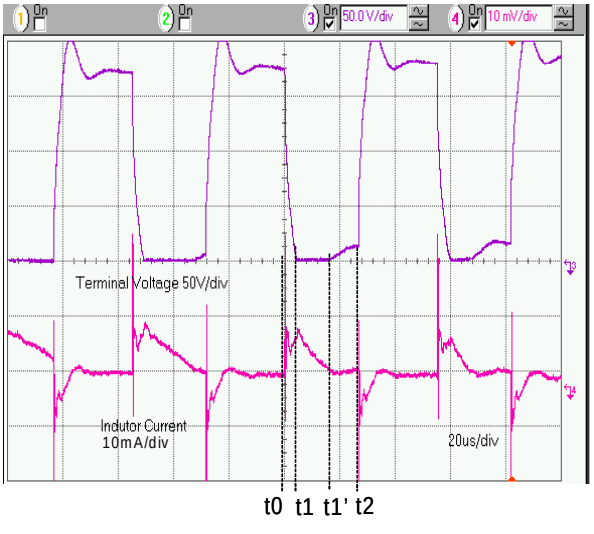
C_{oes} is not a fix value for IGBTs, which depends on the voltage. Figure 4 shows the curve for STGB7NB60HD.

Figure 4. C_{oes} curve



Assuming the back EMF has just passed the rising edge of the zero crossing. When PWM is off, the voltage across the capacitor will be discharged in a resonant way. Figure 5 shows a terminal voltage and the current waveform.

Figure 5. Waveform of floating phase terminal voltage and inductor current



At the time t0, PWM is off.

t0~t1: The capacitor starts to discharge by the inductance. At the beginning, since the capacitance is small, the discharging rate is very fast, but as the voltage reduces, the rate drops. At time t1, the capacitor is fully discharged, and the diode D turns on. The current passes through the diode and the voltage is kept around -0.7v.

t1~t1': The current will decrease linearly from peak to zero because the inductor is reset by (Vd+3/2ec). Vd is the voltage drop of the diode. Large inductance will keep the clamp time longer. At time t1', the inductor current is reset to zero. The back EMF signal shows up in the winding terminal.

Since the back EMF is detected at the end of PWM off period, which is at t2, it is important that the clamp should be ended before t2; otherwise the controller won't be able to detect the zero crossing. Because of the settling time of the resonant transient during PWM off time, the maximum PWM duty is far from 100% duty cycle.

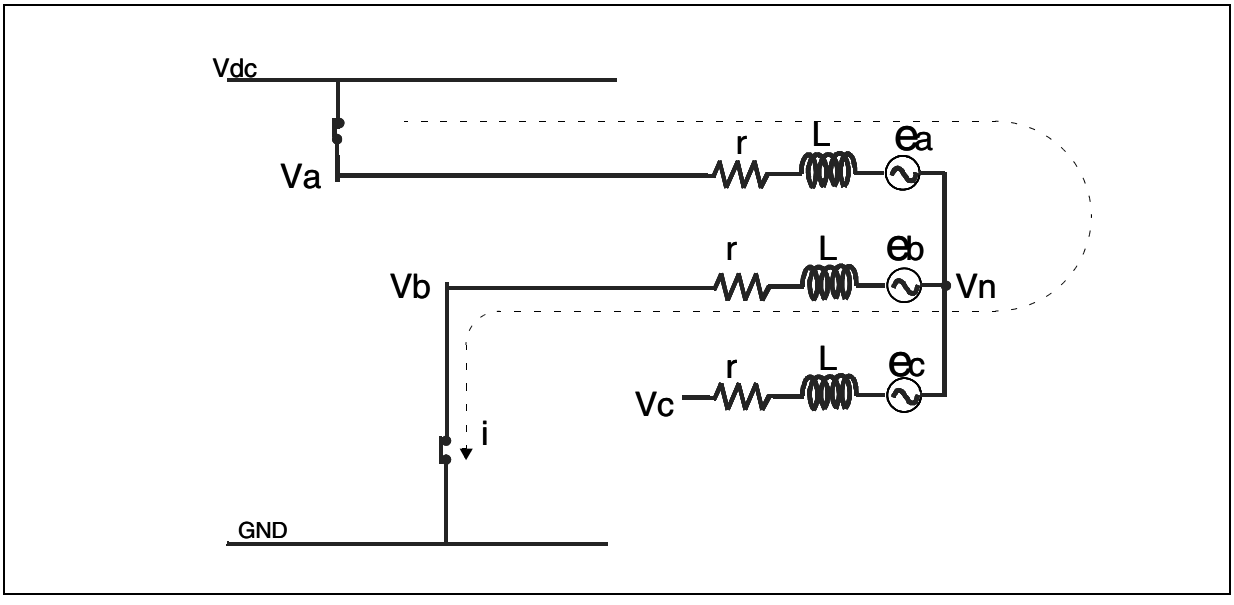
If the back EMF can be detected during on time at high duty cycle, then there is enough time for the resonant transient to settle down. The next chapter explains how to implement it.

2 BACK EMF DETECTION DURING PWM ON TIME

For ST7MC, it is possible to detect the back EMF during PWM on time. At high speed operation (high duty cycle), the controller can detect the back EMF at the end of PWM on time. In this way, the controller avoids the resonant transition time. At low speed operation (low duty cycle), the controller can detect the back EMF at the end of PWM off time. It still has the benefit of no attenuation of back EMF.

First, we can derive the floating phase terminal winding voltage during PWM on time. Assume phase A and B are conducting current, phase C is floating.

Figure 6. Circuit model during PWM on time



From phase A, we have

$$v_n = v_{dc} - ri - L\frac{dt}{dt} - e_a \qquad (3)$$

From phase B, we have

$$v_n = ri + L\frac{di}{dt} - e_b \qquad (4)$$

Voltage drop on power devices is ignored.

From (3) and (4),

$$v_n = \frac{v_{dc}}{2} - \frac{e_a + e_b}{2} \qquad (5)$$

Also from the balance three-phase system, considering fundamental frequency only, we have

$$e_a + e_b + e_c = 0 \qquad (6)$$

From (5) and (6),

$$v_n = \frac{v_{dc}}{2} + \frac{e_c}{2} \qquad (7)$$

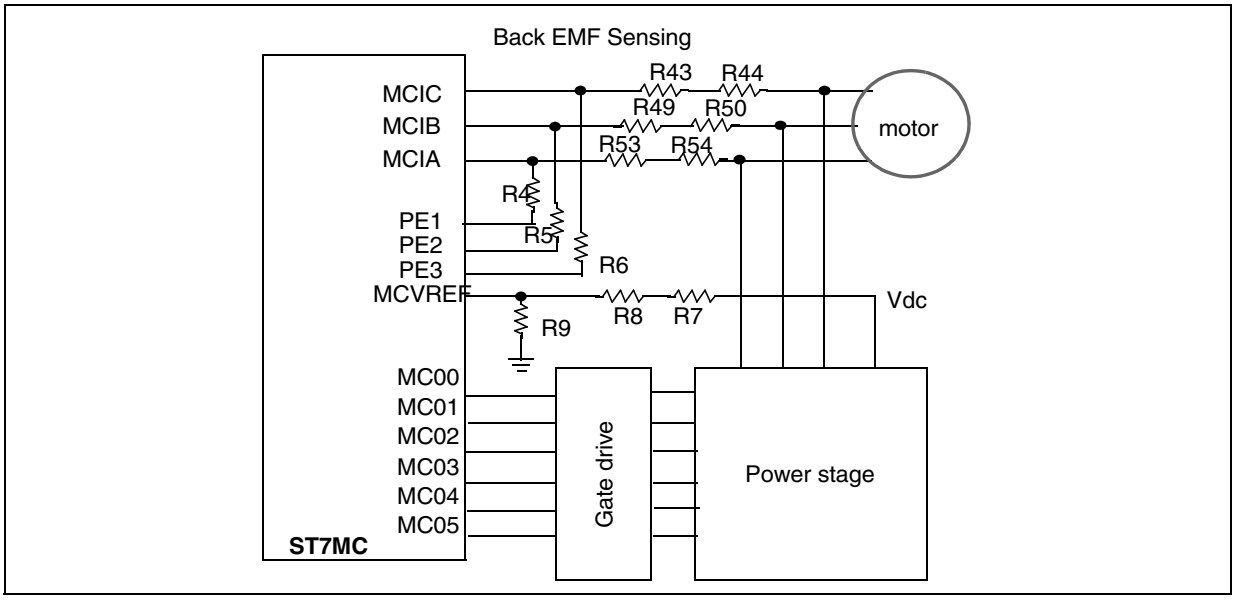
So, the terminal voltage Vc,

$$v_c = e_c + v_n = \frac{3}{2}e_c + \frac{v_{dc}}{2} \qquad (8)$$

During PWM on time, if the terminal voltage is compared to half of the dc voltage, the zero crossing of the back EMF is able to be detected.

The following implementation is based on the ST7MC starter kit.

Figure 7. Hardware implementation



At low PWM duty cycle, PE1, PE2 and PE3 are configured as floating input. There is no attenuation for the signals since R4, R5 and R6 connect to the floating points. The microcontroller detects the zero crossing of the back EMF during PWM off time. The reference voltage is internally set. Then at high duty cycle, PE1, PE2 and PE3 are re-configured as output, set to logic low. All signals are then attenuated by resistor ratio. Meanwhile, the microcontroller will use external voltage, attenuated dc bus voltage Vdc, as the reference for zero crossing detection.

In the starter kit, R43=R44=R49=R50=R53=R54=82k. We should select appropriate resistors for different dc voltage, as shown in the following table.

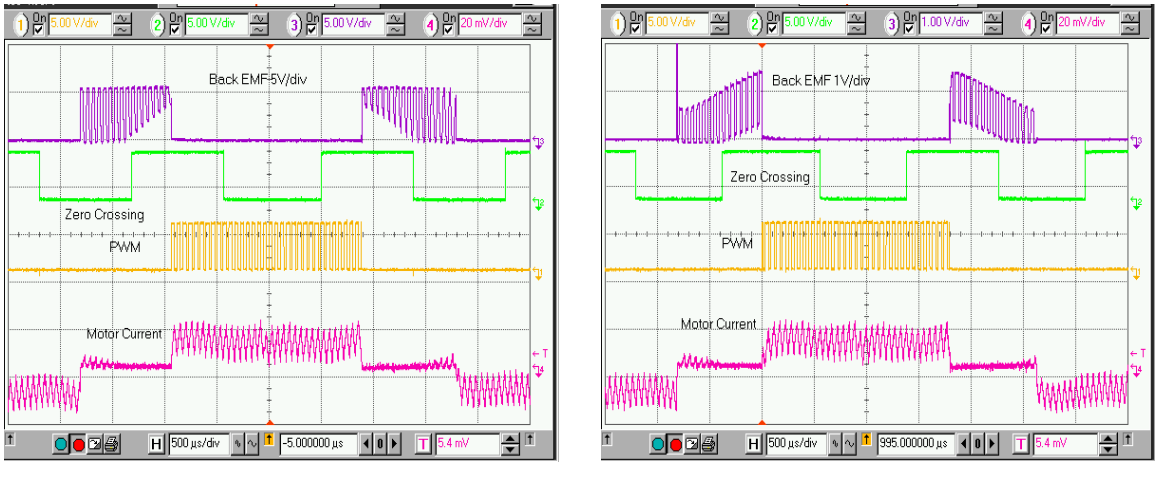
Table 1. Table Resistor selection

Vdc (V)		R4 (k)	R5(k)	R6(k)	R7(k)	R8(k)	R9(k)	Vref(V)
12		100	100	100	150	4.3	36	2.27
24		33	33	33	160	4.7	15	2.00
48		16	16	16	240	18	12	2.13
165		4.7	4.7	4.7	330	2.7	4.7	2.30
330		2.2	2.2	2.2	430	330	5.1	2.20

It is preferred to use 1% resistors. But the performance will be acceptable using 5% resistors. D16, D17, D18, R45, R51, and R55 in the starter kit can be removed if this new scheme is used.

Figure 8 shows the comparison of back EMF detection during off time vs on time. If the back EMF is detected during off, there is no attenuation. The signal is clamped at 5v. If the back EMF is detected during PWM on time, the signal is attenuated.

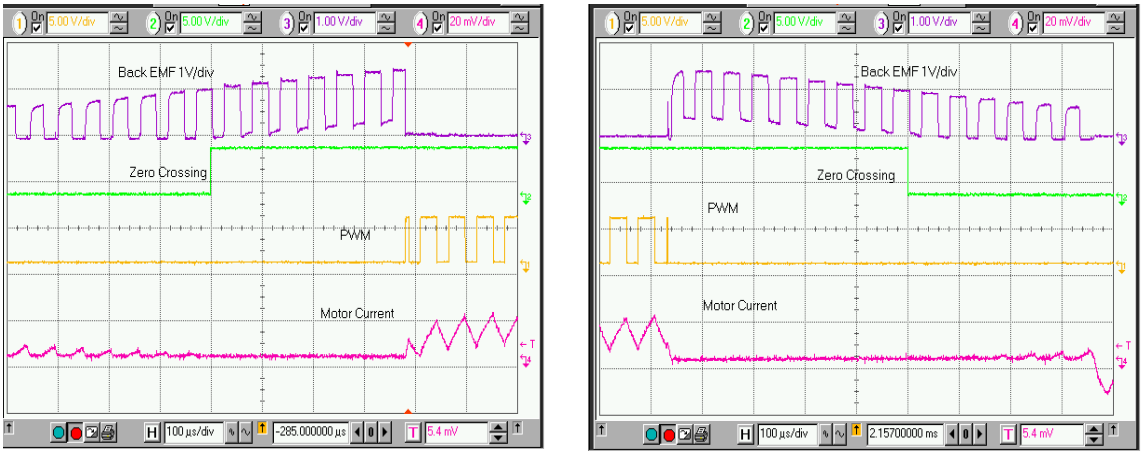
Figure 8. (A) Waveforms for back EMF detection during PWM off time; (B) waveforms for back EMF detection during PWM on time.



(A) (B)

Figure 9 shows the detailed waveform of the zero crossing when the back EMF is detected during PWM on time. From the waveform, we can see that the zero crossing is detected at the end of PWM on time.

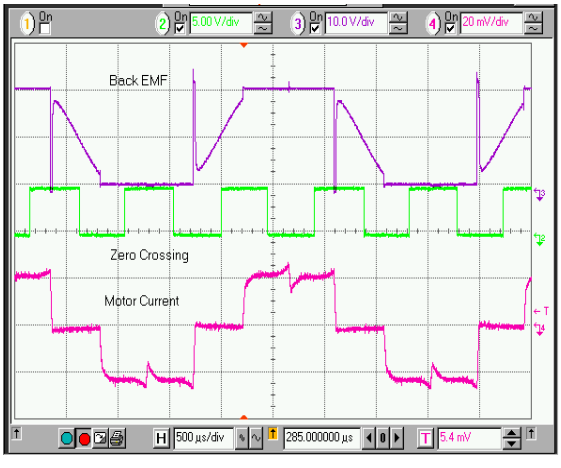
Figure 9. (A) Rising edge of zero crossing for back EMF detection during on time; (B) falling edge of zero crossing for back EMF during on time.



(A) (B)

Figure 10 demonstrates that the system is able to run at 100% duty cycle, and the zero crossing happens at the half of the dc bus voltage.

Figure 10. Waveforms for 100% duty cycle operation.



The software needs some modification as well, which is listed in the appendix.

3 CONCLUSION

The original direct back EMF sensing scheme has the limitation of duty cycle since it requires minimum PWM off time to do the detection. The resonant transient caused by motor inductance and power devices' parasitic capacitance will further limit the duty cycle. The improved direct back EMF sensing scheme, which does the back EMF sensing during PWM on time, eliminates the duty cycle limitation. It can run at 100% duty cycle, and avoid the parasitic resonant transient. During motor start-up and low speed, it is preferable to use the original scheme since there is no signal attenuation; while at high speed, the system can switched to the improved back EMF sensing scheme. With the combination of two detection schemes in one system, the motor can run very well over a wide speed range.

4 REFERENCE

[1] [J.Shao, D.Nolan, and T.Hopkins, “A Novel Direct Back EMF Detection for Sensorless Brushless DC (BLDC) Motor Drives,” Applied Power Electronic Conference (APEC 2002), pp33-38.

5 APPENDIX

Following code will be put in the commutation interrupt routine MTC_C_D_IT.

```
if (MCPUH < threshold_duty)   // if D< threshold_duty , sample at PWM off time.
{
SET_MTC_PAGE(1);
MCONF = mem_MCONF;
SET_MTC_PAGE(0);
MCRC = mem_MCRC;
PEDDR = 0x00;     //PE7 to PE4 floating Input.
PEOR = 0x00;     //PE3 to PE0 floating Input.
}
else         // if D> threshold_duty, sample at PWM on time.
{
SET_MTC_PAGE(1);
MCONF = mem_MCONF_ontime;
SET_MTC_PAGE(0);
MCRC = mem_MCRC_ontime_HF;
PEDDR = 0x0F;     //PE7 to PE4 floating Input
PEOR = 0x0F;     //PE3 to PE0 push pull output
PEDR = 0;       //PE1,2,3=0
}

In the head file MTC_Settings_Sensorless.h, some variables are defined as:

#define mem_MCONF     ((u8)2)  // Sample during PWM off time
#define mem_MCONF_ontime ((u8)162)
 // Sampling during PWM on time, 25us delay
#define mem_MCRC      ((u8)67)     // Internal voltage reference
#define mem_MCRC_ontime_HF((u8)79)
// External reference voltage, Z sampled at high frequency
#define threshold_duty   ((u8)16)
                                  // at fs=18.1k, T=883, this number corresponds to
around 60%
```

6 REVISION HISTORY

Table 2. Document revision history

Date	Revision	Changes
10-Dec-2004	1	Initial release
16-Jul-2007	2	Removed references to obsolete products