AN2035
Application note

Control of whisker growth in Tin alloy coatings

1 Nature of whiskers and whisker mitigation techniques

Some metals show an unusual metallurgical phenomenon: a single, microscopic crystal filament of the metal grows “spontaneously” from its surface. The metals concerned include Zinc, Cadmium, Silver, Tin and some of their alloys. Because of their likeness to microscopic hair, these tiny filaments are commonly referred to as “whiskers”.

Scientists believe that whisker growth is mainly due to internal compressive stresses near the metal surface. Under certain conditions the internal stress can reach a critical level, leading to the formation of whiskers as a way of reducing the system’s internal energy.

Owing to their excellent electrical properties and solderability, and their low cost, pure Tin-plated surfaces have been used for many decades by the electronics industry. Hundreds of billions (trillions by some estimates taking passives and discretes into account) of components have been supplied with pure Tin-plated surface finishes. On top of their low cost, these components operate well and are highly reliable. Only does the occasional occurrence of reliability problems caused by Tin whiskers tarnish their reputation. An easy fix to whisker problems was found, that consisted in adding small amounts of Lead (Pb) – as low as 3% – to the plating. In so doing, the growth of whiskers was effectively prevented.

With the recent European Directive to eliminate Lead from electronic products, there is a renewed interest in Tin and its alloys as a replacement for Lead-bearing alloys. A better understanding of the factors which influence whisker formation and the application of new techniques to control these factors, along with the introduction of modern plating chemistries and processes, allow the electronics industry to pursue this return to pure Tin-plating surface finishes. Since whisker growth is mainly caused by internal compressive stresses, a number of strategies have been developed to prevent stress development within the Tin-plated film. Internal stress in Tin-plated films may originate from a number of causes, among which are:

a) co-deposited impurities, e.g. organics

b) atomic defects, such as those caused by improper plating parameters

c) creation of new phases leading to local volume changes. These may be caused by either metallurgical or chemical reactions.

d) thermal stress caused by mismatches in the Coefficients of Thermal Expansion (CTE) between the Tin film and the base metal (and/or additional films beneath the Tin film).

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Experience has shown that proper plating practices and chemistries are important in preventing whisker formation. Early Tin-plating chemistries were designed to produce a cosmetically appealing shiny surface. This type of plating is known as “bright Tin plating”. The shiny appearance of the tin-plated surface is achieved by adding specialized chemicals to the plating bath, that control the size of the grains (“grain refiners”) and the planarity of the plated surface (“levelers”). Small grains and flat surfaces help reflect the light, thus favoring shiny surfaces. Due to the very nature of the chemistries and the high concentrations of additives required to achieve bright finishes, these early bright Tin-plating chemistries were prone to problems of organics co-deposition and atomic irregularities within the plated film, leading to a higher susceptibility to whisker formation.

Modern chemistries and plating techniques have evolved with a view of preventing earlier problems of contaminant co-deposition and atomic defect creation within the deposited film. One major change in some Tin-plating chemistries is the use of much lower levels of grain refining additives. The result is a duller (or matte) appearance of the Tin plating. For this reason these chemistries are referred to as Matte Tin.

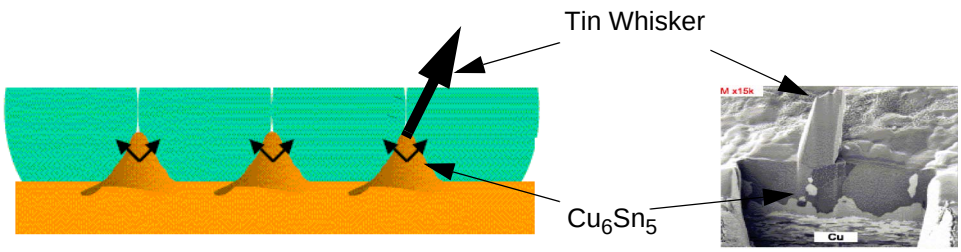
In a joint effort, Infineon, Philips, Freescale and ST Microelectronics (the so-called E4 Initiative) have tested a large number of modern plating chemistries for their resistance to whisker growth. From this study a number of suitable commercial Matte Tin-plating chemistries have been identified.

As mentioned previously, localized phase changes within the Tin film can also cause localized compressive internal stresses. This happens when a volume increase is associated with the phase change.

Since Tin and Copper normally form an intermetallic, Cu6Sn5, in a reaction which produces a significant increase in volume, it is essential to take this into consideration for Tin-plated copper leadframes.

When the Cu6Sn5 intermetallic forms at low temperatures (e.g. room temperature) the reaction tends to take place more specially along the grain boundaries where the diffusion of the combining elements is highest at lower temperatures due to solid-state diffusional kinetics. The net result of the combined penetration and expansion of this growing intermetallic may be envisioned as a “wedge” driven into the Tin layer at the grain boundary. The penetration and growth of Cu6Sn5 intermetallics along grain boundaries is shown in *Figure 1* (schematic and photograph).

Figure 1. Natural growth of InterMetallic Compound (IMC) at room temperature



However, if the Cu_6Sn_5 intermetallic is formed under higher temperature conditions (e.g. around 150°C), a different and more desirable intermetallic structure forms. At higher temperatures bulk diffusion is activated and the intermetallic reaction occurs more uniformly across the entire Tin/Copper interface, not just at the grain boundaries. Since the reaction

rate is virtually uniform across the Tin/Copper interface the resulting Cu6Sn5 structure has practically no “wedges”.

The difference in the Cu6Sn5 structure is clearly demonstrated in the micrographs in *Figure 2*. In these micrographs the Tin was selectively removed by chemical etching, thus exposing the Cu_6Sn_5 intermetallic as well as any copper not covered by the intermetallic.

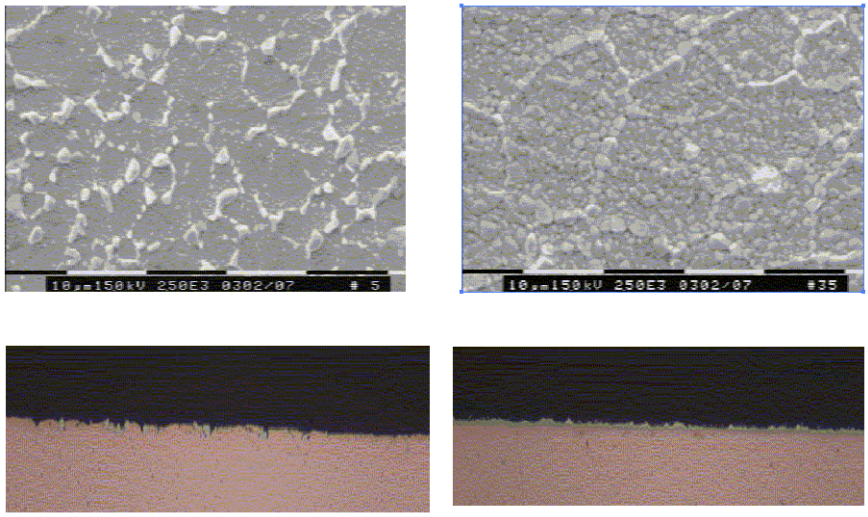
In the micrographs on the left hand side of *Figure 2*, the intermetallic was allowed to form at room temperature over a period of one month. The result is a large, blocky and irregular Cu_6Sn_5 structure located almost exclusively at the grain boundaries.

Note: In this image the large flat spaces between the blocky intermetallic are exposed copper.

By contrast the image on the right hand side of *Figure 2* shows a Cu_6Sn_5 intermetallic formed by baking the part within 24 hours of plating at a temperature of 150°C. In this case the image shows a very uniform layer of Cu_6Sn_5 with virtually no “wedges”.

Note: All of the materials in this image are the Cu_6Sn_5 intermetallic. There is no exposed Copper after etching.

Figure 2. Microscope View of Protection by Post-bake Treatment (1 hour at 150°C)



The ability of a 150°C bake to virtually eliminate the intermetallic “wedges” that lead to large compressive stress at the grain boundaries serves as the basis for the second component of the whisker mitigation strategy adopted by STMicroelectronics.

The second component of the strategy to mitigate whisker growth is to apply a 1-hour 150°C bake within 24hrs to freshly plated Matte-Tin finishes. This has several beneficial effects: the film is annealed and stress due to atomic-level plating defects is reduced. In addition, and more importantly, a stable and uniform Cu_6Sn_5 layer is created that protects against further localized penetration of the intermetallic at grain boundaries, thus avoiding the “wedge” effect that creates compressive stress. Furthermore, the bake creates an additional beneficial layer of Cu_3Sn, underneath the Cu_6Sn_5 layer.

The beneficial effects of the 150°C bake can be seen in the whisker test results shown in *Figure 3*. Regardless of the plating thickness none of the samples had grown whiskers after 400 days of storage at room temperature.

Figure 3. Protection by post-bake treatment (1 hour at 150°C)

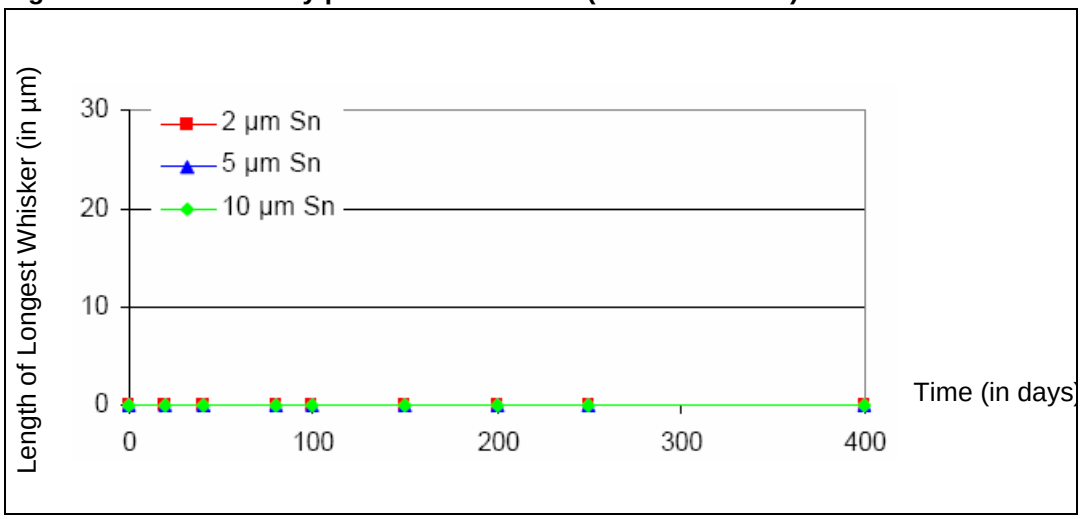
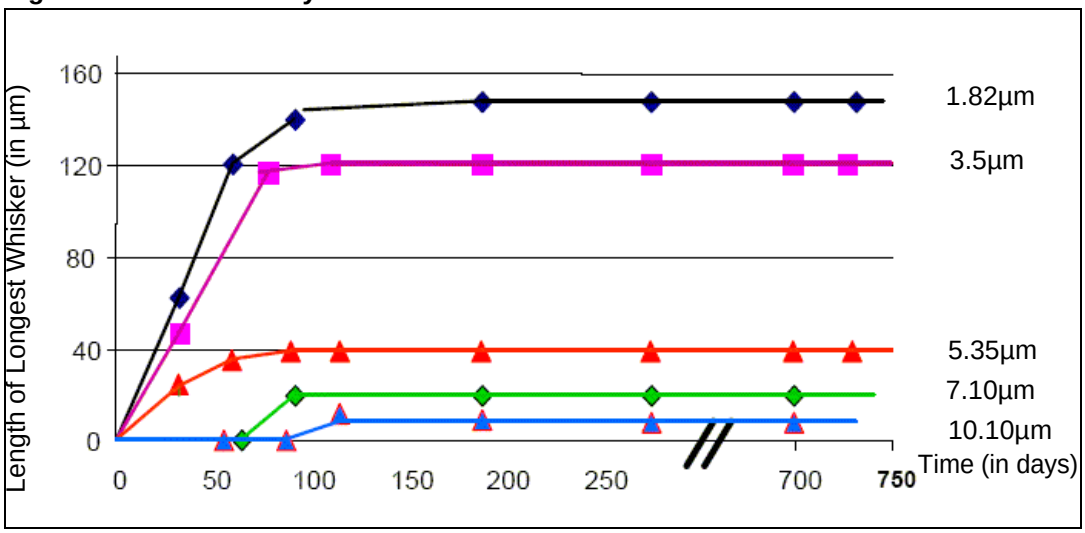


Figure 4. Protection by thickness



The above whisker mitigation techniques have been agreed with all subcontractors and are therefore applied to all ST products.

A "**Whisker Risk Free**" coating does not develop whiskers that can impact electrical performance, or component reliability. The E4 have chosen 50µm as the maximum whisker length at the end of the device life (at the end of whisker assessment tests).

2 Whisker assessment and process qualification

On 1st March 2006, the JEDEC standard organization released the International Standardized Methodology for the assessment of whisker risk: JESD 201 (Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes) to be implemented together with JESD 22A121 (Test Method for Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes).

STMicroelectronics will abide by this standard and re-qualify the Tin plating line in accordance with it.

Since no international standards were available 4 years ago when STM began preparing for the RoHS initiative, customer specifications guided our testing strategy to qualify both our internal and subcontractor plating lines. This qualification plan satisfies more than eighty percent of our customers.

The qualification plan used the following stresses and criteria:

All customer specifications imposed a maximum permissible whisker length of 50µm.

- Ambient storage (15°C to 30°C, at 60 % RH) for 6 months
- Dry air: 50°C to 55°C for 6 months
- Thermal cycles: (–35°C to +125°C) for 500 cycles
- Temperature & Humidity: 85°C at 85%RH for 500 hrs.

A total of about 1500 units from 40 different package types have been tested in this phase, with no evidence of whiskers.

The electronics industry's search for an appropriate set of stresses for testing the susceptibility of Tin-surface finishes to whisker formation has continued over the last 4 years. This search has been strongly influenced by several commercial consortia.

Most attention has been focused on the High Humidity stress since some studies have indicated that this stress may in fact favor whisker growth. However, there is concern that the conclusions of some of these studies were flawed, the results being confounded by the presence of corrosion.

Unfortunately, now as more industry data is being generated, it is apparent that the high-humidity environmental stress state has the ability to introduce corrosion in the test sample and the corrosion may in turn produce spurious secondary whisker formation that is not truly representative of the integrity of the surface finish under study. As a result, the various commercial organizations providing input to the JEDEC task group have changed their recommendations for the humidity stress state used for whisker evaluations at least 4 times (60°C/95%RH, 60°C/93%RH, 60°C/87%RH and 55°C/85% RH) over the last year.

It is still not clear whether applying high-humidity stress conditions for a long period of time either relates to a whisker growth mechanism or to actual field usage. For example, a review of the literature shows no examples of whiskers associated with corrosion and it is clear that whiskers have been observed even in vacuum.

STMicroelectronics along with their E4 partners have continued to study the Matte Tin-plating process and the various stresses used to evaluate these processes.

- **Test Set #1 (started Jan 2004) completed with final readout at 9360 hrs (13 months)**
  - Package : QFP 176L Cu leadframes
  - Plated in Muar plant
  - Solder thickness > 7µm
  - Maximum whisker length after 2000 TC (thermal cycles) single whiskers on 1 unit (27 micron length)
  - Maximum whisker length after 9360 hrs (13 months) at 60°C/93%RH, 1 single whiskers on 1 unit (25 micron length) without associated corrosion.
  - No whiskers observed at ambient storage after 9360 hrs (13 months).
- **Test Set # 2 (started April 2004) completed with final readout at 3600 hrs (5 months)**
  - Package: QFP10 x10 Cu Leadframe
  - Plated in Malta
  - Solder thickess > 7µm
  - Mounting on board with SAC solder paste at 250°C max solder reflow temperature
  - Maximum whisker length after 3096 hrs (5 months) at 60°C/93% RH, 1 single whisker on 1 unit (10 micron length).
- **Test Set # 3 (started April 2004), completed with final readout at 3600 hrs (5 months)**
  - Package: QFP14 x14 Cu Leadframe
  - Plated in Muar
  - Solder thickess > 7µm
  - Mounting on board simulated at 215°C max solder reflow temperature
  - Maximum whisker length after 3689 hrs (6 months) at 60°C/93% RH, no whiskers in all tests.
- **Test Set # 4 (started Nov. 2004), actual read out 6700 hrs (9 months)**
  - Package: Power SO36L (#2 pcs), Power So20L (#1 pc), DPak (#2 pcs)
  - Plated in Muar and Shenzhen plant (2 different chemicals)
  - Solder thickness > 7µm
  - Mounted on Board with SAC solder paste (NO clean flux)
  - NO whiskers found after 6700 hrs exposure at 60°C/93%RH.

3 Whiskers and thermal cycles

In thermal cycles, a different cause of whisker growth exists, which is linked to the mismatch in thermal coefficient of expansion (TCE) between base material and coating layer, rather than to localized internal stress. The TCE of Tin, Copper and A42 are 23ppm/°C, 17 ppm/°C and 4 ppm/°C, respectively. Therefore, whisker growth will be more significant on A42 than on Copper. Whisker length depends also on the extreme lower limit of the thermal cycles: the lower this limit, the longer the whisker.

It must be noted that PbSn finishings, too, have a TCE that is close to the one of Matte Tin. They are exposed to the same whisker growth, and give the same whisker length.

Therefore, Matte Tin behaves in a very similar way to the traditional SnPb coating.

Figure 5. Temperature Cycling SnPb on FeNi42 (250 Cycles of –35 to 125°C)

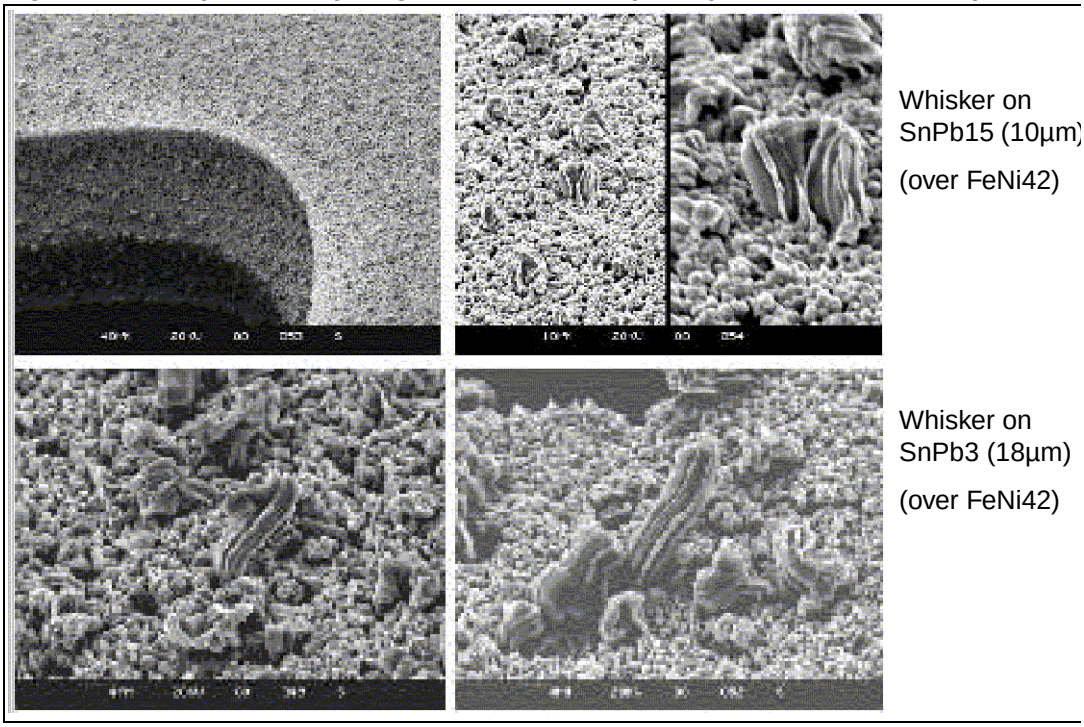
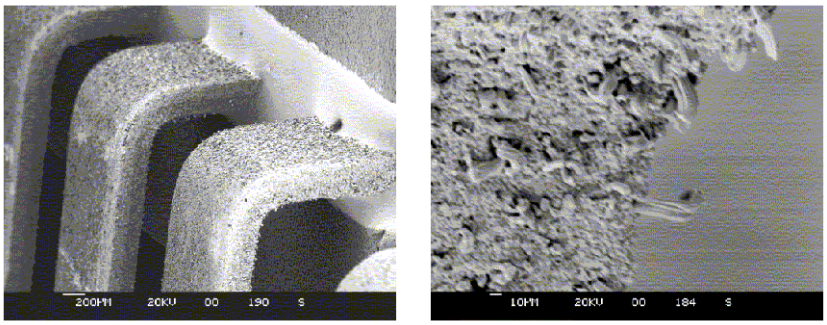


Figure 6. Temperature Cycling Sn 100% (500 Cycles of –35 to 125°C)



4 Revision history

Table 1. Document revision history

Date	Revision	Changes
04-Nov-2004	1	First Issue
10-Apr-2006	2	Title added to *Section 1: Nature of whiskers and whisker mitigation techniques*, section detailed and clarified. *Section 2: Whisker assessment and process qualification* updated to latest results, Additional Tests (NEMI evaluation methodology) title removed and section moved under *Section 2*.