AN2478
Application note

STP08DP05, STP16DP05
Normal mode and error detection features

Introduction

In applications such as electronic advertising or traffic signs that use an IC to drive a matrix of LEDs, it is very important to verify the correct functionality of each output. STMicroelectronics has introduced the STP08DP05 and STP16DP05 featuring output error detection. This application note shows how to utilize the devices under normal mode operative conditions and how to perform error detection.

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1 Device description

The STP08DP05 and STP16DP05 are monolithic, low voltage shift registers. The device contains either an 8-bit (STP08DP05) or a 16-bit (STP16DP05) serial-in, parallel-out shift register that feeds an 8-bit or 16-bit D-type storage register. Eight or sixteen regulated currents are present in the output stage that provide 5-80 mA constant current to drive the LEDs. The secondary device functionality (error detection) provides a status check of the LEDs to detect any possible error during driving.

Figure 1.   Typical application of STP08DP05 and/or STP16DP05 devices
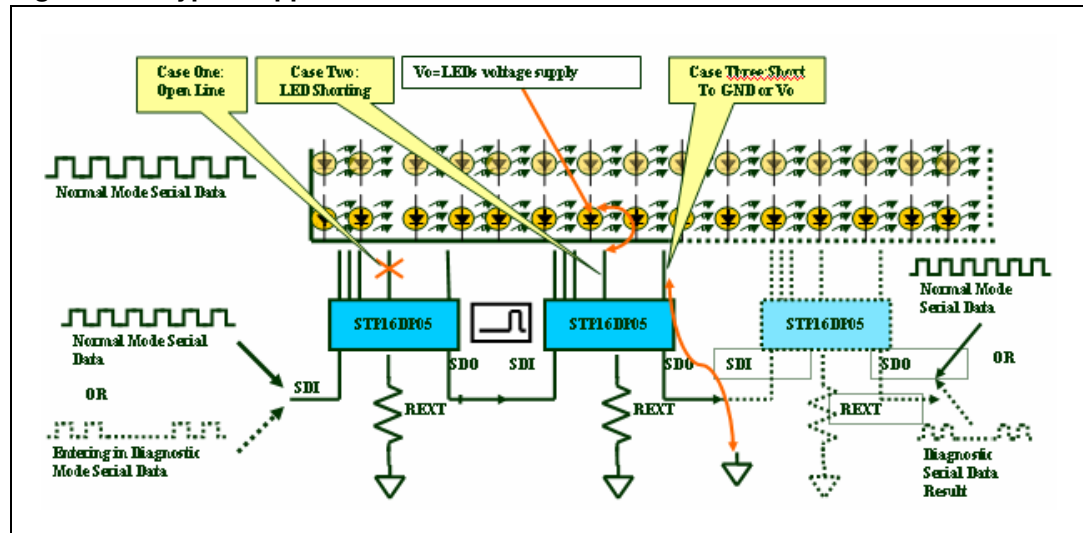
2 Normal mode functionality

During normal mode status, the serial data present on the SDI pin is transferred to the shift register during the CLK rise time signal transition. After 8 CLK pulses for the STP08DP05, or 16 CLK pulses for the STP16DP05, the data loaded on the SDI pin will be shifted to the SDO pin with a typical delay of 15 ns (depending on the clock). This delay guarantees the correct synchronization of the CLK and SDI signals if two or more devices are cascaded. The data present in any register can be transferred to the respective latch when the Latch - Enable (LE/DM1) is "high" (serial to parallel conversion). After this step, data is transferred to the outputs by the output enable (OE/DM2) which turns ON the LEDs at the current set by the external resistor. It is also possible to use the OE/DM2 pin to modify the output ON/OFF duty cycle. This allows an optimization of dimming when two or more devices are used.

Figure 2. Typical functionality in normal mode
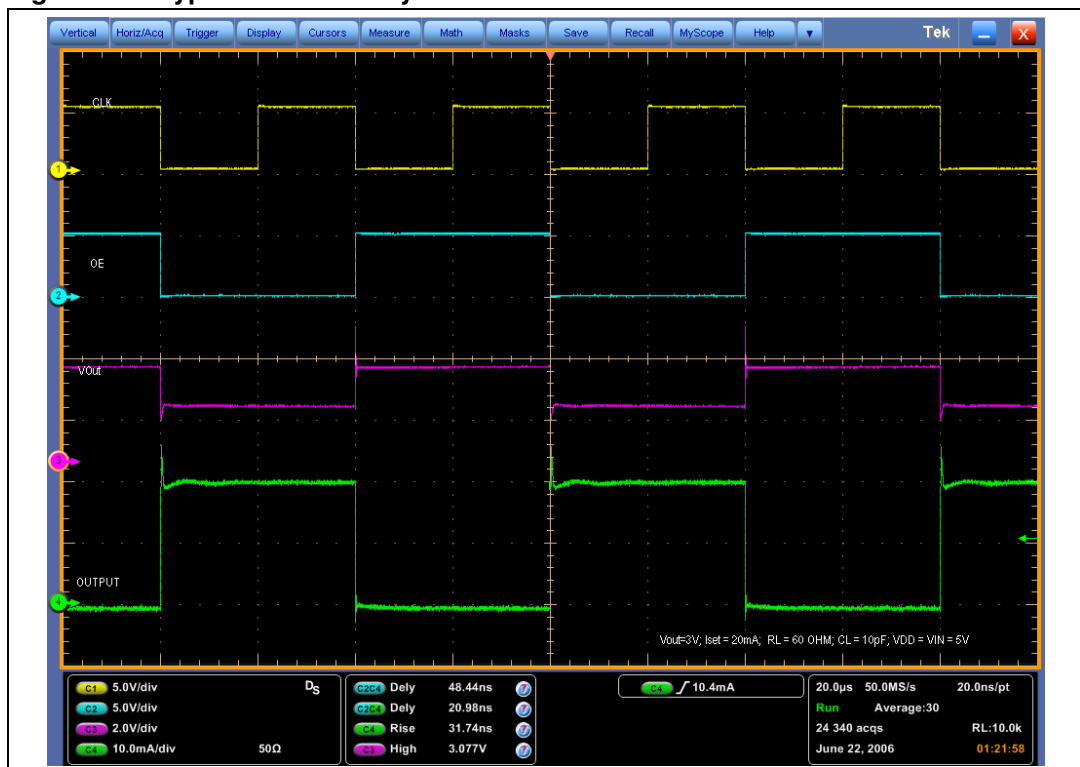
The signals shown on the plot are:

● CLK signal (CH1)

● OE/DM2 signal (CH2)

● Vout level (CH3)

● OutputN (CH4) which turn ON and OFF according to the OE pulse

Under specific applicative conditions, where it is necessary to transfer data directly to the outputs without the OE/DM2 signal (always "low"), the LE/DM1 is synchronized with a CLK signal that transfers the shift register data to the specific output as reported in the following plots.

Figure 3. Typical functionality without OE/DM2 signal and the output switching ON according to LE/DM1 signal
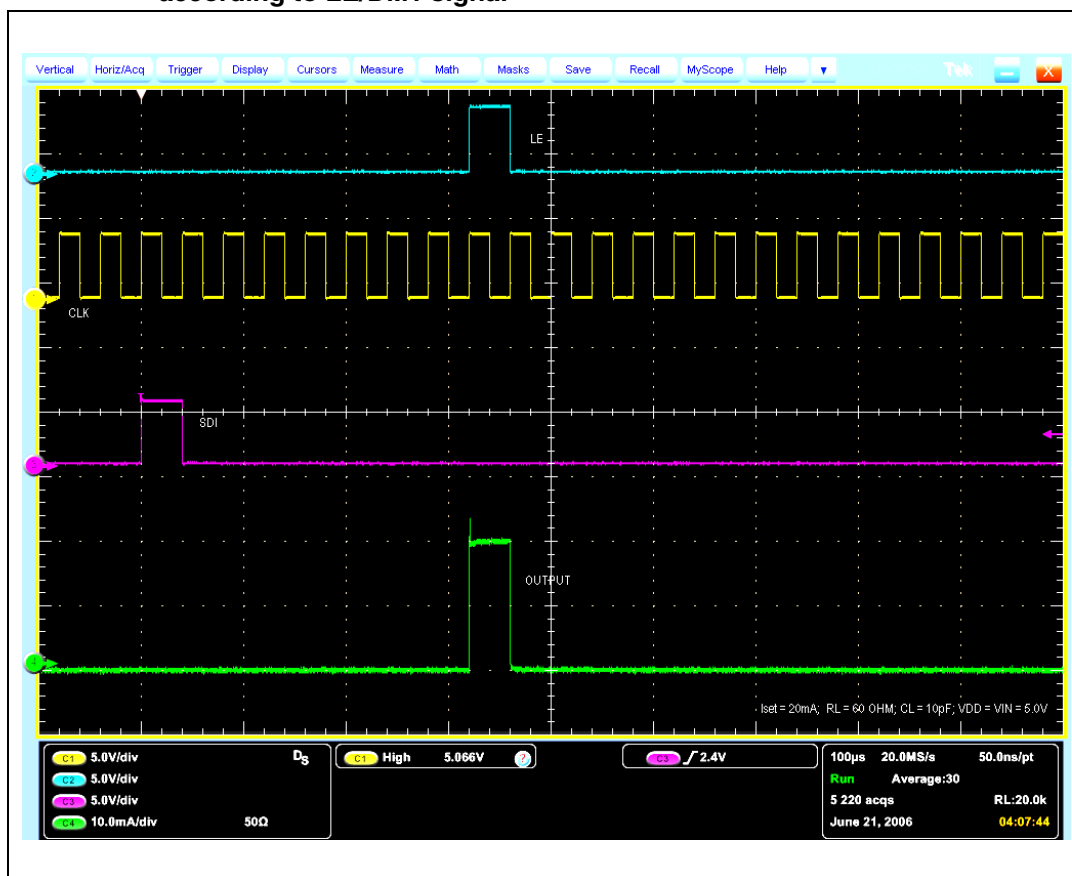
3   Error detection features

This feature allows the output status detection to verify the functionality of the LEDs. The error detection includes both open circuit detection and short circuit detection. From "normal mode", the device is switched to "error mode" by a logic sequence on the OE/DM2 and LE/DM1 pins. The eight data bits (STP08DP05) must be set to "1" in order to set all the outputs ON during detection. The data are latched by LE/DM1. After latching, the outputs are ready for the detection process. When the microcontroller switches the OE/DM2 to "low", the device drives the LEDs in order to analyze if an open or short condition has occurred.

In order to set the SDO output pin to the correct output error detection value, during the acquisition time (OE/DM2 "low"), at least two CLK pulses must be applied before the rising edge of OE/DM2 signal. These CLK pulses must be sent after the minimum detection time (typically 500-600 ns). In this way the data loaded into the shift register will be updated (rewritten) with the error detection data when the OE/DM2 signal turns to "high". Good output results are shown with a "1" logic level, and with a "0" logic level when the output is malfunctioning (short or open condition).

The plots below show all the steps required to perform the error detection for the STP08DP05 and the STP16DP05.

Figure 4.   Error detection sequence for STP08DP05
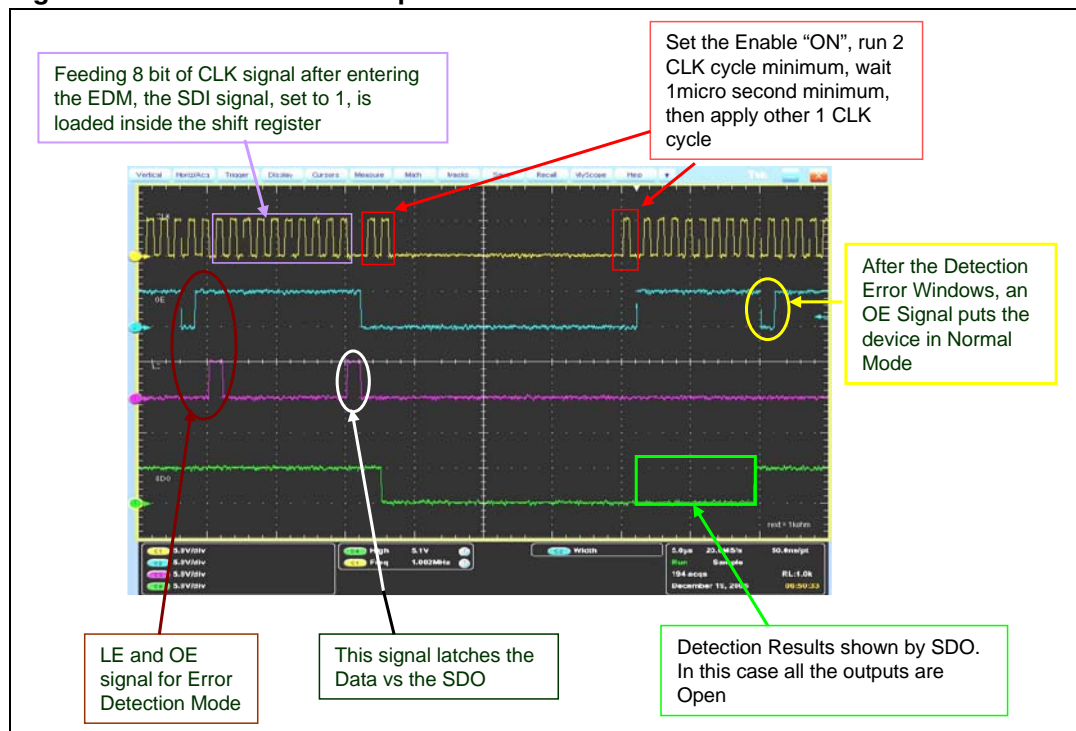
Figure 5. Error detection sequence for STP16DP05
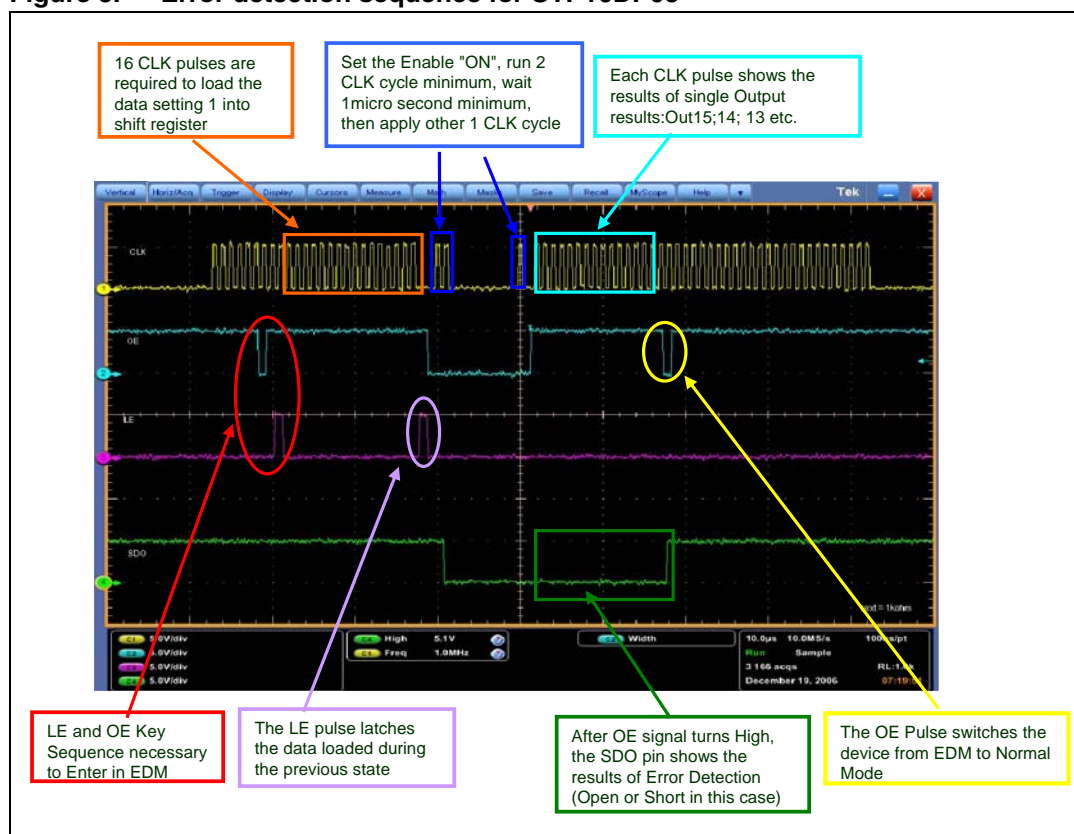
After OE/DM2 turns to "high", the results of the outputs are synchronized with the CLK signal rise time as shown in *Table 1*:

Table 1. STP08DP05 output error detection sequence after OE acquisition

CLK Pulse after OE turn to "high" level	Output results
1° CLK Rise edge	Output7
2° CLK Rise edge	Output6
3° CLK Rise edge	Output5
4° CLK Rise edge	Output4
5° CLK Rise edge	Output3
6° CLK Rise edge	Output2
7° CLK Rise edge	Output1
8° CLK Rise edge	Output0

The same table can also be used for the STP16DP05, but in this case, 16 CLK pulses are necessary and the results are shown following output 15, output 14, etc.

Figure 6.   **STP08DP05 typical error detection results**
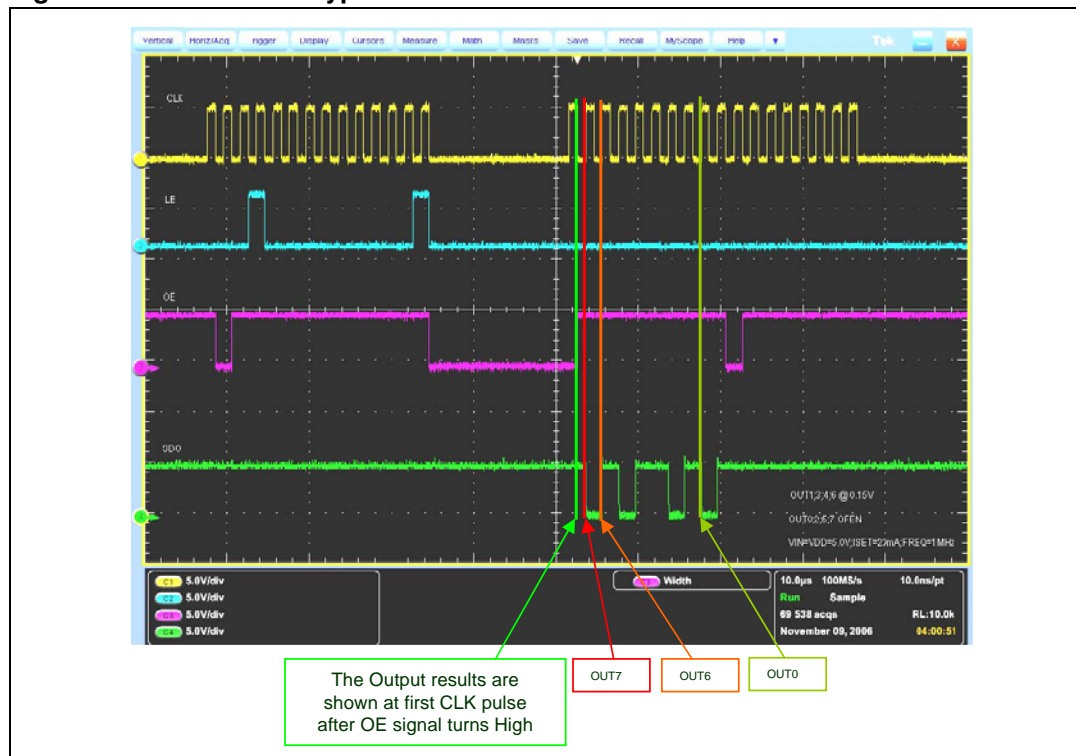
After detection, apply an OE signal to return to normal mode. The following two figures show the pattern necessary to enter error detection mode and return to normal mode.

Figure 7.   **Entering output error detection timing**

Figure 8.   **Resuming normal mode timing**

4 Error detection output test circuit

During the error detection time, the internal structure of the device allows only an output current test. This is done by comparing the current flowing from the output and the current set by the programming resistor "REXT".

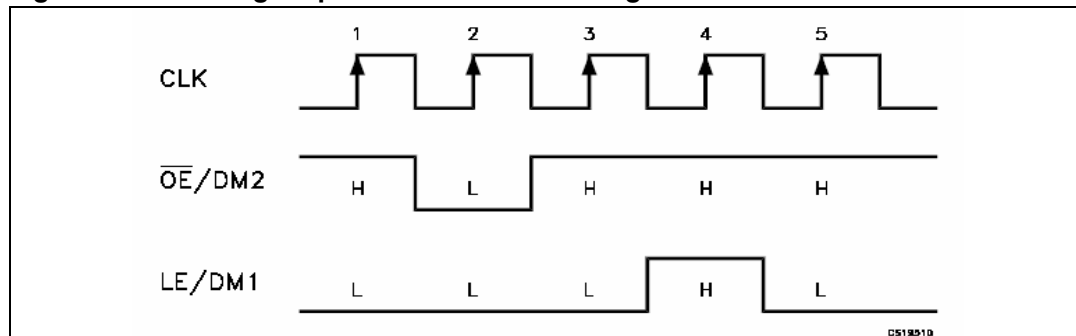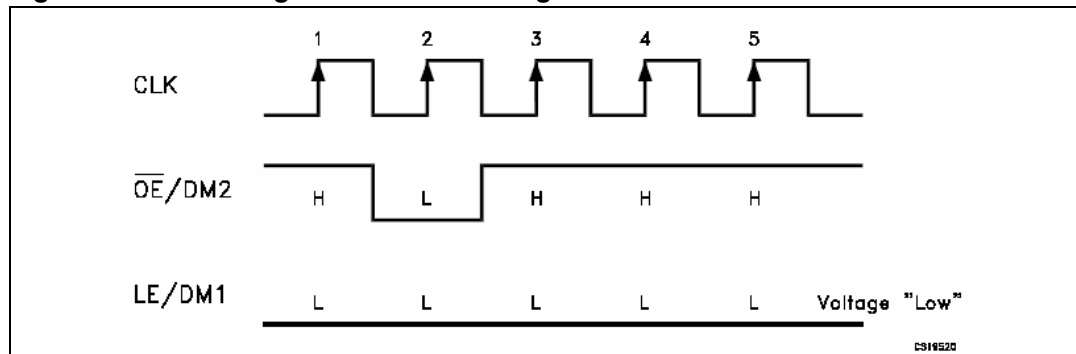If the read current is typically less than 50% of the current set by "REXT", the device marks the output as malfunctioning, and converts the previous data loaded into the shift register from 1 to 0. These results are then transferred by the SDO pin. *Table 2* shows an example of the measured error detection threshold for several output current levels, as set by "REXT".

Table 2.   Error threshold test results

Vdd (V)	Iset (mA)	Measured error threshold
3.3	5	2.27
	10	5.32
	20	8.38
	50	17.91
	80	29.06
5	5	1.88
	10	4.81
	20	6.44
	50	18.54
	80	31.36

To correctly run the output error detection, all signals must be synchronized with the falling edge of the CLK signal. This is necessary to avoid any setup/hold time problems. If this rule cannot be applied due to specific application conditions (data generated by a microcontroller, for example), it is possible to start the OE signal typically at 20 ns of delay after the rise time of the CLK signal. The next two plots show a typical error detection mode problem due to wrong error key (LE/DM1 or OE/DM2).

Figure 9.   Error detection sequence problem due to LE/DM1 synchronization
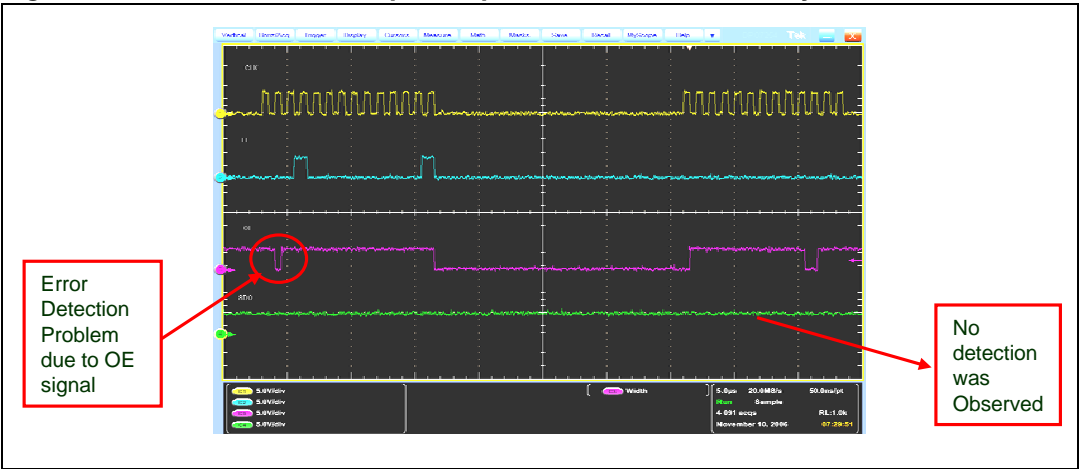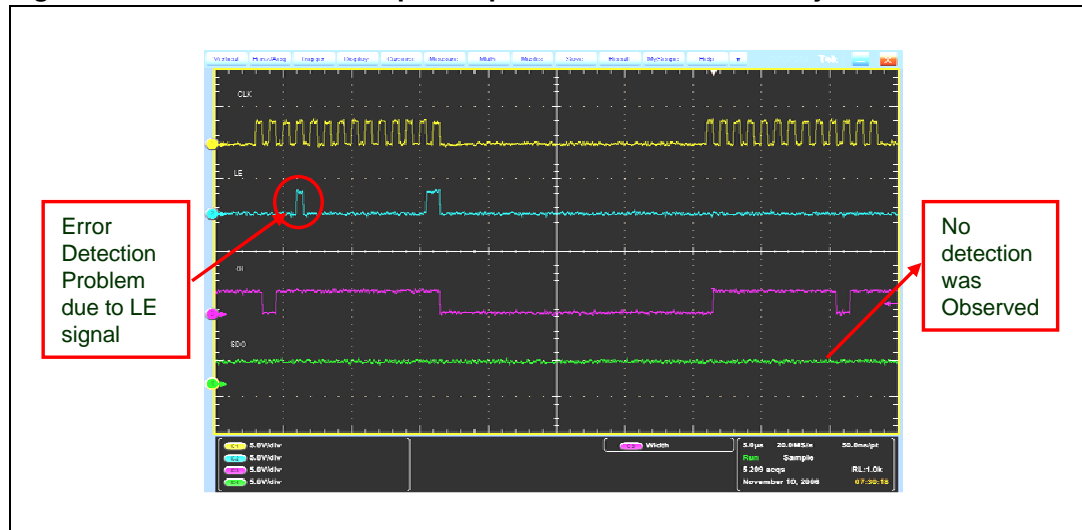
Figure 10.   Error detection sequence problem due to OE/DM2 synchronization

Only one error detection reading can be taken within the acquisition time window. If two or more readings are required, the complete error detection sequence has to be repeated.

4.1   Proper supply LED voltage for correct error detection

For proper error detection it is necessary to set correct supply voltage for the LEDs, otherwise a wrong LED status can be obtained from the LED drivers. During error detection all outputs should be turned ON at least for 1 μs (LED current is set by external resistor) and the output current and output voltage on the driver is measured in order to detect an open load or short circuit (*Figure 11*). There are two detection conditions for which the supply LED voltage must be kept in proper range:

1.   First detection condition: $I_{OutDetect} \leq 0.5 \cdot I_{out}$

If detected current is lower than 50% of current set by the external resistor, it is evaluated as an open load or output short to ground. False error detection can occur if the LED supply voltage is too low, because in this case the detected current is under the defined limit. Minimum voltage for proper error detection can be calculated with the following equation:

Equation 1

$$V_C \geq V_{LEDMAX} + V_{out}$$

V_C: LED supply voltage [V]

V_{LED_MAX}: maximum LED forward voltage [V]

V_{out}: output voltage for current set by external resistor [V]

2.   Second detection condition: $V_{out} \geq 2.5 \, V$

If detected voltage is higher than 2.5 V, it is evaluated as a short on LED or short to V_c. Incorrect error detection can occur if the LED supply voltage is too high, because in this case the detected voltage is above the defined limit. Maximum voltage for proper error detection is calculated with the following equation:

Equation 2

$$V_C \leq 2.5 + V_{LEDMIN}$$

V_{LED_MIN}: minimum LED forward voltage [V]

For example the STEVAL-ILL002V3 uses the OSRAM LED - LB T68C with the current set to 20 mA. The supply voltage for these LEDs was adjusted to 4.49 V, because the LED voltage range for proper error detection is between 4.3 V and 5.5 V.

Equation 3
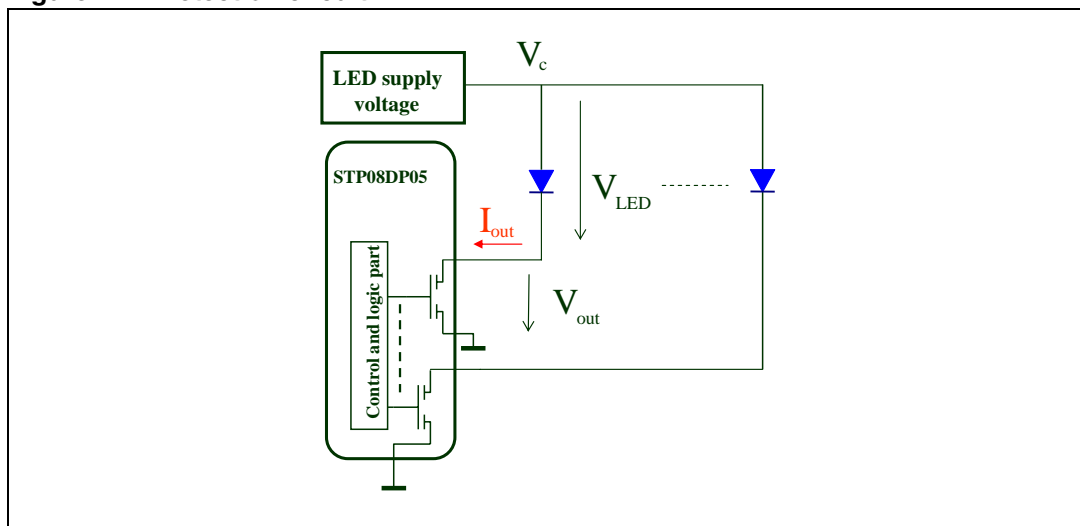
$$V_c \geq V_{LEDMAX} + V_{out} = 4.1 + 0.2 = 4.3 \text{ V}$$

Equation 4

$$V_c \leq 2.5 + V_{LEDMIN} = 2.5 + 3 = 5.5 \text{ V}$$

where $V_{LED\_MAX} = 4.1$ V and $V_{LED\_MIN} = 3$ V.

$V_{out} = 200$ mV - voltage drop on the driver for 20 mA LED current (see datasheet STP16DP05 - same voltage drop as for STP08DP05).

Figure 11.   Detection circuit

5 Evaluation boards with error detection features using STP08DP05 LED drivers

5.1 Description

The main aim of this section is to demonstrate two evaluation boards with error detection features using the new STP08DP05 LED drivers: the STEVAL-ILL002V3 with OSRAM LEDs and the STEVAL-ILL002V4 with VISHAY LEDs (*Figure 12*). The evaluation boards are completely based on an existing solution already described in AN2415, because drivers were replaced by the new STP08DP05. Therefore this section is focused on explaining only the differences in the main features and timing diagram.

Main features of the evaluation board are:

● Brightness regulation
● Blinking speed regulation
● Animated text
● Error detection on outputs
● PC graphic user interface for error detection(GUI)
● DC/DC converter using the L5970D
● Input voltage range of 7 V to 32 V

Two versions of the evaluation boards are available:

● STEVAL-ILL002V3 using OSRAM LEDs
● STEVAL-ILL002V4 using VISHAY LEDs

Figure 12. STEVAL-ILL002V3 or 4 evaluation boards
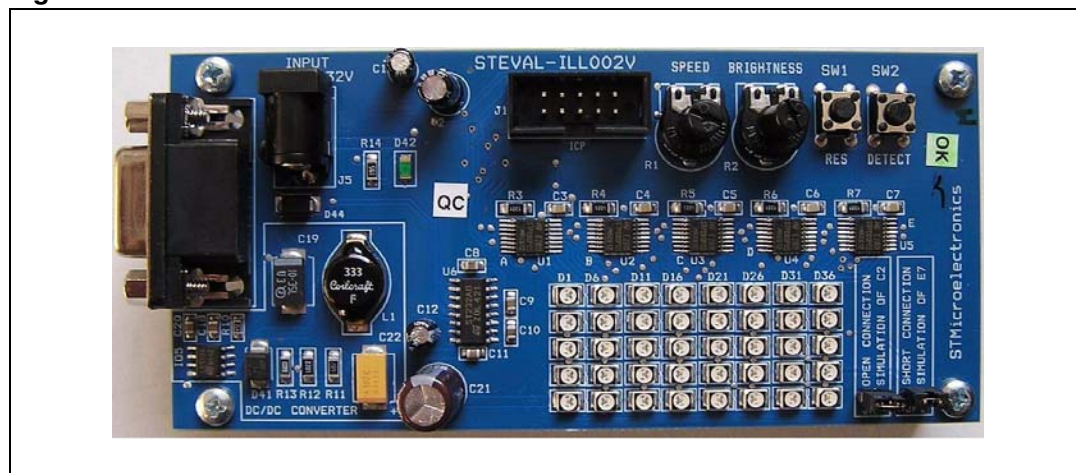
5.2 Timing diagram

The heart of this application is the microcontroller (ST7LITE39) which sends the data through the SPI to the LED drivers. There are five STP08DP05 LED drivers each with eight outputs assembled to allow independent driving of 40 LEDs during normal operational mode and also to detect the status of incorrect LEDs during error detection mode. The implementation method is described in the timing diagrams in this document.

The timing diagram for normal operational mode is shown in *Figure 13* (left side). The yellow waveform is the clock frequency of the SPI set to 2 MHz. Five bytes are sent to the drivers in order to independently control 40 LEDs . When all data are shifted to the drivers (registers) the latch (red waveform) is switched to high and rewrites the storage registers. The OE pin enables the output driver sink current. Current is modulated by the potentiometer which changes the PWM duty cycle on the OE pin (PWM frequency is set at 244 Hz).

More information about timing diagram in normal operation mode is also written in application note AN2141, since the new STP08DP05 is compatible with the previous versions of the LED drivers.

Complete error detection timing diagram for checking the status of all 40 LEDs on the STEVAL-ILL002V3 or 4 is also shown in *Figure 13* (right side). Error detection mode is divided to 5 timing intervals. The first interval allows enterance into error detection mode through generation of a special sequence on the latch and OE pins synchronized by the clock frequency. This sequence is described in *Figure 6*. When the LED drivers enter error detection mode the high level must be sent through SPI to the outputs and then latched. In the next step the status of incorrect LEDs is detected. An enlarged view of the third timing interval is provided in *Figure 14*. The OE is set to low level for at least 1 µs (in this case 50 µs) and one clock cycle (yellow) is applied. The status of the LEDs is obtained when OE is turned to high level as shown in the fourth timing interval (the detection result is read on the SDO on the falling edge of the SPI clock). First, the data are read from the last driver E, then from D, etc. To demonstrate the error detection feature the LED diode 39 (see the schematic diagram in *Figure 16*) was shorted and therefore the results coming from the LED drivers are the following:

● DRIVER A: 1111 1111
● DRIVER B: 1111 1111
● DRIVER C: 1111 1111
● DRIVER D: 1111 1111
● DRIVER E: 1011 1111 (output 6 faults)

As soon as the status of all LEDs is checked the LED drivers should return to the normal operational mode by generating a special sequence during fifth timing interval. The timing diagram for resuming normal mode is also shown in *Figure 7*.

Figure 13.   Timing diagram for the STEVAL-ILL002V3 or 4 evaluation board
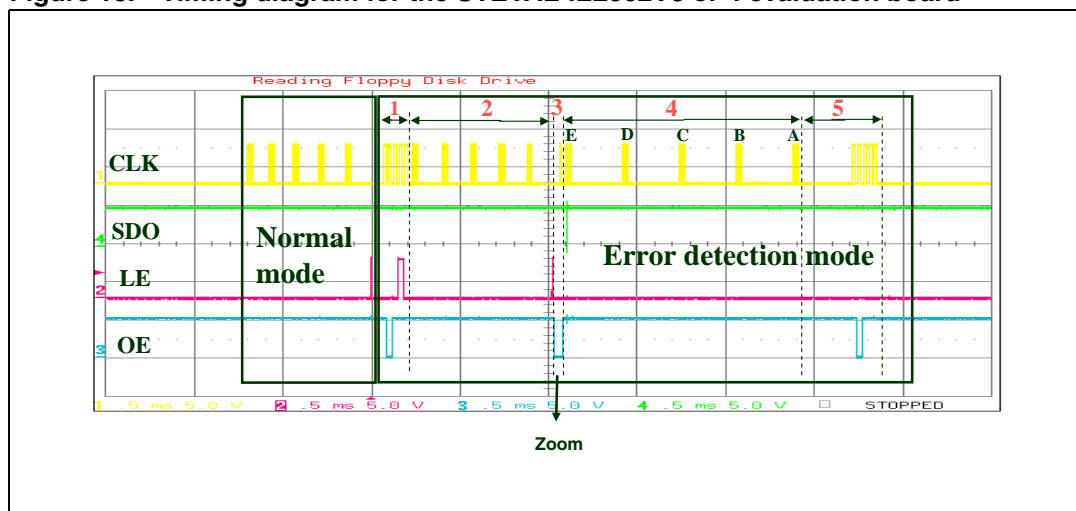
Figure 14.   Detection diagram for STEVAL-ILL002V3 or 4 evaluation board
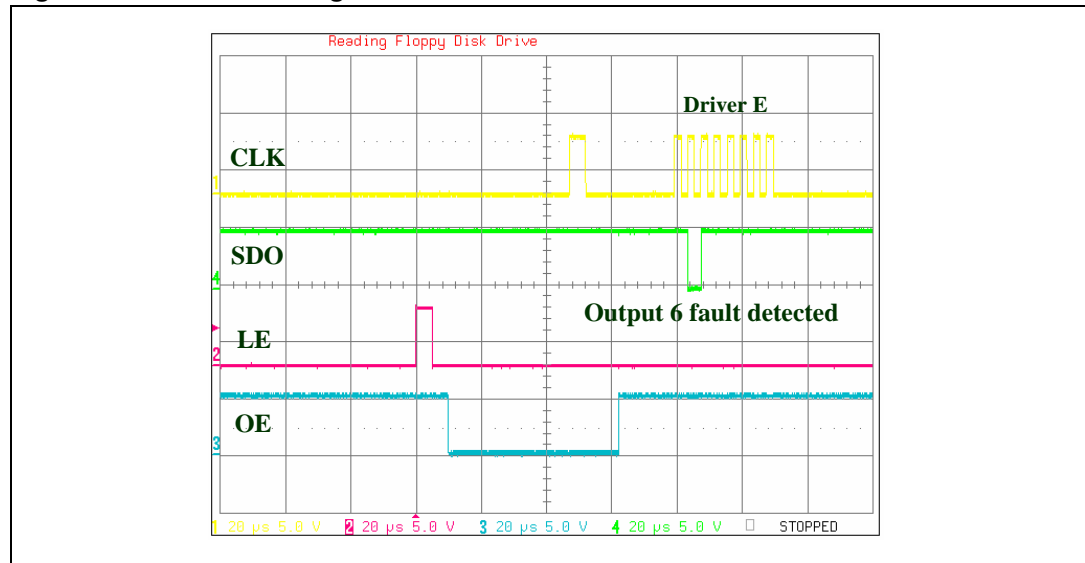
5.3   STP08DP05 vs. STP08CDC596 detection diagram

Figure 15 shows the detection diagram for the STP08DP05 and STP08CDC596 LED drivers.

When the OE pin is "0" the LED drivers check the status of the LEDs. After this the output data (SDO) are read on the falling edge of the clock SPI. The resulting output bits are not the same for both drivers, as shown in the red frames in *Figure 15*. The seventh bit is read like the first for the STP08DP05, but for the STP08CDC596 the sixth bit is read. Therefore if both drivers are used in the application the LED status obtained from the drivers must be corrected by the SW, otherwise an erroneous status is detected (shifted by one bit).

Figure 15.   Detection diagram for STP08DP05 and STP08CDC596 LED drivers

5.4 Schematic diagram

Figure 16. Schematic diagram
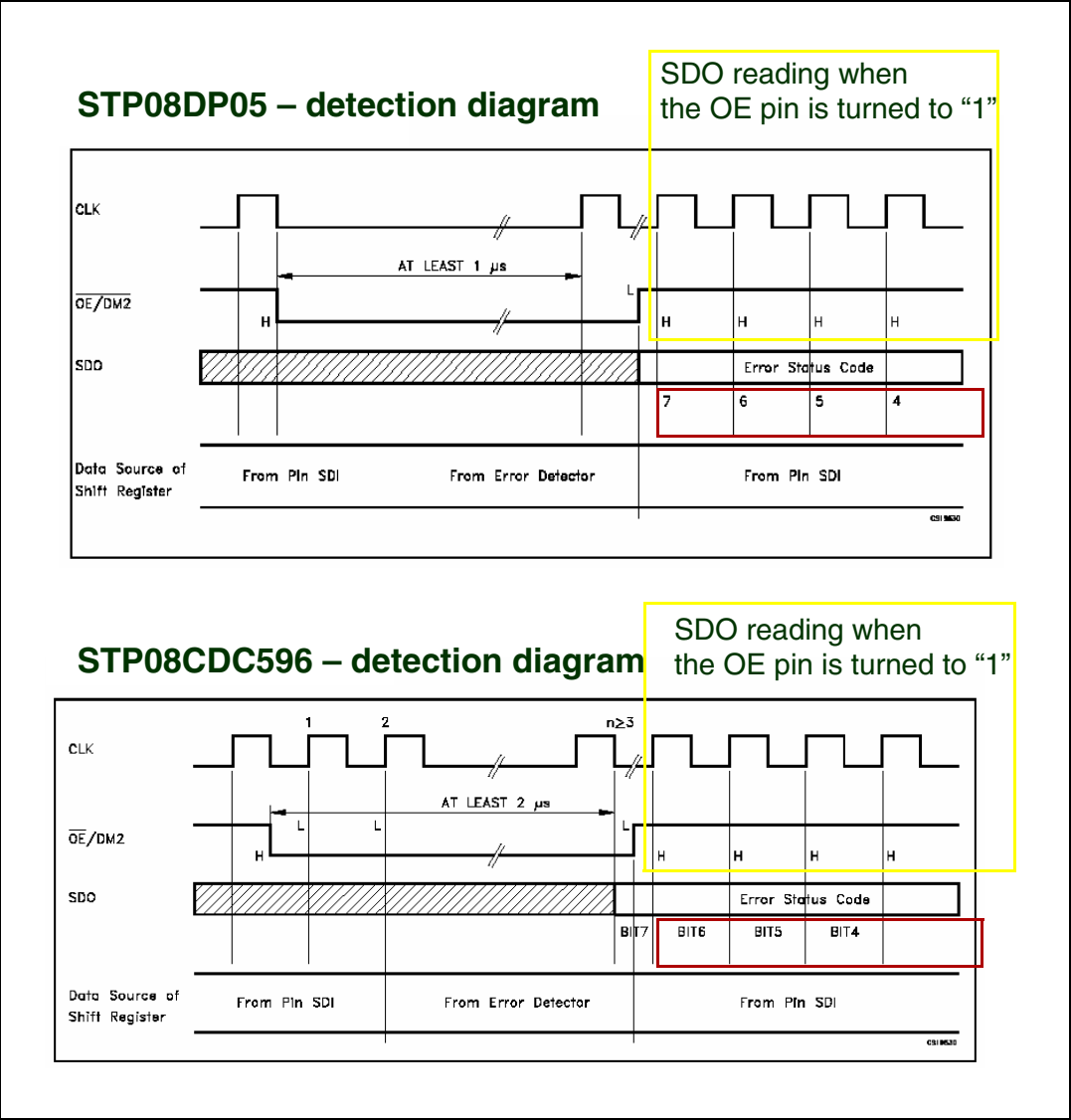
5.5 Bill of materials

Table 3. **Bill of materials**

Item	Qty	Reference	Part	Description	Order code	Supplier
1	2	C1,C12	2.2 µF/50 V	Electrolytic capacitor		
2	1	C2	10 µF/35 V	Electrolytic capacitor		
3	7	C3,C4,C5, C6,C7,C15, C17	100 nF/50 V	Ceramic capacitor SMD 0805		
4	4	C8,C9,C10, C11	470 nF/16 V	Ceramic capacitor SMD 0805		
5a	2	C14,C16	10 nF/50 V	Ceramic capacitor SMD 0805		
5b	1	C13	10 nF/50 V	Ceramic capacitor SMD 1206		
6	1	C18	22 nF/50 V	Ceramic capacitor SMD 0805		
7	1	C19	10 µF/35 V	Tantal capacitor		
8	1	C20	220 pF/50 V	Ceramic capacitor SMD 0805		
9	1	C21	220 µF/25 V	Electrolytic capacitor		
10	1	C22	100 µF/16 V	Tantal capacitor		
11	40	D1,D2,D3, D4,D5,D6, D7,D8, D9,D10, D11,D12, D13,D14, D15,D16, D17,D18, D19,D20, D21,D22, D23,D24, D25,D26, D27,D28, D29,D30, D31,D32, D33,D34, D35,D36, D37,D38, D39,D40	LED	OSRAM SMD BLUE LED LB T68C-P2S1-35 OR VISHAY SMD GREEN LED VLMTG31N2S1 - GS08		OSRAM OR VISHAY
12	1	D41	STPS340U	Diode	STPS340U	STMicroelectronics
13	1	D42	GREEN LED	SMD LED 1206		
14	1	D44	SMAJ33A-TR	Transil	SMAJ33A-TR	STMicroelectronics

Table 3. **Bill of materials (continued)**

Item	Qty	Reference	Part	Description	Order code	Supplier
15	1	IO5	L5970D	DC/DC converter	L5970D	STMicroelectronics
16	2	JP1,JP2	JUMPER	Jumpers + switches		
17	1	J1	ICP	Programming connector		
18	1	J5	CON3	Input connector		
19	1	L1	33 µH	Inductor	DO3316P-333ML	COILCRAFT
20	1	P1	CONNECTOR DB9	CAN connector - 9 pins		
21a	2	R1,R2	10 k	Potenciometers with axis		
21b	2	R8,R9	10 k	SMD resistors 0805		
22	5	R3,R4,R5, R6,R7	1k3	SMD resistors 1206		
23	1	R10	4k7	SMD resistors 0805		
24	1	R11	6k8	SMD resistors 1206		
25	1	R12	2K2	SMD resistors 1206		
26	1	R13	360	SMD resistors 1206		
27	1	R14	560	SMD resistors 1206		
28	2	SW1,SW2	SW PUSHBUTTON	Switch		
29	5	U1,U2,U3, U4,U5	STP08DP05	LED drivers	STP08DP05TTR	STMicroelectronics
30	1	U6	ST232ABN	RS232 driver	ST232ABD	STMicroelectronics
31	1	U7	LE50/SO	Linear voltage regulator	LE50ABD	STMicroelectronics
32	1	U8	ST7lite3	Microcontroller	ST7FLITE39F2M6	STMicroelectronics

6 Conclusion

The new features of STP08DP05 and STP16DP05 allow improved control of the application. The full detection test enables the device to provide feedback to the microcontroller, and the feedback of the error detection can be managed locally or remotely.

7 Revision history

Table 4.   Document revision history

Date	Revision	Changes
07-Mar-2007	1	Initial release
22-May-2007	2	Minor text changes
31-Aug-2007	3	– From *Section 4.1* to *Section 5.5* added – *Chapter 6* modified

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