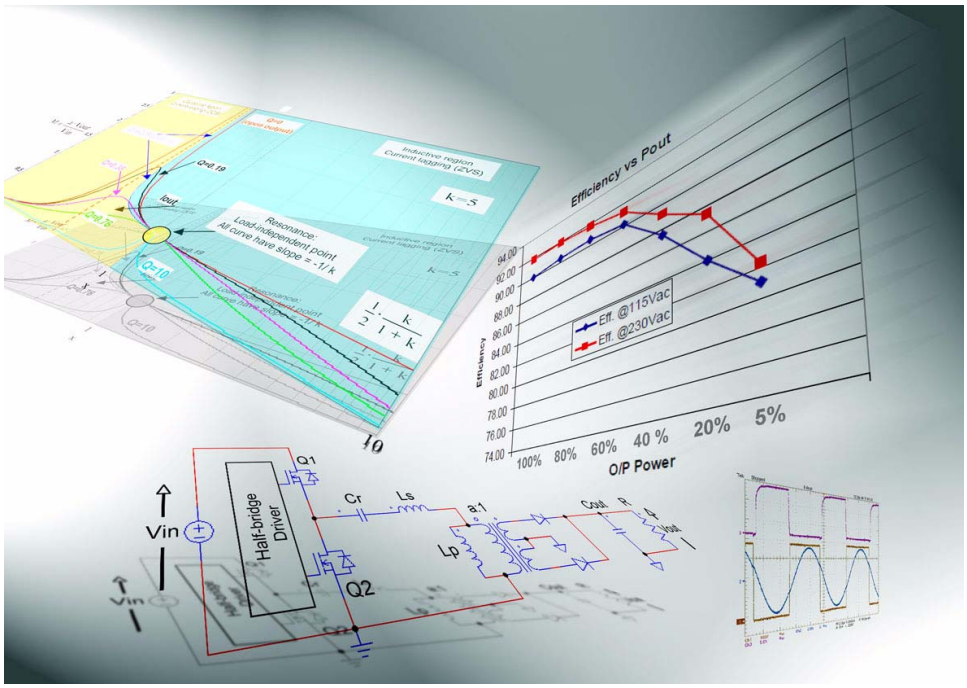
AN2644
Application note

An introduction to LLC resonant half-bridge converter

Introduction

Although in existence for many years, only recently has the LLC resonant converter, in particular in its half-bridge implementation, gained in the popularity it certainly deserves. In many applications, such as flat panel TVs, 85+ ATX PCs or small form factor PCs, where the requirements on efficiency and power density of their SMPS are getting tougher and tougher, the LLC resonant half-bridge with its many benefits and very few drawbacks is an excellent solution. One of the major difficulties that engineers are facing with this topology is the lack of information concerning the way it operates. The purpose of this application note is to provide insight into the topology and help familiarize the reader with it, therefore, the approach is essentially descriptive.

Figure 1. LLC resonant topology schematics and waveforms



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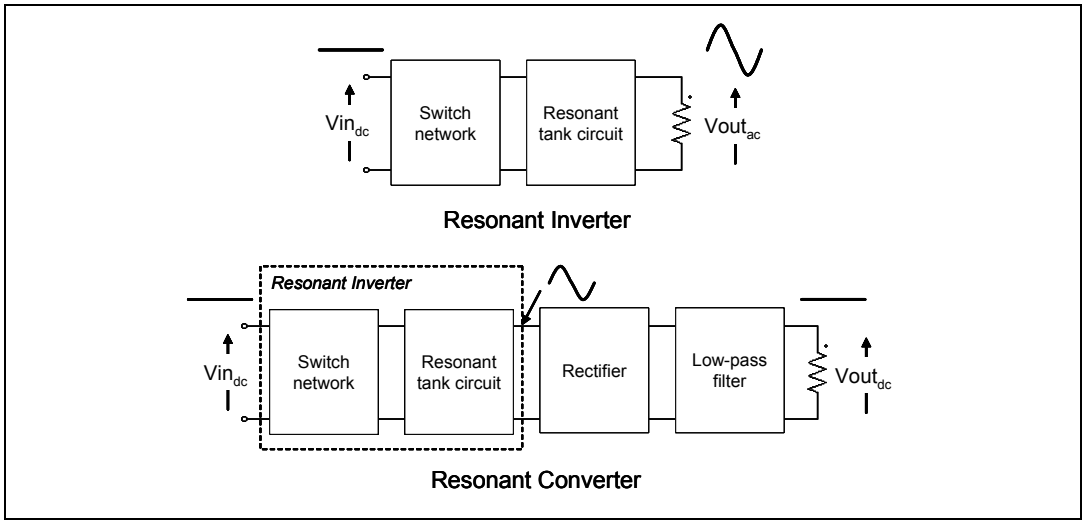
1 Classification of resonant converters

Resonant conversion is a topic that is at least thirty years old and where much effort has been spent in research in universities and industry because of its attractive features: smooth waveforms, high efficiency and high power density. Yet the use of this technique in off-line powered equipment has been confined for a long time to niche applications: high-voltage power supplies or audio systems, to name a few. Quite recently, emerging applications such as flat panel TVs on one hand, and the introduction of new regulations, both voluntary and mandatory, concerning an efficient use of energy on the other hand, are pushing power designers to find more and more efficient AC-DC conversion systems. This has revamped and broadened the interest in resonant conversion. Generally speaking, resonant converters are switching converters that include a tank circuit actively participating in determining input-to-output power flow. The family of resonant converters is extremely vast and it is not an easy task to provide a comprehensive picture. To help find one's way, it is possible to refer to a property shared by most, if not all, of the members of the family. They are based on a "resonant inverter", i.e. a system that converts a DC voltage into a sinusoidal voltage (more generally, into a low harmonic content ac voltage), and provides ac power to a load. To do so, a switch network typically produces a square-wave voltage that is applied to a resonant tank tuned to the fundamental component of the square wave. In this way, the tank will respond primarily to this component and negligibly to the higher order harmonics, so that its voltage and/or current, as well as those of the load, will be essentially sinusoidal or piecewise sinusoidal. As shown in *Figure 2*, a resonant DC-DC converter able to provide DC power to a load can be obtained by rectifying and filtering the ac output of a resonant inverter.

Figure 2. General block diagram of a resonant inverter, the core of resonant converters



Different types of DC-AC inverters can be built, depending on the type of switch network and on the characteristics of the resonant tank, i.e. the number of its reactive elements and their configuration [*1*].

As to switch networks, we will limit our attention to those that drive the resonant tank symmetrically in both voltage and time, and act as a voltage source, namely the half-bridge and the full-bridge switch networks. Borrowing the terminology from power amplifiers,

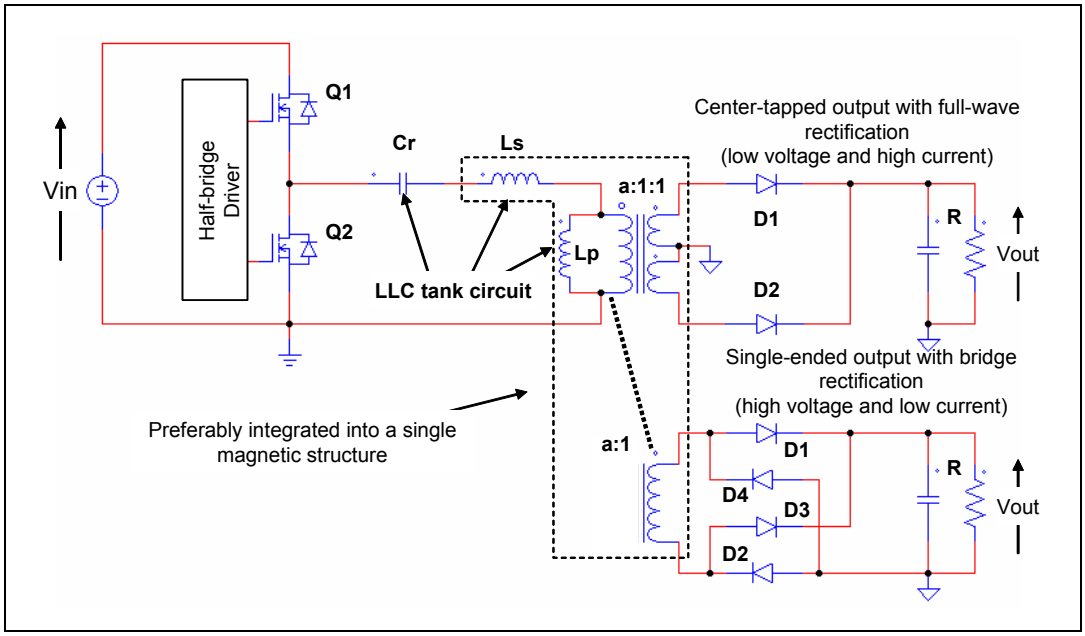
switching inverters driven by this kind of switch network are considered part of the group called "class D resonant inverters".

As to resonant tanks, with two reactive elements (one L and one C) there are a total of eight different possible configurations, but only four of them are practically usable with a voltage source input. Two of them generate the well-known series resonant converter and parallel resonant converter considered in [2] and thoroughly treated in literature.

With three reactive elements the number of different tank circuit configurations is thirty-six, but only fifteen can be used in practice with a voltage source input. One of these, commonly called LCC because it uses one inductor and two capacitors, with the load connected in parallel to one C, generates the LCC resonant inverter commonly used in electronic lamp ballast for gas-discharge lamps. Its dual configuration, using two inductors and one capacitor, with the load connected in parallel to one L, generates the LLC inverter.

As previously stated, for any resonant inverter there is one associated DC-DC resonant converter, obtained by rectification and filtering of the inverter output. Predictably, the above-mentioned class of inverters will originate the "class D resonant converters". Considering off-line applications, in most cases the rectifier block will be coupled to the resonant inverter through a transformer to guarantee the isolation required by safety regulations. To maximize the usage of the energy handled by the inverter, the rectifier block can be configured as either a full-wave rectifier, which needs a center tap arrangement of transformer's secondary winding, or a bridge rectifier, in which case tapping is not needed. The first option is preferable with a low voltage / high current output; the second option with a high voltage / low current output. As to the low-pass filter, depending on the configuration of the tank circuit, it will be made by capacitors only or by an L-C type smoothing filter. The so-called "series-parallel" converter described in [2], typically used in high-voltage power supply, is derived from the previously mentioned LCC resonant inverter. Its dual configuration, the LLC inverter, generates the homonymous converter, addressed in [3], [4] and [5], that will be the subject of the following discussion. In particular we will consider the half-bridge implementation, illustrated in *Figure 3*, but the extension to the full-bridge version is quite straightforward.

Figure 3. LLC resonant half-bridge schematic



In resonant inverters (and converters too) power flow can be controlled by the switch network either by changing the frequency of the square wave voltage, or its duty cycle, or both, or by special control schemes such as phase-shift control. In this context we will focus on power flow control by frequency modulation, that is, by changing the frequency of the square wave closer to or further from the tank circuit's resonant frequency while keeping its duty cycle fixed.

2 The LLC resonant half-bridge converter

2.1 General overview

According to another way of designating resonant converters, the LLC resonant half-bridge belongs to the family of multiresonant converters. Actually, since the resonant tank includes three reactive elements (Cr, Ls and Lp, shown in *Figure 3*), there are two resonant frequencies associated to this circuit. One is related to the condition of the secondary winding(s) conducting, where the inductance Lp disappears because dynamically shorted out by the low-pass filter and the load (there is a constant voltage a V_{out} across it):

Equation 1

$$f_{R1} = \frac{1}{2\pi\sqrt{Ls \cdot Cr}}$$

the other resonant frequency is relevant to the condition of the secondary winding(s) open, where the tank circuit turns from LLC to LC because Ls and Lp can be unified in a single inductor:

Equation 2

$$f_{R2} = \frac{1}{2\pi\sqrt{(Ls + Lp)Cr}}$$

It will be of course $f_{R1} > f_{R2}$. Normally, f_{R1} is referred to as the resonance frequency of the LLC resonant tank, while f_{R2} is sometimes called the second (or lower) resonance frequency. The separation between f_{R1} and f_{R2} depends on the ratio of Lp to Ls. The larger this ratio is, the further the two frequencies will be and vice versa. The value of Lp/Ls (typically > 1) is an important design parameter.

It is possible to show that for frequencies $f > f_{R1}$ the input impedance of the loaded resonant tank is inductive and that for frequencies $f < f_{R2}$ the input impedance is capacitive. In the frequency region $f_{R2} < f < f_{R1}$ the impedance can be either inductive or capacitive depending on the load resistance R. A critical value R_{crit} exists such that if $R < R_{crit}$ then the impedance will be capacitive, inductive for $R > R_{crit}$. For a given tank circuit the value of R_{crit} depends on f. More precisely, in [*6*] it is shown that for any tank circuit configuration (then for the LLC in particular):

Equation 3

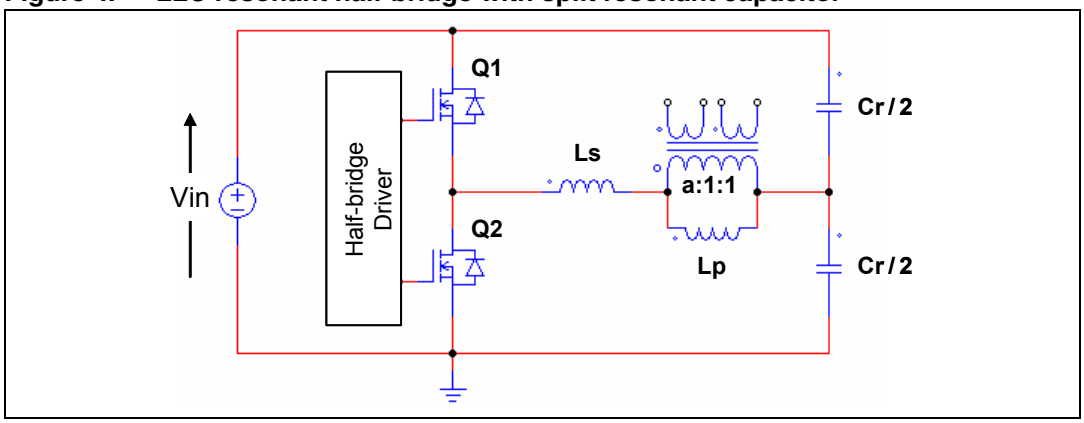
$$R_{crit} = \sqrt{Zo_0 \cdot Zo_\infty}$$

where Zo_0 and Zo_∞ are the resonant tank output impedances with the source input short-circuited and open-circuited, respectively.

For certain reasons that will be clarified in the following sections, the LLC resonant converter is normally operated in the region where the input impedance of the resonant tank has inductive nature, i.e. it increases with frequency. This implies that power flow can be controlled by changing the operating frequency of the converter in such a way that a reduced power demand from the load produces a frequency rise, while an increased power demand causes a frequency reduction.

The Half-bridge Driver switches the two power MOSFETs Q1 and Q2 on and off in phase opposition symmetrically, that is, for exactly the same time. This is commonly referred to as "50% duty cycle" operation even if the conduction time of either power MOSFET is slightly shorter than 50% of the switching period. In fact, a small deadtime is inserted between the turn-off of either switch and the turn-on of the complementary one. The role of this deadtime is essential for the operation of the converter. It goes beyond ensuring that Q1 and Q2 will never cross-conduct and will be clarified in the next sections as well. For the moment it will be neglected, and the voltage applied to the resonant tank will be a square-wave with 50% duty cycle that swings all the way from 0 to V_{in}. Before going any further, however, it is important to make one concept clear.

Figure 4. LLC resonant half-bridge with split resonant capacitor



A few paragraphs above, the impedance of the tank circuit was mentioned. Impedance is a concept related to linear circuits under sinusoidal excitation, whereas in this case the excitation voltage is a square wave.

However, as a consequence of the selective nature of resonant tanks, most power processing properties of resonant converters are associated with the fundamental component of the Fourier expansion of voltages and currents in the circuit. This applies in particular to the input square wave and is the foundation of the First Harmonic Approximation (FHA) modeling methodology presented in [2] as a general approach and used in [4] and [5] for the LLC resonant converter specifically. This approach justifies the usage of the concept of impedance as well as those coming from complex ac circuit analysis.

Coming back to the input square wave excitation, it has a DC component equal to $V_{in}/2$. In the LLC resonant tank the resonant capacitor Cr is in series to the voltage source and under steady state conditions the average voltage across inductors must be zero. As a result, the DC component $V_{in}/2$ of the input voltage must be found across Cr which consequently plays the double role of resonant capacitor and DC blocking capacitor.

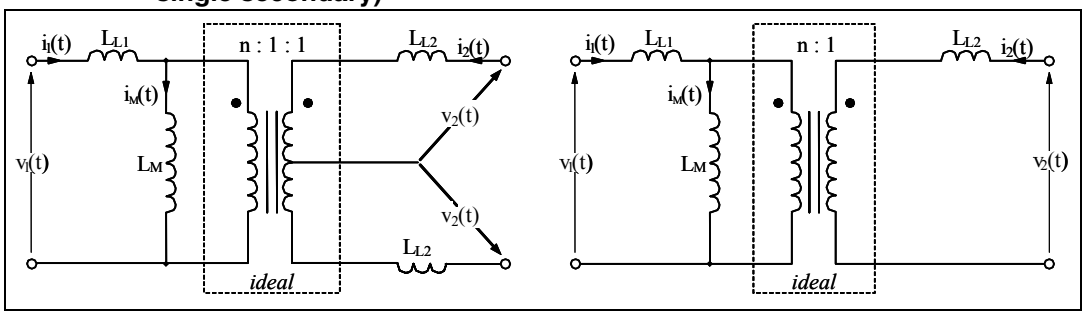
It is possible to see, especially at higher power levels, a slightly modified version of the LLC resonant half-bridge converter, where the resonant capacitor is split as illustrated in *Figure 4*. This configuration can be useful to reduce the current stress in each capacitor

and, in certain conditions, the initial imbalance of the V·s applied to the transformer at start up (see "Converter's start-up" section). Additionally, it makes the input current to the converter look like that of a full-bridge converter, as shown in *Appendix E*, with a resulting reduction in both the input differential mode noise and the stress of the input capacitor. Obviously, the currents through Q1 and Q2 will be unchanged. It is easy to recognize that the two Cr/2 capacitors are dynamically in parallel, so that the total resonant tank's capacitance is again Cr.

The system appears quite bulky, with its three magnetic components. However, the LLC resonant topology lends itself well to magnetic integration. With this technique inductors and transformers are combined into a single physical device to reduce component count, usually with little or no penalty to the converter's characteristics, sometimes even enhancing its operation. To understand how magnetic integration can be done, it is worth looking at the well-known equivalent schematics of a real transformer in *Figure 5* and comparing them to the inductive component set of *Figure 3*.

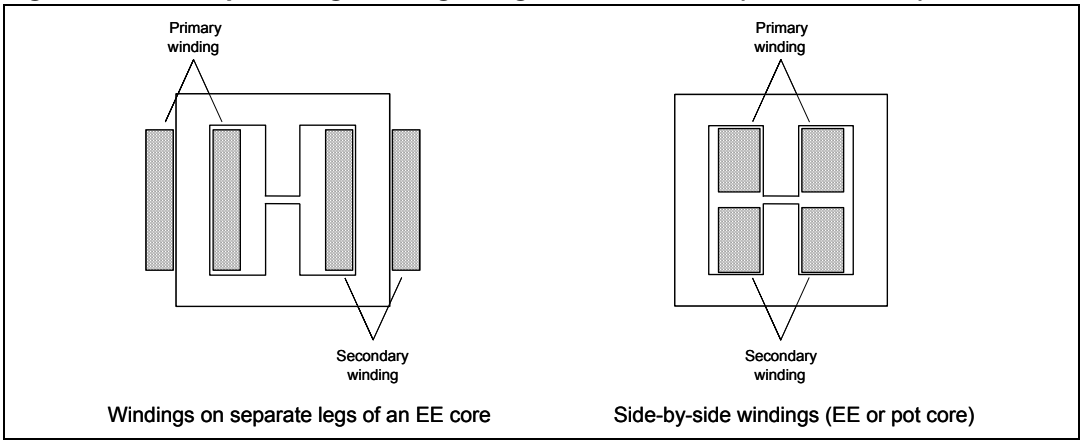
Lp occupies the same place as the magnetizing inductance L_M, Ls the same place as the primary leakage inductance L_{L1}. Then, assuming that we are going to use a ferrite core plus bobbin assembly, Lp can be used as the magnetizing inductance of the transformer with the addition of an air gap into the magnetic circuit and leakage inductance can be used to make Ls.

Figure 5. Equivalent schematic of a real transformer (left, tapped secondary; right, single secondary)



To do so, however, a leaky magnetic structure is needed, which is contrary to the traditional transformer design practice that aims at minimizing leakage inductance. The usual concentric winding arrangement is not recommended here, although higher leakage inductance values can be achieved by increasing the space between the windings.

Figure 6. Example of high-leakage magnetic structures (cross-section)



It is difficult, however to obtain reproducible values, because they depend on parameters (such as winding surface irregularities or spacer thickness) difficult to control. Other fashions are recommended, such as placing the windings on separate core legs (using E or U cores) or side by side on the same leg which is possible with both E and pot cores and shown in *Figure 6*. They permit reproducible leakage inductance values, because related to the geometry and the mechanical tolerances of the bobbin, which are quite well controlled. In addition, these structures possess geometric symmetry, so they lead to magnetic devices with an excellent magnetic symmetry.

However, in the real transformer model of *Figure 5* there is the secondary leakage inductance L_{L2} that is not considered in the model of *Figure 3*. The presence of L_{L2} is not a problem from the modeling point of view because the transformer's equivalent schematic can be manipulated so that L_{L2} disappears (it is transferred to the primary side and incorporated in L_{L1}). This is exactly what has been done in the transformer model shown in *Figure 3*. Then, it is important to underline that Ls and Lp are not real physical inductances (L_{L1}, L_M and L_{L2} are), their numerical values are different ($L_s \neq L_{L1}$, $Lp \neq L_M$), and, finally, the turn ratio a is not the physical turn ratio $n=N_1/N_2$. Ls and Lp can be given a physical interpretation. L_s is the inductance of the primary winding measured with the secondary winding(s) shorted, while Lp is the difference between the inductance of the primary winding measured with the secondary windings open and L_s.

However, L_{L2} is not free from side effects. For a given impressed voltage, L_{L2} decreases the voltage available on the secondary winding, which carries a current i_2, by the drop $L_{L2} \cdot di_2/dt$. This is an effect that is taken into account by the above mentioned manipulation of the transformer model. In addition, in multioutput converters, where there is leakage inductance associated to each output winding, cross-regulation between the various outputs will be adversely affected because of their decoupling effect.

Finally, there is one more adverse effect to consider in the center-tapped output configuration. With reference to *Figure 3* and *5*, when one half-winding is conducting, the voltage $v_2(t)$ externally applied to that half-winding is $V_{out}+V_F$ (V_F is the rectifier forward drop of the conducting diode). With no secondary leakage inductance, this voltage will be found across the secondary winding of the ideal transformer and then coupled one-to-one to the nonconducting half-winding. Consequently, the reverse voltage applied to the reverse-biased rectifier will be $2 \cdot V_{out}+V_F$. If now we introduce the leakage inductance L_{L2}, the drop $L_{L2} \cdot di_2/dt$ adds up to $V_{out}+V_F$ and is reflected to the other half-winding as well. As a result, the reverse voltage applied to the nonconducting rectifier will be increased by $L_{L2} \cdot di_2/dt$. Note that in case of single-winding secondary with bridge rectification, the voltage applied to reverse-biased diodes of the bridge is only $V_{out}+V_F$ and is not affected by L_{L2}. The reason is that the negative voltage of the secondary winding is fixed at $-V_F$ externally and is not determined by internal coupling like in the case of tapped secondary.

It is worth pointing out that the 50% duty cycle operation of the LLC half-bridge equalizes the stress of secondary rectifiers both in terms of reverse voltage - as just seen - and forward conduction current. In fact, each rectifier carries half the total output current under all operating conditions. Then, if compared to similar PWM converters (such as the ZVS Asymmetrical Half-bridge, or the Forward converter), in the center-tapped output configuration the equal reverse voltage typically allows the use of lower blocking voltage rating diodes. This is especially true when using common cathode diodes housed in a single package. A lower blocking voltage means also a lower forward drop for the same current rating, and then lower losses.

It must be said, however, that in the LLC resonant converter the output current form factor is worse, so the output capacitor bank is stressed more. Although the stress level is

considerably lower than that in a flyback converter, as shown in *Table 1*, this is one of the few real drawbacks of the topology.

Table 1. Output stress for LLC resonant half-bridge vs. PWM topologies @ 50% duty cycle

Output current form factors	Forward - ZVS AHB	LLC resonant HB	Flyback (CCM-DCM boundary)
Peak-to-DC ratio	≈1.05÷1.15	$\approx \frac{\pi}{2} = 1.57$	4
Rms-to-DC ratio	≈1	$\approx \frac{\pi}{2\sqrt{2}} = 1.11$	$\sqrt{\frac{8}{3}} \approx 1.63$
AC-to-DC ratio	≈0.03÷0.09	$\approx \sqrt{\frac{\pi^2}{8} - 1} = 0.48$	$\sqrt{\frac{8}{3} - 1} \approx 1.29$

Additional details concerning power losses will be discussed in *Analysis of power losses on page 41*.

To complete the general picture on the LLC resonant converter, there is another aspect that needs to be addressed concerning parasitic components which affect the behavior of the circuit.

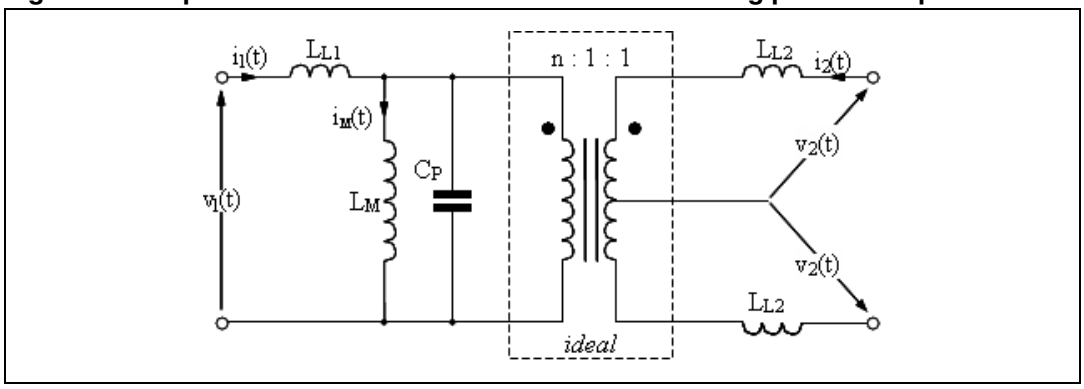
The first parasitic element to consider is the capacitance of the midpoint of the half-bridge structure, the node common to the source of the high-side power MOSFET and to the drain of the low-side power MOSFET. Its effect is that the transitions of the half-bridge midpoint will require some energy and take a finite time to complete. This is linked to the previously mentioned deadtime inserted between the turn-off of either switch and the turn-on of the complementary one, and will be discussed in more detail in *Section 2.2*.

The second parasitic element to consider is the distributed capacitance of transformer's windings. This capacitance, which exists for both the primary and the secondary windings, in combination with windings' inductance, originates what is commonly designated as the transformer "self-resonance". In addition to this capacitance one needs to consider also the junction capacitance of the secondary rectifiers, which adds up to that of the secondary windings and lowers the resulting self-resonance frequency (loaded self-resonance).

The effect of all this parasitic capacitance can be modeled with a single capacitor C_P connected in parallel to L_M as illustrated in *Figure 7*. The resonant tank, as a consequence, turns from LLC to LLCC. This 4^{th}- order tank circuit features a third resonance frequency at the transformer's loaded self-resonance ($f_{LSR} > f_{R1}$). When the operating frequency is considerably lower than f_{LSR} the effect of C_P is negligible. However, at frequencies greater than f_{R1} and if the load impedance is high enough, its effect starts making itself felt, eventually resulting in reversing the transferable power vs. frequency relationship as frequency approaches f_{LSR}. Power now increases with the switching frequency, feedback becomes positive and the converter loses control of the output voltage. The onset of this "feedback reversal" in closed-loop operation is revealed by a sudden frequency jump to its maximum value as the load falls below a critical value (i.e. the frequency exceeds a critical value) and a simultaneous output voltage rise.

In some way, either appropriately choosing the operating frequency range ($<< f_{LSR}$) or increasing f_{LSR}, the converter must work away from feedback reversal. This usually sets the practical upper limit to a converter's operating frequency range.

Figure 7. Equivalent schematic of a transformer including parasitic capacitance



2.2 The switching mechanism

Still another way of classifying resonant converters would include the LLC resonant half-bridge in the family of "resonant-transition" converters. This nomenclature refers to the fact that in this class of converters power switches are driven in such a way that a resonant tank circuit is stimulated to create a zero-voltage condition for them to turn-on.

To understand how this can be achieved in the LLC half-bridge, it is instructive to consider the circuits illustrated in *Figure 8* where the switches Q1 and Q2 that generate the square wave input voltage to the resonant tank are power MOSFETs. Their body diodes DQ1, DQ2 are pointed out because they play an important role. In circuit a), the drain-to-source parasitic capacitances C_{oss1}, C_{oss2} are pointed out as well. In fact, as far as voltage changes of the node HB are concerned, the parasitic capacitances Cgd and Cds are effectively in parallel, then Cgd+Cds=C_{oss} has to be considered.

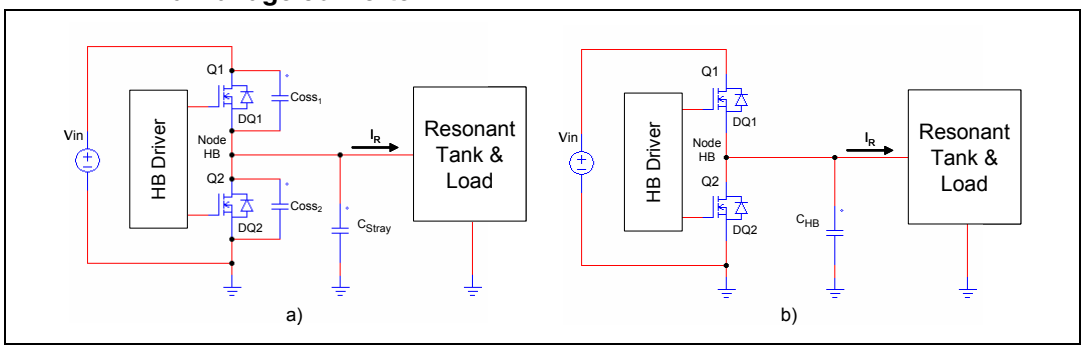
Additionally, other contributors to the parasitic capacitance of the node HB (e.g. that formed between the case of the power MOSFETs and the heat sink, the intrawinding capacitance of the resonant inductor, etc.) are lumped together in the capacitor C_{Stray}. Note that C_{oss1}, like C_{oss2}, is connected between the node HB and a node having a fixed voltage (V_{in} for C_{oss1}, ground for C_{oss2}). Then, as far as voltage changes of the node HB are concerned, C_{oss1} is effectively connected in parallel to C_{oss2} and C_{Stray}. It is convenient to lump all of them together in a single capacitor C_{HB} from the node HB to ground, as shown in the circuit b):

Equation 4

$$C_{HB} = C_{OSS1} + C_{OSS2} + C_{Stray}$$

which we will refer to in the following discussion. Note also that C_{oss1} and C_{oss2} are non-linear capacitors, i.e. their value is a function of the drain-to-source voltage. It is intended that their time-related equivalent value will be considered (see *Appendix A*).

Figure 8. Power MOSFET totem-pole network driving a resonant tank circuit in a half-bridge converter

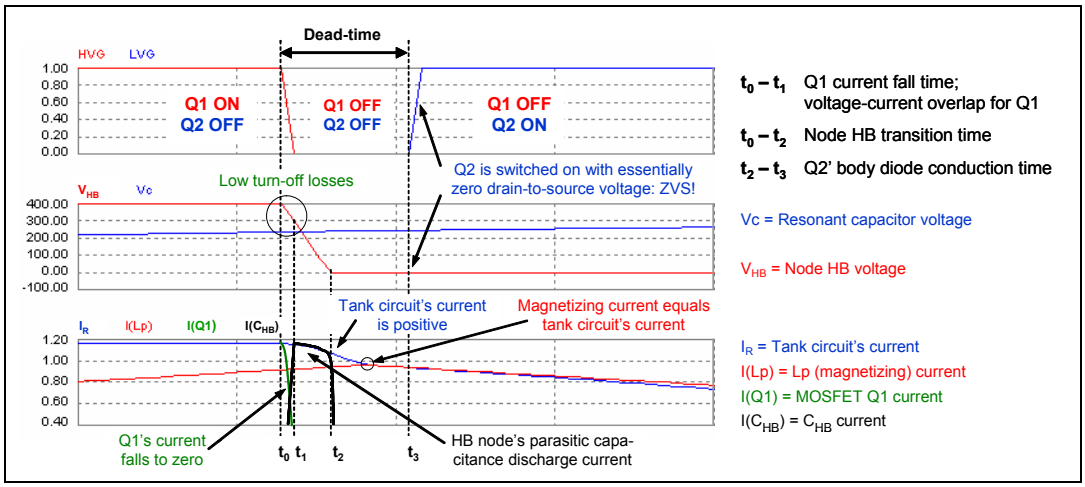


As previously stated, there is no overlap between the conduction of Q1 and Q2. Additionally, a deadtime T_D between the transitions from one state to the other of either switch, where they both are open, is intentionally inserted. It is intended that when Q1 is closed and Q2 is open, the voltage applied to the resonant tank circuit is positive. Similarly we will define as negative the voltage applied to the resonant tank circuit when Q1 is open and Q2 is closed. Consistently with two-port circuits sign convention, the input current to the resonant tank, I_R, will be positive if entering the circuit, negative otherwise.

Let us assume Q1 closed and Q2 open. It is then $I_R = I(Q1)$. Despite that the voltage applied to the circuit is positive ($V_{HB} = V_{in}$), I_R can flow in either direction since we are in presence of reactive elements. Let us suppose that I_R is entering the tank circuit (positive current) in the instant t_0 when Q1 opens, and refer to the timing diagram of *Figure 9*.

The current through Q1 falls quickly and becomes zero at $t = t_1$. Q2 is still open and I_R must keep on flowing almost unchanged because of the inductance of the resonant tank that acts as a current flywheel. The electrical charge necessary to sustain I_R will come initially from C_{HB}, initially charged at V_{in}, which will be now discharged. Provided $I_R(t_1)$ is large enough, the voltage of the node HB will then fall at a certain rate until $t = t_2$, when its voltage becomes negative and the body diode of Q2, DQ2, becomes forward biased, thus clamping the voltage at a diode forward drop V_F below ground. I_R will go on flowing through DQ2 for the remaining part of the deadtime T_D until $t = t_3$, when Q2 turns on and its $R_{DS(on)}$ shunts DQ2. When this occurs, the voltage across Q2 is $-V_F$, a value negligible as compared to the input voltage V_{in}. In the end, this is what is called zero-voltage switching (ZVS): the turn-on transition of Q2 is done with negligible dissipation due to voltage-current overlap and with C_{HB} already discharged, there will be no significant capacitive loss either. Note, however, that there will be nonnegligible power dissipation associated to Q1's turn-off because there will be some voltage-current overlap during the time interval $t_0 - t_1$.

Figure 9. Detail of Q1 ON-OFF and Q2 OFF-ON transitions with soft-switching for Q2



There is an additional positive side effect in turning on Q2 with zero drain-to-source voltage. It is the absence of the Miller effect, normally present in power MOSFETs at turn-on when hard-switched. In fact, as the drain-to-source voltage is already zero when the gate is supplied, the drain-to-gate capacitance Cgd cannot "steal" the charge provided to the gate. The so-called "Miller plateau", the flat portion in the gate voltage waveform, as well as the associated gate charge, is missing here and less driving energy is therefore required. Note that this property provides a method to check if the converter is running with soft-switching or not by looking at the gate waveform of Q2 (which is more convenient because it is source-grounded), as shown in *Figure 10* and *11*.

Figure 10. Q2 gate voltage at turn-on: with soft-switching

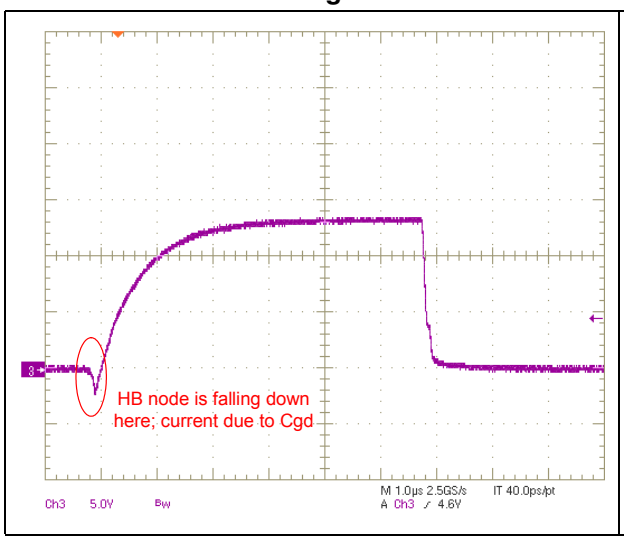
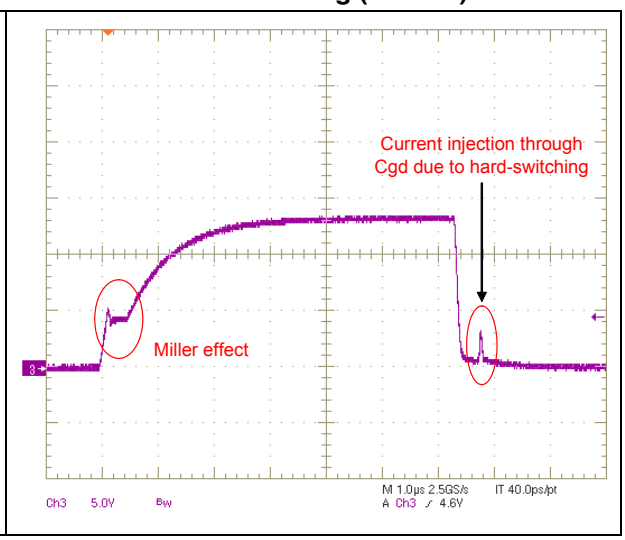


Figure 11. Q2 gate voltage at turn-on: with hard-switching (no ZVS)



With similar reasoning it is possible to understand that the same ZVS mechanism occurs to Q1 when it turns on if I_R is flowing out of the resonant tank circuit (negative current).

In the end we can conclude that, if the tank current at the instant of half-bridge transitions has the same sign as the impressed voltage, both switches will be "soft-switched" at turn-on, i.e. turned on with zero voltage across them (ZVS). It is intuitive that this sign coincidence

occurs if the tank current lags the impressed voltage (e.g. it is still positive while voltage has already gone to zero), which is a condition typical of inductors. In other words, ZVS occurs if the resonant tank input impedance is inductive. The frequency range where tank current lags the impressed voltage is therefore called the "inductive region".

It is worth emphasizing the essential role of DQ1 and DQ2 in ensuring continuity to current flow and clamping the voltage swing of the node HB at $V_{in}+V_F$ and $-V_F$ respectively (the LLC resonant half-bridge belongs to the family of ZVS clamped-voltage topologies). Power MOSFETs, with their inherent body diodes are therefore the best suited power switches to be used in this converter topology. Other types of switches, such as BJT or IGBT, would need the addition of external diodes.

Going back to the state when Q1 is closed and Q2 open, let us now assume that at the instant t_0 when Q1 opens, current is flowing out of the resonant tank towards the input source, i.e. it is negative. This operation is shown in the timing diagrams of *Figure 12*.

With Q1 now open the current will go on flowing through DQ1 throughout the deadtime, and will eventually be diverted through Q2 only when Q2 closes at $t = t_1$, the end of the deadtime. As far as Q1 is concerned, then, there will be no loss associated to turn-off because the voltage across it does not change significantly (it is essentially the same situation seen at turn-on when the converter works in the inductive region).

Q2, instead, will experience now a totally different situation. As DQ1 is conducting during the deadtime, the voltage across Q2 at $t = t_1$ equals $V_{in}+V_F$ so that there will be not only a considerable voltage-current overlap but the energy of C_{HB} will be dissipated inside its $R_{DS(on)}$ as well. In this respect, it is a "hard-switching" condition identical to what normally happens in PWM-controlled converters at turn-on. The associated power dissipation $½C_{HB}V_{in}^2f$ may be considerably higher than that normally dissipated under "soft-switching" conditions and this may easily lead to Q1 overheating, since heat sinking is not usually sized to handle this abnormal condition.

In addition to that, at $t = t_1$ the body diode of Q1, DQ1, is conducting current and its voltage is abruptly reversed by the node HB being forced to ground by Q2. Hence, DQ1 will keep its low impedance and there will be a condition equivalent to a shoot-through between Q1 and Q2 until it recovers (at $t = t_2$).

It is well-known the power MOSFET's body diodes do not have brilliant reverse recovery characteristics. Hence DQ1 will undergo a reverse current spike large in amplitude (it can be much larger than the forward current it was carrying at $t=t_1$) and relatively long in duration (in the hundred ns) that will go through Q2 as well. This spike, in fact, cannot flow through the resonant tank because Ls does not allow for abrupt current changes.

This is a potentially destructive condition not only because of the associated power dissipation that adds up to the others previously considered, but also due to the current and voltage of DQ1 which are simultaneously high during part of its recovery. In fact, there will be an extremely high dv/dt (many tens of V/ns!) experienced by Q1 as DQ1 recovers and the voltage of the node HB goes to zero. This dv/dt may exceed Q1 rating and lead to an immediate failure because of the second breakdown of the parasitic bipolar transistor intrinsic in power MOSFET structure. Finally, it is also possible that Q1 is parasitically turned on if the current injected through its Cgd and flowing through the gate driver's pull down, which is holding the gate of Q1 low, is large enough to raise the gate voltage close to the turn-on threshold (see the spike after turn-off in the graph of *Figure 11*). This would cause a lethal shoot-through condition for the half-bridge leg.

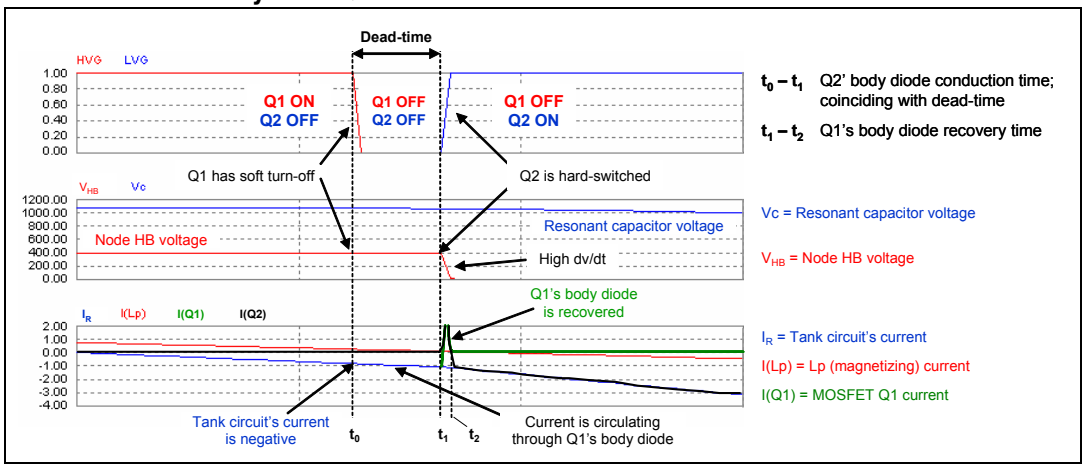
An additional drawback of this operation is the large and energetic negative voltage spikes induced by the recovery of DQ1 because of the unavoidable parasitic inductance of the PCB

subject to its di/dt, which may damage any control IC coupled to the half-bridge leg, not to mention the big EMI generation.

Similarly, it is possible to show that the same series of adverse events will happen to Q1 and Q2, with exchanged roles, when Q2 is turned off if I_R is flowing into the resonant tank circuit (positive current).

The obvious conclusion is that, if the tank current and the impressed voltage at the instant of half-bridge transitions have opposite signs, both switches will be hard-switched and the reverse recovery of their body diodes will be invoked, with all the resulting negative effects. It is intuitive that this sign opposition occurs if the tank current leads the impressed voltage, which is typical of capacitors and then occurs if the resonant tank input impedance is capacitive. This kind of operation is often termed "capacitive mode" and the frequency range where tank current leads the impressed voltage is called the "capacitive region".

Figure 12. Q1 ON-OFF and Q2 OFF-ON transitions with hard switching for Q2 and recovery for DQ1



Then, the converter must be operated in the region where the input impedance is inductive (the inductive region), that is, for frequencies $f > f_{R1}$ or in the range $f_{R2} < f < f_{R1}$ provided the load resistance R is such that $R > R_{crit}$. This is a necessary condition in order for Q1 and Q2 to achieve ZVS, which is evidently a crucial point for the good operation of the LLC resonant half-bridge.

To summarize, ZVS brings the following benefits:

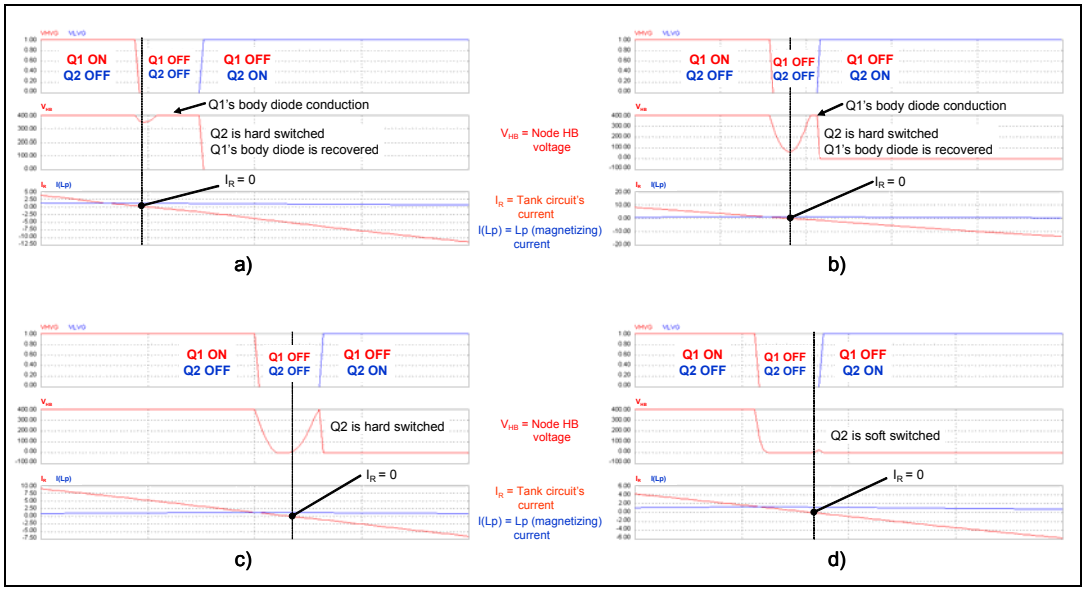
1. low switching losses: either high efficiency can be achieved if the half-bridge is operated at a not too high switching frequency (for example < 100 kHz) or high switching frequency operation is possible with a still acceptably high efficiency (definitely out of reach with a hard-switched converter);
2. reduction of the energy needed to drive Q1 and Q2, thanks to the absence of Miller effect at turn-on. Not only is turn-on speed unimportant because there is no voltage-current overlap but also gate charge is reduced, then a small source capability is required from the gate drivers.
3. low noise and EMI generation, which minimizes filtering requirements and makes this converter extremely attractive in noise-sensitive applications.
4. all of the above-mentioned adverse effects of capacitive mode, which not only impair efficiency but also jeopardize the converter, are prevented.

Note, however, that working in the inductive region is not a sufficient condition in order for ZVS to occur.

In the above discussion, it has been said that the voltage of the node HB could swing from V_{in} to zero "provided I_R is large enough". Of course the same holds if we consider node HB's swing from zero up to V_{in}. What actually happens when Q1 turns off with positive I_R current is that the associated inductive energy level of the resonant tank circuit is maintained at the expense of the energy contained in the capacitance C_{HB}. If the inductive energy ($\propto I_R^2$) is greater than that owned by C_{HB} ($\propto V_{in}^2$) C_{HB} will be completely depleted and the voltage of the node HB will be able to reach $-V_F$, injecting DQ2 and allowing Q2 to turn-on with essentially zero drain-to-source voltage. Similarly, when Q2 turns off with negative current, part or all of the associated inductive energy will be transferred to C_{HB}. If the available inductive energy is greater than that needed to charge C_{HB} up to $V_{in}+V_F$, the node HB will be allowed to swing all the way up until DQ1 is injected, thus clamping the voltage, and Q1 will be able to turn-on with essentially zero drain-to-source voltage.

Seen from a different perspective, the inductive part of the tank circuit resonates with C_{HB}, and this is the origin of the term "resonant transition" used for designating resonant converters having this property. This "parasitic" tank circuit active during transitions is formed by C_{HB} with the series inductance Ls if during the half-bridge transition there is current circulating on the secondary side (so that Lp is shorted out) or with the total inductance Ls + Lp if there is no current conduction on the secondary side.

Figure 13. Bridge leg transitions in the neighborhood of inductive-capacitive regions boundary



The above mentioned energy balance considerations, however, are not still sufficient to guarantee ZVS under all operating conditions. There is an additional element that needs to be considered, the duration of the deadtime T_D.

The first obvious consideration is that the duration of the deadtime represents an upper limit to the time the node HB takes to swing from one rail to the other: in order for the mosfet that is about to turn on to achieve ZVS (i.e. to be turned on with zero drain-to-source voltage), the transition has to be completed within T_D as depicted in *Figure 9*. However, the way the

deadtime and ZVS are related is actually more complex and depends on converter's operating conditions.

It is instructive to see this in *Figure 13*, which shows typical node HB waveforms occurring when working in the inductive region but too close to the capacitive region, so that ZVS is not achieved. They refer to the Q1 →OFF, Q2 → ON transition; those related to the opposite transition are obviously turned upside down.

- Case a) is very close to the boundary between inductive and capacitive regions. Tank current reverses just after Q1 is switched off, a portion of node HB ringing appears as a small "dip", then the tank current becomes negative enough to let the body diode of Q1 start conducting. When Q2 turns on there are capacitive losses and the recovery of the Q1's body diode with all the related issues.
- Case b) is slightly more in the inductive region but still I_R crosses zero within the deadtime. The node HB ringing becomes larger and the body diode of Q1 still conducts for a short time and its recovery is invoked as Q2 turns on.
- Case c) Is even more in the inductive region but still not sufficiently away from the capacitive-inductive boundary. The ringing of the node HB is large enough to reach zero but I_R reverses within the deadtime and the voltage goes up again. At the end of the deadtime the voltage does not reach Vin, hence the body diode of Q1 does not conduct and Q2, when turned on, will experience only capacitive losses.
- Case d) Is further in the inductive region and I_R crosses zero nearly at the end of the deadtime. Q2 is now almost soft-switched with no losses. This can be considered as the boundary of the operating region where ZVS can be achieved with the given duration of T_D.

Note that the resonant tank's current during node HB ringing is lower than the one flowing through Lp. This means that their difference is flowing into the transformer and, consequently, that one of the secondary half-windings is conducting. Therefore, C_{HB} is resonating with Ls only.

This analysis shows that there is a "border belt" in the inductive region, close to the boundary with the capacitive region ($f_{R2} < f < f_{R1}$, $R = R_{crit}$) and that as converter's operation is moved away from the capacitive-inductive boundary and pushed more deeply in the inductive region there is a progressive behavior change from hard-switching to soft-switching. In the cases a and b the inductive energy in the resonant tank is too small to let the node HB even swing "rail-to-rail"; moving away from the boundary, as shown in case c, the energy is higher and allows a rail-to-rail swing, but it is not large enough to keep the node HB "hooked" to the rail throughout the deadtime T_D. If the converter is operated in this border belt, Q1 and Q2 will be hard-switched at turn-on and, in cases such as case a and case b, the body diode of the just turned off power MOSFET is injected and then recovered as the other power MOSFET turns on.

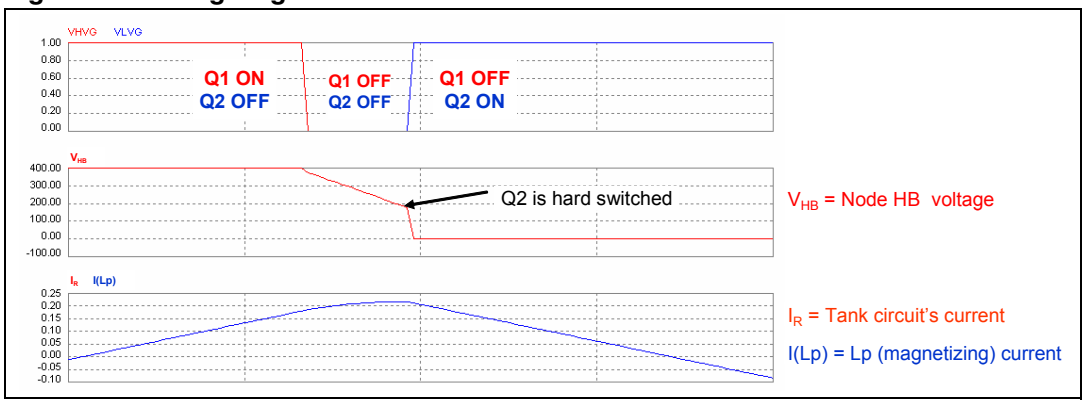
Case b and, especially, case c highlight that it is possible to look at the deadtime T_D also from another standpoint: looking at those waveforms, one might conclude that the current I_R at the beginning of the deadtime is too low or, conversely, that the deadtime is too long. In case c, for example, if the dead-time had been approximately half the value actually shown, Q2 would have been soft-switched at turn-on. Of course, the more appropriate interpretation depends on whether T_D is fixed or not.

These cases are related to heavy load conditions.

Figure 14 shows a case typical of no-load conditions, where ZVS is not achieved because of a too slow transition of the node HB so that it does not swing completely within the deadtime T_D. In this case the situation seems less stressful than operating in the capacitive region.

There is no body diode conduction and, consequently, no recovery. Q1 will be almost soft-switched at turn-off, while Q2 will have capacitive losses at turn-on. It is true that the turn-on voltage is lower than V_{in}, thus the associated energy of C_{HB} is lower, but at no-load the operating frequency is usually considerably higher than in the capacitive region, then these power losses may easily overheat Q1 and Q2. Finally, note in *Figure 14* that I(Lp) is exactly superimposed on I_R, then the secondary side of the transformer is open and C_{HB} is resonating with the total inductance Ls+Lp.

Figure 14. Bridge leg transitions under no-load conditions



From what we have seen we can conclude that the conditions in order for the half-bridge switches to achieve ZVS are:

1. Under heavy load conditions, as one switch turns off, the tank current must have the same sign as the impressed voltage and be large enough so that both the rail-to-rail transition of the node HB is completed and the current itself does not reverse before the end of the deadtime, when the other switch turns on.
2. With no-load, the tank current at the moment one switch turns off (which has definitely the same sign as the impressed voltage) must be large enough to complete the node HB transition within the deadtime, before the other switch turns on.

Both conditions can be translated into specifying a minimum current value I_{Rmin} that needs to be switched when either power MOSFET turns off. In general, different I_{Rmin} values are needed to ensure ZVS at heavy load and at no-load. One can simply pick the greater one to ensure ZVS under any operating condition by design. On the other hand, this minimum required amount of current is to the detriment of efficiency.

At light or no-load a significant current must be kept circulating in the tank circuit, just to maintain ZVS, in spite of the current delivered to the load that is close to zero or zero. Using ac-analysis terminology, a certain amount of reactive energy is required even with no active energy.

Finally, also at heavy load the value of I_{Rmin} to be specified is the result of a trade-off. In fact, its value is directly related to the turn-off losses of both Q1 and Q2. The higher the switched current is, the larger the switching loss due to voltage-current overlap will be.

The discussion on the switching mechanism has been focused on the primary-side switches, and the conditions in order for them to achieve soft-switching (ZVS at turn-on, precisely) have been found. One important merit of the LLC resonant converter is that also the rectifiers on the secondary side are soft-switched. They feature zero-current switching (ZCS) at both turn-on and turn-off. In fact, at turn-on the initial current is always zero and ramps up with a relatively low di/dt, so that forward recovery does not come into play. At turn-off they become reverse biased when their forward current is already zero, so that their

reverse recovery is not invoked. This topic will be addressed in *Section 2.3*, where it will be shown that this property is inherent in the topology, hence it occurs regardless of converter's design or operating conditions.

2.3 Fundamental operating modes

The LLC resonant half-bridge converter features a considerable number of different operating modes, which stem from its multiresonant nature. Essentially, the term "multiresonant" means that the configuration of the resonant tank may change within a single switching cycle. We have seen that there are two resonant frequencies, one (the higher) associated to either of the secondary rectifiers conducting, the lower one associated to both rectifiers non-conducting. Then, depending on the input-to-output voltage ratio, the output load and the characteristics of the resonant tank circuit, the secondary rectifiers can be always conducting (with the exception of a single point in time), which is referred to as CCM (Continuous Conduction Mode) like in PWM converters, or there can be finite time intervals during which neither of the secondary rectifiers is conducting. This will obviously be called a DCM (Discontinuous Conduction Mode) operating mode.

Different kinds of CCM and DCM operating modes exist, although not all of them can be seen in a given converter, some are not even recommended, like those associated with capacitive mode operation. However, in all CCM modes the parallel inductance Lp is always shunted by the load resistance reflected back to the primary side, so that it never participates in resonance, rather it acts as an additional load to the remaining LC resonant circuit. Similarly, in all DCM modes, there will be some finite time intervals where Lp, being no longer shunted from the secondary side, becomes part of resonance.

In the following we will consider four fundamental operating modes and use the nomenclature defined in [*3*]:

1. Operation at resonance, when the converter works exactly at $f = f_{R1}$;
2. Above-resonance operation, when the converter works at a frequency $f > f_{R1}$. Moving away from resonance, we will consider three sub-modes:
   a) CCMA operation at heavy load;
   b) DCMA operation at medium load;
   c) DCMAB operation at light load;
3. Below-resonance operation, when the converter works at a frequency $f_{R2} < f < f_{R1}$ with a load resistor $R > R_{crit}$. Moving away from resonance, we will consider two sub-modes:
   a) DCMAB operation at medium-light load;
   b) DCMB operation at heavy load;
4. Below-resonance operation, when the converter works at a frequency $f_{R2} < f < f_{R1}$ with a load resistor $R < R_{crit}$ (capacitive mode), corresponding to the CCMB operating mode defined in [*3*];

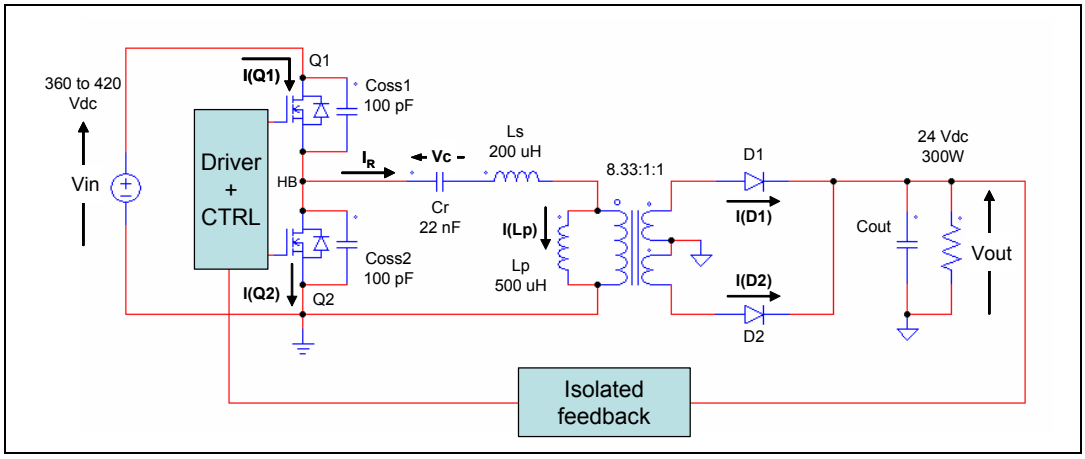
In addition, two extreme operating conditions will be considered:

1. No-load operation (cutoff)
2. Output short-circuit operation

It is interesting to point out that, unlike PWM converters where DCM operation is invariably associated to light load operation and CCM to heavy load operation, in the LLC resonant converter this combination does not hold.

To illustrate the above-mentioned operating modes we will refer to the reference converter shown in *Figure 15*. The discussion will start from the inspection of the main waveforms in a switching cycle, highlighting each subinterval where the circuit assumes a topological state and deducing the properties of the converter when operated in that mode from those waveforms. Half-bridge leg transitions are considered instantaneous. Their features have been already discussed.

Figure 15. Reference LLC converter for the analysis of the fundamental operating modes



2.3.1 Operation at resonance ($f = f_{R1}$)

In this operating mode it is possible to distinguish six fundamental time subintervals within a switching cycle, which are illustrated in *Figure 16*.

The first subinterval and, then, the instant t_0 can be chosen quite arbitrarily. We fix t_0 as the instant when, with Q1 conducting and Q2 open, the tank current I_R has a positive-going zero-crossing.

a) $t_0 \rightarrow t_1$. Q1 is ON and Q2 is OFF. This is the "energy taking" phase, when current flows from the input source to the tank circuit, so that energy is positive and both refills the resonant tank and supplies the load. The operating point of Q1 is in the first quadrant (current is flowing from drain to source). D2 is reverse-biased with a voltage $-2 \cdot V_{out}$ (it is actually larger because of the contribution from the secondary leakage inductance L_{L2}). D1 is conducting, so Lp is shorted by the output load reflected back to the primary side and the voltage across it is fixed at $a \cdot V_{out}$. Lp, then, is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when Q1 is switched off at $t=t_1$, I_R reaches its maximum value, after that it starts decaying. Note that at $t=t_1$ I_R=I(Lp) and then I(D1)=0.

b) $t_1 \rightarrow t_2$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_1$ I(Q1)=I(Lp)=I_R is greater than zero and provides the energy to let the node HB swing from V_{in} to 0, so that the body diode of Q2, DQ2, is injected. This allows I_R to flow. The voltage across Lp reverses to $-a \cdot V_{out}$ and the slope of its current changes sign. D2 starts conducting while D1 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). This phase ends when Q2 is switched on at $t=t_2$.

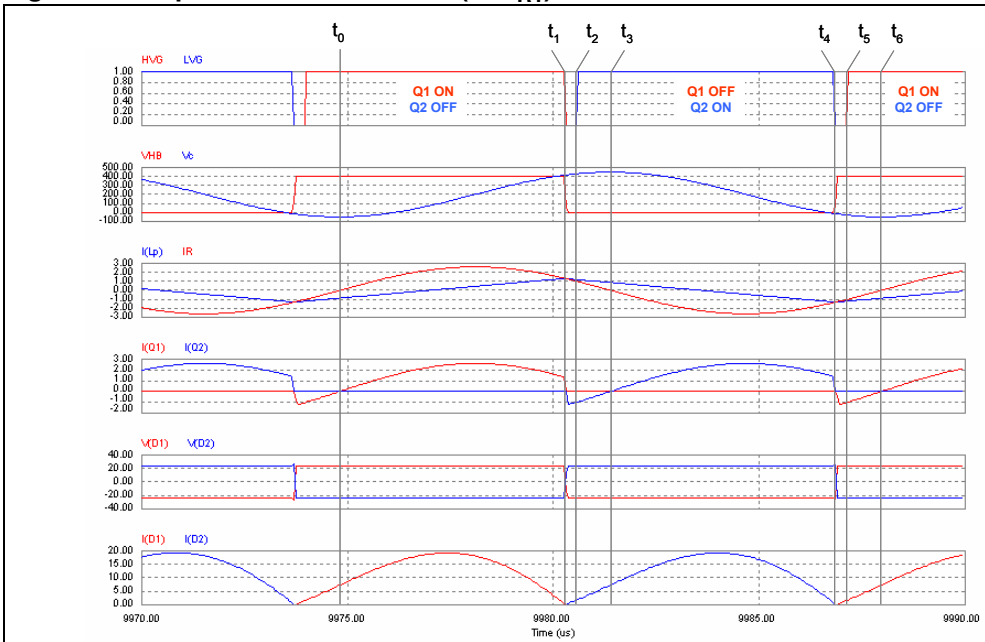
c) $t_2 \rightarrow t_3$. Q1 is OFF and Q2 is ON. At $t=t_2$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. Note that now

the operating point of Q2 is in the third quadrant, current is flowing from the source to drain. D2 keeps on conducting and the voltage across Lp is $-a \cdot V_{out}$, so that Lp is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_3$.

d) $t_3 \rightarrow t_4$. Q1 is OFF and Q2 is ON. Tank circuit current, which is zero at $t=t_3$ becomes negative. D1 is non-conducting and its reverse voltage is approximately $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). Lp's current has a negative slope, so the voltage across Lp must be negative. Since the diode D2 is conducting, this voltage will be equal to $-a \cdot V_{out}$. Lp, then, is not participating in resonance, Cr is resonating with Ls only and I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when Q2 is switched off at $t=t_4$, I_R reaches its minimum value, after that it starts increasing. Note that at $t=t_4$ $I_R=I(Lp)$ and then $I(D2)=0$.

e) $t_4 \rightarrow t_5$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_4$ $I(Q2)=-I(Lp)=-I_R$ is greater than zero and provides the energy to let the node HB swing from 0 to V_{in}, so that the body diode of Q1, DQ1, is injected. This allows I_R to flow back to the input source. The voltage across Lp reverses to a V_{out} and its current slope changes sign. D1 starts conducting while D2 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). This phase ends when Q1 is switched on at $t=t_5$.

Figure 16. Operation at resonance ($f = f_{R1}$): main waveforms



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

f) $t_5 \rightarrow t_6$. Q1 is ON and Q2 is OFF. At $t=t_5$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. Note that now the operating point of Q1 is in the third quadrant, current is flowing from the source to drain. This phase, along with the preceding one can be referred to as the "external energy recirculation phase": current is negative (coming out of the input terminal) despite that the impressed voltage is positive so that the input energy is

negative, i.e. it is returned to the input source. D1 keeps on conducting and the voltage across Lp is $a \cdot V_{out}$, so that Lp is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_6$ and another switching cycle starts.

Remarks

1. Parallel inductor Lp never resonates and its current is essentially triangular (note: the real magnetizing current is sinusoidal and cannot be seen on the oscilloscope). The LLC converter, then, can be regarded as a series LC resonant half-bridge (composed by Ls and Cr) that supplies a reactive RL load (composed by Lp and R_{ac}, the equivalent ac resistor loading the converter, as defined in [2] and reflected back to the primary side). This standpoint provides considerable insight into the operation of the converter, as shown in some of the following remarks.
2. In a resistively loaded series LC tank operating at resonance, the impressed voltage and the tank current are exactly in-phase, hence the switched current is zero and, thereby, ZVS cannot be achieved. The effect of adding an inductor (Lp) in parallel to the resistive load is to provide tank current with the phase shift (lagging) necessary to switch a current greater than zero, so that ZVS becomes now possible at resonance. As shown in the diagrams of *Figure 16*, the tank circuit current lags the impressed voltage by an angle φ equal to:

Equation 5

$$\varphi = 2\pi\frac{t_6 - t_4}{t_6 - t_0}$$

so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_1)$ and $I_R(t_4)$ are large enough to complete the HB node swing well within the deadtimes (t_1, t_2) and (t_4, t_5) respectively. It is not difficult to recognize that the angle φ is the phase of the input impedance of the loaded resonant tank evaluated at $f=f_{R1}$. Additionally, since the impedance of a series LC tank operating at resonance is zero, it is possible to state that the input impedance of the LLC resonant tank at resonance equals the impedance of the RL load.

3. Generally speaking, in a series LC tank operating at resonance, the voltage drop across L is equal in module and opposite in sign to the drop across C at all times (this is why its impedance is zero). In our specific case the drop across the series Cr-Ls will be zero, so that it is possible to write the following voltage balance equations:

Equation 6

$$V_{in} - \frac{V_{in}}{2} = a \cdot V_{out} \qquad \text{Q1 ON, Q2 OFF}$$

$$-\frac{V_{in}}{2} = -a \cdot V_{out} \qquad \text{Q1 OFF, Q2 ON}$$

both of them resulting in the following relationship:

Equation 7

$$\frac{V_{in}}{2} = a \cdot V_{out}$$

This is a fundamental property of the LLC resonant half-bridge: operating at $f=f_{R1}$ implies that input and output voltages fulfill (1) and, vice versa, if input and output voltages meet *Equation 7* the converter is operating at $f=f_{R1}$. Then, the fact that the converter operates at resonance or not, for a given output voltage V_{out} and a given turn

ratio a (n), depends only on the input voltage, not on the load and on the parameters of the resonant tank. From the design point of view, since V_{in} and V_{out} are specified, one can decide the input voltage where to operate at resonance by choosing the turns ratio a. $V_{in}/2=a \cdot V_{out}$ considered as the 1:1 conversion ratio for the LLC resonant half-bridge.

4. The logical consequence of LLC converter's ability to operate at resonance independently of the output load is that the LLC resonant half-bridge can deliver any power if operated at resonance. This can be seen also in another way. As the impedance of the series Cr-Ls is zero, the RL load R_{ac}//Lp "sees" the impressed voltage directly or, in other words, it is supplied by an ideal voltage source. This is a "singularity" in LLC converter's operation, sometimes referred to as the "load-independent" point, where the usual energy vs. frequency relationship does not hold. Actually, the inevitable voltage drops across the resistive elements of the real-world circuit (such as power MOSFETs' $R_{DS(on)}$, winding resistance, secondary rectifier's drop, etc.) cause a slight dependence of the frequency on the load. Note that this is a situation analog to that of CCM-operated PWM converters, where duty cycle is ideally independent of the load, in reality slightly dependent because of losses.
5. Energy is taken from the input source only from t_0 to t_1, the "energy taking" phase, then for less than half the switching period, while from t_1 to t_4 energy recirculates internally to allow energy flow to the load while Q1 is not conducting. This low "duty cycle" of the input current can be a limiting factor in terms of power handling capability, especially if the input voltage is low. This consideration suggests the use of the half-bridge topology in high input voltage applications (e.g. with a PFC front-end, which provides a 400 V input rail). The natural improvement to this limitation is the full-bridge topology, where phase d) becomes active as well.
6. Tank circuit current lag φ originates the external energy recirculation phase from t_4 to t_6 during which energy flow is negative (impressed voltage and input current have opposite signs). This energy subtracts to that drawn from the input during the energy taking phase a), hence reducing the net energy flow from the input source to the load each cycle. This energy can be regarded as reactive energy and cos φ as the input power factor. Making φ as small as possible (i.e. increasing Lp) would shorten the duration of the external energy recirculation phase and reduce the amount of reactive energy, thus improving the energy transfer process. This, however, would also reduce $I_R(t_1)$ and $I_R(t_4)$, hence φ can be reduced as long as ZVS is maintained.
7. Recalling that the current switched at turn-off by Q1, $I_R(t_1)$ and by Q2, $I_R(t_4)$ determine their switching losses, it is straightforward that keeping φ to the minimum value that ensures ZVS of Q1 and Q2 provides an optimum design. Of course, component tolerance must be adequately accounted for, thus φ must be larger than the minimum required and the typical operation will be suboptimal.
8. The secondary rectifiers D1 and D2 start conducting as Q2 and Q1 turn-off respectively. The initial current is zero and also its di/dt is low, thus they have a soft turn-on. D1 and D2 cease to conduct exactly when Q1 and Q2 turn-off, respectively. These are also the moments when the voltages across D1 and D2 reverse. As a result, neither D1 nor D2 experience a voltage reversal while conducting a forward current. Reverse recovery, with all its adverse effects, does not occur. Note that, in this respect, this is a situation identical to that of a PWM converter operating on the boundary between CCM and DCM.

2.3.2 Operation above resonance ($f > f_{R1}$)

In this operating mode the converter exhibits its usual frequency vs. load characteristic. We will consider three submodes where, in a closed-loop regulated system, CCM operation

progressively turns into DCM operation as the output load is reduced and frequency is moved away from resonance.

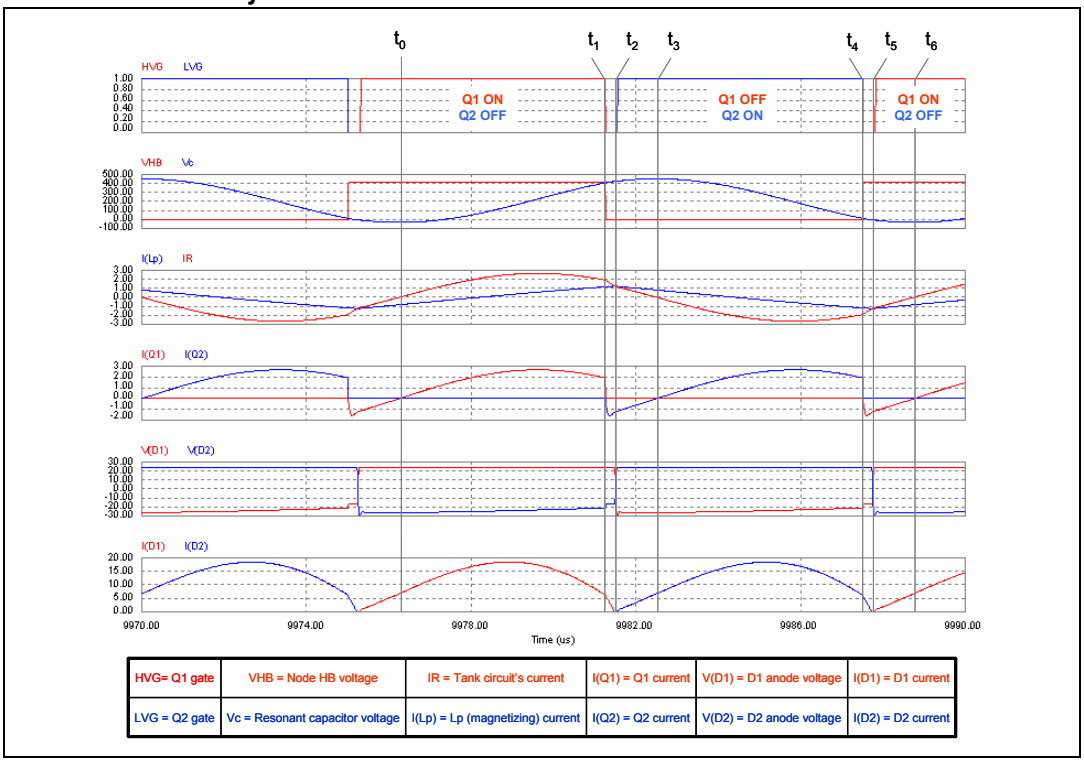
CCMA operation at heavy load

Also in this case it is possible to identify six fundamentals subintervals. The relevant waveforms are illustrated in the timing diagram of *Figure 17*. Again, t_0 is the instant when, with Q1 conducting and Q2 open, the tank current I_R has a positive-going zero-crossing.

a) $t_0 \rightarrow t_1$. Q1 is ON and Q2 is OFF. This is the "energy taking" phase. It is identical to the corresponding phase seen in the operation at resonance with the only difference that at the end of this phase, at $t=t_1$, it is still $I_R > I(Lp)$ and then $I(D1)>0$.

b) $t_1 \rightarrow t_2$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_1$ I_R is greater than zero and provides the energy to let the node HB swing from V_{in} to 0, so that the body diode of Q2, DQ2, is injected. This allows I_R to flow; I_R slope changes to a higher negative value, so that it quickly approaches I(Lp), which is still increasing with the same slope. D1 conducts until I_R equals I(Lp), and then becomes reverse biased, with a negative voltage equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown), I(Lp) slope changes sign and D2 starts conducting. This phase ends when Q2 is switched on at $t=t_2$. Note that the time Tz needed for I_R to hit I(Lp) is related to their values at $t=t_1$ and their slopes after $t=t_1$ and not to the duration of the deadtime T_D. Here it is $Tz = T_D$ just by chance.

Figure 17. Operation above resonance ($f > f_{R1}$): main waveforms in CCMA operation at heavy load



c) $t_2 \rightarrow t_3$. Q1 is OFF and Q2 is ON. At $t=t_2$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. This phase, which ends when $I_R=0$ at $t=t_3$, is identical to the (t_2, t_3) phase of the operation at resonance.

d) $t_3 \rightarrow t_4$. Q1 is OFF and Q2 is ON. It is identical to the phase (t_3, t_4) seen in the operation at resonance with the only difference that at the end of this phase, at $t=t_4$, it is still $I_R < I(Lp)$ and then $I(D2)>0$.

e) $t_4 \rightarrow t_5$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_4$ I_R is (in absolute value) greater than zero and provides the energy to let the node HB swing from 0 to V_{in}, so that the body diode of Q1, DQ1, is injected. This allows I_R to flow back to the input source. I_R changes to a higher slope, so that it quickly approaches I(Lp), which is still decreasing with the same slope. D2 conducts until I_R equals I(Lp), after that it becomes reverse biased, with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown), I(Lp) slope changes sign and D1 starts conducting. This phase ends when Q1 is switched on at $t=t_5$. Again, the time Tz needed for I_R to hit I(Lp) is only by chance equal to T_D as shown.

f) $t_5 \rightarrow t_6$. Q1 is ON and Q2 is OFF. At $t=t_5$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. This phase, which ends when $I_R=0$ at $t=t_6$, is identical to the (t_5, t_6) phase of the operation at resonance.

Remarks

1. In this "above-resonance" CCM submode the parallel inductor Lp never resonates and the LLC converter can be regarded as a series LC resonant half-bridge supplying a reactive RL load.
2. As shown in the diagrams of *Figure 17*, the tank circuit current lags the impressed voltage by an angle φ equal to:

Equation 8

$$\varphi = 2\pi \frac{t_6 - t_4}{t_6 - t_0}$$

so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_1)$ and $I_R(t_4)$ are large enough to complete the HB node swing well within the deadtimes (t_1, t_2) and (t_4, t_5) respectively. Still φ is the phase of the input impedance of the loaded resonant tank evaluated at $f=f_{R1}$, but now since the impedance of the series LC tank is no longer zero, it is different from the impedance of the RL load.

3. In the series Cr-Ls tank circuit operating above resonance the voltage drop across it is positive (the inductive reactance is larger in module than the capacitive reactance), i.e. the plus sign is located on the side of the node HB. The obvious conclusion is that:

Equation 9

$$a \cdot V_{out} < \frac{V_{in}}{2}$$

Then, when operating above resonance, for a given input voltage the LLC resonant half-bridge will provide an output voltage lower than that available at resonance and vice versa, with a given output voltage the LLC resonant half-bridge will operate above resonance with an input voltage greater than $2 \cdot n \cdot V_{out}$. In this case the conversion ratio, intended as previously mentioned is < 1, then the LLC is said to have a "step-down" or "buck" characteristic when operating above resonance.

4. When operating above resonance, the Thevenin-equivalent schematic of the LLC resonant tank as seen by the load has finite impedance (no more zero as when operating at resonance). When the load current increases, for a given frequency (open-

loop operation) the voltage conversion ratio diminishes. For a given V_{out} (closed-loop operation) operating frequency needs to get back closer to resonance.

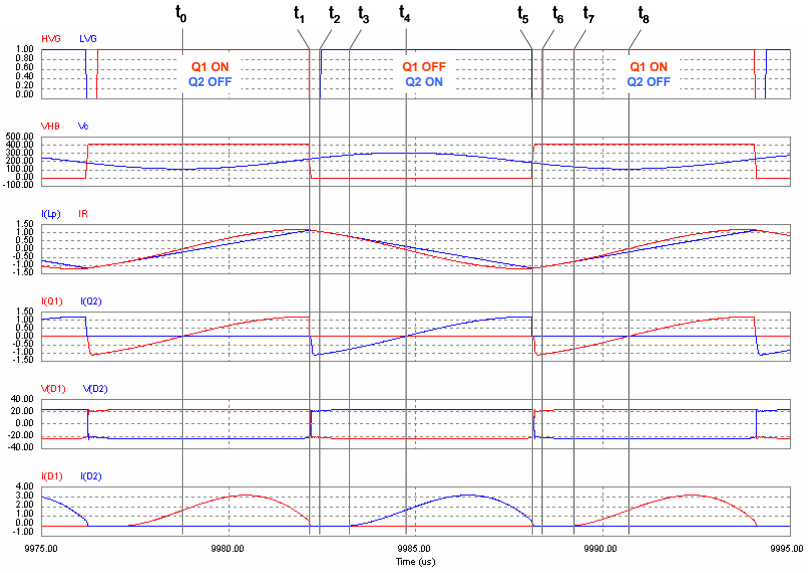
5. The secondary rectifiers D1 and D2 start conducting as Q1 and Q2 turn-on respectively. The initial current is zero and also its di/dt is low, thus they have a soft turn-on. D1 and D2 cease to conduct when tank circuit's current I_R equals Lp's current I(Lp). The transformer's secondary current is a·[I_R-I(Lp)], then the equality I_R = I(Lp) means that the secondary rectifiers current is zero as well. Unlike when operating at resonance, this does not happen synchronously with the half-bridge leg transitions (I_R < I(Lp) at t=t_1 and I_R > I(Lp) at t=t_4). However as the leg transition occurs I_R and I(Lp) are "forced" to become equal, then the current of the conducting diode goes to zero. The physical reason for that is the presence of Ls. When there is a transition of the half-bridge leg the resulting voltage change is not immediately directly impressed on the transformer (C can be considered as a short circuit during transitions, i.e. the voltage across it can be considered constant) but falls across Ls that acts as a "shock absorber". This leaves I(Lp) unchanged but pushes I_R towards I(Lp), forcing a rate of change that is approximately:

Equation 10

$$\frac{dI_R}{dt} \approx \begin{cases} -\dfrac{Vc + a \cdot V_{out}}{Ls} & t \in (t_1, t_2) \\ \dfrac{V_{in} - Vc + a \cdot V_{out}}{Ls} & t \in (t_4, t_5) \end{cases}$$

Only when I_R equals I(Lp) and no current is flowing through the secondary rectifier previously conducting can the voltage across the primary winding of the transformer reverse and hence also the voltage across the secondary rectifiers. In the end, also in this case they are reverse-biased only when their current has gone to zero, thus ensuring ZCS.

Figure 18. Operation above resonance (f > f_{R1}): main waveforms in DCMA operation at medium load



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

DCMA at medium load

In this "above-resonance" DCM submode it is possible to identify eight fundamentals subintervals. The relevant waveforms are illustrated in the timing diagram of *Figure 18*.

Two new subintervals, namely (t_2, t_3) and (t_6, t_7), appear just after the deadtimes of the half-bridge leg transitions (t_1, t_2), (t_5, t_6), respectively. The other six phases are exactly identical to those of the CCM above-resonance mode.

a) $t_2 \rightarrow t_3$. Q1 is OFF and Q2 is ON. At $t=t_2$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. Note that the operating point of Q2 is in the third quadrant, current is flowing from the source to drain. D1 is nonconducting but the voltage across the secondary windings is still too low to let D2 conduct, then still I_R = I(Lp) is a portion of a sinusoid having a frequency $f = f_{R2}$. This phase ends when D2 starts conducting at $t=t_3$.

b) $t_6 \rightarrow t_7$. Q1 is ON and Q2 is OFF. At $t=t_6$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. Note that the operating point of Q1 is in the third quadrant, current is flowing from the source to drain. D2 is nonconducting but the voltage across the secondary windings is still too low to let D1 conduct, then still I_R = I(Lp) is a portion of a sinusoid having a frequency $f = f_{R2}$. This phase ends when D1 starts conducting at $t=t_7$.

Remarks

1. In this "above-resonance" DCM submode the multiresonant nature of the LLC converter shows up. In a switching cycle there are two time intervals just after bridge-leg transitions during which no current is flowing on the secondary side (hence this is DCM operation), then the entire transformer's primary inductance Ls+Lp resonates and the second resonance frequency f_{R2} appears. At the transitions of the half-bridge leg the resonant current I_R is still slightly greater than I(Lp) in absolute value, so it takes a very small portion of the deadtimes for the two currents to equal each other. Then, the first one starts as I_R equals I(Lp) slightly after t_1 and ends at $t= t_3$. The second one starts slightly after t_5 and ends at $t= t_7$.
2. As shown in the diagrams of *Figure 18*, the tank circuit current is still lagging the impressed voltage, so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_1)$ and $I_R(t_5)$ are large enough to complete the HB node swing well within the deadtimes (t_1, t_2) and (t_5, t_6) respectively. However, as compared to CCM mode, the duration of the energy taking phase (t_0, t_1) is shorter, the external recirculation phase is longer and the displacement angle φ:

Equation 11

$$\varphi = 2\pi\frac{t_8 - t_6}{t_8 - t_0}$$

gets close to $\pi/2$. Using ac terminology, the active energy is lower and the reactive energy is higher.

3. The secondary rectifiers D1 and D2 start conducting during the conduction period of Q1 and Q2, respectively. Both the initial current and also its di/dt are zero, thus they have a soft turn-on. D1 and D2 cease to conduct when tank circuit's current I_R equals Lp's current I(Lp). In this case this is almost synchronous with either switch turn-off. Again, only when I_R equals I(Lp) and no current is flowing through the secondary rectifier previously conducting can the voltage across the primary winding of the transformer reverse and hence also the voltage across the secondary rectifiers. In the

end, also in this case they are reverse-biased only when their current has gone to zero, thus ensuring ZCS.

4. Essentially, the reason why D2 does not conduct during (t_2, t_3) and D1 does not during (t_6, t_7) is that the voltage across the transformer (given by V_{in} - Vc) is not large enough so that the voltage developed across Lp (given by the inductive divider ratio Lp/(Ls+Lp)) and reflected to the secondary side can forward-bias D2 or D1. In formulae, this is expressed as:

Equation 12

$$(V_{in}(t) - Vc(t))\frac{Lp}{Ls + Lp} \leq a \cdot V_{out}$$

DCMAB at light load

In this "above-resonance" DCM sub-mode it is possible to identify ten fundamental subintervals. The relevant waveforms are illustrated in the timing diagram of *Figure 19*.

Two more new subintervals, namely (t_1, t_2), (t_6, t_7) appear just before the deadtimes of the half-bridge leg transitions (t_2, t_3), (t_7, t_8), respectively. The remaining eight phases are exactly identical to those of the DCMA above-resonance mode.

a) $t_1 \rightarrow t_2$. Q1 is ON and Q2 is OFF. At $t=t_1$ I_R equals I(Lp) and then I(D1) becomes zero before Q1 turns off at $t=t_2$, when this phase ends, and remains zero until $t=t_2$. During this interval the *Equation 12* is met and the current I_R = I(Lp) is a portion of a sinusoid having a frequency f = f_{R2}.

b) $t_6 \rightarrow t_7$. Q1 is OFF and Q2 is ON. At $t=t_6$ I_R equals I(Lp) and then I(D2) becomes zero before Q2 turns off at $t=t_7$, when this phase ends, and remains zero until $t=t_7$. During this interval the *Equation 12* is met and the current I_R = I(Lp) is a portion of a sinusoid having a frequency f = f_{R2}.

Remarks

1. The transition between this DCMAB mode and the previous DCMA is marked by the I_R = I(Lp) condition occurring exactly at t = t_1 of *Figure 18*.
2. In this "above-resonance" DCM submode, in a switching cycle there are two time intervals (t_1, t_4), (t_6, t_9) during which no current flows on the secondary side (hence this is DCM operation) and then the entire transformer's primary inductance Ls+Lp resonates and f_{R2} appears. Considering each half-cycle, nonconductive intervals appear at the beginning and the end.
3. As shown in the diagrams of *Figure 19*, the tank circuit current is still lagging the impressed voltage, so that they have the same sign at half-bridge leg transitions. Furthermore, the switched currents $I_R(t_2)$ and $I_R(t_6)$ are large enough to complete the HB node swing well within the deadtimes (t_2, t_3) and (t_7, t_8) respectively. As compared to DCMA mode, the duration of the energy taking phase (t_0, t_1) is even shorter, the external recirculation phase is longer and the displacement angle φ:

Equation 13

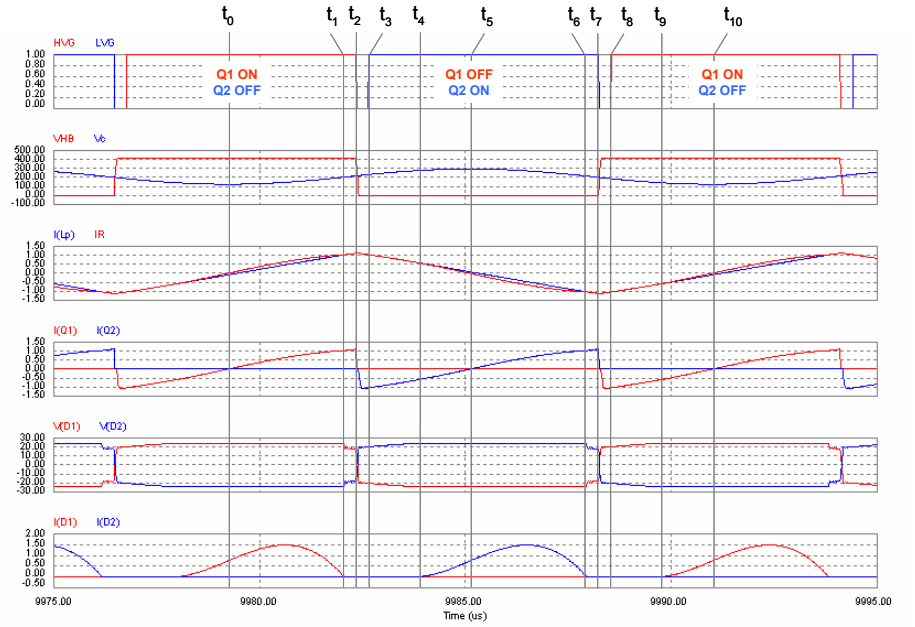
$$\varphi = 2\pi\frac{t_{10} - t_8}{t_{10} - t_0}$$

is even closer to $\pi/2$. Most of the energy in the tank circuit is reactive.

4. As to the secondary rectifiers, they start conducting during the conduction period of Q1 and Q2, respectively. Both the initial current and also its di/dt are zero, thus they have a

soft turn-on. They cease to conduct before the transitions of the half-bridge. The operation is DCM, then ZCS occurs by definition.

Figure 19. Operation above resonance (f > f_{R1}): main waveforms in DCMAB operation at light load



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

2.3.3 Operation below resonance (f_{R2} < f < f_{R1}, R>R_{crit})

In this operating mode the converter still exhibits its usual frequency vs. load characteristic. We will consider two submodes where, in a closed-loop regulated system, DCM operation gets deeper and deeper as the output load is increased and frequency is moved away from resonance.

DCMAB at medium-light load

This "below-resonance" DCM submode is exactly equal to the above-resonance DCMAB submode previously considered. The waveforms are shown in *Figure 20* and it is possible to see that they match those shown in *Figure 19*.

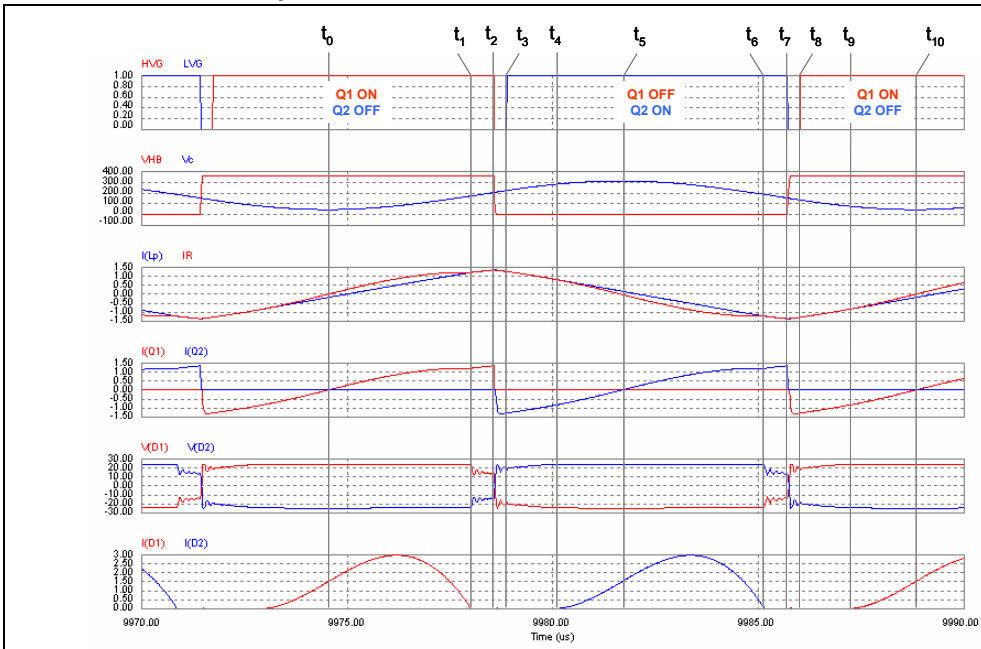
Note only that in this case the condition I_R = I(Lp) at t=t_1 occurs at a considerably higher power level than in the case of the above-resonance DCMAB submode (2:1 in the example shown).

DCMB at heavy load

This "below-resonance" DCM submode, which is unique to below resonance operation, actually comprises two submodes (DCMB2 & DCMB1) as frequency goes away from resonance. Their waveforms do not differ much, only those of DCMB2 will be shown. It is possible to identify eight fundamentals subintervals and the relevant waveforms are

illustrated in the timing diagram of *Figure 21*. Again, t_0 is the instant when, with Q1 conducting and Q2 open, the tank current I_R has a positive-going zero-crossing.

Figure 20. Operation below resonance ($f_{R2} < f < f_{R1}$, $R>R_{crit}$): main waveforms in DCMAB operation



a) $t_0 \rightarrow t_1$. Q1 is ON and Q2 is OFF. This is the "energy taking" phase, when current flows from the input source to the tank circuit, so that energy is positive. The operating point of Q1 is in the first quadrant (current is flowing from drain to source). D2 is nonconducting and its reverse voltage is approximately $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). D1 is conducting as well, so the voltage across Lp is a V_{out}. Lp, then, is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when I_R equals I(Lp) and, then, I(D1)=0 at $t=t_1$, I_R reaches its maximum value, after that it starts decaying.

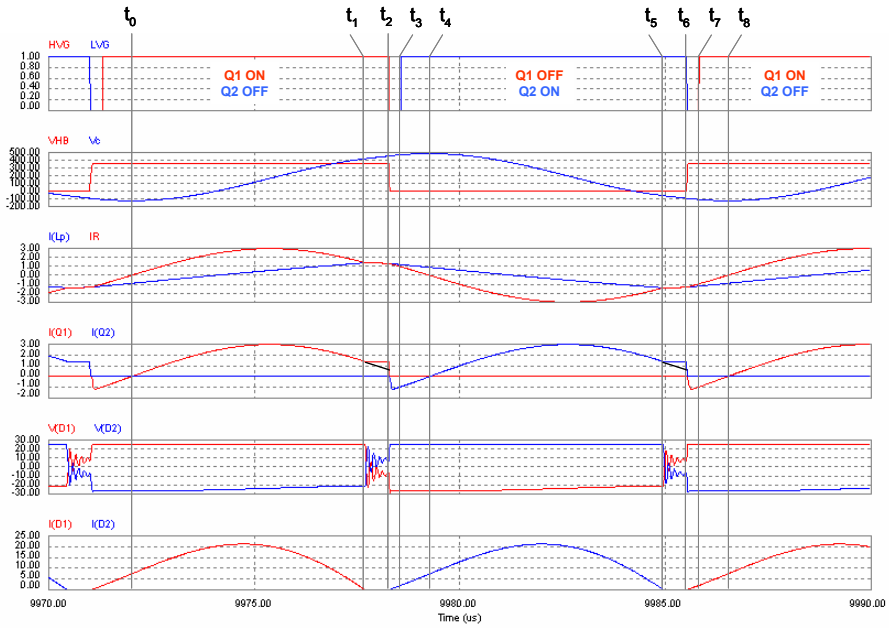
b) $t_1 \rightarrow t_2$. Q1 is ON and Q2 is OFF. At $t=t_1$ I(D1) becomes zero and I_R equals I(Lp), that is before the conduction time of Q2 ends. Both D1 and D2 are nonconducting and Lp, no longer shunted by the load reflected to the primary side, goes effectively in series to Ls and participates to resonance. I_R is a portion of a sinusoid having a frequency $f = f_{R2}$. Depending on the tank circuit's parameters and on the operating conditions, this portion can be similar to a straight line, as shown in the diagrams of *Figure 21*. This phase ends when Q1 is switched off at $t=t_2$.

c) $t_2 \rightarrow t_3$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_2$ $I(Q1)=I(Lp)=I_R$ is greater than zero and provides the energy to let the node HB swing from V_{in} to ground, so that the body diode of Q2, DQ2, is injected. This allows I_R to flow. The voltage across Lp reverses to $-a \cdot V_{out}$. D2 starts conducting while D1 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$

(plus the contribution from L_{L2}, not shown here). This phase ends when Q2 is switched on at $t=t_3$.

d) $t_3 \rightarrow t_4$. Q1 is OFF and Q2 is ON. At $t=t_3$ I_R is diverted from DQ2 to the $R_{DS(on)}$ of Q2, so that no significant energy is lost during the turn-on transient. Note that now the operating point of Q2 is in the third quadrant, current is flowing from the source to drain. D2 keeps on conducting and the voltage across Lp is $-a \cdot V_{out}$, so that Lp is not participating in resonance and Cr is resonating with Ls only. I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_4$.

Figure 21. Operation below resonance ($f_{R2} < f < f_{R1}$, $R>R_{crit}$): main waveforms in DCMB2 operation



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

e) $t_4 \rightarrow t_5$. Q1 is OFF and Q2 is ON. The tank circuit current, which is zero at $t=t_4$ becomes negative. D1 is nonconducting and its reverse voltage is approximately $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). Lp's current has a negative slope, so the voltage across Lp must be negative. Since the diode D2 is conducting this voltage will be equal to $-a \cdot V_{out}$. Lp, then, is not participating in resonance, Cr is resonating with Ls only and I_R is a portion of a sinusoid having a frequency $f = f_{R1}$. During this phase, which ends when I_R equals I(Lp) and, thereby, I(D2) is zero at $t=t_{15}$. I_R reaches its minimum value, after that it starts increasing.

f) $t_5 \rightarrow t_6$. This phase mirrors (t_1, t_2). At $t=t_5$ I(D2) becomes zero and I_R equals I(Lp), that is before the conduction time of Q1 ends. Both D1 and D2 are nonconducting and Lp, no longer shunted by the load reflected to the primary side, goes effectively in series to Ls and participates to resonance. I_R is now a portion of a sinusoid having a frequency $f = f_{R2}$. This phase ends when Q2 is switched off at $t=t_6$.

g) $t_6 \rightarrow t_7$. This is the deadtime during which both Q1 and Q2 are OFF. At $t=t_6$ $I_R = I(Lp)$ is (in absolute value) greater than zero and provides the energy to let the node HB swing from 0 to V_{in}, so that the body diode of Q1, DQ1, is injected. This allows I_R to flow back to the input source. The voltage across Lp reverses to a V_{out}, D1 starts conducting while D2 is reverse biased with a negative voltage approximately equal to $2 \cdot V_{out}$ (plus the contribution from L_{L2}, here not shown). This phase ends when Q1 is switched on at $t=t_7$.

h) $t_7 \rightarrow t_8$. Q1 is ON and Q2 is OFF. At $t=t_7$ I_R is diverted from DQ1 to the $R_{DS(on)}$ of Q1, so that no significant energy is lost during the turn-on transient. Note that now the operating point of Q1 is in the third quadrant, current is flowing from the source to drain. This phase, along with the preceding one is the "external energy recirculation phase": current is negative (coming out of the input terminal) despite that the impressed voltage is positive so that the input energy is negative, i.e. it is returned to the input source. D1 is still conducting and the voltage across Lp is a V_{out}, so that Lp is not participating in resonance anymore and Cr is resonating with Ls only. I_R is again a portion of a sinusoid having a frequency $f = f_{R1}$. This phase ends when $I_R=0$ at $t=t_8$ and another switching cycle begins.

Remarks

1. Also in this "below-resonance" DCM submode the multiresonant nature of the LLC converter shows up. From t_1 to t_2 and from t_5 to t_6 the secondary rectifiers are both open and the second resonance frequency f_{R2} appears. This is one of the fundamental advantages of the LLC resonant converter over the traditional LC series-resonant converter. In fact it helps keep operation away from capacitive mode. Although the tank circuit current I_R lags the impressed voltage (being $R>R_{crit}$ by assumption) so that they have the same sign at half-bridge leg transitions, the switching period is longer than the resonant period, $1/f_{R1}$. Then I_R, which is decaying (in absolute value), might come close to zero or even reverse if it still evolved according to the same sinusoid at frequency $f=f_{R1}$ (see the extrapolated black lines drawn in (t_1, t_2) and (t_5, t_6)). This lower frequency sinusoid "holds up" the tank current, hence ensuring that the switched currents $I_R(t_2)$ and $I_R(t_6)$ do not change sign and have amplitude large enough to complete the HB node swing well within the deadtimes (t_2, t_3) and (t_6, t_7) respectively, i.e. ZVS.
2. In the series LC tank Ls-Cr operating below resonance with $R>R_{crit}$ the voltage drop across the L-C series is negative (the capacitive reactance is larger in module than the inductive reactance), i.e. a minus sign is located at the node HB. As a result:

Equation 14

$$a \cdot V_{out} > \frac{V_{in}}{2}$$

Then, when operating below resonance, for a given input voltage, the LLC resonant half-bridge will provide an output voltage higher than that available at resonance, and vice versa, with a given output voltage the LLC resonant half-bridge will operate below a resonance if the input voltage is lower than $2 \cdot V_{out}$. In other words, the conversion ratio, intended as previously mentioned, is > 1, then the LLC is said to have a "step-up" characteristic when operating below resonance.

3. The secondary rectifiers D1 and D2 start conducting when Q2 and Q1 are switched off, respectively. The initial current is zero and its di/dt is low, thus they have a soft turn-on.

They cease to conduct before the transitions of the half-bridge. The operation is DCM, then ZCS occurs by definition.

4. Essentially, the reason why D2 does not conduct during (t_1, t_2) and D1 does not during (t_5, t_6) is that during these subintervals the condition expressed by *Equation 12* is met.
5. The waveforms in DCMB1 are very similar, only the portion of sinusoid at f = f_{R2} decays to zero more quickly. While DCMB2 is characterized by the duration of the intervals (t_1, t_2) and (t_5, t_6) that gets longer as frequency is reduced, in DCMB1 the duration of these intervals starts decreasing quite rapidly to reach zero at the boundary with capacitive mode operation. The "border belt" adjacent to the capacitive region is included in the region where DCMB1 occurs, thus it can be a good design practice to limit the operation of the converter to the DCMB1-DCMB2 boundary.

2.3.4 Capacitive-mode operation below resonance ($f_{R2} < f < f_{R1}$, $R<R_{crit}$)

In this operating mode, unique to below-resonance operation and corresponding to the CCMB operating mode defined in [3], it is possible to distinguish six fundamental time subintervals within a switching cycle, as illustrated in the timing diagrams of *Figure 22*.

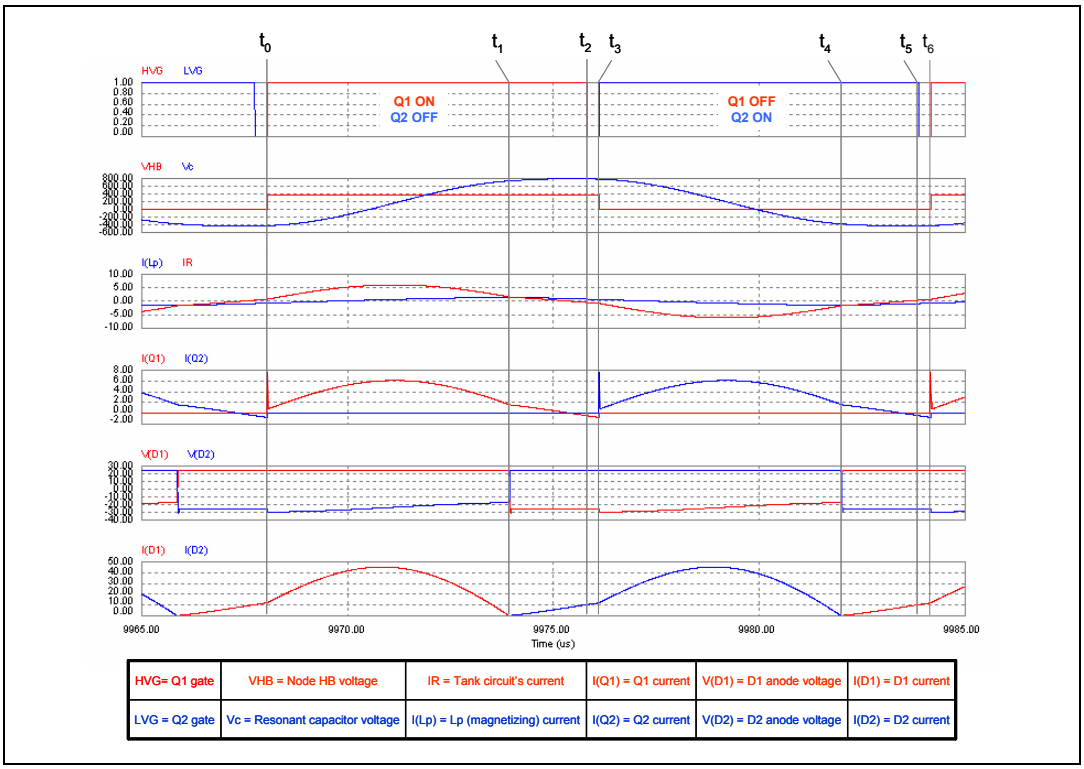
In this case it is convenient to define t_0 as the instant when Q1 is switched on.

a) $t_0 \rightarrow t_1$. The tank current $I_R(t_0)$ as Q1 is switched on is already positive: this means that in the just finished deadtime it was flowing through the body diode of Q2, DQ2. Actually, this is confirmed by the voltage V_{HB} of the half-bridge midpoint which was previously zero and is abruptly pulled up to V_{in} exactly at $t=t_0$ with a large dv/dt. The body diode DQ2 is then reverse-recovered and a large current spike flows through Q1 and DQ2 until the latter recovers completely. Functionally this is similar to a cross-conduction of the half-bridge leg. Very high di/dt may occur and, as a result, large voltage spikes are generated across the parasitic inductances experiencing this large di/dt. The voltage V_{HB} may have large positive overshoots. During this phase when energy is taken from the input source, the tank current reaches its maximum value and then decays. The phase ends when I_R=I(Lp) and, then, I(D1)=0 at $t=t_1$.

b) $t_1 \rightarrow t_2$. Unlike what happens in the below-resonance DCMB2 submode, where there was insufficient voltage across the resonant capacitor to forward-bias D2, here Vc is much larger and D2 starts conducting immediately at $t=t_1$. I_R starts decreasing, becoming lower than I(Lp) and eventually crosses zero before Q1 turns off, which marks the end of the this phase at $t=t_2$.

c) $t_2 \rightarrow t_3$. This is the deadtime during which both Q1 and Q2 are OFF. During this phase I_R is already negative and further decreasing. Since Q1 is off, it is flowing through DQ1. Note that the voltage of the half-bridge midpoint V_{HB} does not change. This phase ends when Q2 turns on at $t=t_3$.

Figure 22. Capacitive mode operation below resonance ($f_{R2} < f < f_{R1}$, $R<R_{crit}$): main waveforms



d) $t_3 \rightarrow t_4$. The tank current $I_R(t_3)$ as Q2 is switched on is already negative and flowing through the body diode of Q1, DQ1. The voltage of the half-bridge midpoint, V_{HB}, is abruptly pulled down to ground at $t=t_3$ with a large dv/dt. The body diode DQ1 is then reverse-recovered and a large current spike flows through Q2 and DQ1 until the latter recovers completely. Again there is a condition functionally equivalent to a cross-conduction of the half-bridge leg. Very high di/dt may occur and, as a result, large voltage spikes are generated across the parasitic inductances experiencing this large di/dt. The voltage V_{HB} may have large negative undershoots. During this phase energy is internally recirculated, the tank current reaches its minimum value and then increases. The phase ends when I_R=I(Lp) and, then, I(D2)=0 at $t=t_4$.

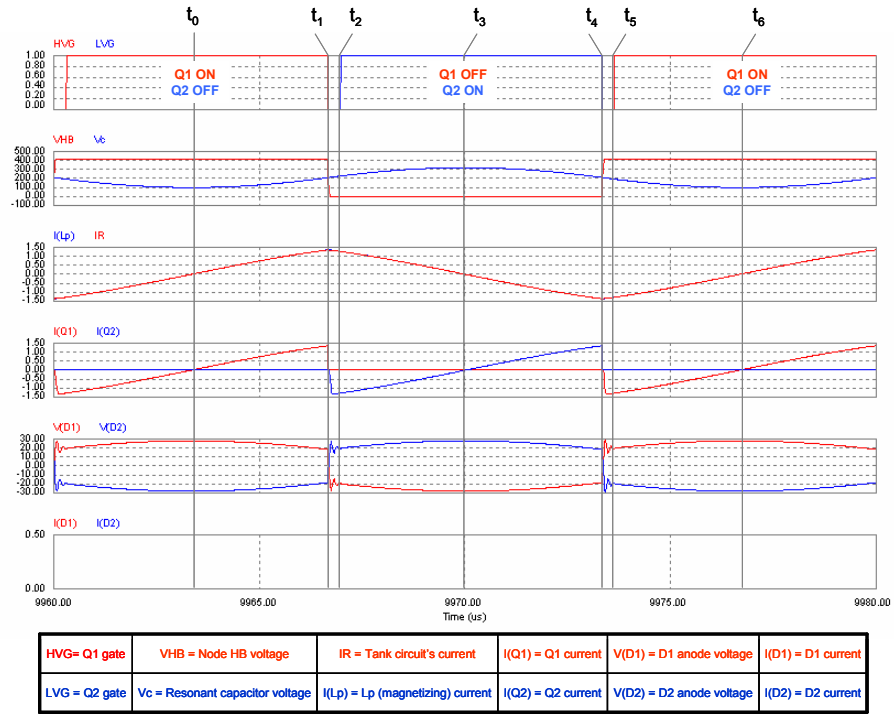
e) $t_4 \rightarrow t_5$. This phase mirrors exactly (t_1, t_2). The voltage across the resonant capacitor is so large that D1 is forward-biased and, thereby, starts conducting immediately at $t=t_4$. I_R starts increasing, becoming higher than I(Lp) and eventually crosses zero before Q2 turns off, which marks the end of this phase at $t=t_5$.

f) $t_5 \rightarrow t_6$. This is the deadtime during which both Q1 and Q2 are OFF. During this phase I_R is already positive and increasing. Since Q2 is off, it is flowing through DQ2. Note again that the voltage of the half-bridge midpoint V_{HB} does not change. This phase ends when Q2 turns on at $t=t_3$ and another switching cycle begins.

Remarks

1. In the below-resonance capacitive mode operation, since current is continuously flowing on the secondary side, this is a CCM mode (as already stated, it corresponds to the CCMB mode defined in [3].
2. The physical reason of this CCMB operation is, as previously pointed out, the large voltage developed across the resonant capacitor. A large energy level must be circulating in the tank circuit and this is consistent with $R<R_{crit}$ condition in order for the capacitive mode to take place. Capacitive operating mode is then likely to occur under heavy load, overload or short circuit conditions and appropriate countermeasures must be taken to handle this.
3. Note that in all the inductive modes the absolute value of the switched currents (i.e. the current I_R when either power MOSFET is switched off) is always greater than (in CCM mode above resonance) or equal to (in all DCM modes) the current I(Lp). In the capacitive mode, instead, the absolute value of the switched currents is lower than that in Lp. This consideration is useful when analyzing the transitions of the node HB.
4. Unlike the other modes, in capacitive mode the secondary rectifiers D1 and D2 start conducting during the conduction period of Q2 and Q1, respectively. The initial current is zero and its di/dt is low, thus they have a soft turn-on. Also in this case the voltage across the secondary rectifiers reverses as a result of their currents going to zero. Then, ZCS is maintained even under these conditions and it is possible to conclude that the secondary rectifiers are soft-switched at both turn-on and turn-off under all operating conditions and that this property is inherent in the topology. In fact no assumption has been made about the tank circuit's parameters.

Figure 23. No-load operation (cutoff): main waveforms



2.4 No-load operation

The ability to operate under no-load conditions is another peculiar characteristic of the LLC resonant half-bridge converter. The typical waveforms in this operating mode, called also "cutoff" mode, which can occur at frequencies both above, below and at the resonant frequency f_{R1}, as demonstrated in [3], are illustrated in the timing diagrams of *Figure 23*.

Note that it is I_R=I(Lp), then I(D1)=I(D2)=0, throughout the entire switching cycle. I_R is made by portions of sinusoid at f=f_{R2}, but looks very much like a triangular waveform. In order for this operation to occur, the voltage developed across Lp and reflected to the secondary side has to be lower than the output voltage throughout the entire switching cycle, so that either secondary rectifier cannot be forward-biased. In other words, *Equation 12* has to be met for $t \in (t_0, t_6)$. The ability of the converter to operate with no-load can be easily deducted by *Equation 12* itself. However big the peak value of $V_{in}(t)$-Vc(t) is and provided $a \cdot V_{out}$ is not zero, it is possible to find a value of Lp that meets condition (α). In the end, no-load operation is not an intrinsic property of the LLC resonant converter (like ZCS for the secondary rectifiers) but it can be achieved with an appropriate design of the tank circuit.

The difference with respect to the LC series resonant converter is apparent. If $Lp \rightarrow \infty$ the LLC converter turns into the LC one but $Vc \rightarrow 0$ because there is no current through the resonant tank and the only possible equilibrium condition is $V_{in} = a \cdot V_{out}$. If the input and output voltage have a different ratio, output voltage regulation will be impossible.

Seen from a different standpoint, under no load conditions and at a frequency considerably higher than f_{R1}, the resonant capacitor Cr "disappears" ($Vc(t) \approx V_{in}/2$) and the output voltage is given by the inductive divider made up by Ls and Lp as shown by the equivalent circuit of *Figure 24*. Then, if the voltage conversion ratio is greater than the inductive divider ratio, regulation will be possible at some finite frequency, otherwise it will not be. From *Equation 12*, substituting $V_{in(t)} = V_{in}$ and, then, $Vc(t) = V_{in}/2$, it is possible to find a necessary condition in order for the converter to be able to regulate at zero load:

Equation 15

$$\frac{Lp}{Ls + Lp} \leq 2\frac{a \cdot V_{out}}{V_{in}}$$

Lp, then, plays a key role. It not only makes zero load operation possible but allows soft-switching under these conditions too, as already discussed. The price to pay for that is the considerable tank current I_R=I(Lp) circulating in the circuit and illustrated in *Figure 23*. This circulation is not lossless. Power is dissipated in power MOSFET, the resonant capacitor and the transformer.

This prevents the LLC resonant converter from achieving extremely low input power levels at no load, unless appropriate countermeasures are taken. The most effective way to reduce no-load consumption to a very low level is to let the converter operate intermittently ("burst-mode" or "pulse-skipping" operation). In this way, the average value of the tank current can be reduced at an almost negligible value. Furthermore, the average switching frequency will be considerably lowered thus minimizing the residual turn-off switching losses.

2.5 Overload and short circuit operation

The equivalent schematic of the converter under short circuit conditions is illustrated in *Figure 25*. The inductance Lp is actually shunted by an extremely low impedance, so that the LLC circuit reduces to a series LC circuit. The transformer will work as a "current transformer", so that the output current will be a times the primary (input) current Iin. It is

intuitive that the impedance of the Ls-Cr resonant tank plays a key role. Note that this impedance becomes zero at f = f_{R1}. Two cases will be considered:

1. The converter always works above resonance (some means is provided to bottom-limit the operating frequency at a value $f_m > f_{R1}$). The control loop, in the attempt to keep the output voltage regulated, will reduce the switching frequency to the minimum value f_m. In this case the converter still operates in the inductive region (CCM submode) and ZVS is ensured. However, the impedance of the Ls-Cr tank circuit can be very low and then the current Iin can reach very high values, the closer the minimum frequency to f_{R1} is, the lower the impedance and the higher the current will be.
2. The converter can operate below resonance (some means is provided to bottom-limit the operating frequency at a value f_m such that $f_{R2} < f_m < f_{R1}$). Again, the control loop, in the attempt to keep the output voltage regulated, will reduce the switching frequency to the minimum value f_m. In this case, the input current will be limited by the impedance of the Ls-Cr tank circuit at a value that is as lower as f_m is lower. However the capacitive region is entered and ZVS is lost, with all the consequent troubles previously mentioned. The waveforms will be similar to those in *Figure 22*.

Figure 24. Circuit's equivalent schematic under: no-load conditions

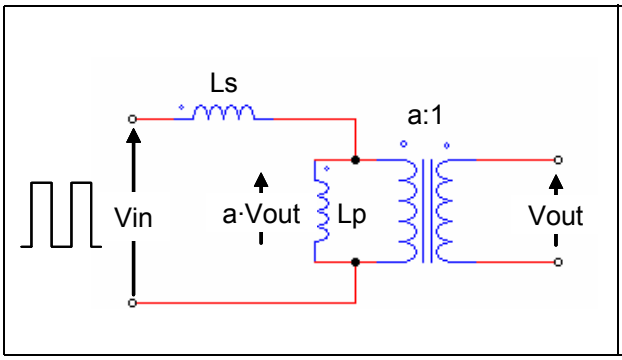
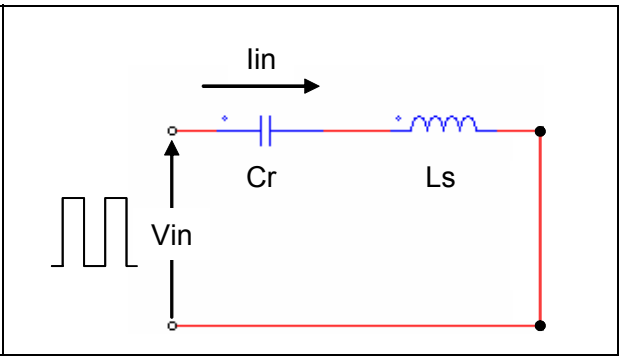


Figure 25. Circuit's equivalent schematic under: short-circuit conditions



It is interesting to see what happens under short circuit if the converter is operating at resonance (f = f_{R1}). Tank circuit's impedance is zero, then the short circuit is directly connected across the input source and the current Iin is theoretically unlimited. Theoretically, switching frequency should not change (the system is working in the load-independent point). In real-world operation, Iin, though reaching very high values, will be limited by the parasitic resistance of the short-circuit mesh, the ESR of Cr and by transformer's nonidealities. Additionally, the drop across the secondary rectifiers does not reflect a true short circuit on the primary side. Because of the parasitic resistances, the output voltage will drop and the control loop will react pushing the operating frequency to the minimum f_m, which, realistically, must be lower than f_{R1} if operation at resonance is allowed. In the end this will fall into case 2.

Still with reference to case 2, it is worth remembering that the capacitive region is entered and ZVS for MOSFETs is lost as $R_{crit} = \sqrt{Zo_0 \cdot Zo_\infty}$, well before short circuit.

From the above analysis it is possible to draw the following conclusions:

1. Two major issues arise under overload or short circuit conditions: very high current levels, and capacitive mode operation (with loss of ZVS, etc.). This makes the operation of the LLC resonant converter under overload or short circuit inherently unsafe if no overcurrent protection (OCP) is used, just like in conventional PWM-controlled converters. OCP will have to prevent not only the tank current from exceeding unsafe

values but also ZVS from being lost. In principle, its setpoint must be such that the condition $R>R_{crit}$ is always fulfilled.

2. Limiting the minimum operating frequency of the converter is not always effective. It prevents losing ZVS under overload or short circuit only if this minimum value is above the resonant frequency f_{R1}. Thereby, relying on just limiting the minimum operating frequency would force giving up the below-resonance operating region and its interesting properties, severely limiting the usability range of the converter. Furthermore, the problem of having too high circulating current would be still unsolved.
3. Converters are often specified to have peak load demands that are considerably higher than the maximum continuous power, and whose duration is such that it cannot be averaged by the output capacitor bank. While these peak loads may be thermally irrelevant, from the electrical standpoint they must be considered as steady-state. OCP circuits must not be triggered and the converter must be designed so that the condition $R>R_{crit}$ is not violated under these transient conditions as well.

The inspection of the waveforms under heavy load conditions shows that, unlike PWM-controlled converters, the peak current in a switching cycle is not reached at the end of the conduction time of either MOSFET. This suggests that the usual cycle-by-cycle current limitation so widely used in PWM-controlled converters is not applicable to LLC resonant converters.

The simplest and also most immediate action to take in response to the detection of an overload or short circuit condition is to increase the operating frequency. It is advantageous to push the frequency well above the resonance frequency f_{R1}, so that the converter definitely operates in the inductive region, and ZVS is maintained, with the input current kept under control by the inductive reactance of the tank circuit.

However, this frequency rise is not typically sufficient to effectively limit the short-circuit output current at safe values. In fact, on one hand, the input impedance of the tank circuit in the inductive region is essentially proportional to frequency. Since there are practical limits on the maximum operating frequency (it rarely exceeds 3-4 times f_{R1}), the short circuit tank current can still be considerably large. On the other hand, as the output voltage drops because of the action of the OCP circuits, the voltage reflected across Lp becomes smaller and smaller. Then, less and less current flows through Lp and the transformer tends to transfer all the primary current to the output.

As a consequence, the short circuit output current can be still much higher than the nominal full-load current and the resulting stress, especially for the secondary rectifiers, might be unacceptable. In addition to current limiting it is therefore advisable to provide some timed shutdown protection that either forces an intermittent operation of the converter to drastically reduce the average value of the output current or latches it off if the OCP circuits are active for more than some time.

2.6 Converter's startup

Like in PWM-controlled converters, startup is quite a critical moment that needs to be properly handled in LLC resonant converter as well. When the converter is first switched on (or also while it is recovering after a protection shutdown) the energy flow should be progressively increased to allow a slow buildup in output current and voltage. This is commonly known as "soft-start". Doing otherwise, high and potentially destructive currents might be drawn from the input source and through the power devices in an attempt to charge the output capacitors and bring the output voltage to the regulated value.

Since at startup the output capacitors are discharged, the startup phase can be regarded as a "temporary short circuit" (where, however, the output voltage is allowed to increase) and actually it has to be handled like a short circuit as mentioned in the previous section. To minimize energy flow, the initial switching frequency will have to be much higher than the resonance frequency f_{R1}, so that the converter operates in the inductive region, ZVS is maintained and the input current is kept under control by the inductive reactance of the tank circuit. The frequency will be allowed to progressively decay until the output voltage comes close to the regulated value and the control loop closes and takes over.

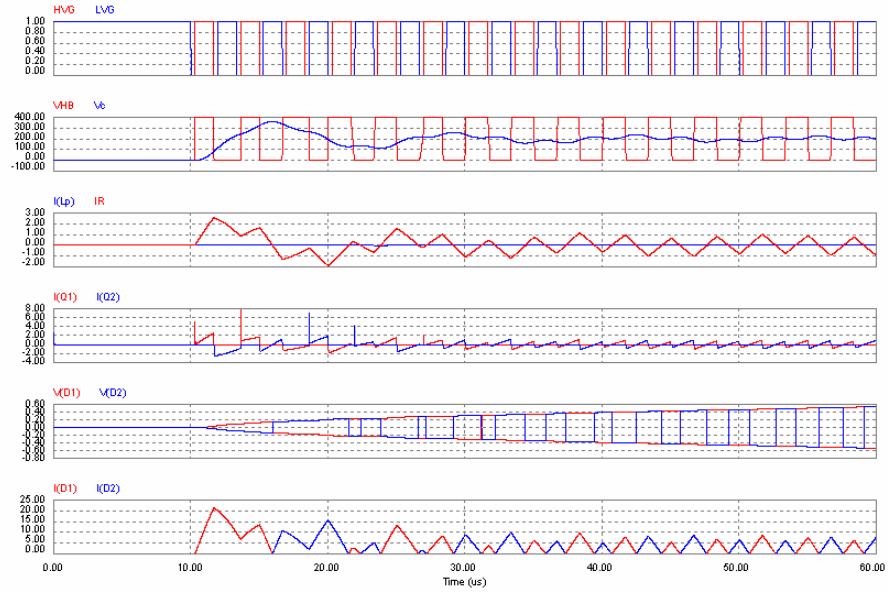
Some typical waveforms at startup for the converter of *Figure 15* are shown in *Figure 26*, where the initial frequency is set at 300 kHz (against $f_{R1} \approx$ 76 kHz).

In the LLC resonant converter there is an additional phenomenon that shows up just at the very beginning and causes higher resonant tank current to flow and ZVS loss.

As mentioned in the *Section 2*, the resonant capacitor Cr plays the double role of resonant capacitor and DC blocking capacitor. This essentially means that the resonant voltage on Cr is superimposed on a DC value that equals $V_{in}/2$ because the half-bridge is driven with 50% duty cycle. As a result, the primary of the transformer is symmetrically driven by a $\pm V_{in}/2$ square wave. This is true when steady-state operation has been reached.

At startup the initial voltage across Cr is zero and for the first few cycles the voltage seen by the transformer when the high-side power MOSFET Q1 is on is considerably different from the voltage seen when Q2 is on. The transformer driving voltage will tend to become symmetrical as switching cycles follow one another and Cr is charged at the steady state DC level. During the Cr charge transient the v·s unbalance can be quite high and this makes the tank current irregular in the first few cycles, with peak values that can be considerably higher than the steady-state peak-to-peak current expected at the starting frequency. Additionally, the fundamental ZVS conditions ("when one switch turns off, the tank current must have the same sign as the impressed voltage") may be violated so that even capacitive mode operation can be observed.

Figure 26. Converter's startup: main waveforms



HVG= Q1 gate	VHB = Node HB voltage	IR = Tank circuit's current	I(Q1) = Q1 current	V(D1) = D1 anode voltage	I(D1) = D1 current
LVG = Q2 gate	Vc = Resonant capacitor voltage	I(Lp) = Lp (magnetizing) current	I(Q2) = Q2 current	V(D2) = D2 anode voltage	I(D2) = D2 current

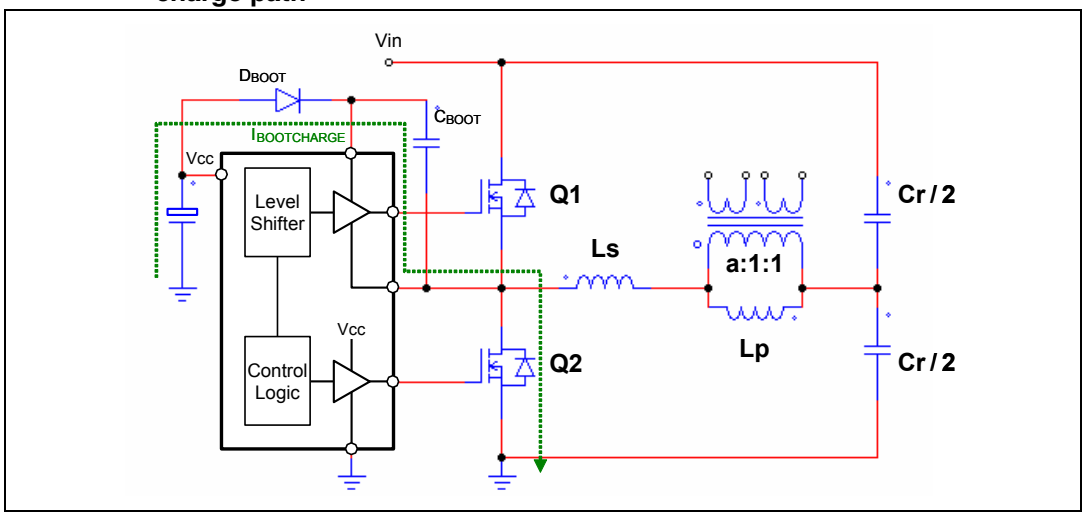
This phenomenon is well-known in push-pull and half-bridge topologies and is sometimes referred to as "flux doubling" because the transformer's magnetic flux excursion, which normally swings by $2B_{pk}$ from $-B_{pk}$ to $+B_{pk}$ under steady state operation, in the first cycle goes from 0 to $2B_{pk}$. Fortunately, if the integrated magnetics approach is used, there will be no risk of saturation. Flux doubling will concern only the resonant inductor Ls, which is mostly associated to the transformer's leakage inductance that, by definition, cannot saturate because the relevant flux is developed in air.

Although not inherently hazardous, (capacitive mode and ZVS loss will typically occur in the first two-three cycles, then the associated stress level is practically negligible) this phenomenon is not nice to see. To eliminate or, at least, minimize it, the split capacitor configuration of *Figure 4* can be used in some cases. In fact, the initial voltage across each capacitor will be close to $V_{in}/2$ (equal to $V_{in}/2$ if the two capacitors had exactly the same value), then there will be only a minimum transient.

However, this is ineffective with many control ICs with high-side MOSFET driving capability using capacitive bootstrap. To guarantee an adequate precharge of the bootstrap capacitor to correctly drive the high-side MOSFET Q1 since the first cycle, the low-side MOSFET Q2 is turned on for some time before starting to operate (as shown in *Figure 26*), which discharges completely the lower Cr/2 capacitor. This bootstrap precharge mechanism, shown in *Figure 27*, makes ineffective also any pull-up that could precharge Cr.

In this case the initial current peak cannot be completely eliminated, just reduced by either using a higher starting frequency or by forcing the duty cycle to start from a value considerably smaller than 50% and letting it widen progressively.

Figure 27. High-side driving with bootstrap approach and bootstrap capacitor charge path



2.7 Analysis of power losses

Conduction power losses on the primary side are located in the power MOSFETs, in the resonant capacitor Cr and the transformer (for convenience the secondary winding losses can be incorporated). On the secondary side, losses will be essentially located in the secondary rectifiers, although those in the output capacitors cannot be neglected, at least as far as capacitor selection is concerned.

Unless the converter is running at very high frequency, which would make turn-off losses dominant, $R_{DS(on)}$ is usually the major source of power loss in power MOSFET. In the total loss budget, however, the power wasted in power MOSFETs is usually a minor contributor, especially when the converter is powered from the output of a PFC preregulator (400 V typ.). It is not uncommon to see power MOSFETs running cool with minimum heat sinking.

The resonant capacitor Cr dissipates because of its own ESR. For this reason, especially when very high efficiency is required, Cr should be a low-loss one, suited for AC/pulse applications. Polypropylene film capacitors are the preferred choice.

Concerning the transformer, high frequency copper losses need to be particularly addressed. In fact, eddy currents and proximity losses are considerable, especially in the side-by-side winding arrangement because of the high transverse flux. Litz-type or multistrand wire is a must for both primary and secondary windings.

Switching losses are essentially located in the power MOSFET Q1 and Q2. As previously stated, the value of the switched current at heavy load (I_{Rmin}) is a trade-off between the need for ensuring ZVS for both Q1 and Q2 and their turn-off losses. The higher the switched current is, the higher the margin for ZVS will be, but at the expense of larger switching loss due to voltage-current overlap. It is intuitive that the optimum design, in terms of total dynamic losses minimization, is the one that uses for I_{Rmin} the minimum value necessary to achieve ZVS. It still provides zero capacitive turn-on losses with minimum switching losses at turnoff. Since component tolerance must be accounted for, and losing ZVS must be avoided not only for efficiency reasons but also to prevent troubles, adequate margin needs to be considered and the typical operation will be suboptimal.

Secondary rectifiers are usually the components where the majority of power losses occur. Assuming the rectifiers are identical, their cumulative conduction losses are given by:

Equation 16

$$Pd = \begin{cases} V_{th} I_{out-dc} + R_d I_{out-rms}^2 & \text{full - wave rectification} \\ 2(V_{th} I_{out-dc} + R_d I_{out-rms}^2 & \text{bridge rectification} \end{cases}$$

where V_{th} is the rectifier's threshold voltage and R_d its dynamic resistance. With bridge rectification, losses are almost double because there are always two diodes in the conduction path (we say "almost" because of the lower blocking voltage rating, so that V_{th} and R_d are expected to be slightly lower for the same current rating). Hence this arrangement is preferred when the output voltage is high. Firstly, the efficiency loss due to the rectifiers (which is $\propto 2\ V_F/V_{out}$) becomes less significant. Secondly, the higher the output voltage is, the more a lower blocking voltage requirement becomes beneficial.

As compared to the ZVS Asymmetrical Half-bridge and the Forward converter, conduction losses (for the same technology and blocking voltage) would be slightly greater because of the worse current form factor that would increase the term, but this is compensated by the absence of recovery and its associated losses. In the end, considering also that in the LLC resonant half-bridge there is no secondary choke with its associated losses, it is expected that the total secondary losses will be lower.

2.8 Small-signal behavior

It is essential to know the small-signal behavior of the LLC resonant converter to be able to design the feedback loop. In line with the approach followed to describe its steady-state

operation, here only a qualitative description will be given, which is the result of a characterization by simulation [7] (refer to *Section 4*).

As stated many times, the operating frequency is the parameter that allows regulation of the input-to-output energy flow. The control-to-output transfer function G(jω) that characterizes the small-signal behavior of the LLC resonant converter will then be defined as:

Equation 17

$$\frac{\hat{V}_o}{\hat{f}} = G(j\omega)$$

In the overall converter's dynamics it is convenient to separate the contribution of the "inverter" part and that of the rectifying and filtering block that transforms the inverter in a converter. This is quite a useful concept of superposition because it gives considerable physical insight. Regardless of the operating mode of the inverter and, then, of its contribution to converter's dynamics, the rectifying and filtering block always introduces a low frequency pole associated to the output capacitor, the load resistance and the open-loop output impedance Zo_0 of the resonant tank, plus a zero due to the output capacitor and its ESR (equivalent series resistor). This pole moves with the load (frequency is higher at heavy load, lower at light load) because of the changes in Zo_0, while the zero is at an essentially fixed frequency, exactly like in PWM converters.

Different types of dynamic behavior, corresponding to different pole distributions of G(jω), can be observed depending on the operating mode. Again we will consider operation at, above and below resonance.

2.8.1 Operation above resonance ($f > f_{R1}$)

In this operating mode the converter features a special characteristic typical of resonant converters, the so-called "beat frequency double pole", i.e. two complex and conjugate poles having their imaginary part at the difference between the switching frequency f and the resonant frequency f_{R1}. In addition to this double pole, contributed by the inverter part, there is the pole-zero pair associated to the output filter. If f is significantly higher than f_{R1}, the system can be regarded as a single-pole system.

As switching frequency moves close to resonant frequency, the beat frequency double pole will move to lower frequency. When the switching frequency is very close to resonant frequency, the beat frequency double pole will eventually split and become two real poles. One moves to higher frequencies and the other moves to lower frequencies as switching frequency gets closer and closer to resonant frequency. Finally, the split pole moving to low frequency will merge with the low frequency pole caused by the output filter and form a double pole. This type of characteristic is very similar to that of the conventional series LC converter.

Provided the converter is not operating too close to resonance, as long as it runs in CCM, the pole distribution tends not to change significantly. In DCM operation, instead, the beat frequency double pole will more pronouncedly move to higher frequencies and the low frequency pole to lower frequencies. At light load, the converter can then be regarded as a single-pole system.

Concerning how the resonant tank characteristics affect the small-signal behavior, the parallel inductor Lp has no practical effect. Conversely, increasing the impedance of the resonant tank (i.e. increasing Ls and reducing Cr while keeping the same f_{R1}), the DC gain will increase. Also the low frequency pole changes with the resonant tank impedance (it

gets higher at low impedance). In fact, the low frequency pole is not determined by the load resistor alone but by the output impedance of the tank circuit as well.

2.8.2 Operation below resonance ($f_{R2} < f < f_{R1}$, $R>R_{crit}$)

In this operating mode the converter's dynamics changes considerably. In the left half-plane, there are three poles and one zero but no beat frequency double pole. The pole distribution is quite insensitive to switching frequency as compared to that in the above resonance operation. The pole that in the above resonance operation was moving to higher frequency when switching frequency was approaching resonance here moves back to lower frequencies as switching frequency is further reduced going away from resonance. Its position, however does not change much. The low-frequency double pole is minimally affected too.

A Right Half Plane Zero (RHPZ) can be observed that moves with switching frequency but, fortunately, it stays typically away from the low frequency region of interest in the design of the feedback loop.

Approaching capacitive region, beat frequency dynamics tends to appear again. The phase has an abrupt 180º shift just beyond the capacitive region threshold (feedback from negative turns into positive).

Starting from heavy load conditions, at first the Q associated to the low frequency double pole decreases. The RHPZ shifts to higher frequencies and leaves the stage. Further reducing the load, the Q of the low frequency double pole increases. At very light load the low frequency double pole splits, one moves to higher frequencies and the other to lower frequencies. Again, at very light load the converter can be regarded as a single-pole system.

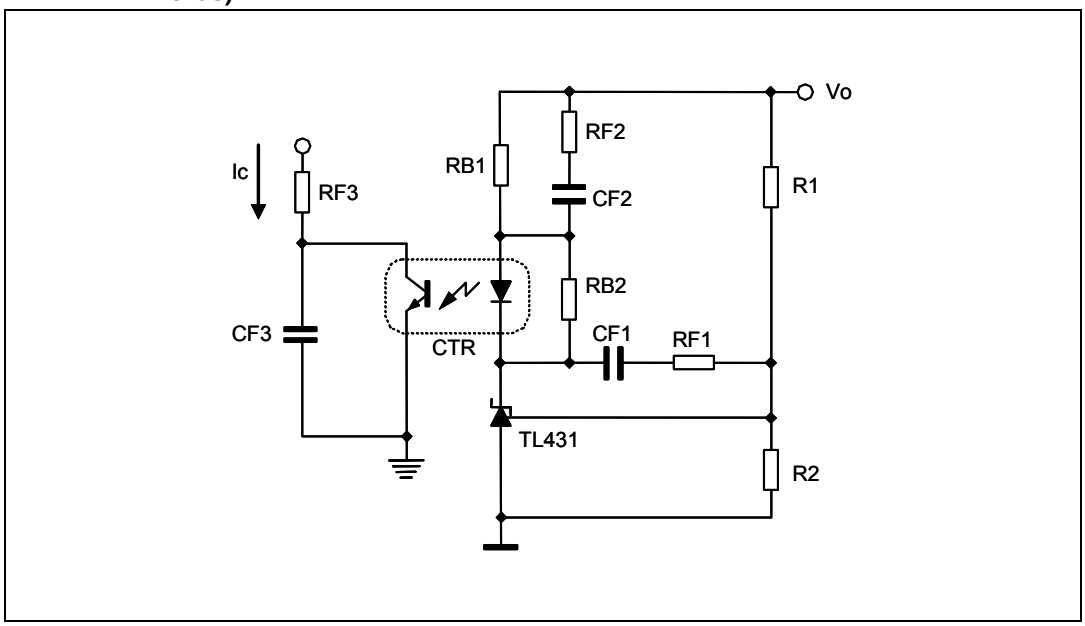
Unlike in the above resonance operation, in this case the parallel inductor Lp has a considerable impact on the DC gain of the converter. Additionally, it affects the RHPZ as well. Larger values for Lp tends to shift it to lower frequencies. As far as the impedance of the resonant tank is concerned, the effect is the same as in the above resonance operation.

2.8.3 Operation at resonance ($f = f_{R1}$)

Operation at resonance can be regarded as the borderline between the two previously considered operating modes. The behavior will not be different from that seen just above (and just below) resonance: two low-frequency poles, one high-frequency pole and the ESR zero. The same behavior can be seen as far as load dependence is concerned.

The compensation of the error amplifier must consider the different types of small-signal behavior that the converter can exhibit, especially if it is designed to operate both above and below resonance. The challenge comes essentially from its second-order behavior exhibited in its operation close to resonance frequency due to the low frequency double pole. To properly compensate that, the best option is a type 3 amplifier, i.e. a compensator with one pole at the origin plus two poles and two zeros at finite frequencies. The pole at the origin gives excellent load and line regulation characteristics. The two zeros are placed at low frequency to compensate the double pole of the control-to-output transfer function, by counteracting their phase lag. The poles are placed to compensate the ESR zero and provide more attenuation at switching frequency. A practical implementation of this compensator is shown in *Figure 28* along with the relationship between the component values and its transfer function.

Figure 28. Frequency compensation with an isolated type 3 amplifier (3 poles + 2 zeros)



Equation 18

$$\frac{\hat{I}_C}{\hat{V}_o} = \frac{CTR}{s(R1 \cdot RB1 \cdot CF1)} \cdot \frac{1 + s(RB1 + RF2)CF2}{1 + sRF2 \cdot CF2} \cdot \frac{1 + s(R1 + RF1)CF1}{1 + sRF3 \cdot CF3}$$

3 Conclusion

The operation of the LLC resonant converter has been examined in detail and its most important properties have been deduced by inspection of its salient waveforms under different operating conditions. To summarize, the most significant merits of this topology are:

- Soft-switching of all semiconductor devices: ZVS (zero-voltage switching) at turn-on for the MOSFETs and ZCS (zero-current switching) at both turn-on and turn-off for the secondary rectifiers. The first property results from a correct design of the resonant tank. The second one is a natural feature of the topology.
- Ability to accommodate an extremely broad load range, including zero load, with an acceptable frequency variation. Also this property results from a correct design of the resonant tank.
- Magnetic integration, which allows the combination of different magnetic devices into a single physical device.
- Smooth waveforms: the current is piecewise sinusoidal with no steep edges. The voltage, although a square wave, does not have very high dv/dt edges. EMI emissions are considerably low and filtering requirements are relatively loose.
- As a result of all the above merits, high-efficiency, high switching frequency capability, high power density are typical characteristics of the converters based on this topology.

The most significant facts concerning the design of an LLC resonant converter are:

- The quantities that determine whether the converter operates at resonance, above resonance or below resonance are essentially the input and the output voltages and the transformer's turn ratio. There is just a second-order dependence on the load current due to the variation of the voltage drop across parasitic elements such as winding resistance, rectifier drop, etc.
- Operation at resonance looks like the preferred operating point, where load regulation is ideally zero, where tank current is maximally sinusoidal and where CCM operation minimizes peak tank current for a given power throughput. Whenever possible (e.g. when the LLC converter is powered by a PFC preregulator) it seems a good design strategy to design the converter to work at resonance under nominal conditions, and use below resonance operation to handle mains voltage dips and above resonance operation to handle light load or transient overshoots of the input voltage.
- The ability to operate under no-load conditions and to ensure ZVS operation depend essentially on the transformer's magnetizing inductance. Its value has to be traded off against the switching losses at full load operation and the input consumption at no-load.
- Avoiding capacitive mode operation is a must. It is a too risky operating mode and any design procedure should not leave this fundamental aspect out of consideration.
- Overcurrent and short circuit protection must be provided. They will not only have to prevent excessive currents from flowing in both the resonant tank, the transformer and the output rectifiers but also avoid entering capacitive mode operation.
- Soft-start is highly recommended. At startup there is a situation very similar to a short circuit and, if not properly controlled, potentially destructive currents might flow in the half-bridge leg and the resonant tank.

4 References

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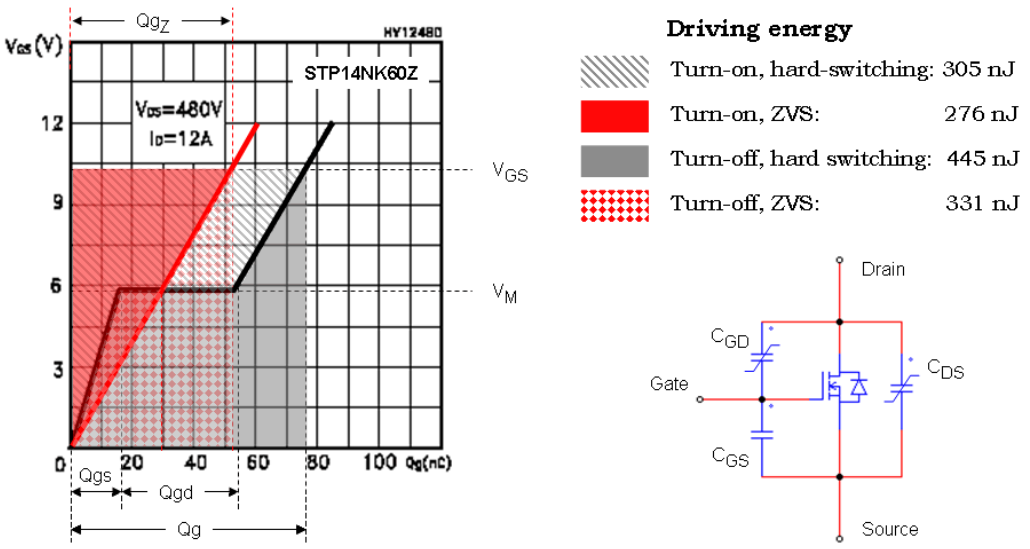
Appendix A Power MOSFET driving energy in ZVS operation

When power MOSFETs are switched on under ZVS conditions, i.e. when their drain-to-source is already zero, Miller effect due to drain-to-source voltage modulation is absent. This reduces the gate charge required to turn the power MOSFET fully on, the turn-on energy, as well as the total driving energy. This can be conveniently examined on the gate-charge characteristic of the device (see *Figure 29*).

Figure 29. Comparison of gate-charge characteristics with and without ZVS



The black curve is the normal piecewise-linear gate-charge curve. The first portion is that related to the charge of the input capacitance C_{GS}+C_{GD}, and Qgs is the charge needed to bring the gate voltage up to the plateau value V_M that lets the power MOSFET carry the specified current. The flat portion is the so-called "Miller plateau", where the gate voltage does not increase because the drain-to-source voltage is falling and C_{GD} is wiping out the charge supplied to the gate until the charge Qgd has been supplied. The third rising portion is related to the overcharge of C_{GS}+C_{GD} needed to minimize $R_{DS(on)}$. Note that the slope of this line is lower than that of the first portion. This is due to the modulation of C_{GD}, which is now considerably larger (C_{GS} is essentially constant). The total gate charge supplied to the gate to bring its voltage up to the final value V_{GS} is Qg. The values of Qgs, Qgd, Qg are specified on the datasheet for given V_{GS}, V_{DS}, I_D.

The grey-hatched area included between the gate-charge curve and the V_{GS} horizontal line is the energy lost in the gate driver to charge the gate up to the final value V_{GS} and turn the power MOSFET fully on. Its value can be found with simple geometric considerations:

Equation 19

$$E_{ONHS} = \frac{1}{2}[QgsV_M + (Qg + Qgs + Qgd)(V_{GS} - V_M)]$$

The grey-shaded area below the gate charge curve represents the energy lost in the gate driver to discharge the gate from V_{GS} to zero. Its value can be simply found from the difference of the total driving energy, represented by the rectangle enclosed by the Q-V axes and the Qg and V_{GS} lines:

Equation 20

$$E_{HS} = Qg \cdot V_{GS}$$

and E_{ON_HS}:

Equation 21

$$E_{OFF\_HS} = Qg \cdot V_{GS} - E_{ON\_HS}$$

In case of ZVS, instead, the associated gate-charge curve is the red line. Its slope is equal to that of the third portion of the normal gate-charge characteristic, because C_{GD} has the final value since the beginning. By geometrical considerations, the total gate charge Qg_Z to provide in this case will be:

Equation 22

$$Qg_Z = \frac{V_{GS}}{V_{GS} - V_M}[Qg - (Qgs + Qgd)]$$

while the energy lost in the gate driver to charge the gate up to the final value V_{GS} and turn the power MOSFET fully on and represented by the red-shaded area will be:

Equation 23

$$E_{ON\_ZVS} = \frac{1}{2} Qg_Z V_{GS} = \frac{1}{2} \cdot \frac{V^2_{GS}}{V_{GS} - V_M}[Qg - (Qgs + Qgd)]$$

At turn-off, the Miller effect will be present but to a lower degree. In fact, the operating point will initially move along the red line until the gate voltage reaches the Miller plateau V_M (that associated to the switched current at turn-off). From that point on, it will move along the black curve. The energy associated to turn-off will be:

Equation 24

$$E_{OFF\_ZVS} = \frac{1}{2(V_{GS} - V_M)}[(V^2_{GS} + V^2_M)(Qg - Qgd) - V_{GS}(V_{GS} + V_M)Qgs]$$

and the total driving energy:

Equation 25

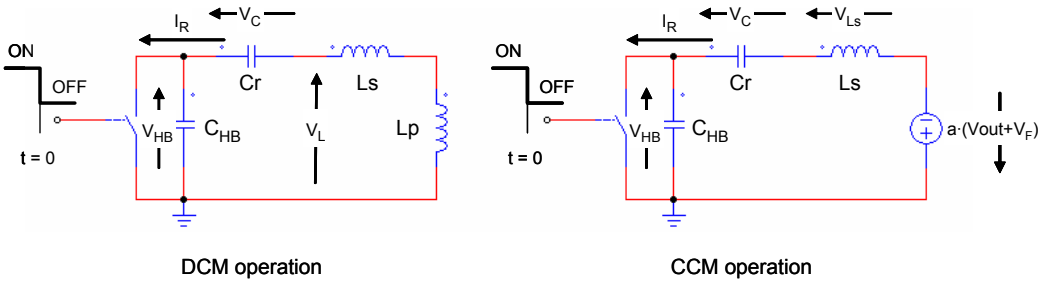
$$E_{ZVS} = \frac{1}{2(V_{GS} - V_M)}[(2V^2_{GS} + V^2_M)(Qg - Qgd) - V_{GS}(2V_{GS} + V_M)Qgs]$$

For the power MOSFET used in the example of *Figure 29* (STP14NK60Z), the datasheet specifies: Qgs = 13.2 nC, Qgd = 38.6 nC, Qg = 75 nC @ V_{GS} = 10 V. Substituting these values and V_M = 5.8 V_{in} (*Equation 19*) to (*Equation 25*) we find: E_{ON_HS} = 305 nJ, E_{HS} = 750 nJ, E_{OFF_HS} = 445 nJ, Qg_Z = 55 nC, E_{ON_ZVS} = 276 nJ, E_{OFF_ZVS} = 331 nJ and E_{ZVS} = 607 nJ. Then, the total gate charge is decreased by 20 nC (-27%) and the total gate driving energy by 143 nJ (-19%).

Appendix B Resonant transitions of half-bridge midpoint

To analyze the transitions of the half-bridge midpoint node HB when either Q1 or Q2 is turned off, it is necessary to schematize the equivalent circuit during the transient. For simplicity only the turn-off of Q2 will be considered, being obvious that the turn-off of Q1 will be exactly mirror-symmetrical. Different circuits need to be considered, depending on whether the converter is operated in a DCM mode or a CCM mode. These equivalent circuits are shown in *Figure 30*.

Figure 30. Equivalent circuit to analyze the transitions of the half-bridge midpoint node when Q2 turns off



In fact, in the case of DCM operation, since the secondary windings are open, Lp is part of the circuit and is effectively in series to Ls to form a single inductor Ls+Lp. In CCM operation, instead, since the secondary windings are conducting there is a constant voltage equal to $\pm a \cdot (V_{out}+V_F)$ across Lp and then this can be replaced by a voltage generator (placed as shown in *Figure 30* in the case under consideration). In either circuit, Q2 is replaced by an ideal switch that opens at t=0.

Resonant tanks are again involved during the transitions, hence the denomination "resonant transitions" given to the swings of the node HB. Considering the operation of the LLC resonant converter in its entirety, then, there are four associated resonant frequencies.

C_{HB} is the total parasitic capacitance of the node HB already discussed in *Section 2.2: The switching mechanism* and illustrated in *Figure 8* and that will be the topic of the next section. Note that during the transient Cr and C_{HB} are effectively in series. However, since normally $Cr >> C_{HB}$ (typically, two orders of magnitude), the combined capacitance will be $\approx C_{HB}$ and the changes of the V_C voltage during the transient can be neglected, so that it is possible to assume $V_C = V_C(0)$ during the transient and replace Cr with a constant voltage generator $V_C(0)$.

The value of $V_C(0)$ can be determined on the basis of the following considerations. The value of at the end of the conduction cycle of Q1, $V_C(Ts/2)$, is given by:

Equation 26

$$V_C\left(\frac{Ts}{2}\right) = V_C(0) + \frac{1}{Cr}\int_0^{\frac{Ts}{2}} I_R(t)dt$$

Note that the integral in *Equation 26* is the total charge provided to Cr during the conduction time of Q1, when the converter draws current from the input source. This charge can be expressed also as the product of the DC input current Iin times the switching period, then:

Equation 27

$$V_C\left(\frac{Ts}{2}\right) = V_C(0) + \frac{Iin}{Cr}Ts$$

On the other hand, remembering that V_C has a DC value equal to $V_{in}/2$, for symmetry the following identity holds true:

Equation 28

$$V_C\left(\frac{Ts}{2}\right) - \frac{V_{in}}{2} = \frac{V_{in}}{2} - V_C(0)$$

By combination of (*Equation 39*) and (*28*) we find:

Equation 29

$$V_C(0) = \frac{1}{2}\left(V_{in} - \frac{Iin}{Cr}Ts\right)$$

$$V_C\left(\frac{Ts}{2}\right) = \frac{1}{2}\left(V_{in} + \frac{Iin}{Cr}Ts\right)$$

After some algebraic manipulations, it is possible to find that the equations governing the operation of the circuits in *Figure 30* are:

Equation 30

$$\begin{cases} \frac{d^2V_{HB}}{dt} + \frac{1}{C_{HB}(Ls+Lp)}V_{HB} = \frac{V_C(0)}{C_{HB}(Ls+Lp)} & \text{DCM} \\ \frac{d^2V_{HB}}{dt} + \frac{1}{C_{HB}Ls}V_{HB} = \frac{V_C(0) - a\cdot(V_{out}+V_F)}{C_{HB}Ls} & \text{CCM} \end{cases}$$

with the following initial conditions:

Equation 31

$$V_{HB}(0) = 0, \left.\frac{dV_{HB}}{dt}\right|_{t=0} = \frac{I_R(0)}{C_{HB}}$$

The solutions of these equations are:

Equation 32

$$V_{HB}(t) = \begin{cases} V_{DD}\sin(\omega_{DD}t - \varphi_{DD}) + V_C(0) & \text{DCM} \\ V_{CC}\sin(\omega_{CC}t - \varphi_{CC}) + V_C(0) - a\cdot(V_{out}+V_F) & \text{CCM} \end{cases}$$

with

Equation 33

$$\omega_{DD} = \frac{1}{\sqrt{(Ls+Lp)C_{HB}}}, \varphi_{DD} = \tan^{-1}\left(\frac{V_C(0)}{I_R(0)}\sqrt{\frac{C_{HB}}{Ls+Lp}}\right), V_{DD} = \frac{V_C(0)}{\sin\varphi_{DD}}, \omega_{CC} = \frac{1}{\sqrt{LsC_{HB}}},$$

$$\varphi_{CC} = \tan^{-1}\left(\frac{V_C(0) - a\cdot(V_{out}+V_F)}{I_R(0)}\sqrt{\frac{C_{HB}}{Ls}}\right), V_{CC} = \frac{V_C(0) - a\cdot(V_{out}+V_F)}{\sin\varphi_{CC}}$$

The expression of the tank current will be:

Equation 34

$$I_R(t) = C_{HB}\frac{dV_{HB}(t)}{dt} = \begin{cases} C_{HB}\cdot V_{DD}\cdot \omega_{DD}\cdot \cos(\omega_{DD}t-\omega_{DD}) = \dfrac{I_R(0)}{\cos\omega_{DD}}\cos(\omega_{DD}t-\varphi_{DD}) & \text{DCM} \\ C_{HB}\cdot V_{CC}\cdot \omega_{CC}\cdot \cos(\omega_{CC}t-\omega_{CC}) = \dfrac{I_R(0)}{\cos\omega_{CC}}\cos(\omega_{CC}t-\varphi_{CC}) & \text{CCM} \end{cases}$$

Equations (*Equation 30*) to (*34*) apply in the time interval (0, T_T), where T_T is the time needed for the voltage V_{HB} to reach V_{in}. T_T can be calculated from (*Equation 32*) taking (*33*) into account; the result is:

Equation 35

$$T_T = \begin{cases} \dfrac{1}{\omega_{DD}}\left[\varphi_{DD} + \sin^{-1}\left(\dfrac{V_{in}-V_C(0)}{V_{DD}}\right)\right] & \text{DCM} \\ \dfrac{1}{\omega_{CC}}\left[\varphi_{CC} + \sin^{-1}\left(\dfrac{V_{in}-V_C(0)+a\cdot(V_{out}+V_F)}{V_{CC}}\right)\right] & \text{CCM} \end{cases}$$

To achieve ZVS, the value of T_T given by (*Equation 35*) must not exceed the deadtime T_D to make sure that Q1 is turned on with zero drain-to-source voltage.

Note that in CCM operation there may be an additional constraint on the time interval where equations (*Equation 30*) to (*34*) are applicable. The current $I_R(t)$ will be described by *Equation 34* either until T_T or until it equals the current flowing through Lp (see *Figure 9*), whichever condition occurs first. We will assume that $I_R(t)=I(Lp)$ occurs after T_T.

With the usual values of all the involved quantities, the phase angles φ_{CC} and φ_{DD} are both considerably less than unity, then it is possible to use the approximation $\varphi \approx \sin\ \varphi \approx \tan\varphi$ for both of them. With this simplification (*Equation 35*) can be expressed as:

Equation 36

$$T_T = \frac{V_{in}}{I_R(0)}C_{HB}$$

for both CCM and DCM modes, which is equivalent to considering C_{HB} charged by a constant current $I_R(0)$.

Considering that in CCM operation above resonance it is $V_{in} > 2\cdot a\cdot(V_{out} + V_F)$ and, again, that $V_C(0) \le V_{in}/2$, φ_{CC} is always negative. As a result, $I_R(t)$ has its peak for negative t values and decays in (0, T_T). In DCM operation, if the input current is lower than a critical value, it is $V_C(0) > 0$ and, then, φ_{DD} positive. Thereby, $I_R(t)$ has its peak for positive t values, thus it initially increases and then decays in (0,T_T). In this case, which happens at light load and with no load, the approximation $I_R(t) = I_R(0)$ is excellent. Still in DCM operation, but with an input current exceeding that critical value, it is $V_C(0) < 0$ and, then, φ_{DD} negative, which happens below resonance at heavy load. However, as compared to what happens in CCM operation, the associated resonance period is longer, thus the change in $I_R(t)$ is lower and the approximation $I_R(t) = I_R(0)$ is still good. This is illustrated in *Figure 31* and *32*.

Figure 31. Voltage of HB node vs time (see *Equation 32*)

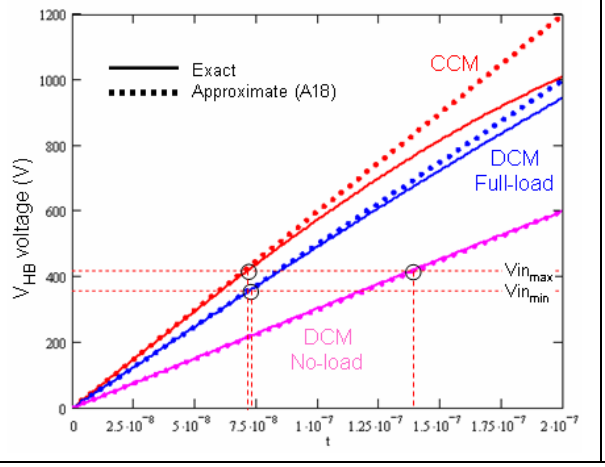
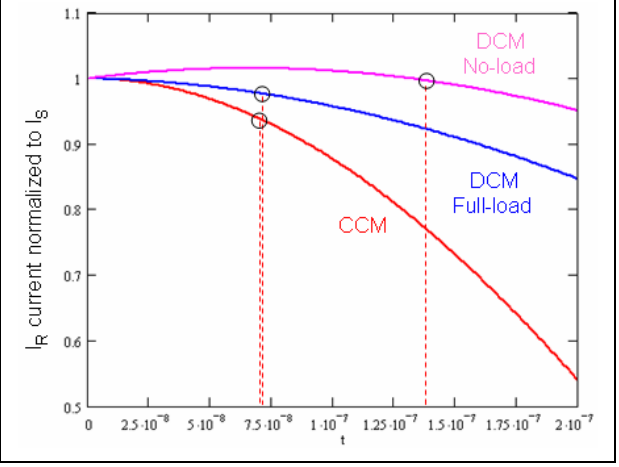


Figure 32. Resonant current vs time (see *Equation 34*)



In the end, the approximation (*Equation 36*) provides a relationship that is sufficiently accurate for design purposes under all operating conditions. Fortunately the conditions where accuracy is worst (CCM) are not critical as far as ZVS is concerned because the switched current $I_R(0)$ is greater than it is under all other conditions.

To achieve ZVS for both switches, a necessary condition is that $T_T \leq T_D$. An additional constraint comes from the condition that the tank current I_R has to keep its sign unchanged during the time interval $(0, T_D)$. Should the current become zero in that interval, the body diode of Q1 would not be forward biased any more and the voltage V_{HB}, no longer constrained to Vin, would experience oscillations at an angular frequency equal to either ω_{DD} or ω_{CC}. Q1 would then be turned on with a drain-to-source voltage in general greater then zero.

In practical cases, when the converter is operated at or above resonance the tank current crosses zero with a considerable delay after the end of the deadtime, especially in DCM modes, where the phase lag φ described by *Equation 5* or *8* or *11* or *13* tends to $\pi/2$; hence, this constraint can be disregarded. It becomes significant when working below resonance and close to the boundary between the capacitive and the inductive mode (CCMB mode).

Under the assumption $T_T < T_D$, in the time interval (T_T, T_D) *Equation 34* no longer apply and I_R is again a portion of sinusoid having frequency f_{R1}, which can be described by an equation of the type:

Equation 37

$$I_R(t) = I_{Rpk}\sin(2\pi f_{R1}t - \varphi)$$

In order for the tank current to keep the same sign during the remainder of the deadtime, the following condition must be fulfilled:

Equation 38

$$2\pi f_{R1}T_D - \varphi > 0$$

Appendix C Power MOSFET effective C_{oss} and half-bridge midpoint's transition times

Unlike linear capacitors, which have a capacitance value independent of the applied voltage, power MOSFET C_{oss} is a nonlinear capacitance, i.e. its value is a function of the drain-to-source voltage V_{DS}. Assuming a p-n step junction for the body-drain diode, with good approximation the C_{oss} vs. V_{DS} relationship can be expressed as:

Equation 39

$$\frac{C_{oss}(V_{DS1})}{C_{oss}(V_{DS2})} \approx \sqrt{\frac{V_{DS2}}{V_{DS1}}}$$

Power MOSFETs manufacturers usually specify the value of C_{oss} at V_{DS} = 25 V (with V_{GS}=0 at 1 MHZ), From (*Equation 39*) the C_{oss} at a given voltage V_{DS} will be:

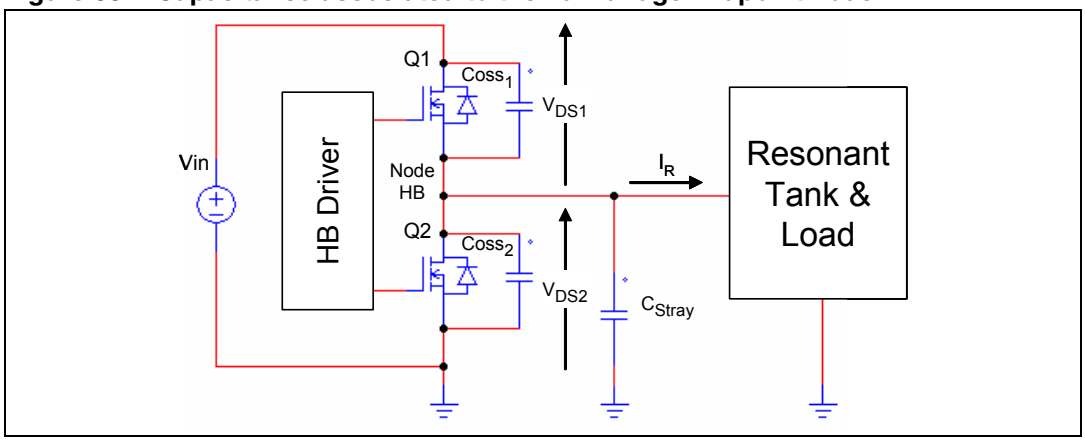
Equation 40

$$C_{oss}(V_{DS}) = C_{oss25}\sqrt{\frac{25}{V_{DS}}} = \frac{5}{\sqrt{V_{DS}}}C_{oss25}$$

Generally speaking, C_{oss} has a twofold role in switching losses mechanism in power MOSFET:

1. at turn-on C_{oss} is discharged and the energy stored in it is dissipated inside the MOSFET's $R_{DS(on)}$, thus giving origin to the so-called "capacitive losses". This is not significant in the LLC resonant converter because power MOSFETs are operated in ZVS and capacitive losses are zero, and then it will not be considered.
2. at turn-off the rate of rise of its voltage determines the voltage-current overlap that originates switching losses. This is significant in the LLC resonant converter.

Figure 33. Capacitance associated to the half-bridge midpoint node



It is worth noticing that, although the C_{oss} of the two power MOSFETs in the half-bridge are effectively connected in parallel, however they experience different V_{DS} voltages at any time. If V_{in} is the DC input voltage, and with reference to the circuit shown in *Figure 33*, the following relationship holds true:

Equation 41

$$V_{DS1} - V_{DS2} = V_{in}$$

Then, assuming that the two MOSFETs are identical to one another (so that $C_{oss25\text{-}1} = C_{oss25\text{-}2} = C_{oss25}$), and referring to the voltage of the half-bridge midpoint V_{HB} (= V_{DS2}), their individual C_{oss} will be:

Equation 42

$$C_{oss1} = \frac{5}{\sqrt{V_{DS1}}}C_{oss25} = \frac{5}{\sqrt{V_{in} - V_{HB}}}C_{oss25}$$

Equation 43

$$C_{oss2} = \frac{5}{\sqrt{V_{DS2}}}C_{oss25} = \frac{5}{\sqrt{V_{HB}}}C_{oss25}$$

and their instantaneous cumulative value will be:

Equation 44

$$Coss(V_{HB}) = C_{oss1} + C_{oss2} = 5\left(\frac{1}{\sqrt{V_{HB}}} + \frac{1}{\sqrt{V_{in} - V_{HB}}}\right)C_{oss25}$$

The diagram of equations (*Equation 43*) and (*Equation 44*) are shown in *Figure 34*. The branch-constitutive equation of the capacitor C_{oss}:

Equation 45

$$I_{C_{oss}}(t) = C_{oss}(V_{HB})\frac{dV_{HB}}{dt} \Rightarrow I_{C_{oss}}(t)dt = C_{oss}(V_{HB})dV_{HB}$$

can be integrated by variable separation.

Figure 34. C_{oss} capacitances vs. half-bridge midpoint's voltage

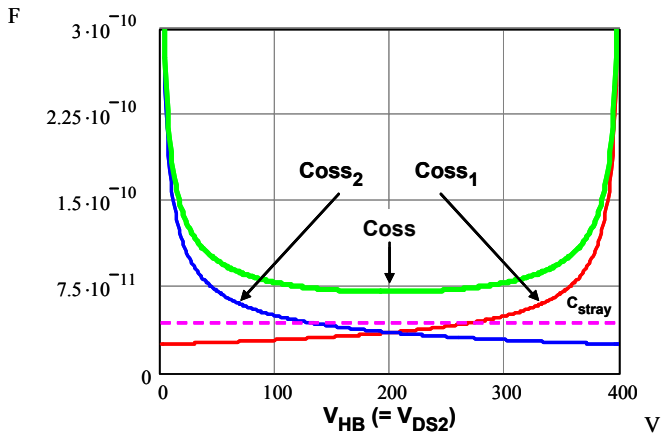
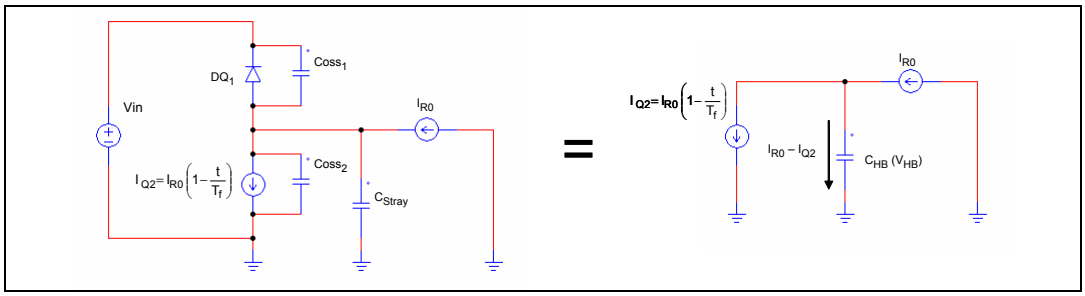


Figure 35. Simplified schematic to analyze transition times of the node HB when Q2 turns off



Assuming that $V_{HB}|_{t=0}$ it is possible to write:

Equation 46

$$\int_0^{tf} I_{C_{oss}}(\tau)d\tau = \int_0^{V_{HB}} C_{oss}(V)dV$$

Note that the left-hand side is the total charge $Q_{oss}(V_{HB})$ supplied to $C_{oss}(V_{HB})$ to raise its voltage up to the level V_{HB}. Substituting (*Equation 44*) in (*Equation 46*) and developing, it is possible to find:

Equation 47

$$Qoss(V_{HB}) = 10(\sqrt{V_{HB}} + \sqrt{V_{in}} - \sqrt{V_{in} - V_{HB}})C_{oss25}$$

Considering again the turn-off of Q2, as a consequence of the discussion of the previous section, the equivalent schematic of the circuit during the turn-off of Q2 is illustrated in *Figure 35*, where the tank circuit is then replaced by a constant current source equal to the switched current I_{R0}. Additionally, the turn-off of Q2 is assumed to be linear in time:

Equation 48

$$I_{Q2} = \begin{cases} I_{R0}\left(1 - \frac{t}{T_f}\right) & 0 \le t \le T_f \\ 0 & t > T_f \end{cases}$$

where T_f is the time the current I_{Q2} takes to become zero. The total capacitance of the node HB will be:

Equation 49

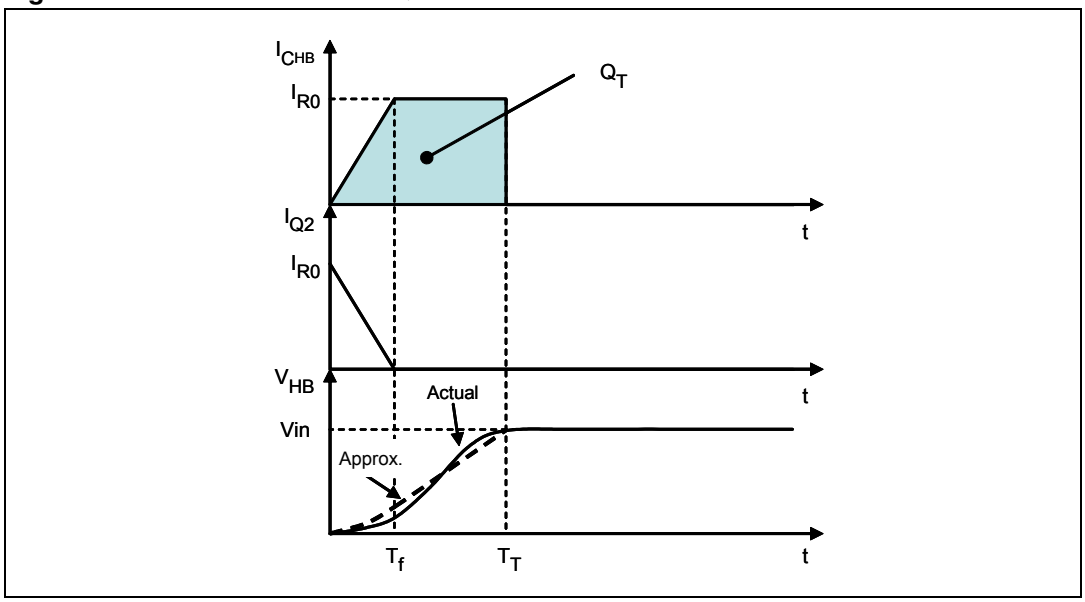
$$C_{HB}(V_{HB}) = C_{Stray} + C_{oss}(V_{HB})$$

C_{HB} will be charged by the current $I_{CHB} = I_{R0} - I_{Q2}$ until V_{HB} equals the input voltage V_{in} and DQ1 turns on, thus clamping V_{HB} at V_{in}. Let us assume that the time T_T needed for the voltage of the node HB to reach V_{in} is greater than T_f. The main quantities during the transient are illustrated in *Figure 36*. The total charge Q_T delivered to C_{HB} in the interval $(0, T_T)$ will be:

Equation 50

$$Q_T = \frac{1}{2}I_{R0}T_f + I_{R0}(T_T - T_f) = I_{R0}\left(T_T - \frac{T_f}{2}\right)$$

Figure 36. Schematization of Q2 turn-off transient



This charge will be partly stored in C_{Stray} and partly in C_{oss}. The charge in C_{Stray} will obviously be $C_{Stray} \cdot V_{in}$, then the one stored in C_{oss} will be given by (*Equation 47*) substituting V_{in} in V_{HB}:

Equation 51

$$Qoss(V_{in}) = 20\sqrt{V_{in}}C_{oss25}$$

A linear capacitance C_{HB} equivalent to $C_{HB}(V_{in})$ will have the same total charge Q_T stored in it when its voltage equals V_{in}. Then it is possible to write:

Equation 52

$$Q_T = C_{Stray}V_{in} + 20\sqrt{V_{in}}C_{oss25} = C_{HB}V_{in}$$

which yields:

Equation 53

$$C_{HB} = C_{Stray} + \frac{20}{\sqrt{V_{in}}}C_{oss25}$$

The capacitance value defined by (*Equation 53*) has to be used in calculations related to transition time of the node HB, as far as ZVS is concerned.

As previously stated, to achieve ZVS the transition of the node HB must be completed within the deadtime T_D inserted between the transitions from one state to the other of either switch, that is, $T_T \leq T_D$. Combining (*Equation 46*) and (*Equation 48*) and solving for T_T:

Equation 54

$$T_T = \frac{T_f}{2} + \frac{C_{Stray}V_{in} + 20\sqrt{V_{in}}C_{oss25}}{I_{R0}} = \frac{T_f}{2} + \frac{C_{HB}V_{in}}{I_{R0}} \leq T_D$$

Depending on the data available, (*Equation 54*) can be used for finding either the minimum value of I_{R0} (called I_{Rmin} in the text) or the maximum value of C_{HB} or the minimum value of T_D .

In datasheets of many power MOSFET manufacturers, it is customary to find an "equivalent output capacitance" denoted with C_{osseq} and defined as a constant equivalent capacitance giving the same charging time as C_{oss} when the drain-to-source voltage V_{DS} increases from 0 to 80% of the rated voltage V_{DSS}.

From the above discussion it is easy to recognize that the linear capacitance equivalent to the C_{oss} of a single MOSFET charged at a voltage V_{DS} is:

Equation 55

$$C_{osseq}(V_{DS}) = \frac{10}{\sqrt{V_{DS}}} C_{oss25}$$

then, as per the above definition:

Equation 56

$$C_{osseq} = \frac{10}{\sqrt{0.8 \cdot V_{DSS}}} \cdot C_{oss25} \approx \frac{11.2}{\sqrt{V_{DSS}}} C_{oss25}$$

The actual value provided in the datasheet can be different from the theoretical value given by (*Equation 56*), depending on the silicon cell design and density of the particular power MOSFET. For an assigned power MOSFET, whose C_{osseq} is specified, by combining with (*Equation 55*), equation (*Equation 53*) can be re-written as:

Equation 57

$$C_{HB} = C_{Stray} + 2\sqrt{\frac{V_{DSS}}{V_{in}}} C_{osseq}$$

Appendix D Power MOSFETs switching losses at turn-off

The nonlinearity of C_{oss} (refer to *Figure 34*) makes the voltage of the node HB increase slowly at its low values and its high values, and much faster when it is half way in its swing (see the solid V_{HB} waveform labeled "Actual" in *Figure 36*). Typically, the current through either Q1 or Q2 during their respective turn-off transients flows during the initial part of the transition of the node HB, i.e. when its value is changing more slowly. This reduces the voltage-current overlap and, consequently, the associated power loss with respect to a linear capacitor. However, the mathematical expression of the loss is extremely complex, therefore it is more useful to provide a conservative estimate using the equivalent linear capacitance C_{HB} defined by (*Equation 53*). The associated V_{HB} curve is the dotted one labeled "Approx." in *Figure 36* (under the assumption $T_f < T_T$).

Again with reference to the turn-off of Q2, the voltage on the node HB can be found by integration of the branch-constitutive equation of C_{HB}:

Equation 58

$$I_{C_{HB}}(t) = C_{HB}\frac{dV_{HB}}{dt} \Rightarrow V_{HB}(t) = \frac{1}{C_{HB}}\int_0^t I_{C_{HB}}(t)dt = \frac{1}{C_{HB}}\int_0^t [I_{R0} - I_{Q2}(t)]dt$$

Power loss due to voltage-current overlap (switching loss) will occur only during the time interval (0, T_f) where I_{Q2} is non-zero, then (*Equation 54*) will be considered in this interval only; substituting (*Equation 48*) in (*Equation 58*) we find:

Equation 59

$$V_{HB}(t) = \frac{1}{C_{HB}}\int_0^t \frac{I_{R0}}{T_f}tdt = \frac{I_{R0}}{2 \cdot C_{HB} \cdot T_f}t^2 \qquad t \in (0, T_f)$$

Note that in the remainder interval (T_f, T_T) the voltage V_{HB} will change linearly with time because charged by the constant current I_{R0}. The energy lost because of voltage-current overlap will be calculated by integration of the product of (*Equation 59*) times (*Equation 48*):

Equation 60

$$E_{off}(Q2) = \int_0^{T_f} I_{Q2}(t) \cdot V_{HB}(t)dt = \frac{I^2_{R0}}{2C_{HB} \cdot T_f}\int_0^{T_f} t^2\left(1 - \frac{t}{T_f}\right)dt = \frac{(I_{R0} \cdot T_f)^2}{24C_{HB}}$$

Power loss will be obtained multiplying the energy loss given by (*Equation 60*) by the operating frequency f_{sw}:

Equation 61

$$P_{off}(Q2) = E_{off}(Q2)f_{sw} = \frac{(I_{R0} \cdot T_f)^2}{24C_{HB}}$$

The same loss occurs to the high-side power MOSFET Q1 as well, thereby, the total switching loss will be:

Equation 62

$$P_{off_{TOT}} = \frac{(I_{R0} \cdot T_f)^2}{12C_{HB}} \cdot f_{sw}$$

A more accurate analysis could be done observing in *Figure 34* that C_{oss1} (C_{oss2} in case we consider Q1's turn-off) changes little during the first portion of the transient, so that it might be considered constant. With this approach, from (*Equation 44*) it is possible to assume:

Equation 63

$$C_{oss}(V_{HB}) \approx 5\left(\frac{1}{\sqrt{V_{HB}}} + \frac{1}{\sqrt{V_{in}}}\right)C_{oss25}$$

and, from (*Equation 49*), taking (*Equation 63*) into account:

Equation 64

$$C_{HB}(V_{HB}) \approx C_{Stray} + 5\left(\frac{1}{\sqrt{V_{HB}}} + \frac{1}{\sqrt{V_{in}}}\right)C_{oss25} = \left(C_{Stray} + \frac{5}{\sqrt{V_{in}}}Coss_{25}\right) + \frac{5}{\sqrt{V_{HB}}}C_{oss25}$$

Designating:

Equation 65

$$C_{HBF} = C_{Stray} + \frac{5}{\sqrt{V_{in}}}C_{oss25}$$

substituting (*Equation 64*) in (*Equation 46*), integrating both sides and solving for V_{HB} it is possible to find:

Equation 66

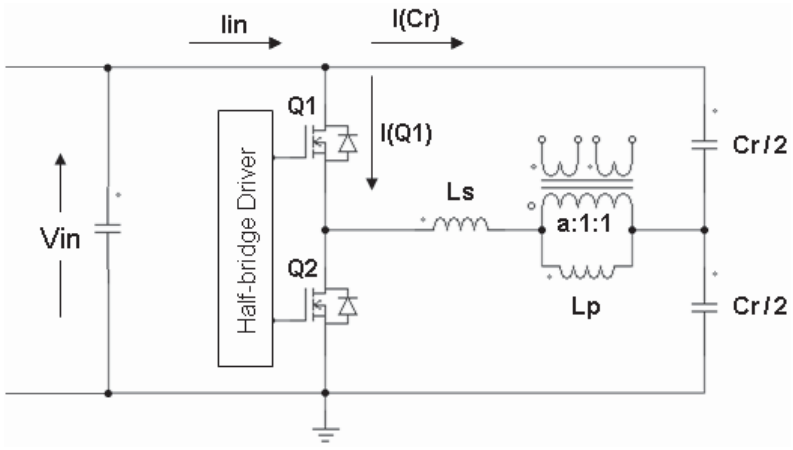
$$V_{HB}(t) = \frac{1}{C_{HBF}}\left[\frac{I_{R0}}{2 \cdot T_F}t^2 - 10\frac{C_{oss25}}{C_{HBF}}\left(\sqrt{25 \cdot C^2_{oss25} + \frac{C_{HBF}I_{R0}}{2 \cdot T_F}t^2} - 5C_{oss25}\right)\right]$$

Inserting this result in (*Equation 60*) and integrating would yield the turn-off energy, however the result is complex and of little practical use, hence it will not be provided.

Appendix E Input current in LLC resonant half-bridge with split resonant capacitors

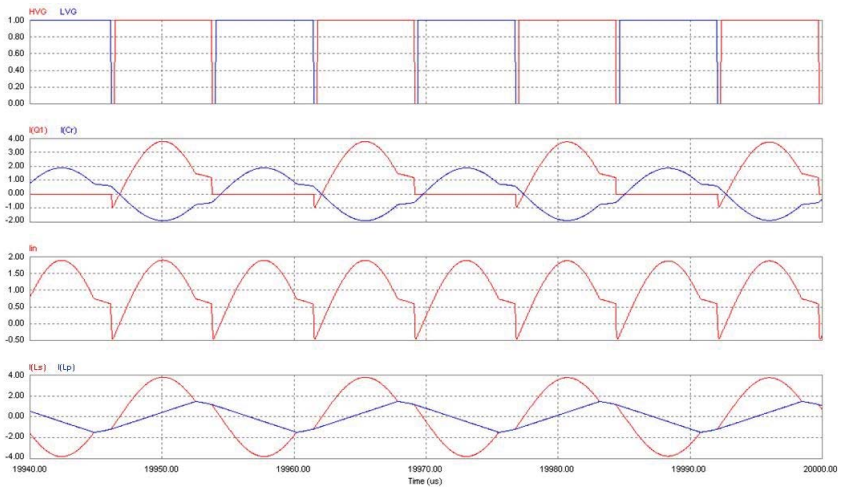
An interesting property of the LLC resonant half-bridge with split resonant capacitors is the shape of the input current. Unlike the single capacitor version, where the input current Iin equals the current through the high-side switch Q1, I(Q1), in this case Iin is given by the superposition of I(Q1) and the current through the high-side resonant capacitor I(Cr), as shown in *Figure 37*.

Figure 37. Input current components in a split-capacitor LLC resonant half-bridge



The current I(Cr) with the direction defined in *Figure 37* is in phase opposition to I(Q1) and to the current through the series resonant inductor I(Ls); also, its instantaneous amplitude is half that of I(Ls) since it is equally split between the two resonant capacitors. As a result, when Q1 is ON, I(Cr) is negative and Iin equals I(Q1) diminished by I(Cr); when Q1 is OFF and I(Q1)=0, Iin = I(Cr) is positive and provides a continuous input current flow. This is shown in the timing diagrams of *Figure 38*.

Figure 38. Timing diagram showing currents flow in the converter of *Figure 37*



Note that the input current is the same as in a full-bridge converter, where during each half switching period there is a conducting path drawing current from the input source.

With the same DC value of Iin, then, the split capacitor configuration makes its peak and squared rms values are cut in half. Unlike bridge converters, however, the currents I(Q1) and I(Q2) keep the same value as in the single capacitor half-bridge version.

It is then advantageous to use the split capacitor configuration to reduce not only the ac current requirements on the resonant capacitors but also the ac current in the input capacitor and the differential-mode conducted noise. It is then easy to find this solution at higher power levels but it is advisable to use it also when there is no front-end PFC pre-regulator. In this case, in fact, the differential-mode noise that the input EMI filter is required to mitigate is that generated by the resonant half-bridge converter (whereas, with a PFC front-end the noise generated by this stage would be largely dominant), thus it is possible to maximally benefit from the reduction of its differential-mode component.

Revision history

Table 2. Document revision history

Date	Revision	Changes
06-May-2008	1	Initial release
15-Sep-2008	2	Modified: *Section 2.1*, *2.2*, *Appendix B* Added: *Appendix E*