# AN2864
# Application note

## VIPER17L demonstration board with wide-range input, 5 V / 1 A output and optimized standby performance

## Introduction

In consumer applications like LCD TVs, DVD players, set-top boxes and others, it is desirable to be able to switch on or switch off the application directly from the remote control. It is therefore necessary to supply the remote control receiver even when the equipment is not in use (standby mode). In standby mode only a minimum load (in the range of a few tens of a mW) is present at the power supply output. Often there are a few mA of load present at the 5 V or 3.3 V power supply output. Even if no load is applied to the power converter, some power is still sunk by the mains to keep the converter alive. The load for the mains is constant (24 hours per day) giving a good contribution to the total consumption of the equipment.

From this consideration arises the need to reduce the consumption of the power supply as low as possible when it is light loaded or even when it is not loaded.

Consumer equipment manufacturers often give different criteria for measuring the standby performance of a power supply, depending on both the characteristics of the equipment and their own considerations. In order to evaluate the standby power supply performance, a good starting point is the measurement of power consumption when the unit is not loaded. The STEVAL-ISA058V1 demonstration board is presented with a power consumption of 30 mW in no load condition.

**Figure 1. STEVAL-ISA058V1 demonstration board for the VIPER17L**

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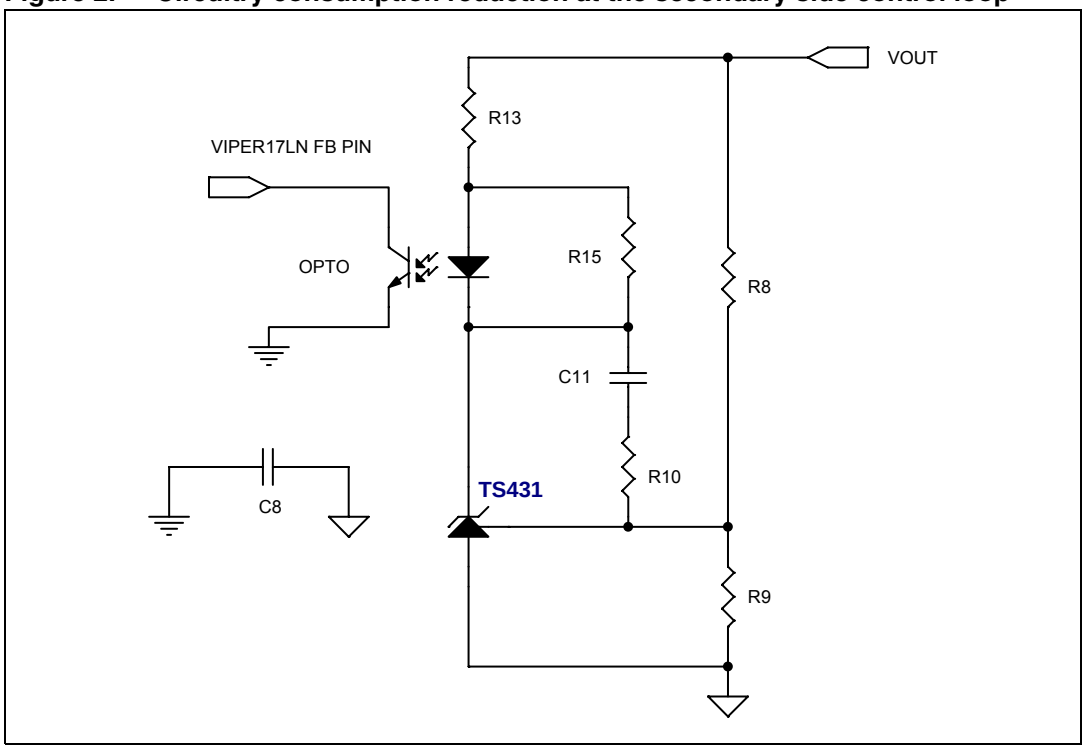
# 1 Tips for reducing the standby consumption

In this section, minimizing the standby power consumption in a flyback isolated converter is analyzed, as well as how the new VIPER17L device can help to achieve this.

When light loaded or in a no load condition, most of the losses are switching losses that are almost proportional to the switching frequency. It should be considered that even if no external load is connected to the power supply, some power needs to be processed in order to sustain the operation of the VIPER17L and the circuitry at the secondary side, which senses the output voltage and closes the control loop (see *Figure 2*). The burst mode operation of the VIPER17L significantly reduces the average switching frequency of the converter, when light loaded or completely no-loaded. Basically, when the converter switches to burst mode operation, the lower the load, the lower the average switching frequency. So, in order to reduce the average switching frequency to as low as possible, the control loop should be designed to minimize the required power so as to sustain the operation of the circuitry which closes the control loop at the secondary side.

## 1.1 Reduction of circuitry consumption at the secondary side control loop

**Figure 2. Circuitry consumption reduction at the secondary side control loop**




Usually, in an isolated flyback converter where the output is directly sensed for control loop input, the TL431 is used, which is a device that contains an error amplifier and a voltage reference. For a TL431 the minimum bias current is 1 mA. In order to guarantee this bias current in every operating condition, a 1 kΩ resistor is connected in parallel with the photo-diode of the opto-coupler (R15, see *Figure 2*). If, instead of the TL431, a device with a lower

minimum bias current is used, the resistance value of R15 can be increased, reducing the equivalent load. In the STEVAL-ISA058V1 demonstration board a TS431, rather than the TL431, is used. The minimum bias current of this device is 60 µA, so the R15 value can be increased up to 15 kΩ, reducing significantly the load due to the voltage reference and the error amplifier.

Moreover, the resistance values used to sense the output voltage (R8 and R9 in the schematic shown in *Figure 2*) must be quite high. The requirements of the regulation loop must also be taken into account. It should be kept in mind that increasing the resistance above a certain value will not improve the standby performance significantly. As a rule-of-thumb, the current through these resistors should be in the range of the TS431 device bias current. In the present case, the output voltage of the converter is 5 V and the R8 and R9 selected values are of 120 kΩ (R8) and 39 kΩ (R9), respectively, which gives a total value of 159 kΩ (R8 + R9) with a current of 31 µA.

## 1.2 Burst mode operation

As the load decreases, the voltage on the FB pin of the VIPER17L decreases also. When it falls below the burst mode threshold (typ. 450 mV), the converter stops switching. With no switching, no power can be processed or delivered to the converter outputs. The auxiliary winding delivers no energy to the VIPER17L logic, which is now supplied by the energy stored in the capacitor connected between the $V_{DD}$ pin and GND. In order to reduce the discharge of this capacitor during burst mode operation, when the device is not switching, the device control logic reduces its consumption by turning off all unused or unnecessary internal blocks. The circuitry connected to the output of the converter is supplied by the energy stored in the output capacitors, which are discharged, leading to output voltage drops that cause the feedback loop reaction. The voltage on the feedback pin starts to rise again. When the feedback pin voltage exceeds the burst mode threshold, plus any hysteresis (450 mV + 50 mV, typ. values), the switching operation restarts and both the output capacitor and the capacitor connected on the $V_{DD}$ pin are recharged. The result is intermittent operation where the average power delivered to the load is exactly that which is necessary, and the average switching frequency is significantly reduced. Burst mode operation is not a new idea, but the converter design can be optimized to take as much advantage of it as possible.

When the device operates in burst mode, the average switching frequency is relative to the total load that the converter must supply. In the total load the bias currents of the components at the secondary side used for closing the feedback loop are also included. If one considers that during burst mode operation the drain peak current is almost constant, this means that the average switching frequency is proportional (see *Equation 1*) to the power delivered to the secondary and the auxiliary winding. From this consideration arises the need to reduce, as much as possible, the power consumption of the VIPER17L control logic as well as the additional circuitry needed to close the feedback loop or perform other functions. By doing so, the total load of the converter, the average switching frequency and the switching losses are reduced.

**Equation 1**

$$P_{out} = \eta \cdot \frac{1}{2} \cdot L_p \cdot I^2_{DRAIN\_PK} \cdot f_{sw\_avg}$$

## 1.3 VIPER17L consumption

The VIPER17L current consumption is 1.8 mA maximum for the L version when switching. When the device is not switching and the FB pin voltage goes below the burst mode thresholds, the current consumption is reduced to 900 µA. Clearly, lowering device consumption contributes to the reduction of total power consumption, but it also presents other advantages. The control loop senses the output voltage and modulates the power processed according to the load on the output, in order to keep the output voltage constant at the target value. The voltage that supplies the VIPER17L is not regulated, but should follow the output voltage according to the auxiliary to secondary windings turn ratio.

The winding coupling is never perfect in a real transformer. Even if the output voltage is well regulated, the auxiliary voltage changes according to the load ratio between output and auxiliary voltage. The cross-regulation problem inherent in flyback converters is well-known in power electronics literature [1]. Even if it is not discussed here, it is important to remember that the auxiliary voltage used for the VIPER17L device supply increases as the ratio between output and auxiliary current increases, and decreases as this ratio decreases. Even if no external load is present, the circuitry used for sensing the output voltage and closing the control loop sinks some current. In an optimized converter, for very low standby consumption this current is very low. It is then possible that the auxiliary voltage (voltage on the $V_{DD}$ pin) drops below the $V_{DD\_OFF}$ threshold of the VIPER17L (8.5 V max [2]) leading to device shutdown. In this case, the device begins to operate in hiccup mode (continuous shutdown and startup) and no longer guarantees the output voltage regulation. Keeping the current consumption of the VIPER17L low, at least when operating in burst mode, means increasing the above ratio between the output current and auxiliary current. This helps to keep the auxiliary voltage above the device $V_{DD\_OFF}$ threshold.

## 1.4 Transformer

For the purpose of reducing the switching losses, some consideration should be given to the transformer.

The primary parasitic capacitance is the capacitance measured at the primary side with the other transformer windings open. In order to measure it using an LCR meter, the frequency needs to be set as high as 1 MHz. The primary parasitic capacitance causes switch-on losses as it is fast-charged each time the MOSFET is turned on and the charging current dissipates energy within the MOSFET itself. Reducing this capacitance as low as possible, this type of loss will be minimized.

With reference to*Equation 1*, it is clear that a further reduction of the switching frequency can be obtained by increasing, as much as possible, the primary inductance of the transformer ($L_P$), (according to other design considerations also). In fact, if it is assumed that the power the converter must process to sustain a certain load is constant, raising the primary inductance increases the energy processed during each switching cycle (for the same drain peak current) and the number of switching cycles per unit of time, which means that the average switching frequency decreases.

# 2 STEVAL-ISA058V1 board description

## 2.1 Electrical specifications

The electrical specifications of the STEVAL-ISA058V1 demonstration board are listed in *Table 1*.

**Table 1. Electrical specifications**

| Symbol | Parameter | Value |
|---|---|---|
| $V_{IN}$ | Input voltage range | [90 $V_{RMS}$; 265 $V_{RMS}$] |
| $V_{OUT}$ | Output voltage | 5 V |
| $I_{OUT}$ | Max output current | 1 A |
| $\Delta_{VOUT\_LF}$ | Precision of output regulation | ±5% |
| $\Delta_{VOUT\_HF}$ | High frequency output voltage ripple | 50 mV |

These electrical specifications often meet the requirements of an auxiliary power supply for LCD or PDP TVs and external adapters.

## 2.2 Schematic and bill of material

The schematic of the board is shown in *Figure 3* and the bill of materials is given in *Table 2*.

**Figure 3. STEVAL-ISA058V1 schematic**

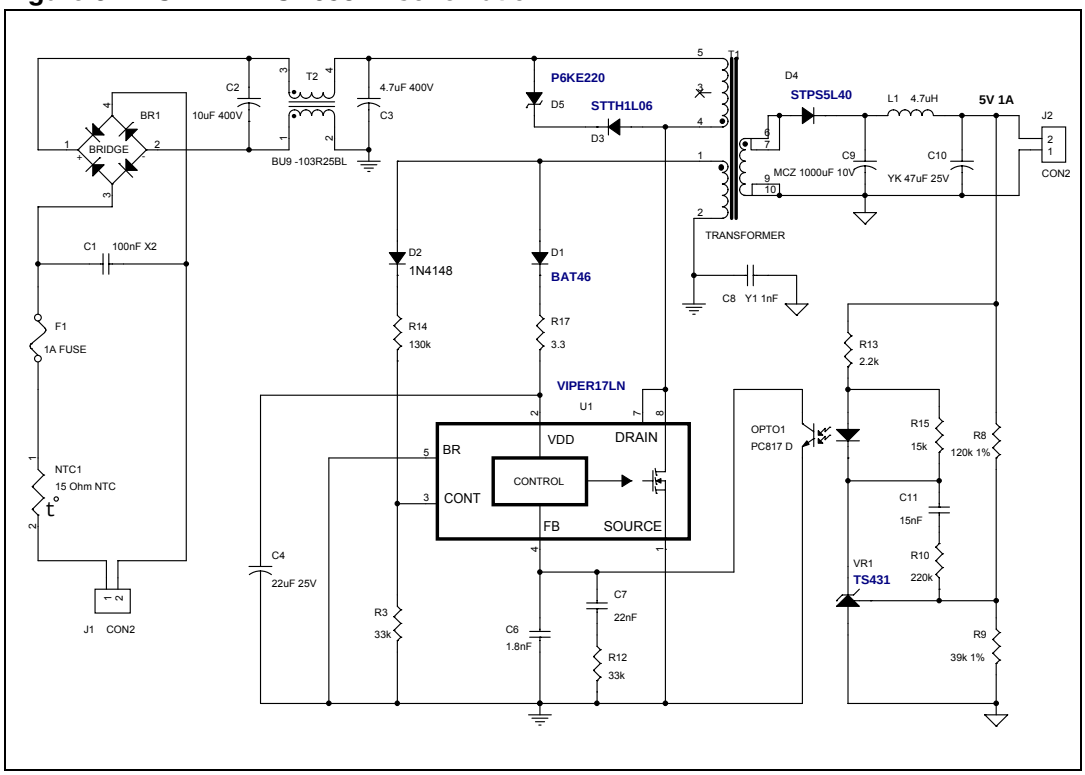


**Table 2. Bill of material**

| Reference | Part | Technology | Manufacturer | Manufacturer code |
|---|---|---|---|---|
| BR1 | DF06M | Miniature glass passivated single-phase bridge rectifier | General Semiconductor | DF06M |
| C1 | 100 nF | EMI suppressor capacitor MKP X2 type | EPCOS | B32922 |
| C2 | 10 µF 400 V | Aluminium electrolytic capacitor | Panasonic | ECA2GHG100 |
| C3 | 4.7 µF 400 V | Aluminium electrolytic capacitor | Panasonic | ECA2GHG4R7 |
| C4 | 22 µF 35 V | Aluminium electrolytic capacitor | Panasonic | ECEA1VKS220 |
| C6 | 1.8 nF | Ceramic capacitor | KEMET | C0805F182K5RAC |
| C7 | 22 nF | Ceramic capacitor | KEMET | C0805F223K5RAC |
| C8 | 2.2 nF | Y1 ceramic capacitor | Cera-Mite | 440LD22 10PCM |
| C9 | 1000 µF 10 V | Aluminium electrolytic capacitor MCZ series | Rubycon | |
| C10 | 47 µF 25 V | Aluminium electrolytic capacitor YK series | Rubycon | |
| C11 | 15 nF | Ceramic capacitor | KEMET | C0805F103K5RAC |
| D1 | BAT46 | Small signal Schottky diode | STMicroelectronics | BAT46 |
| D2 | 1N4148 | High speed diode | Philips | 1N4148 |
| D3 | STTH1L06 | Turbo 2 ultra fast high voltage rectifier | STMicroelectronics | STTH1L06 |
| D4 | STPS5L40 | Power Schottky rectifier | STMicroelectronics | STPS5L40 |
| D5 | P6KE220 | Transil | STMicroelectronics | P6KE220 |
| F1 | 1A FUSE | Fuse | Schurter | 0034.6615 |
| L1 | 4.7uH | Inductor | Panasonic | ELC08D4R7E |
| NTC1 | 16 Ω NTC | NTC | EPCOS | B57236S160M |
| OPTO1 | PC817D | Opto-coupler | Sharp | PC817D |
| R3,R12 | 33 kΩ 1% | Resistor | | |
| R8 | 120 kΩ 1% | Resistor | | |
| R9 | 39 kΩ 1% | Resistor | | |
| R10 | 220 kΩ | Resistor | | |
| R13 | 2.2 kΩ | Resistor | | |
| R14 | 130 kΩ | Resistor | | |
| R15 | 15 kΩ | Resistor | | |
| R17 | 3.3 kΩ | Resistor | | |
| T1 | Transformer | High frequency transformer | Pulse | PH0132NL |
| T2 | BU9 -103R25BL | Common mode choke | Coilcraft | BU9 -103R25BL |
| U1 | VIPER17LN | VIPER device | STMicroelectronics | VIPER17LN |
| VR1 | TS431 | Voltage reference | STMicroelectronics | TS431AIZ-AP |

## 2.3 Transformer

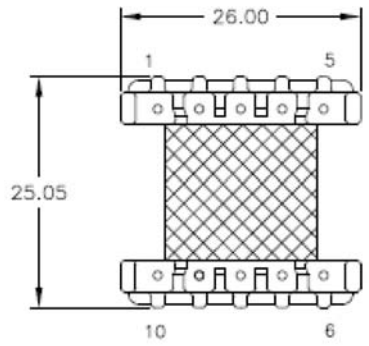
The transformer characteristics are listed in the table below.

**Table 3. Transformer characteristics**

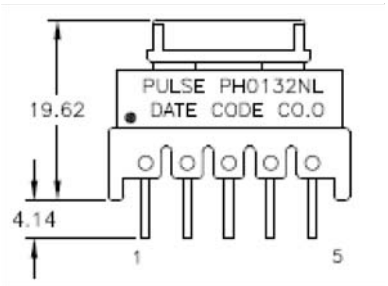
| Transformer information | Value | Characteristics |
|---|---|---|
| Manufacturer | Pulse | |
| Part number | PH0132NL | |
| Primary inductance (4-5) | 3.3 mH +/- 10% | Fr = 10 kHz, $T_A$ = 25 °C |
| Leakage primary inductance (4-5) | 100 µH max | (6,7,9,10) shorted<br>Fr = 100 kHz, $V_{RMS}$ = 0.1 V, $T_A$ = 25 °C |
| Primary to secondary turn ratio (4-5)/(6,7-9,19) | 14.82 ± 3% | Fr = 10 kHz, $V_{RMS}$ = 0.1 V, $T_A$ = 25 °C |
| Primary to auxiliary turn ratio (4-5)/(1-2) | 6.27 ± 3% | Fr = 10 kHz, $V_{RMS}$ = 0.1 V, $T_A$ = 25 °C |
| Insulation | 4 kV | Primary to secondary |

The illustrations below show the size (mm), the pin connection and the pin distances (mm) of the transformer.

**Figure 4. Transformer size**

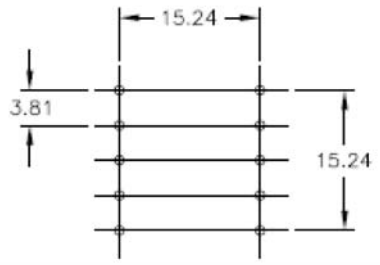



(a) Bottom view

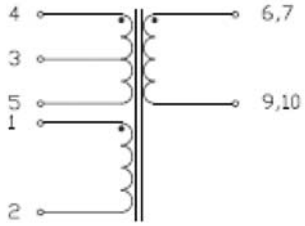



(b) Side view

**Figure 5. Transformer pin diagram and transformer electrical schematic**




(a) Pin distances




(b) Electrical diagram

# 3 Testing the board

## 3.1 Typical board waveforms

The STEVAL-ISA058V1 demonstration board must operate with a wide range of input voltages. For this reason, the waveforms are reported for the minimum, maximum and nominal input voltage values.

*Figure 6* and *Figure 7* show the drain current and the drain voltage waveforms at the nominal input voltage values, which are 115 $V_{AC}$ and 230 $V_{AC}$ for a maximum load (1 A). *Figure 8* and *Figure 9* show the waveforms for the same load condition, but with the minimum input voltage values (90 $V_{AC}$) in *Figure 8* and the maximum ones (265 $V_{AC}$) in *Figure 9*.

**Figure 6. Drain current and voltage at full load 115 $V_{AC}$**

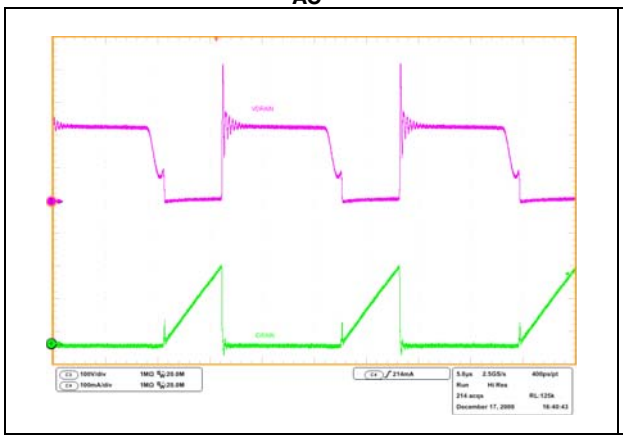


**Figure 7. Drain current and voltage at full load 230 $V_{AC}$**

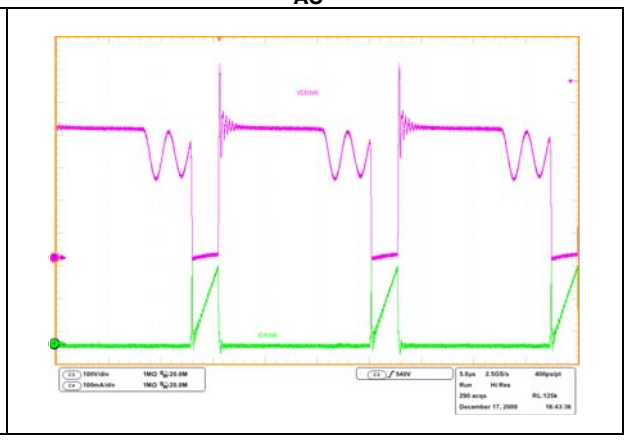


**Figure 8. Drain current and voltage at full load 90 $V_{AC}$**

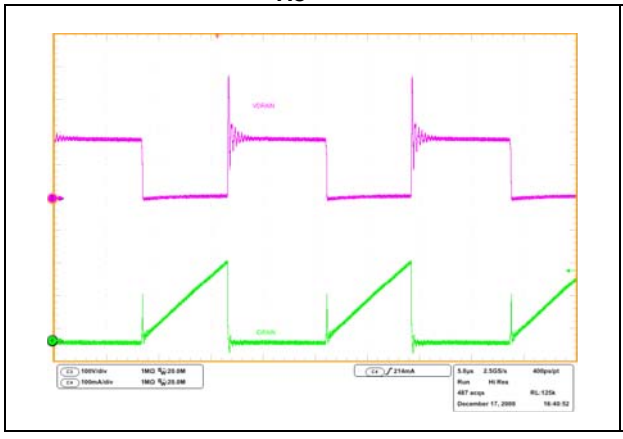
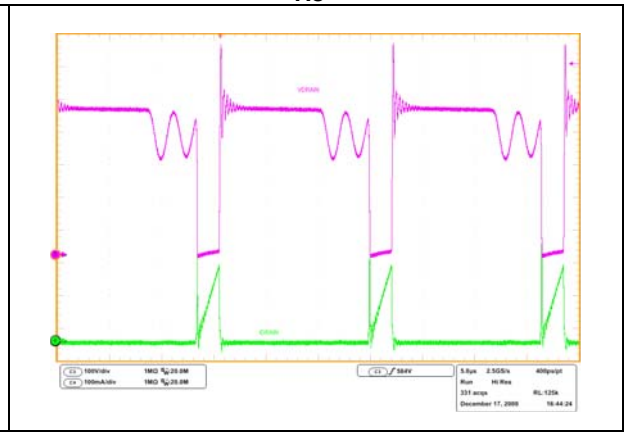


**Figure 9. Drain current and voltage at full load 265 $V_{AC}$**



## 3.2 Precision of the regulation and output voltage ripple

The output voltage of the board is measured in different line and load conditions. Results are reported in *Table 4*. The output voltage variation range is a few mV for all the tested conditions. The $V_{DD}$ voltage is also measured to verify that it is within the operating range of the device.

**Table 4. Output voltage and $V_{DD}$ line-load regulation**

| $V_{INAC}$ (V) | No load | | Half load | | Full load | |
|---|---|---|---|---|---|---|
| | $V_{OUT}$ (V) | $V_{DD}$ (v) | $V_{OUT}$ (V) | $V_{DD}$ (V) | $V_{OUT}$ (V) | $V_{DD}$ (V) |
| 90 | 5.05 | 10.7 | 5.04 | 23.5 | 5.04 | 25.4 |
| 115 | 5.06 | 10.6 | 5.04 | 24.1 | 5.04 | 25.4 |
| 230 | 5.06 | 10.6 | 5.04 | 25.3 | 5.04 | 25.4 |
| 265 | 5.06 | 10.4 | 5.04 | 25.2 | 5.04 | 25.4 |

The ripple at the switching frequency superimposed on the output voltage is also measured. The high frequency voltage ripple across capacitor C9 ($V_{OUT\_FLY}$), which is the output capacitor of the flyback converter before the LC filter, is also measured to verify the effectiveness of the LC filter. The results are reported in *Table 5*.

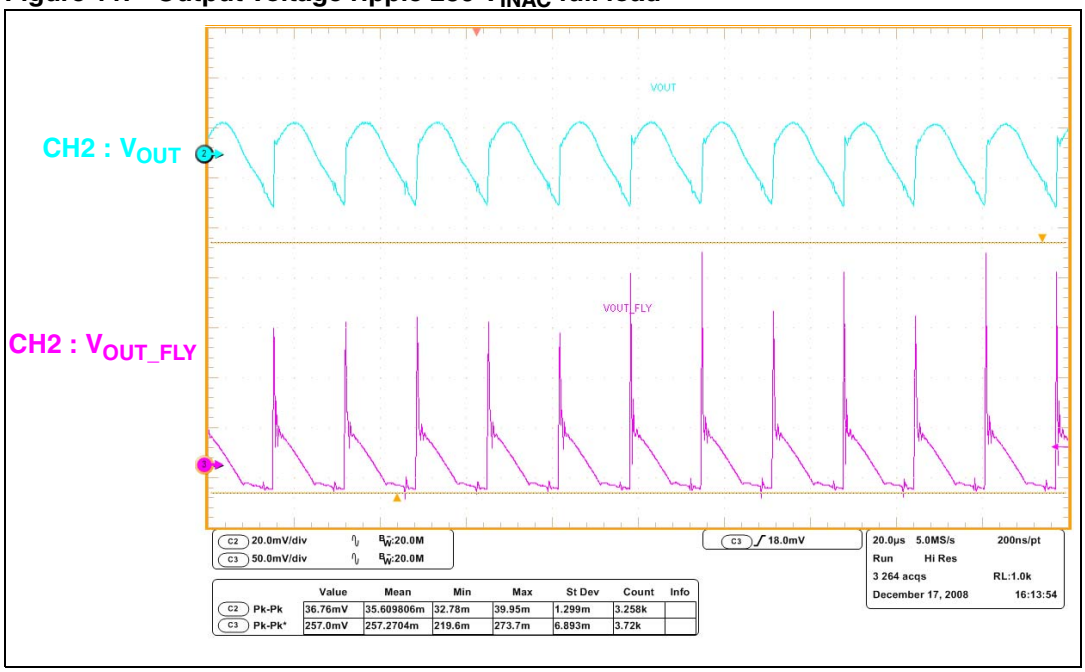
**Table 5. High frequency output voltage ripple**

| $V_{INAC}$ ($V_{RMS}$) | No load | | Half load | | Full load | |
|---|---|---|---|---|---|---|
| | $V_{OUT}$ (mV) | $V_{OUT\_FLY}$ (mV) | $V_{OUT}$ (mV) | $V_{OUT\_FLY}$ (mV) | $V_{OUT}$ (mV) | $V_{OUT\_FLY}$ (mV) |
| 90 | 11.1 | 94.1 | 26.0 | 192 | 41.5 | 261 |
| 115 | 10.9 | 90.9 | 26.1 | 192 | 39.7 | 269 |
| 230 | 12.8 | 102 | 26.5 | 201 | 40 | 274 |
| 265 | 14.7 | 110 | 26.7 | 194 | 39.4 | 270 |

The waveforms of the two voltages ($V_{OUT}$ and $V_{OUT\_FLY}$) are reported in the figures below.

**Figure 10. Output voltage ripple 115 $V_{INAC}$ full load**


**Figure 11. Output voltage ripple 230 $V_{INAC}$ full load**




When the device works in burst mode, a lower frequency ripple is present. In this mode of operation the converter does not supply continuous power to its output. It alternates the period when the power MOSFET is kept off and no power is processed by the converter and the period when the power MOSFET is switching and power flows towards the converter output. Even if no load is present at the output of the converter, during no switching periods the output capacitors are discharged by their leakage currents and the currents required to supply the part of the feedback loop present at the secondary side. During the switching

period, the output capacitance is recharged. *Figure 12* and *Figure 13* report the output voltage and the feedback voltage values when the converter is not loaded.

**Figure 12. Output voltage ripple 115 $V_{INAC}$ no load (burst mode)**

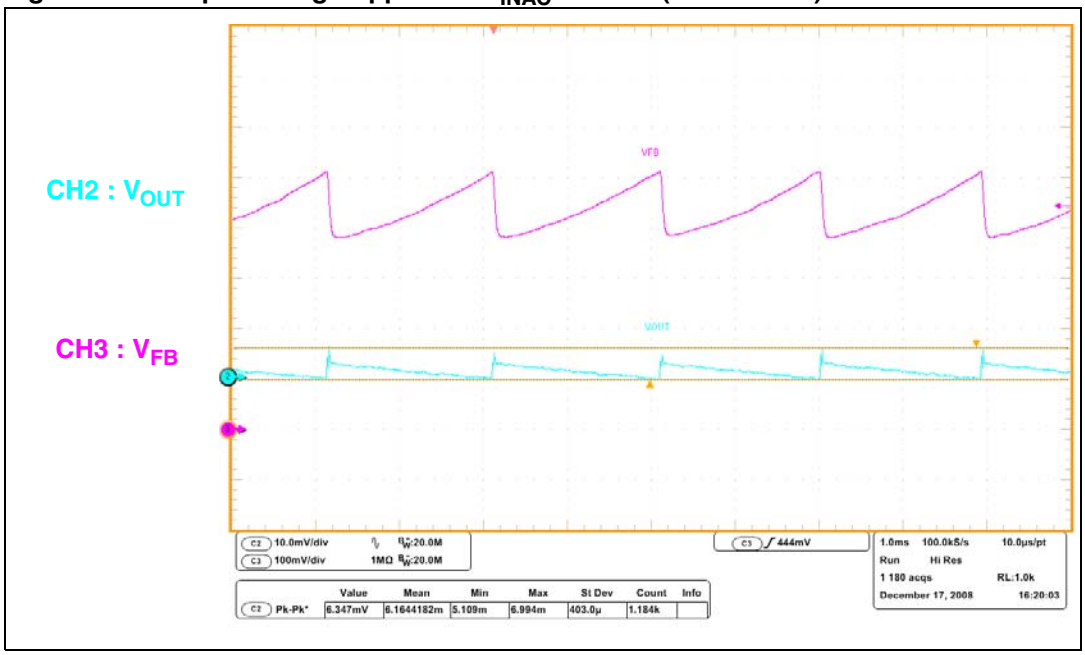



**Figure 13. Output voltage ripple 230 $V_{INAC}$ no load (burst mode)**

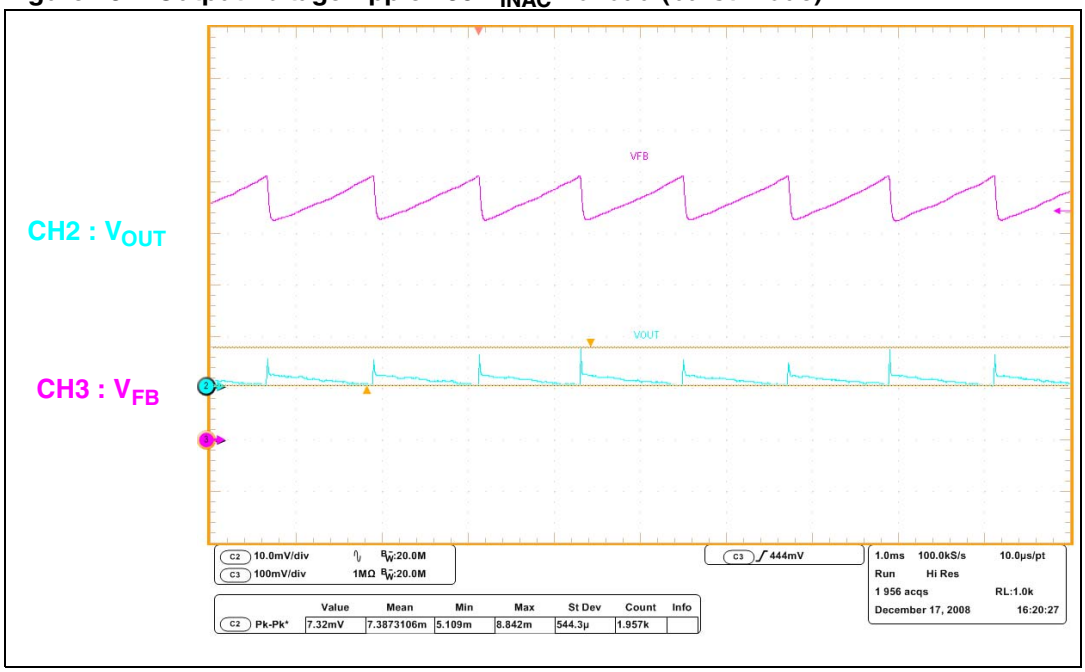


*Table 6* shows the value of the burst mode frequency ripple measured at different operating conditions. The measured ripple in burst mode operation is very low (always below 25 mV).

**Table 6. Burst mode-related output voltage ripple**

| $V_{IN}$ | No load (mV) | 10 mA load (mV) | 25 mA load (mV) |
|---|---|---|---|
| 90 | 9.11 | 13.4 | 11.3 |
| 115 | 8.72 | 11.1 | 11.9 |
| 230 | 8.84 | 12.3 | 15.1 |
| 265 | 8.86 | 12.2 | 15.8 |

## 3.3 Efficiency

The efficiency of the converter is measured in different load and line voltage conditions. In accordance with the ENERGY STAR® average active mode testing efficiency method, the measurements are done with different load values (full load, 75%, 50%, 25%) for each input voltage. The results are given in *Table 7*.

**Table 7. Efficiency**

| $V_{INAC}$ (VRMS) | Efficiency (%) | | | |
|---|---|---|---|---|
| | Full load (1 A) | 75% load (0.75 A) | 50% load (0.5 A) | 25% load (0.25 A) |
| 90 | 78.6 | 80.8 | 81.0 | 82.1 |
| 115 | 80.3 | 81.3 | 83.2 | 82.7 |
| 230 | 79.8 | 81.7 | 80.5 | 77.6 |
| 265 | 79.4 | 81.7 | 79.7 | 74.8 |

For better visibility, the results are also plotted in the diagrams that follow. *Figure 14* shows the efficiency versus $V_{IN}$ for the four different load values and *Figure 15* the value of the efficiency versus load for different input voltages.

**Figure 14. Efficiency vs. $V_{IN}$**

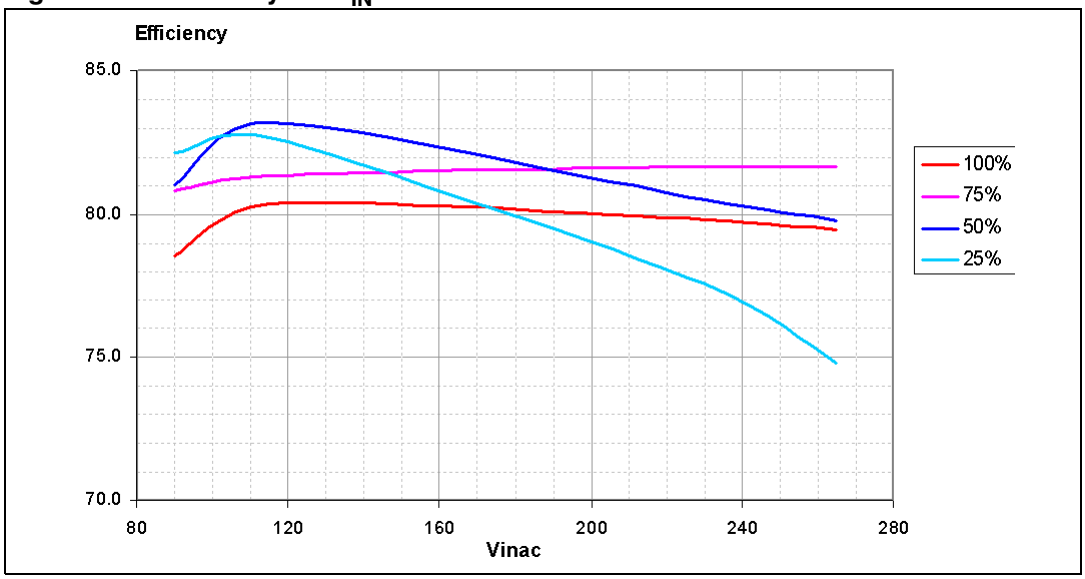
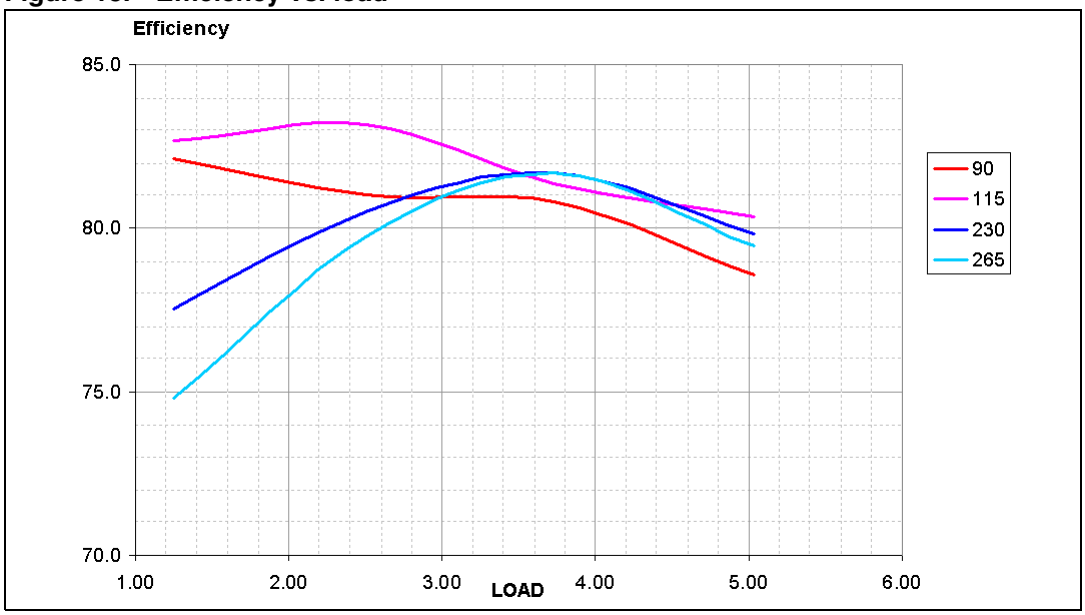



**Figure 15. Efficiency vs. load**




The active mode efficiency is defined as the average of the efficiencies measured in different load conditions. These different load conditions are: 25%, 50%, 75% and 100% of the maximum load. *Table 8* reports the active mode efficiency calculated from the measured values displayed in *Table 7*. For better visibility, the values of *Table 8* are also plotted in *Figure 16*. *Figure 17* reports the averaged efficiency value versus load (average is measured considering the efficiency at different input voltage).

Table 8. Active mode efficiencies

| $V_{INAC}$ ($V_{RMS}$) | Efficiency (%) |
|---|---|
| 90 | 80.6 |
| 115 | 81.9 |
| 230 | 79.9 |
| 265 | 78.9 |

Figure 16. Active mode efficiency vs. $V_{IN}$

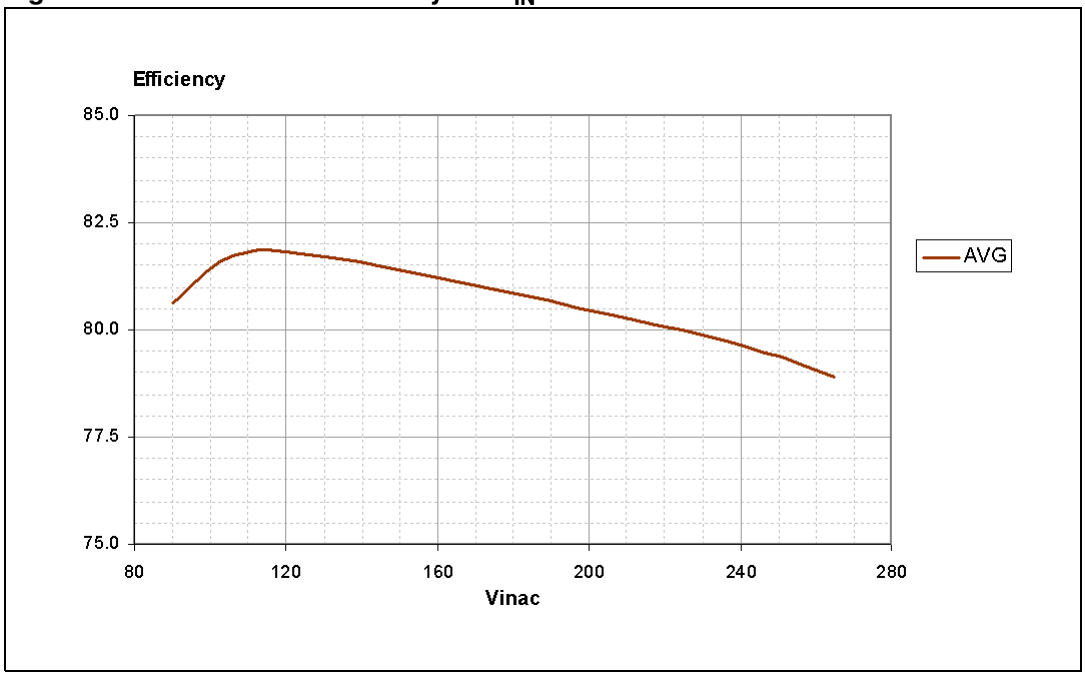
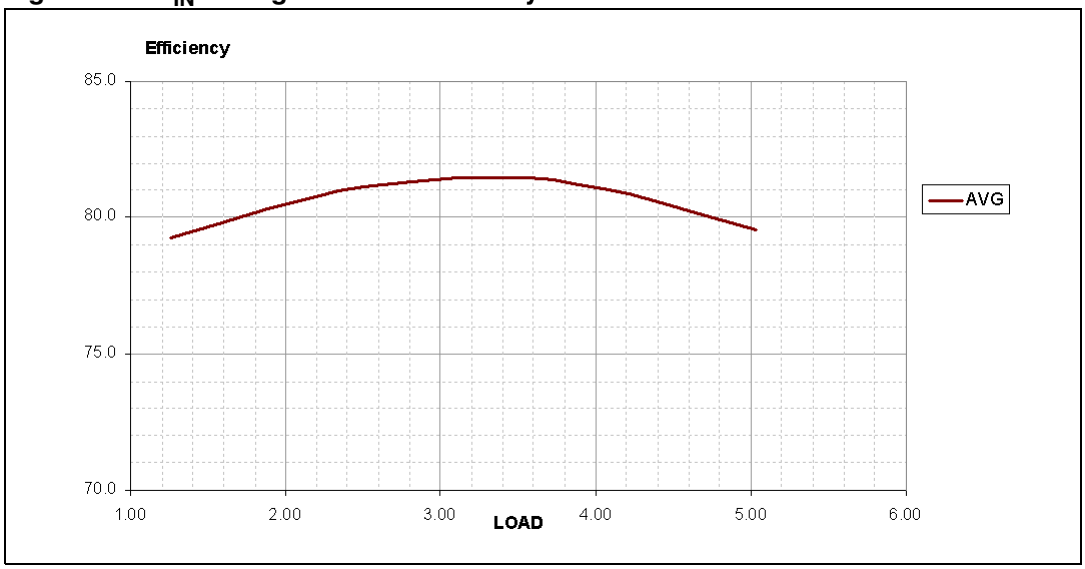



Table 9. Line voltage averaged efficiency vs. load

| Load (% of full load) | Efficiency (%) |
|---|---|
| 100 | 79.39 |
| 75 | 79.85 |
| 50 | 78.67 |
| 25 | 75.56 |

**Figure 17. $V_{IN}$ average vs. load efficiency**




In version 2.0 of the ENERGY STAR® program requirements for single voltage external AC-DC power supplies [2], the power supplies are divided into two categories: low voltage power supplies and standard power supplies according to the nameplate output voltage and current. In order to be considered a low voltage power supply, an external power supply must have a nameplate output voltage lower than 6 V and a nameplate output current higher than or equal to 550 mA.

The tables below report the EPA energy efficiency criteria for AC-DC power supplies in active mode for standard and low voltage models.

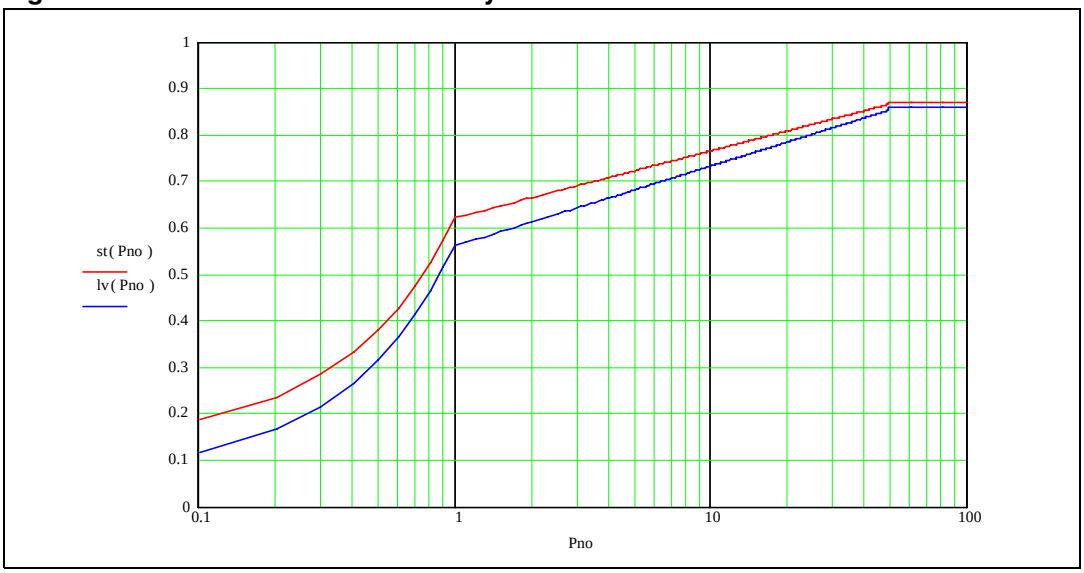
**Table 10. Energy efficiency criteria for standard models**

| Nameplate output power ($P_{no}$) | Minimum average efficiency in active mode (expressed as a decimal) |
|---|---|
| 0 to ≤ 1 watt | ≥ 0.48*Pno+0.140 |
| > 1 to ≤ 49 watts | ≥ [0.0626 * ln ($P_{no}$)] + 0.622 |
| > 49 watts | ≥ 0.870 |

**Table 11. Energy efficiency criteria for low voltage models**

| Nameplate output power ($P_{no}$) | Minimum average efficiency in active mode (expressed as a decimal) |
|---|---|
| 0 to ≤ 1 W | ≥ 0.497 *$P_{no}$ + 0.067 |
| > 1 to ≤ 49 W | ≥ [0.075 * ln ($P_{no}$)] + 0.561 |
| > 49 W | ≥ 0.860 |

**Figure 18. ENERGY STAR® efficiency criteria**




The ENERGY STAR® efficiency criteria are plotted in  where the red line indicates the criteria for standard models and the blue line the criteria for low voltage models.

The power supply presented here belongs to the low voltage power supply category and in order to be compliant with ENERGY STAR® requirements needs to have efficiency higher than 68.2%. For all the considered input voltages the efficiency (see *Table 8*), the results are higher than the recommended value.

## 3.4 Light load performance

The input power of the converter is measured in no load conditions for different input voltages. The results are reported in *Table 12*.

**Table 12. No load input power**

| $V_{IN}$ AC ($V_{RMS}$) | $P_{IN}$ (mW) |
|---|---|
| 90 | 13.50 |
| 115 | 13.70 |
| 230 | 21.20 |
| 265 | 25.00 |

In version 2.0 of the ENERGY STAR® program [2], the power consumption of the power supply when it is not loaded is also taken into account. *Table 13* reports the criteria for compliance.

**Table 13. Energy consumption criteria for no load**

| Nameplate output power ($P_{no}$) | Maximum power in no load for AC-DC EPS |
|---|---|
| 0 to = 50 W | < 0.3 W |
| > 50 watts < 250 W | < 0.5 W |

The board performance is much better than required, as the power consumption is approximately twelve times lower than the ENERGY STAR® limit. However, even if the performance seems to be disproportionately better than required, it should be noted that AC-DC adapter or battery charger manufacturers often have very strict requirements regarding no load consumption. For example, in the case of converters used as an auxiliary power supply in LCD TVs, the line filter is often the big line filter of the entire power supply, which significantly increases standby consumption.

Even if the ENERGY STAR® program has no other requirements regarding light load performance, to provide complete information the input power and efficiency of the STEVAL-ISA058V1 demonstration board in two other low load cases is also reported. *Table 14* and *Table 15* display the low load performance when the output load is 25 mW and 50 mW, respectively.

**Table 14. Low load performance 25 mW of load**

| $V_{IN\_AC}$ | $P_{OUT}$ (mW) | $P_{IN}$ (mW) | Eff. (%) | $P_{IN}$-$P_{OUT}$ (mW) |
|---|---|---|---|---|
| 90 | 25.0 | 44.3 | 56.4 | 19.3 |
| 115 | 25.0 | 45.3 | 55.2 | 20.3 |
| 230 | 25.0 | 56.1 | 44.6 | 31.3 |
| 265 | 25.0 | 59.4 | 42.1 | 34.4 |

**Table 15. Low load performance 50 mW of load**

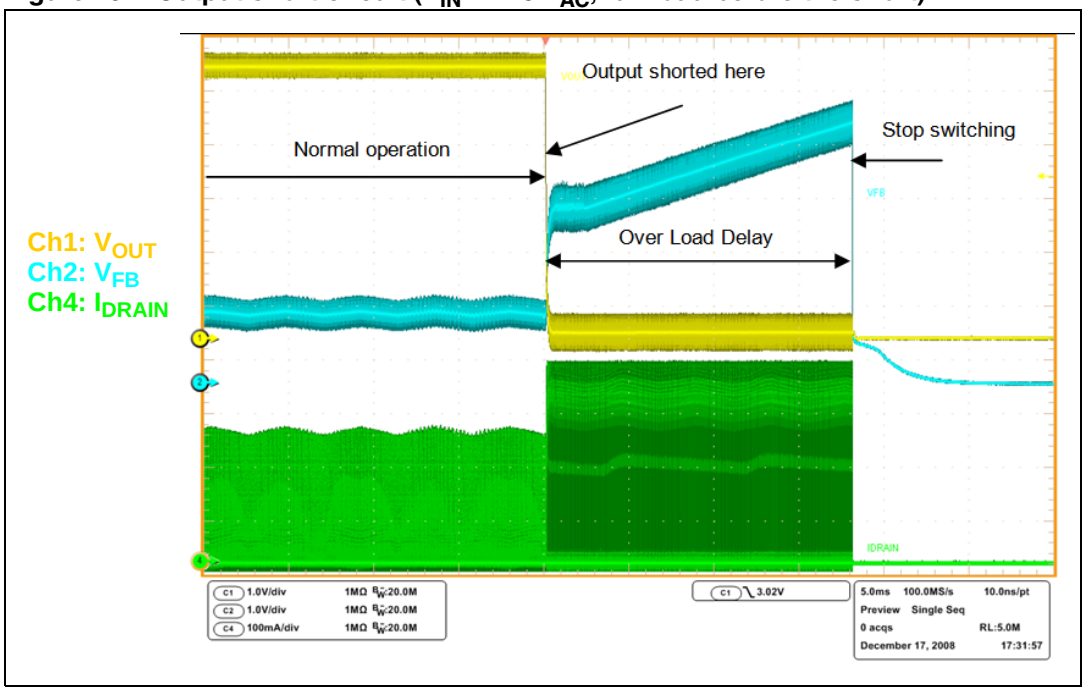
| $V_{IN\_AC}$ | $P_{OUT}$ (mW) | $P_{IN}$ (mW) | Eff. (%) | $P_{IN}$-$P_{OUT}$ (mW) |
|---|---|---|---|---|
| 90 | 50.00 | 74.3 | 67.3 | 24.3 |
| 115 | 50.00 | 75.7 | 66.1 | 25.7 |
| 230 | 50.00 | 86.1 | 58.1 | 36.1 |
| 265 | 50.00 | 95.5 | 52.4 | 45.5 |

## 3.5 Overload protection

The VIPER17L has several protection features, one of which protects against overload or output short-circuit. If the load power demand increases, then the output voltage decreases and the feedback loop reacts by increasing the voltage on the feedback pin. The feedback pin voltage rise increases the PWM current set point, augmenting the power delivered to the output until this power equals the load power. If the load power demand exceeds the converter power capability (which can be adjusted using the RLIM), the voltage on the feedback pin keeps rising but the power delivered remains stable. When the feedback pin voltage exceeds the $V_{FB\_lin}$ (3.3 V typ), the VIPER17L interprets this as a warning of an overload event. Before shutting down the system, the device waits for a time fixed by the capacitor of the feedback pin. In fact, if the voltage on the feedback pin exceeds the $V_{FB\_lin}$, then the internal pull-up is disconnected and the pin starts sourcing a 3 µA current that charges the capacitor connected to it. As the voltage on the feedback pin reaches the $V_{FB\_olp}$ threshold (4.8 V typ.) the VIPER17L stops switching and is not permitted to switch again until the $V_{DD}$ voltage goes below the $V_{DD\_RESTART}$ (4.5 V typ.) and rises up again to the $V_{DD\_ON}$ (14 V typ.).

*Figure 19* shows the behavior of the converter when the output is shorted.

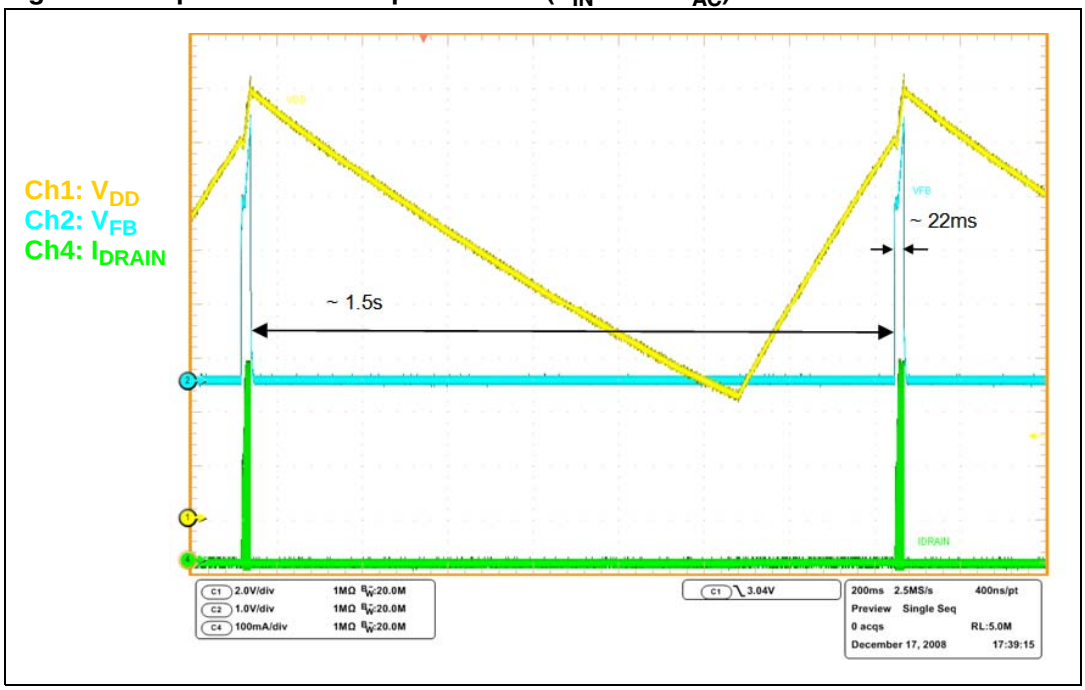
**Figure 19. Output short-circuit ($V_{IN}$ = 115 $V_{AC}$, full load before the short)**




If the short-circuit is not removed, the system switches into auto-restart mode. When a short-circuit is permanently applied on the output, the behavior displayed is a shorter MOSFET switching period, the converter attempts to deliver as much power as possible to the output and a longer period when the device does not switch and no power is processed.

The duty cycle of the power delivery is very low (around 1.5%) and the average power throughput is also very low (see *Figure 20*).

**Figure 20. Operation with output shorted ($V_{IN}$ = 115 $V_{AC}$)**

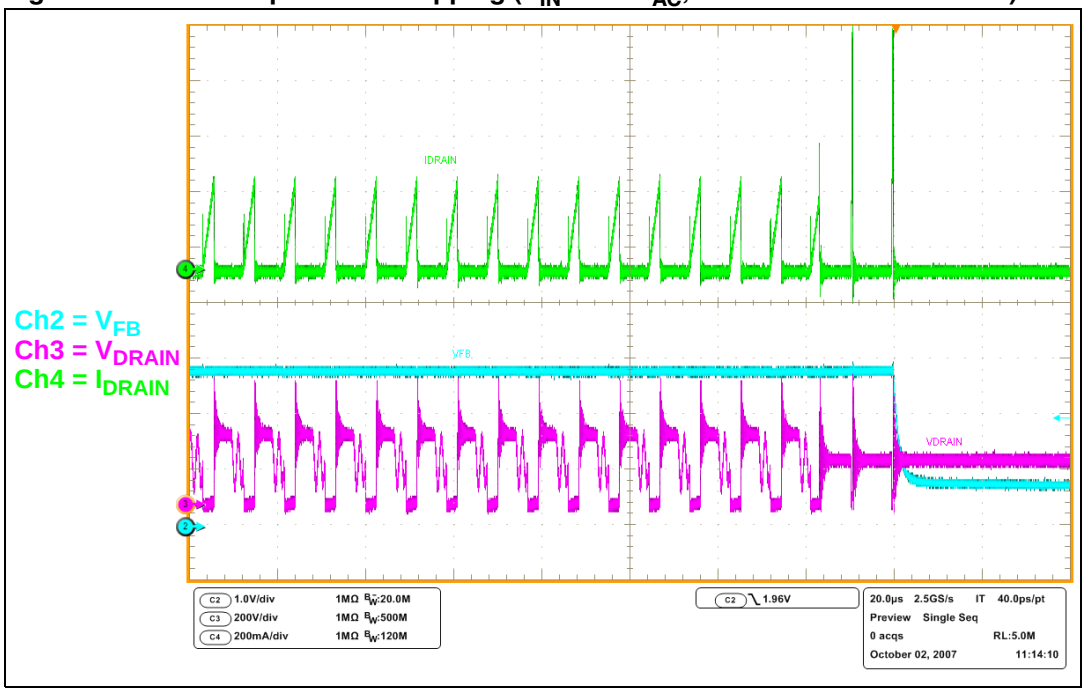



## 3.6 Secondary winding short-circuit protection

The VIPER17L is equipped with an adjustable first level of primary overcurrent limitation that switches off the power MOSFET if this level is exceeded. This limitation acts cycle-by-cycle and its main purpose is to limit the maximum deliverable output power. A second level of primary non-adjustable overcurrent protection is also present, fixed at 600 mA (typical value). If the drain current exceeds this 2nd OCP (second overcurrent protection) threshold, the device enters into a warning state. At the next cycle, the MOSFET is switched on and if the second level of overcurrent protection is exceeded again, the device assumes that a secondary winding short-circuit or a hard saturation of the transformer has occurred, so the MOSFET is no longer allowed to switch on and the device stops operating. In order to enable the MOSFET to switch on again, the $V_{DD}$ voltage must be recycled. That is, $V_{DD}$ must go down to $V_{DD\_RESTART}$, then rise up to $V_{DD\_ON}$. When the VIPER17L is switched on again ($V_{DD}$ equals $V_{DD\_ON}$), the MOSFET switching can restart. If the cause of the 2nd overcurrent protection activation is not removed, the device switches into auto-restart mode.

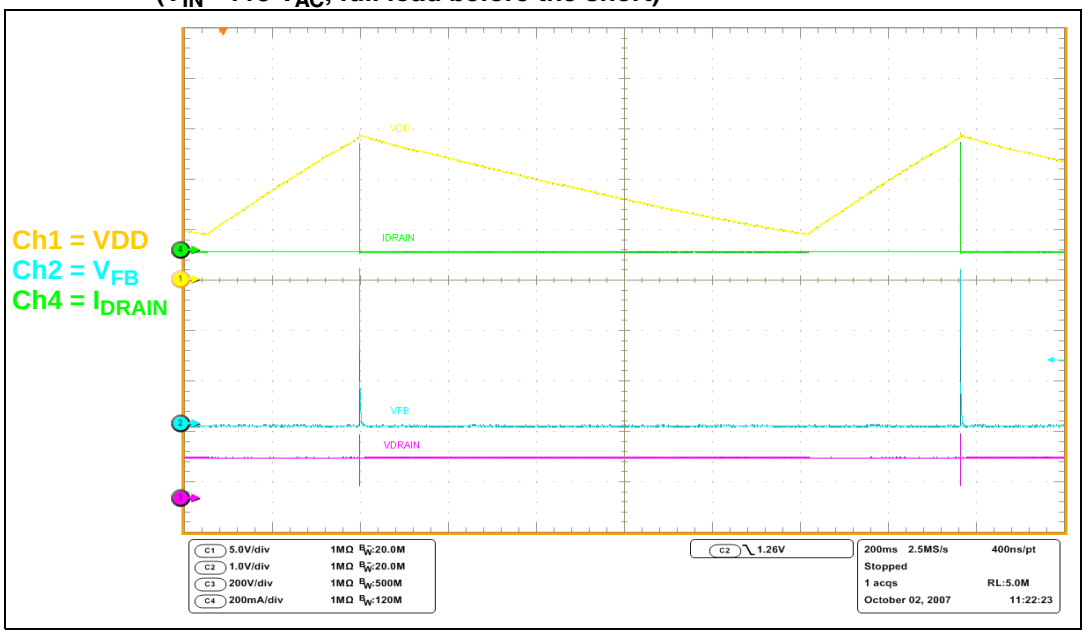
This protection was tested on the STEVAL-ISA058V1demonstration board. The secondary winding of the transformer was shorted in different operating conditions. *Figure 21* and *Figure 22* show the behavior of the system during the tests.

**Figure 21. 2nd OCP protection tripping ($V_{IN}$ =115 $V_{AC}$, full load before the short)**




In *Figure 21*, while the board is working in full load condition with an input voltage of 115 $V_{AC}$, the secondary winding is shorted. The short on the secondary winding leads to very high drain current, which activates the 2nd OCP protection. Without this protection the converter runs continuously up to the activation of the overload protection, which requires a few tens of milliseconds, with very high currents in the power section of the VIPER17L and in the transformer

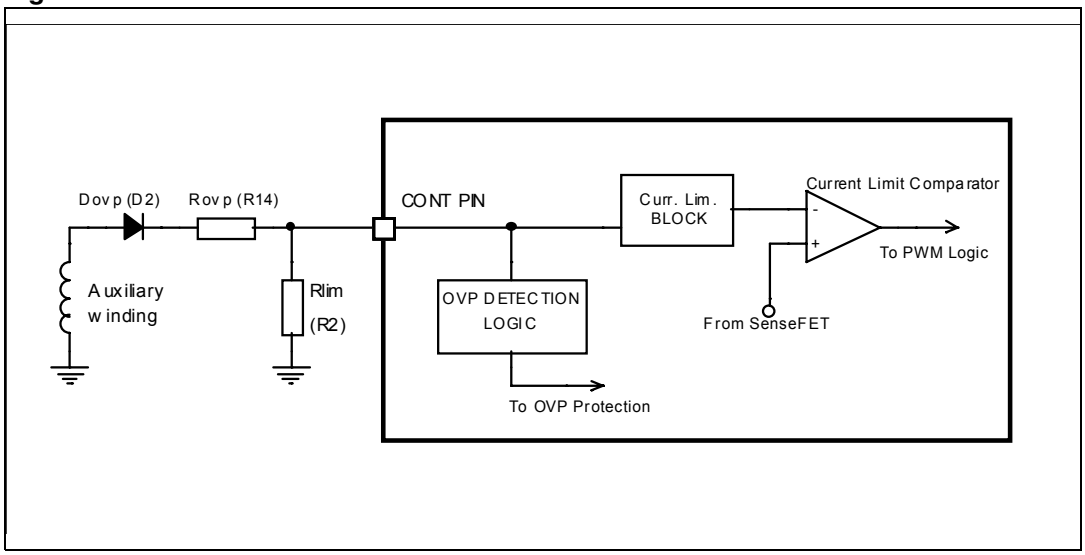
**Figure 22. Operating with secondary winding shorted restart mode ($V_{IN}$ =115 $V_{AC}$, full load before the short)**



## 3.7 Output overvoltage protection

Output over-voltage protection is implemented by monitoring the voltage across the auxiliary winding during the MOSFET off time through the D2 diode and the resistor dividers R3 and R14 (see schematic in *Figure 2*), which are connected to the CONT pin of the VIPER17L. If the voltage on the CONT pin exceeds the $V_{OVP}$ thresholds (3 V typ.), an overvoltage event is assumed and the device is no longer allowed to switch. To re-enable the operation, the $V_{DD}$ voltage must be recycled. In order to provide high noise immunity and avoid spikes erroneously triggering the protection, a digital filter is implemented so that the CONT pin has to sense a voltage higher than the $V_{OVP}$ for four consecutive cycles before stopping the operation.

**Figure 23. OVP circuit**




The value of the output voltage when the protection should be triggered can be set through proper selection of the resistor dividers R3 and R14. While R3 is selected with consideration to the maximum power that the converter has to manage, R14 is selected according to the following formula.

**Equation 2**

$$R_{OVP\_(R14)} = \frac{R_{LIM\_(R2)}}{3V} \cdot \left( \frac{N_{AUX}}{N_s} \cdot V_{OUT\_OVP} - V_{drop\_D_{ovp\_(D2)}} - 3V \right)$$

The protection is tested by disconnecting the opto-coupler from the feedback pin and light loading the converter. In this way the converter operates in open loop and delivers the most power possible. The excess power over the load charges the output capacitance, increasing the output voltage, since the OVP is tripped and the converter stops working.

In *Figure 24* it can be observed that the output voltage (Ch1, yellow waveform) increases and as it reaches the value of 6.6 V the converter stops switching. In the same figure the CONT pin voltage (Ch3, magenta waveform) and the drain current (Ch4, green waveform) are shown. The crest value of the CONT pin voltage tracks the output voltage. In *Figure 25*, the last switching cycles before the protection is triggered are reported in detail.

**Figure 24. OVP protection**

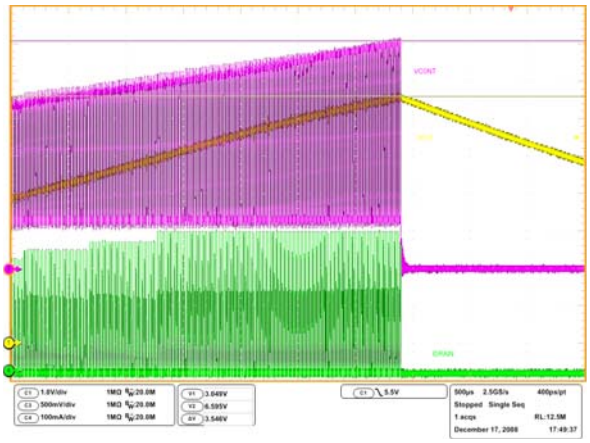
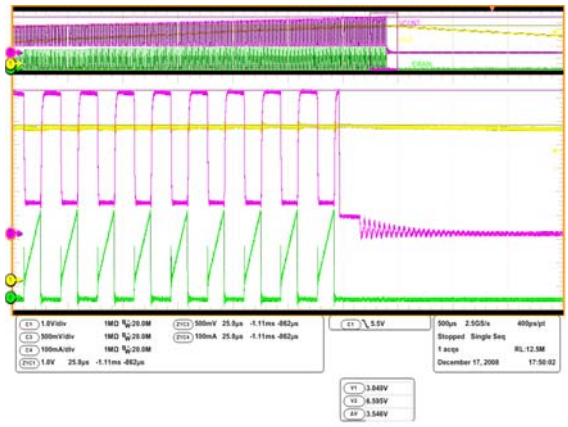


**Figure 25. OVP protection (detail)**



It is possible not to implement this protection, if it is not necessary. This is done by excluding diode D2 and resistor R14, thereby also reducing the number of components.

## 3.8 EMI measurements

A pre-compliant test in accordance with European standard EN55022 (Class B) is also performed. Results are displayed in *Figure 26* and *Figure 27*:

**Figure 26. 115 $V_{AC}$**

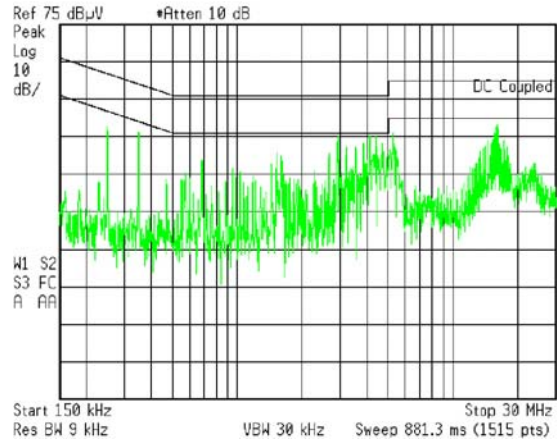
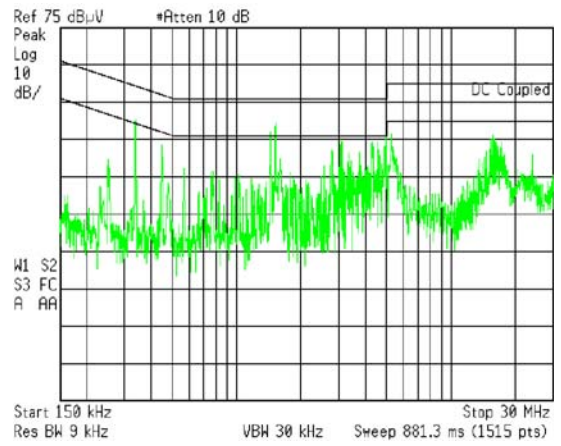



**Figure 27. 230 $V_{AC}$**



# 4 Conclusion

This application note examines the issue of minimizing the power consumption of a flyback converter in light load or no load conditions, and provides some practical design guidelines. The advantages of using the new VIPER17L device for this purpose are highlighted and an optimized demonstration board (order code STEVAL-ISA058V1) for standby consumption is presented. The measured performance is very good; for example, no load input power of 25 mW at maximum line (265 $V_{AC}$). The efficiency is also good and compliant with EPA 2.0 external power supply requirements.

# 5 References


- Cross regulation in flyback converter: analytic model (IEEE 1999)
- ENERGY STAR® program requirements for single voltage external AC-DC adapter (Version 2.0)
- VIPER17L datasheet

# 6 Revision history

Table 16. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 12-Jul-2009 | 1 | Initial release |