



## STUSBCD01B configuration and operation

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### Introduction

With the ever-increasing number of mobile devices adopting the USB bus as the standard communication port and source for recharging, a standardization of the characteristics of the charging devices and methods to detect them is required to optimize the performance of the charging process and reduce the risks of damaging standard USB ports.

The new USB battery charging specification provides rules and guidelines to follow when designing new USB architectures capable of battery charging and when defining new charging host ports. The specification also extends the range of current which can be drawn from a USB port.

In order to be able to distinguish between this new class of USB ports, standard USB host ports and dedicated chargers, the new specification also defines detection methods which must be used to determine the right amount of current the portable device can draw from the USB bus. This also guarantees backward compatibility with standard USB ports.

The STUSBCD01B is a USB charging detection IC developed on the base of the USB battery charging specification which can be easily added in new platforms to provide them with charging detection capability.

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## 1 STUSBCD01B description

The STUSBCD01B is the ideal solution for all mobile products using the USB bus for battery charging. It can be used in all USB architectures (low-, full- or high-speed) where the transceiver or the battery charger does not have smart charger detection. The STUSBCD01B implements two different detection methods to distinguish between dedicated chargers, charging host ports and standard host ports.

The device can be fully controlled through digital inputs (software detection mode) and is also able to perform the charger detection automatically when the battery voltage is too low to allow the application controller to be operative (hardware detection mode). A  $V_{BAT}$  referred open-drain output (detect) is available for direct control over the USB charging controller.

The STUSBCD01B also provides a clamping circuit which can be used to protect each USB IC connected to the USB  $V_{BUS}$  against overvoltage. The device requires few external components and its power consumption is extremely low.

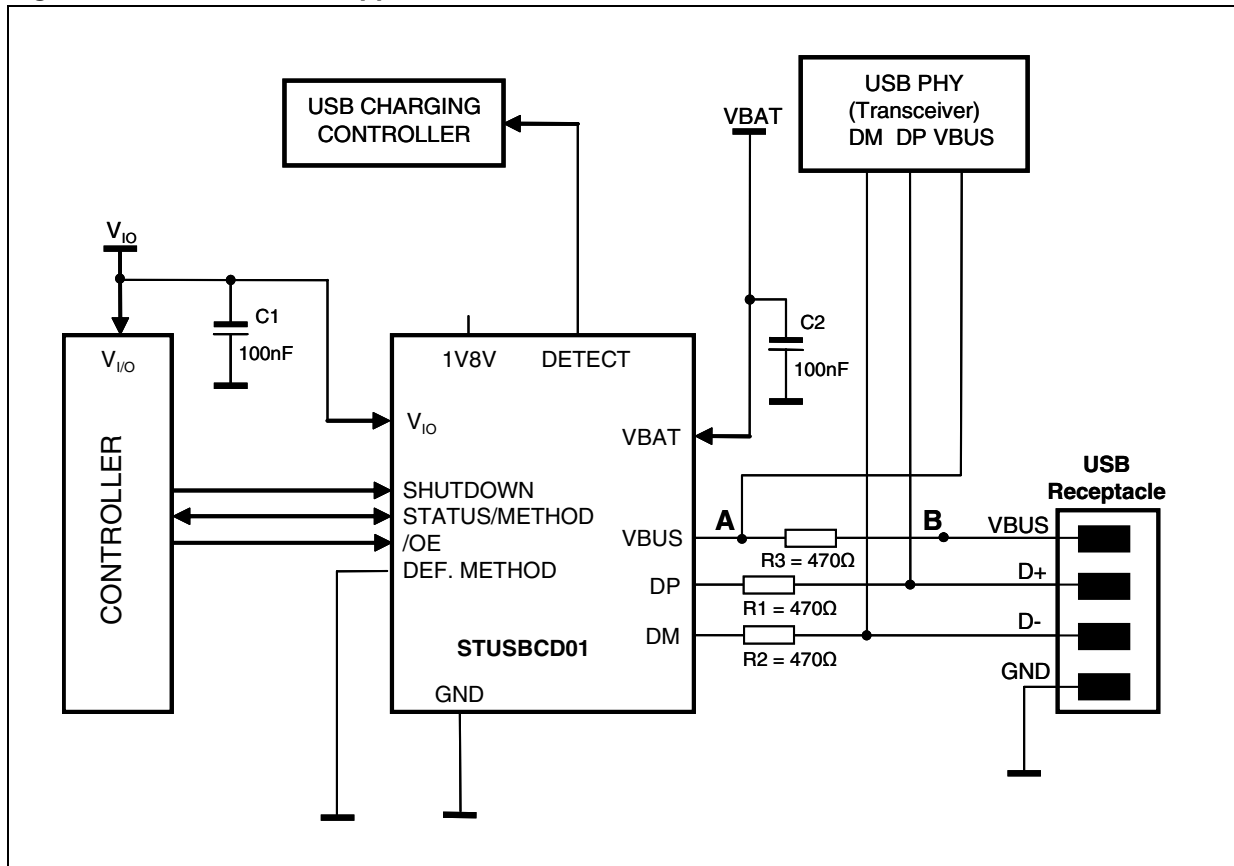
## 2 Application circuit

The STUSBCD01B requires only five external components:

- two capacitors to bypass the power supplies to ground
- one resistor for the  $V_{BUS}$  clamping circuit
- two series resistors on the DP/DM data lines

Figure 1 shows the typical application circuit for the STUSBCD01B.

Figure 1. STUSBCD01B application circuit



The STUSBCD01B can operate in two different modes: hardware detection mode, which does not require external control, and software detection mode. The user can choose between two different detection methods: dedicated method and current sink method. More details on each operating mode are provided in the following paragraphs. The operating mode is defined by the status of the digital I/Os,  $V_{BAT}$  voltage,  $V_{IO}$  voltage and default method input. See [Table 1](#) for a summary of all operating conditions.

Table 1. STUSBCD01B operating modes

$V_{BAT}$	$V_{IO}$	$V_{BUS}$	Shutdown	Status/method pin	Default method pin	Operating mode
< 2.2 V	-	-	-	-	-	Power down
> 2.2 V	Not present	Not present	-	-	-	Standby (no SW control)
> 2.2 V	Not present	Present	-	-	$V_{BAT}$	Active, HW detection, current sink method
> 2.2 V	Not present	Present	-	-	GND	Active, HW detection, dedicated method
> 2.2 V	Present	Present	$V_{IO}$	-	-	Standby (SW control)
> 2.2 V	Present	Not present	-	-	-	Standby (SW control)
> 2.2 V	Present	Present	GND	$V_{IO}^{(1)}$	-	Active, SW detection, current sink method
> 2.2 V	Present	Present	GND	GND <sup>(1)</sup>	-	Active, SW detection, dedicated method

1. The level of the Status/Method pin is read and latched on the falling edge of the shutdown input signal. When detection is finished, this pin becomes output.

SW = Software; HW = Hardware; "-" = Don't Care

The external resistors are very important to guarantee proper operation:

- The R1 and R2 series resistors are needed to mask the DP/DM pins' parasitic capacitance which is seen on the bus during high-speed USB communication. Removing these resistors might lead to degradation of USB high-speed signal quality and eye pattern failure. A value of 470  $\Omega$  is suggested in order to have optimal performance;
- The R3 resistor is required for the  $V_{BUS}$  clamping feature. If a value of 470  $\Omega$  is used, the  $V_{BUS}$  pin voltage (node A) never exceeds 6 V when USB  $V_{BUS}$  voltages up to 10 V are applied (node B). Every device needing overvoltage protection must be connected to the  $V_{BUS}$  pin of the STUSBCD01B as shown in [Figure 1: STUSBCD01B application circuit](#) (node A). Bus-powered devices cannot take advantage of this clamping feature because high currents drawn from the USB  $V_{BUS}$  voltage would cause a voltage drop over the R3 resistor. If this voltage drop is too high, the device's  $V_{BUS}$  comparators would read a false  $V_{BUS}$  level which might lead to malfunctioning. It is therefore strongly recommended to connect bus-powered USB devices directly to the USB receptacle's  $V_{BUS}$  line (node B).

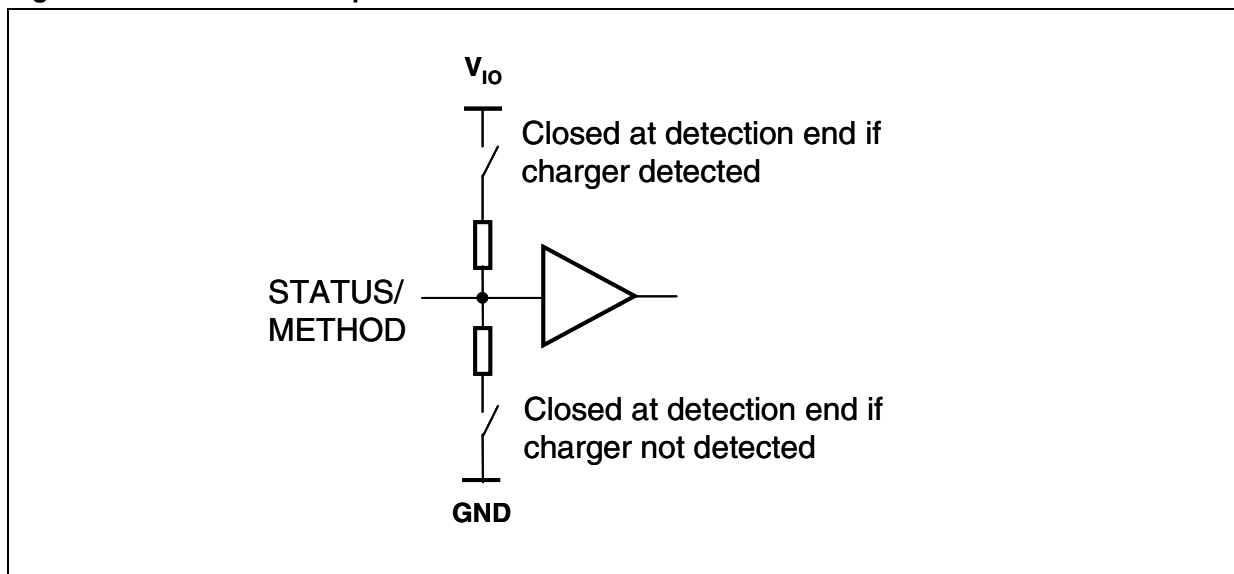
### 3 Interface and control pins

The STUSBCD01B is controlled and communicates with the controller using 5 I/Os. While shutdown and  $\overline{OE}$  are standard  $V_{IO}$  referred CMOS inputs, the remaining pins (Status/Method, default method and detect) have different characteristics.

#### 3.1 Status/method pin

This pin is either input or output depending on the operating conditions. It is input before the start of the detection process (used to set the detection method) and is output at the end of the detection process (it outputs the result of the detection). The application designer should program the application controller so that it sets the level of this pin ( $V_{IO}$  or GND) before the detection starts and maintains it during the falling edge of the shutdown signal (when the value is internally latched). The STUSBCD01B then outputs the detection result (at the end of detection) on this pin and therefore the application should read it after the maximum detection time has passed (see parameters  $T_{VBUS\_DET\_CS}$  and  $T_{VBUS\_DET\_DC}$  on the STUSBCD01B datasheet). The output structure is not a standard CMOS output but consists of a weak pull-up or a weak pull-down ( $\sim 10\text{ k}\Omega$ ) connected to the pin depending on the detection result as shown in figure 2.

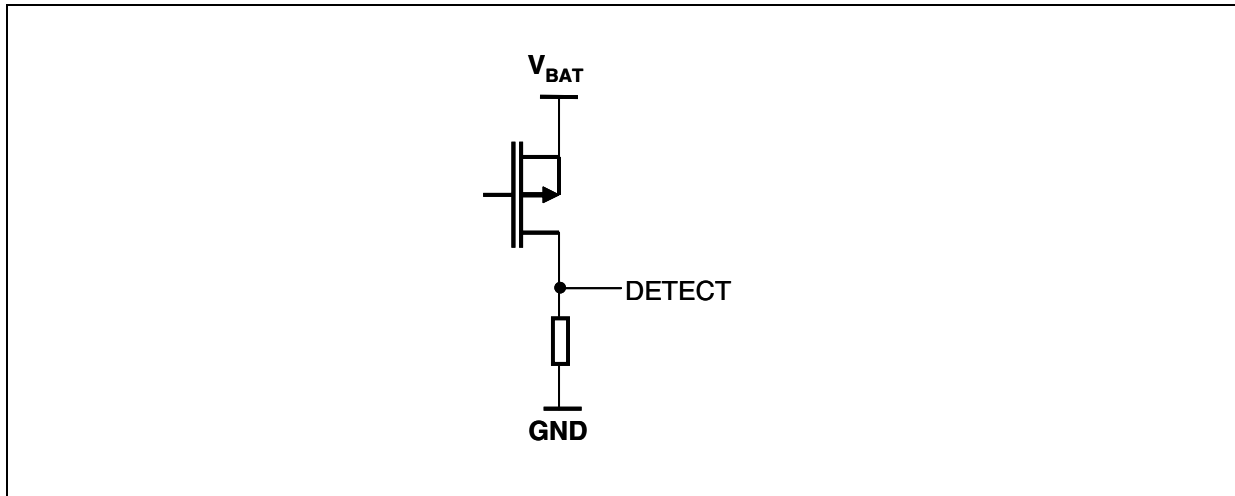
Figure 2. Status/method pin I/O



#### 3.2 Detect pin

This pin is an open-drain output which can be used as a  $V_{BAT}$  referred signal for the detection result. It is always enabled in hardware detection mode, while in software detection mode it is enabled/disabled by the  $\overline{OE}$  (active low) digital input. When enabled, the open-drain structure (see [Figure 3](#)) uses a PMOS transistor to pull the pin high ( $V_{BAT}$ ) when the detection is successful, otherwise an internal pull-down resistor ( $\sim 300\text{ k}\Omega$ ) keeps the output low.

Figure 3. Detect pin output



### 3.3 Default method pin

This pin is a  $V_{BAT}$  referred digital input. It is used to choose the detection method in hardware detection mode. Its level is ignored in software detection mode. It has to be driven high for the current sink method, low for the dedicated method.

*Note:* This pin must never be left floating to avoid increased power consumption.

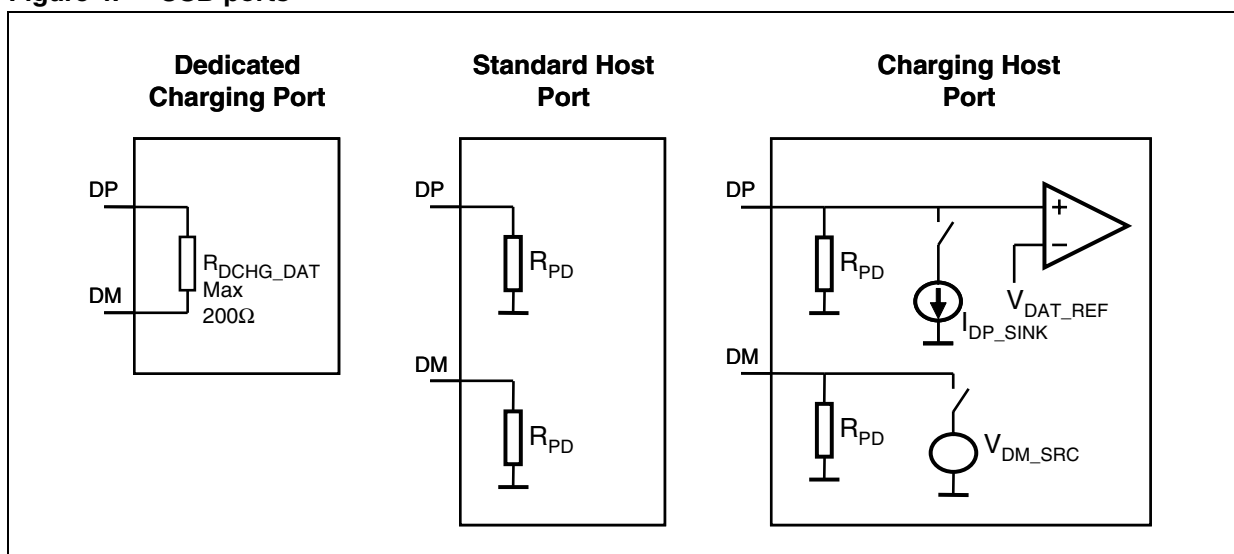
## 4 Current sink detection method

The STUSB01B's current sink detection method is suitable to detect both dedicated USB chargers (e.g. wall chargers) and charging host ports and distinguish them from standard USB host ports. See figure 4 for a simplified schematic description of these devices.

A dedicated charger typically shorts the USB DP/DM lines with a resistance not greater than  $200\ \Omega$ , while standard USB host ports have pull-down resistors connected to DP and DM ( $14.25 - 24.80\ \text{k}\Omega$ ).

A charging host port is normally not distinguishable from standard host ports but if it detects that an external device connected to its DP/DM lines is attempting to perform a detection, then it simulates a short between DP/DM, applying a voltage source to DM ( $V_{DM\_SRC} = 0.5 - 0.7\ \text{V}$ ) and a current sink to DP ( $I_{DP\_SINK} = 50 - 150\ \mu\text{A}$ ).

Figure 4. USB ports



After a stable  $V_{BUS}$  voltage has been detected, if the STUSB01B is enabled, the state machine starts the detection procedure which consists of the following steps:

- Phase 1: a current sink is connected to the DM pin ( $I_{DAT\_SINK} = 50 - 100\ \mu\text{A}$ );
- Phase 2: 5 ms (min) after DM current sink is connected, a voltage source ( $V_{DAT\_SRC} = 0.615 - 0.7\ \text{V}$ ) is applied to the DP pin and maintained for at least 100 ms;
- When the detection finishes, both the current sink and the voltage source are disconnected from the DP/DM pins. If the detection is successful, 40 ms (min.) after the end of the detection process, the detect and/or Status/Method outputs are pulled high.

The detection process can be interrupted if one of the following conditions is satisfied:

- $V_{BUS}$  voltage goes low;
- Shutdown input is pulled high (only in SW detection mode);
- Voltage levels on the DP/DM pins are different than expected.

The detection is successful if the DM pin is low during phase 1 and it goes high for at least 20 ms during phase 2.



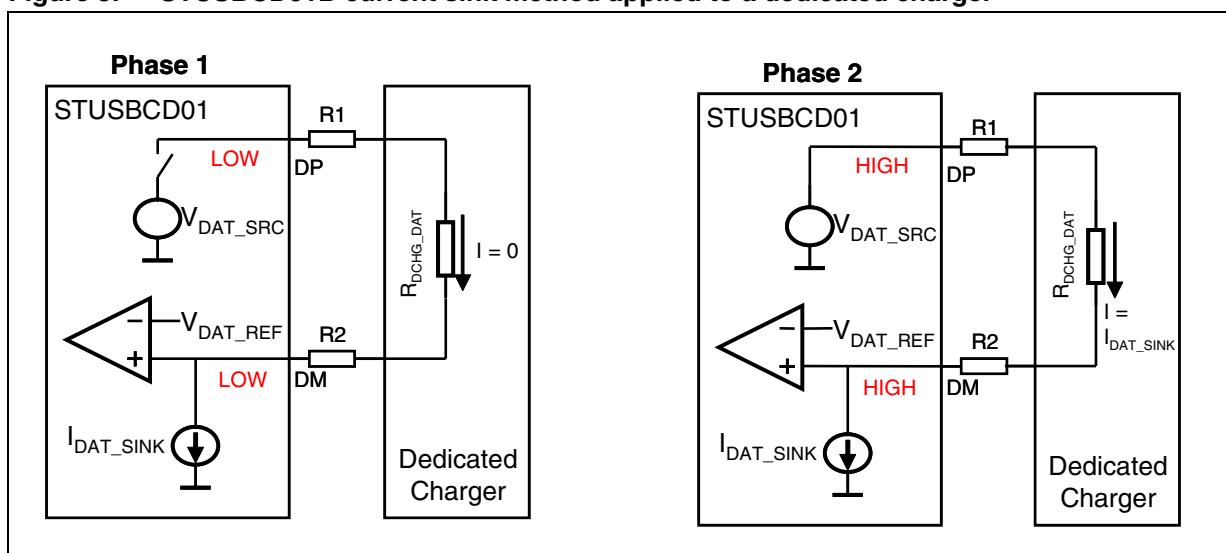
The DM check during phase 1 is needed to ensure that PS2 to USB adapters, pulling the DM line high, are not recognized as chargers. If a PS2 port is recognized as a charger, the high current drawn during the charging process could damage old PC motherboards which is why the detection is stopped if the DM line is high during this phase.

On the other hand, if DM is low during phase 1, phase 2 is entered. If a dedicated charging port is connected to the DP/DM lines, the voltage source connected to the DP line pulls the DM line over the  $V_{DAT\_REF}$  threshold because of the short-circuit between DP and DM inside the charging port. The same happens when a charging host port is connected. After detecting the  $V_{DAT\_SRC}$  voltage on the DP line, the charging host port connects a voltage source to the DM line which exceeds the  $V_{DAT\_REF}$  threshold.

Both ports allow the detection to be successful.

On the other hand, if a standard host port is connected to the DP-DM lines, the DM voltage during phase 2 is always low because of the pull-down resistor connected to it. This causes the detection to fail.

**Figure 5. STUSBCD01B current sink method applied to a dedicated charger**



The maximum value of  $R_{DCHG\_DAT}$  recognized as a charger can be easily calculated:  $V_{DAT\_SRC}$  minus the voltage drop on the series  $R1+R2+ R_{DCHG\_DAT}$  must not go below  $V_{DAT\_REF}$ . The worst-case conditions are obtained using the minimum value of  $V_{DAT\_SRC}$  and  $(R1+R2)$  and the maximum value for  $V_{DAT\_REF}$  and  $I_{DAT\_SINK}$ :

#### Equation 1

$$V_{DAT\_SRC(min)} - I_{DAT\_SINK(max)}(R1+R2+R_{DCHG\_DAT}) > V_{DAT\_REF(max)}$$

Therefore,

#### Equation 2

$$R_{DCHG\_DAT} < [(V_{DAT\_SRC(min)} - V_{DAT\_REF(max)})/I_{DAT\_SINK(max)}] - (R1+R2)_{(max)}$$

Considering 1% tolerance for  $R1$  and  $R2$  (470  $\Omega$  nominal) and min/max values taken from the USB battery charging specification and the STUSBCD01B datasheet, we obtain:

#### Equation 3

$$R_{DCHG\_DAT} < [(0.615-0.34)/(100*10^{-6})] - (470*2*1.01) = 1800.6 \Omega$$

This shows that even by adding R1 and R2 series resistors there is still enough margin over the dedicated charger’s detection ( $R_{DCHG\_DAT(max)} = 200 \Omega$  according to USB specs).

In the case of charging host ports,  $V_{DM\_SRC}$  is applied directly to R2 as shown in figure 6. The maximum value for R2 which allows a charging host port to be recognized as the charger after it applies  $V_{DM\_SRC}$  and  $I_{DP\_SINK}$  to DM and DP can be calculated as follows:

**Equation 4**

$$V_{DM\_SRC(min)} - R2 * (I_{DAT\_SRC(max)}) > V_{DAT\_REF(max)}$$

**Equation 5**

$$R2 < (V_{DM\_SRC(min)} - V_{DAT\_REF(max)}) / I_{DAT\_SINK(max)}$$

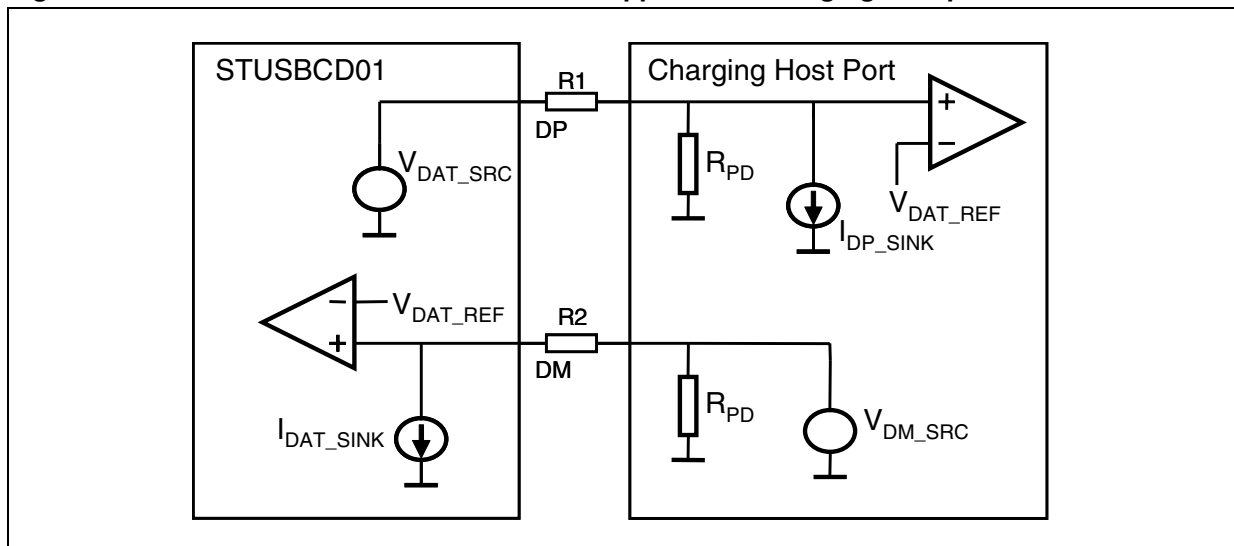
That is:

**Equation 6**

$$R2 < (0.5 - 0.34) / (100 * 10^{-6}) = 1600 \Omega$$

A value of 470  $\Omega$  (1%) is therefore well within limits.

**Figure 6. STUSBCD01B current sink method applied to a charging host port**



## 5 Dedicated charger detection method

The STUSB CD01B's current sink detection method is not able to distinguish between a charging host port and a dedicated charger. If the result of the current sink method detection is positive, the user may want to perform a new detection to understand what kind of charger is connected. The dedicated charger detection method is successful only if a dedicated charger is connected to the DP/DM lines. If the STUSB CD01B is enabled and configured to use this method, after a stable  $V_{BUS}$  voltage is detected, the state machine starts the following operations:

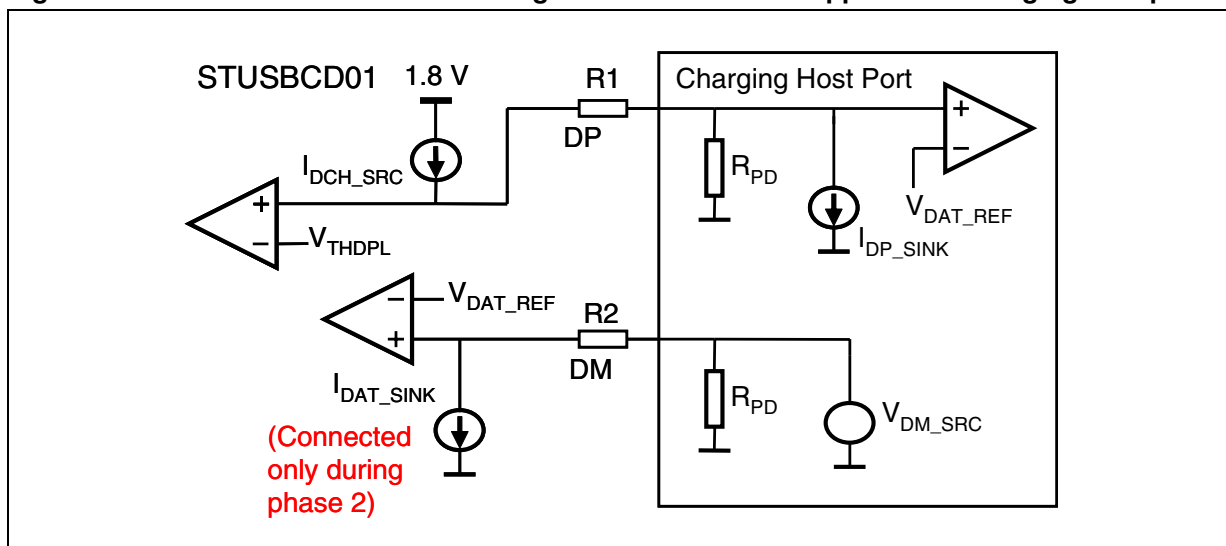
- Phase 1: a current source ( $I_{DCH\_SRC} = 15 - 30 \mu A$ ) is connected to the DP line. If at the end of this phase (100 ms min), both DP and DM lines are high, the detection proceeds to phase 2;
- Phase 2:  $I_{DAT\_SINK}$  current sink (same as in current sink method, 50 - 100  $\mu A$ ) is connected to the DM line for at least 40 ms.

If at the end of phase 2 both DP and DM are low, the detection is successful and detect and/or Status/Method outputs are pulled high.

If a standard host port is connected, the dedicated charger detection method stops at phase 1 because the pull-down resistor on the host side pulls the DM line low.

The case of a charging host port (CHP) is a little bit more complex. During phase 1, the CHP connects the  $I_{DP\_SINK}$  current sink to the DP line. This current sink is stronger than  $I_{DCH\_SRC}$  and therefore pulls the DP line low, causing the detection to fail (the voltage drop over the R1 resistor is negligible because of the low current flowing in it). If for some reason the voltage drop over  $I_{DP\_SINK}$  or R1 is higher than expected and the voltage at the STUSB CD01B's DP pin exceeds the  $V_{DAT\_REF}$  threshold, the state machine proceeds to phase 2 which fails because the DM line is driven high by  $V_{DM\_SRC}$  connected inside the HCP (the DM line is expected to be low during phase 2). This scenario is shown in figure 7.

**Figure 7. STUSB CD01B dedicated charger detection method applied to a charging host port**



The maximum value for the R2 resistor can be easily calculated:

### Equation 7

$$V_{DM\_SRC(min)} - R2 * (I_{DAT\_SINK(max)}) > V_{DAT\_REF(max)}$$

**Equation 8**

$$R2 < (V_{DM\_SRC(min)} - V_{DAT\_REF(max)}) / (I_{DAT\_SINK(max)})$$

**Equation 9**

$$R2_{(max)} = (0.5 - 0.34) / (100 * 10^{-6}) = 1600 \Omega$$

This result is consistent with the value in [Equation 6 on page 10](#).

In the case of a dedicated charger, the maximum DP/DM short resistance which is detected as a charger can be calculated as follows. During phase 1, the value is not significant as  $I_{DAT\_SINK}$  is off, therefore the resistor series ( $R1 + R_{DCHG\_DAT} + R2$ ) is connected to a high voltage on the DP side and is floating on the DM side. The voltage is high on both sides.

During phase one, the DM voltage is equal to the voltage drop over  $I_{DAT\_SINK}$ . This current sink is designed to have a maximum voltage drop, while in operation, of 150 mV. This value is lower than  $V_{DAT\_REF}$  so it is not critical. In order for the detection to be successful, the DP line must also be low during phase 2:

**Equation 10**

$$V_{IDAT\_SINK(max)} + I_{DAT\_SINK(max)} * [R_{DCHG\_DAT} + (R1 + R2)_{(max)}] < V_{THDPL(min)}$$

**Equation 11**

$$R_{DCHG\_DAT} < [(V_{THDPL(min)} - V_{IDAT\_SINK(max)}) / I_{DAT\_SINK(max)}] - (R1 + R2)_{(max)}$$

Considering 1% tolerance for R1 and R2 (470  $\Omega$  nominal) we obtain:

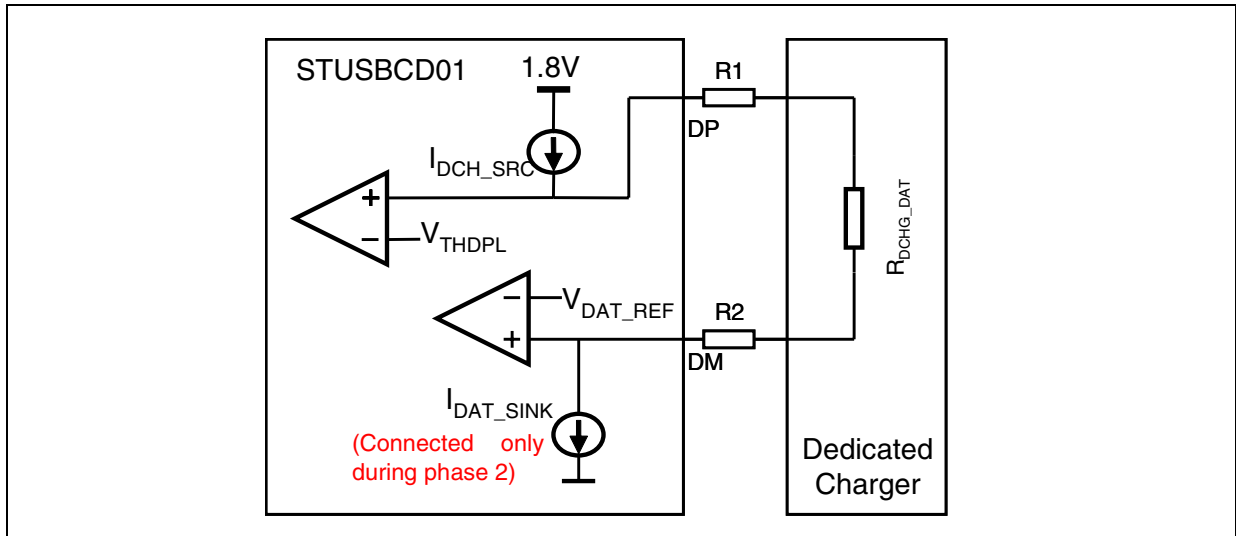
**Equation 12**

$$R_{DCHG\_DAT(max)} = [0.6 - 0.15] / (100 * 10^{-6}) - (470 * 2 * 1.01) = 3550.6 \Omega$$

This result is higher than the one found in [Equation 3 on page 9](#) for the current sink method. The actual result is even higher than this because in the above calculation we have considered a maximum value for the current flowing in the resistors higher than the real one. In fact, having two different current sources on the same branch causes the current to be set to the value of the weak current source (max 30  $\mu$ A).

This shows that both methods are quite robust and there is sufficient margin in the choice of the R1 and R2 resistor values.

Figure 8. STUSBCD01B dedicated charger detection method applied to a dedicated charger



## 6 Software detection and hardware detection

If the battery voltage is not high enough to wake up the application controller but is higher than 2.2 V, the STUSBCD01B can perform an automatic detection to allow the user to start charging the battery and make its voltage reach a value which will wake up the ASIC. This automatic detection is called hardware detection while the ASIC controlled detection is referred to as software detection.

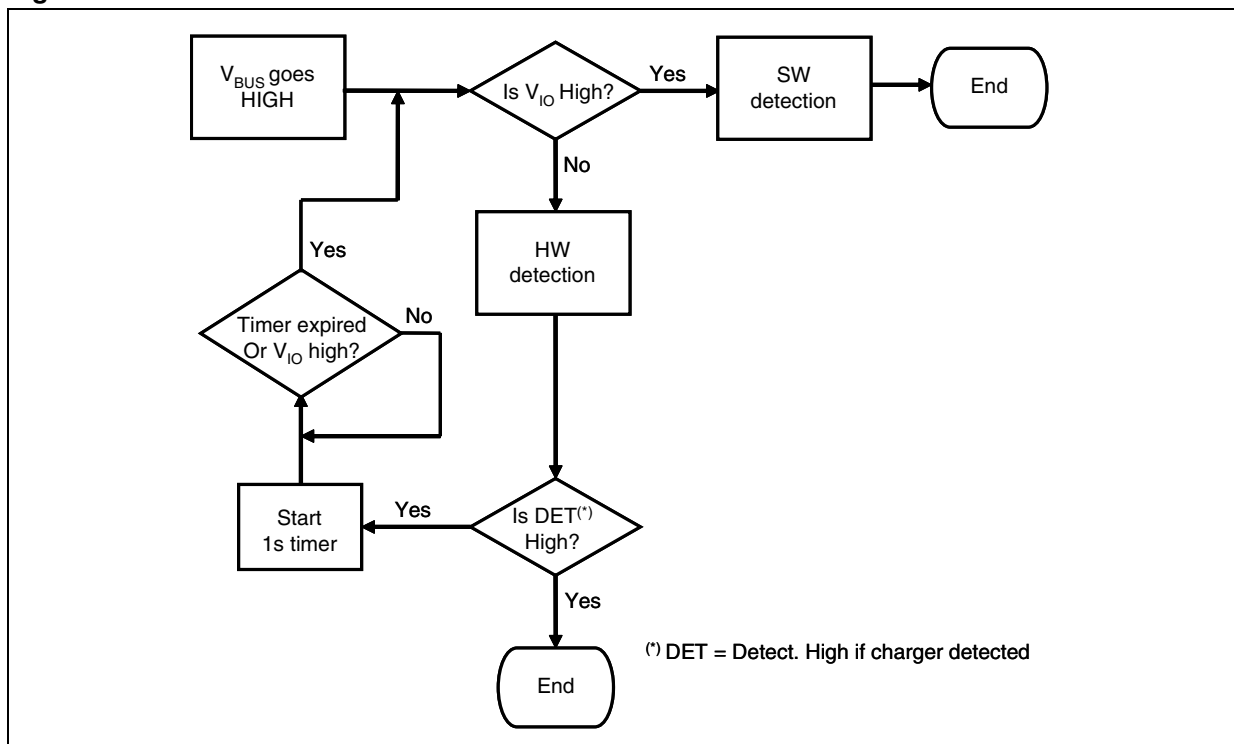
When the ASIC wakes up, the result of the hardware detection is available until the STUSBCD01B is reset.

The hardware detection mode is automatically entered when the  $V_{IO}$  voltage is not available. In this mode of operation all  $V_{IO}$  referred inputs are ignored and the detection method is set using the default method pin as described in [Table 1 on page 5](#).

As in the software detection mode, the start of the detection process is triggered by the  $V_{BUS}$  voltage going high. If the detection fails but the  $V_{BUS}$  voltage is still present, a new detection is performed once per second in an infinite loop as shown in the simplified flowchart in figure 9. This periodic detection is stopped only if:

- the detection result is positive;
- the  $V_{BUS}$  voltage drops under the  $V_{TH\_VBUS}$  threshold;
- the  $V_{IO}$  voltage goes high.

**Figure 9. HW/SW detection flowchart**



## 7 References

- STUSBCD01B datasheet
- USB battery charging draft specification rel.1.1.

## 8 Revision history

**Table 2. Document revision history**

Date	Revision	Changes
21-Sep-2009	1	Initial release.



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