AN2872
Application note

Super wide-range buck converter based on the VIPer16

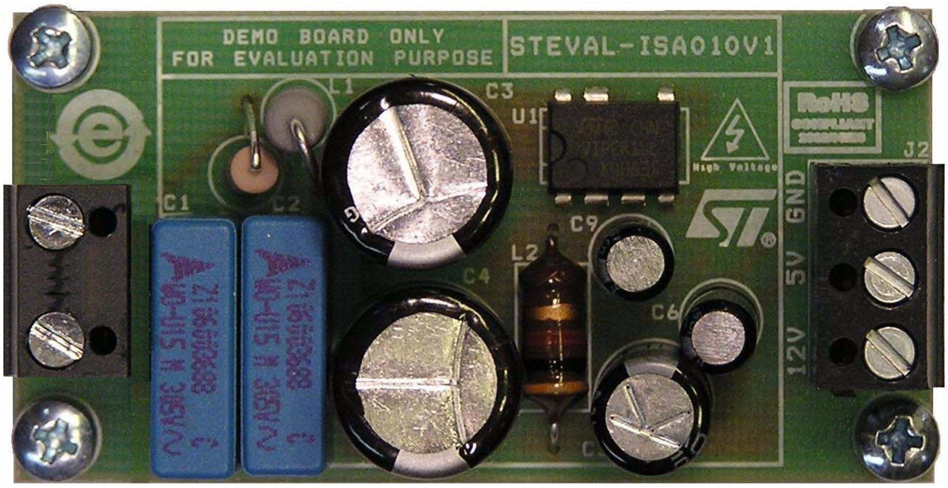
1 Introduction

This document describes the STEVAL-ISA010V1 demonstration board, which is designed as an example of a simple non-isolated auxiliary power supply for a range of input voltages from 85 VAC to 500 VAC.

There is an ever-increasing demand for small power supplies capable of working without voltage range limitations, even at nominal levels of 400 VAC and 415 VAC, respectively. The real voltage levels can reach 500 VAC (415 V + 20%). The major markets for this type of SMPS are home appliances and metering.

The new STMicroelectronics™ family of monolithic converters is well-suited for this range of input voltages, thanks to the 800 V avalanche-rugged MOSFET integrated within the same package with the control chip. This application note describes a low power SMPS with a buck topology using STMicroelectronics' VIPer16 fixed-frequency off-line converter as a main circuit. The VIPer16 device includes an 800 V rugged power switch, a PWM controller, programmable overcurrent, overvoltage, overload, a hysteretic thermal protection, soft-start and safe auto-restart after any fault condition removal. Burst mode operation at light load combined with the very low consumption of the device helps to meet standby energy-saving regulations. The significant benefit of this new chip derives from the jitter of the switching frequency and the possibility to supply the chip directly from the DC HV bus, so auxiliary supply is not mandatory. The VIPer16 is suitable for flyback or buck topologies, and thanks to an internal self-supply circuit it does not require an auxiliary supply.

Figure 1. The STEVAL-ISA010V1 demonstration board



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2 Main characteristics

The main characteristics of the SMPS are listed below:

- Input:
  - V_{IN}: 85 - 500 VAC
  - f: 45 - 66 Hz
- Output:
  - 12 V ± 10%
  - 5 V ± 4%
  - 150 mA total (5 V and 12 V output) output current for full input voltage range
- Standby: 96 mW at 230 VAC
- Short-circuit: protected
- PCB type and size:
  - FR4
  - Single side 70 µm
  - 27 x 45 mm
- Isolation: non isolated - N connected to output GND
- EMI: In accordance with EN55022 - class B
- EMC: Surge - IEC 61000-4-5 - 2 kV
- EMC: Burst - IEC 61000-4-4 - 8 kV

3 Description

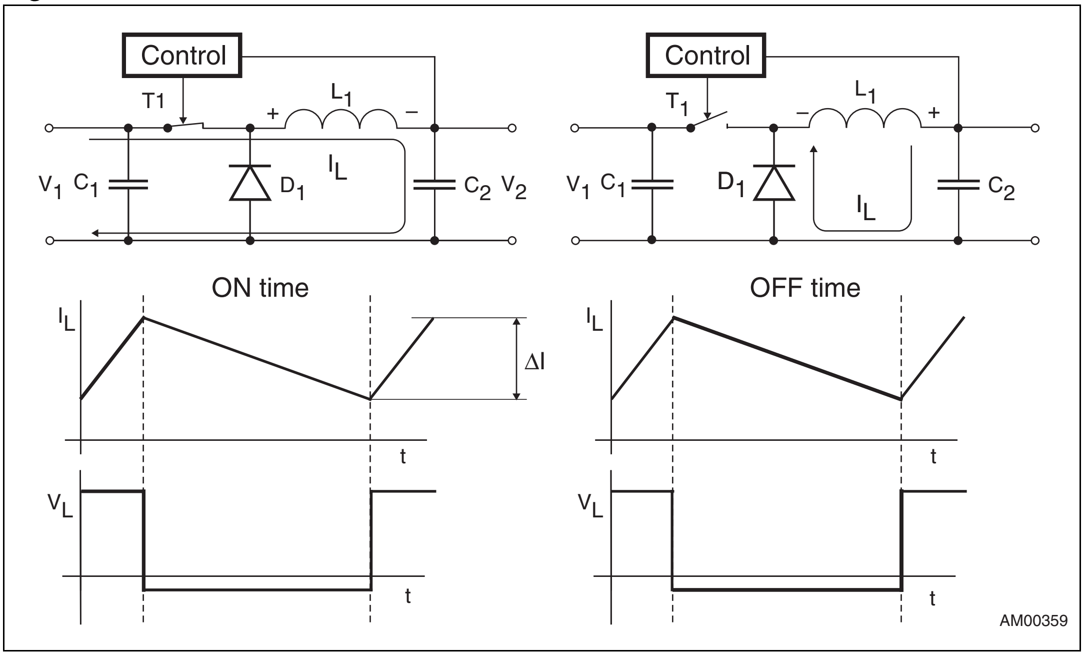
3.1 Theory of operation

The detailed calculation and principles of the buck converter for mains voltage operating range is described in *Section 6: References*:*1.* and *References*:*2.* The basic ideas and most important behaviors of the buck converter for mains applications is described in the chapters that follow.

3.1.1 The basic principle of the buck converter

The schematic of the buck converter is shown in *Figure 2*. During the ON time, the control circuit makes the high side switch T_1 conduct. The input DC voltage is connected to L_1 and output capacitor C_2 during the ON time. Assuming the voltage across C_2 is constant and the input voltage is constant, the voltage drop over L_1 is constant (V_1 - V_2). The constant voltage over the inductor causes a linear increase in the current through inductor L_1. The slope of the inductor current is proportional to the inductance of the inductor and the level of voltage drop over the inductor.

Figure 2. Buck converter schematic



After T_1 is switched OFF, the low side switch (diode D_1) conducts. If we assume, for simplification purposes, the voltage drop over the diode is zero, then the voltage drop over inductor L_1 is equal to the output voltage (voltage drop over C_2). Because the voltage across the inductor is different (compare ON time), the slope of inductor current is also different.

The behavior of a buck converter can be expressed by *Equation 1*.

Equation 1

$$\Delta I = \frac{(V_1 - V_2)t_{ON}}{L} = \frac{V_2 t_{OFF}}{L}$$

The regulator of the circuit measures the output voltage, compares it with the reference voltage and modifies the duration of the ON time to keep the output voltage constant.

In cases where the inductor current is operating in the continuous mode (the current does not cross zero at full load) the duty cycle can be obtained using *Equation 2*. This formula follows from *Equation 1*. Another method to obtain *Equation 2* is to consider the buck converter as a low pass filter (L_1, C_2), connected to a rectangular signal and that the low pass filter generates a mean value.

Equation 2

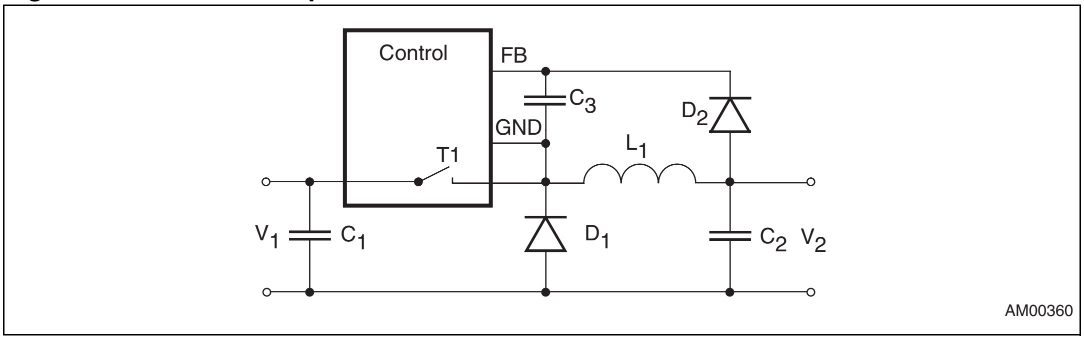
$$\delta = \frac{V_2}{V_1}$$

3.1.2 Practical aspects of a buck converter dedicated for mains and 3-phase input

The application of a mains or 3-phase buck converter using a simple monolithic device results in several special conditions. A few of the most important are described in the following paragraphs.

The operation of a buck converter such as that of the diagram in *Figure 2* requires an active high side switch. Therefore, the monolithic device (with integrated N-channel MOSFET) is also connected on the high side (between + of bulk capacitor and inductor). The GND of the controller connected to the source of the MOSFET refers to the high side of the inductor (see *Figure 3*). This wiring of circuit causes the feedback signal not to be directly sensed from the output due to the shift of the GND of output voltage and controller. Basically, there are two ways to move the information regarding the output voltage from the output to the controller. The first way is to apply an optocoupler between the output and the converter. The additional error amplifier and reference (typically TL431 or a simple Zener diode) must be assembled to drive the LED of the optocoupler. This method gives high precision of the output voltage level and low load regulation. However, it also increases the cost and space requirements. The second principle is to use a replica of the output voltage stored in the auxiliary capacitor during OFF time. The schematic in *Figure 3* shows the principle connection of the components. The auxiliary capacitor C_3 is charged during the OFF time from inductor L_1 to the same voltage level as capacitor C_2. It can be expected that the voltage drop over both capacitors (C_2 and C_3) must be equal. However, in real applications the voltages are not exactly the same. This difference is caused by the difference in the discharge current of capacitors, different capacitance and different voltage drop on diodes D_1 and D_2. An important effect of the variance of the voltage drop of C_2 and C_3 is the fact that only C_2 is charged during ON time. Due to this behavior it is possible to see a theoretically unlimited increase in the output voltage at light or no load, because the energy delivered during the ON time is higher than the total energy required by the load. Therefore, an additional load (resistor) or voltage limiter (Zener diode) is required on the output to protect the output capacitor and the load against overvoltage at light load.

Figure 3. **Standard implementation of a buck converter with a monolithic device**



The second important behavior of a buck converter dedicated for mains applications follows from the ratio between the input and output voltage. As derived from *Equation 2* the duty cycle is very low when the ratio between the input and output is very high. This also means the ON time must be very short. It is possible for the ON time required for correct operation to be shorter than the minimum ON time of the controller defined in the datasheet (the maximum duration of the minimum ON time of the VIPer16 is 450 ns. see *Section 6*: *3*). In this case the SMPS delivers more energy than the controller, which is compensated by the skipping of some pulses. This leads to higher ripple of the output voltage. This effect can be compensated by applying a higher inductance value and a lower switching frequency.

The last technical point discussed in this paragraph concerns the input bulk capacitor in applications dedicated to very high input AC voltage. In this case, the input voltage is up to 500 VAC. The DC voltage can reach voltage levels of up to 707 VDC. The input bulk capacitor must be able to sustain such voltage levels. Unfortunately, there are no standard aluminum capacitors on the market suitable for this voltage, so two capacitors connected in series have been applied.

The series connection of two capacitors has two effects on the voltage drop over each capacitor. The first is an influence over the tolerance of the capacitance and the second is an influence over the leakage current.

Regarding the tolerance, the worst case is that one capacitor's capacitance is at the maximum upper limit and the second at the lower limit. *Equation 3* defines the voltage distribution on each capacitor for this configuration:

Equation 3

$$V_{C1,\ C2} = \frac{V_{MAX}}{2}(1 \pm \delta)$$

where

V_{C1} is the voltage across the capacitor with higher capacitance (the sign "–" in the brackets)

V_{C2} is the voltage drop on the capacitor with lower capacitance (the sign "+" in the brackets)

V_{MAX} is the DC voltage bus

δ is the tolerance of the capacitors expressed as a percentage

If the voltage bus is 707 V and the tolerance is 20%, the highest possible voltage across the capacitor is 424 VDC. Therefore, for this voltage range, the use of 450 V capacitors is recommended.

The leakage current can cause additional unbalancing of the voltages and an increase in the voltage drop of one capacitor over the allowed limit. If the leakage currents of both capacitors are the same, no problem is presented. But in cases where there is a difference in leakage currents (which is the case in practical applications) this difference will cause the capacitor with lower leakage to be charged by this difference and the voltage over this capacitor will rise, risking exceeding the voltage defined in the datasheet. To avoid this effect, so-called balancing resistors are applied parallel to the electrolytic capacitors. The correct value of the balancing resistors can be calculated from the difference in the leakage currents and applied voltage. Unfortunately, the maximum difference in leakage currents is not defined. It is possible, however, that the calculations for the balancing resistors are available the technical documentation of some aluminum capacitor manufactures. An examination of these documents reveals that there is not a single method and each manufacturer uses different calculation methods, each of which unfortunately can give very different values. Technical notes describing the calculations of balancing resistors can be found in *Section 6: References*: *4*, *5*, *6*, *7.* Typically, the value of balancing resistors is in the range of hundreds of kΩ to several MΩ

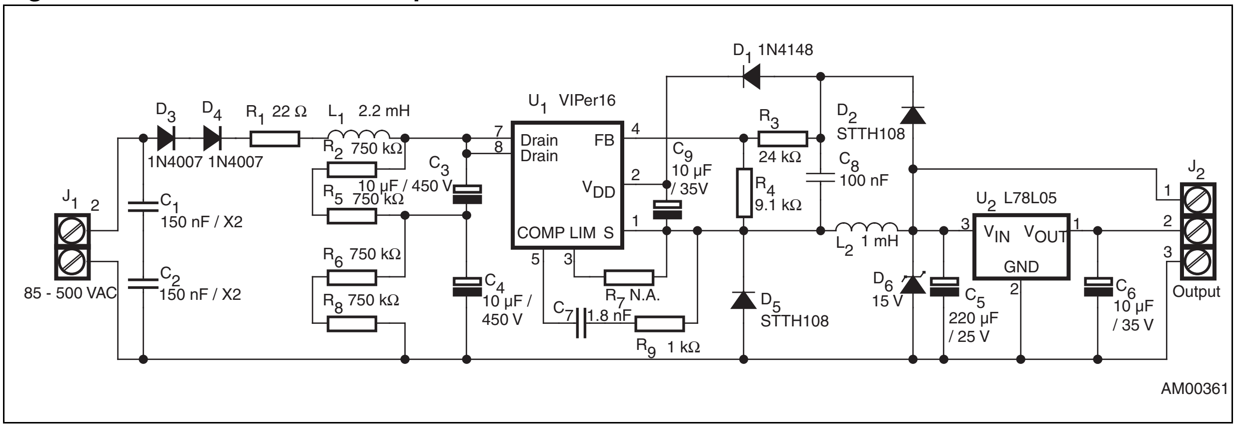
The drawback of using balancing resistors is the constant input load. The additional constant load caused by balancing resistors is mainly visible in the standby consumption and reduction of efficiency at low power SMPS. It is recommended to set the value of the balancing resistors to the maximum level, respecting the technical recommendations of the manufacturer of the aluminum capacitors selected.

3.2 Converter schematic

The schematic of the converter is shown in *Figure 4*. It consists of three sections: an input, a high voltage DC-DC converter and a linear regulator.

The input sections integrates a rectifier (D_3, D_4) of the input RMS voltage, an EMI filter (C_1, C_2, L_1, C_3, C_4), protection (R_1) and bulk capacitors (C_3, C_4) which store energy for the DC-DC converter when the input voltage is low. Because there is 500 VAC applied, which means a DC level over 700 V, the foil and electrolytic capacitors are connected in series. This is due to the fact that the standard foil safety capacitors are produced for 440 VAC, and the maximum DC voltage for standard electrolytic capacitors is 450 V. As the electrolytic capacitors have different leakage current, the balancing resistors (R_2, R_5, R_6, R_8) must be applied to guarantee that the voltage of each capacitor does not exceed the maximum rating even at maximum input voltage.

Figure 4. Schematic of the step-down converter based on the VIPer16L



The high voltage DC-DC section is a buck converter based on the VIPer16. It converts the input high DC voltage stored in capacitors C_3 and C_4 to output. The high side switch is a MOSFET integrated in the VIPer16. The low side switch of the buck converter is freewheeling diode D_5 (800 V / 1 A). The energy is saved in inductor L_2 and output capacitor C_5 during the ON time, when the MOSFET is conducting. The ON time (and consequently also the duty cycle) is very short (in the range several %) due to the high ratio between the input and the output voltage. During the OFF time, the MOSFET is switched OFF and diode D_5 conducts. Inductor L_2 is discharged to the output and to capacitors C_5 and C_8 through diodes D_2 and D_5. As the inductor L_2 is, during OFF time, connected to C_8 and C_5 the voltage drop over C_8 (used for feedback regulation) is similar to the output voltage level. Diode D_1 is also applied, though not mandatory for correct operation, to reduce the power consumption of the VIPer16 and consequently the standby power.

The VIPer16 operates in current mode. The FB pin is connected to the input of the error amplifier, the output of the error amplifier is visible on the COMP pin and is connected to the input of the built-in comparator for comparing the value from the output of the error amplifier to the drain current. The voltage level expected on the FB pin is 3.3 V. It is possible to see a rise in the output voltage at low or almost no load for this type of buck converter. This effect is caused by the capacitor C8 discharging faster than C5 at light or no load, and C5, moreover, is charged at every ON time. Consequently, the voltage over C8 is constant while the voltage over C5 rises. To protect the output capacitors and the load against overvoltage at light load, Zener diode D_6 is included, limiting the output voltage to 15 V. It is possible to use a simple resistive load instead of the Zener diode. The value of the minimum load depends on the complete configuration of the components. If linear regulator U_2 is not used, the value of the resistor is 12 kΩ (1 mA load), which could reduce the output voltage to a similar level as the Zener diode.

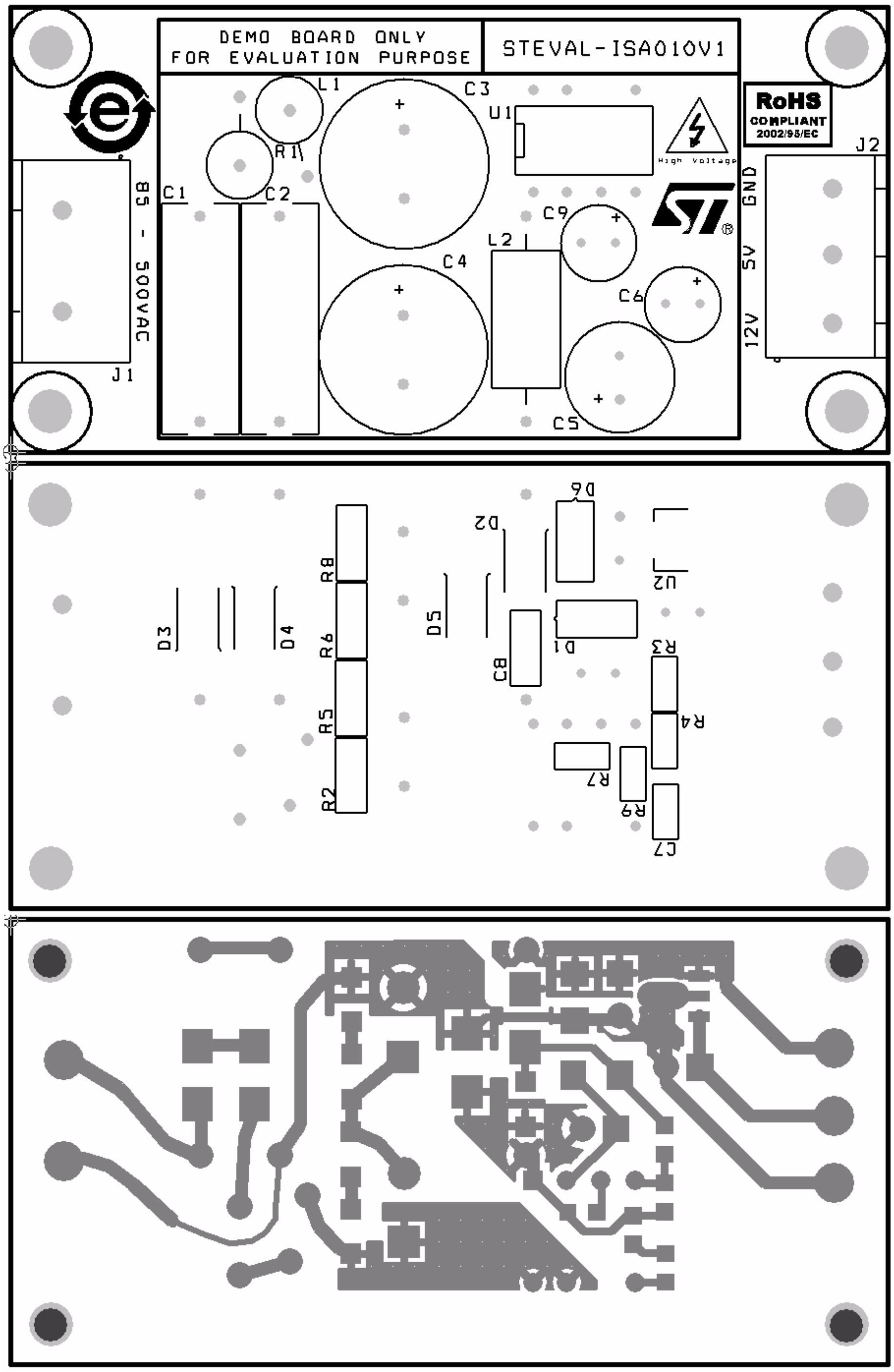
Regarding current limitation, other features of VIPer16 can be activated by assembling resistor R_7, but it is not originally assembled to allow the delivery of maximum power.

A simple linear regulator is also assembled, generating 5 V on the output as an option to complete the basic idea of generating 12 V and 5 V outputs. It should be highlighted that the VIPer16 can also directly generate a 5V output (instead of 12 V). The 5 V can be set by changing the value of resistor R_3 to 4.7 kΩ.

3.3 PCB

The converter is assembled on a single layer 65 x 33 mm, 70 µm, FR4 PCB. The PCB layout, position of the components and silk screen are illustrated in *Figure 5*. The part of the PCB dedicated to the converter itself is 43 x 27 mm in size.

Figure 5. PCB layout of the buck converter (top, bottom, bottom layout)



3.4 Bill of material

The components assembled on the board are listed in the *Table 1*.

Table 1. List of components

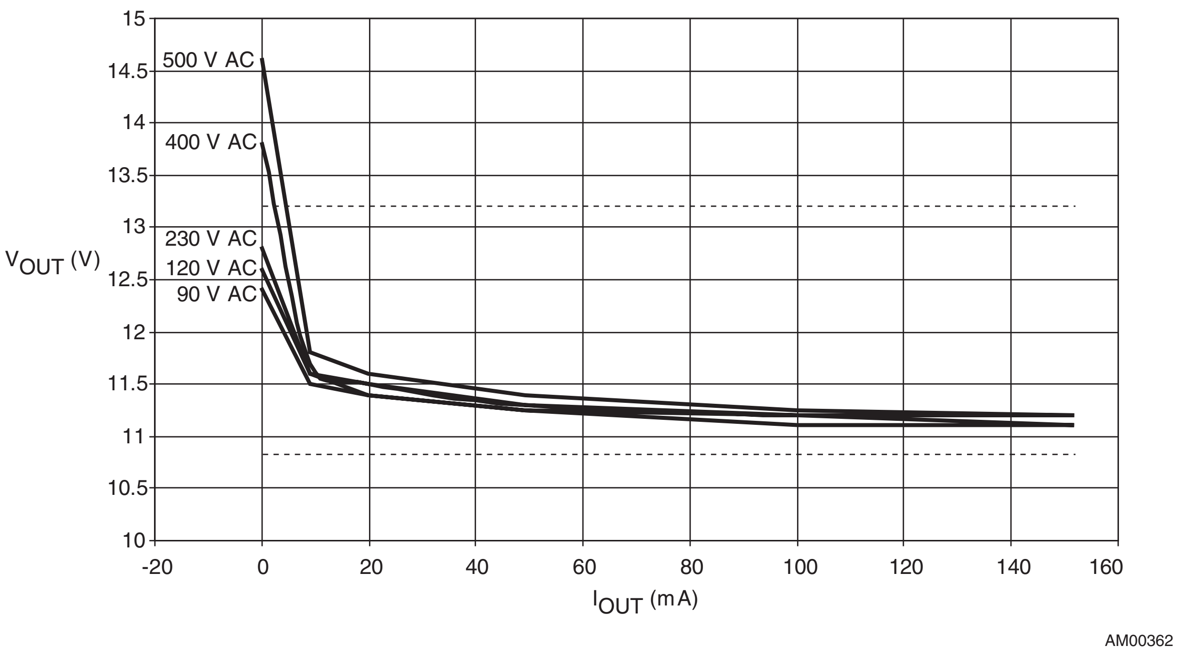
Ref.	Part type / value	Description	Size	Supplier
R_1	22 Ω / 2 W	Resistor		
R_2	750 kΩ / 5% / 0.25 W	Chip resistor	1206	
R_3	24 kΩ / 1% / 0.1 W	Chip resistor	0805	
R_4	9.1 kΩ / 1% / 0.1 W	Chip resistor	0805	
R_5	750 kΩ / 5% / 0.25 W	Chip resistor	1206	
R_6	750 k Ω / 5% / 0.25 W	Chip resistor	1206	
R_7	N. A.	Chip resistor	0805	
R_8	750 kΩ / 5% / 0.25 W	Chip resistor	1206	
R_9	1 kΩ / 5% / 0.1 W	Chip resistor	0805	
C_1	150 nF / 305 VAC / X2	Foil capacitor	18 x 6 x RM15	Epcos - B32922C3154M
C_2	150 nF / 305 VAC / X2	Foil capacitor	18 x 6 x RM15	Epcos - B32922C3154M
C_3	10 µF / 450 V	Aluminium capacitor	R12.5 RM 10	
C_4	10 µF / 450 V	Aluminium capacitor	R12.5 RM 10	
C_5	220 µF / 25 V	Aluminium capacitor	R8 RM 3.8	
C6	10 µF / 35 V	Aluminium capacitor	R5 RM2.5	
C_7	1.8 nF / 50 V	Chip capacitor	0805	
C_8	100 nF / 50 V	Chip capacitor	0805	
C_9	10 µF / 35 V	Aluminium capacitor	R5 RM2.5	
L_1	1 mH / 200 mA	Inductor		
L_2	1 mH / 300 mA	Inductor		
D_1	1N4148	Silicon diode	SOD80	
D_2	STTH108	Ultrafast diode	SMA	STMicroelectronics
D_3	1N4007	Silicon diode 1 A / 1 kV	MELF	
D_4	1N4007	Silicon diode 1 A / 1 kV	MELF	
D_5	STTH108	Ultrafast diode	SMA	STMicroelectronics
D_6	15 V	Zener diode	SOD80	
U1	VIPer16L	Converter	DIP 7	STMicroelectronics
U_2	L78L05	Regulator	SOT89	STMicroelectronics

4 Experimental results

4.1 Load regulation and output voltage ripple

The 12 V output is affected by the load due to the effects described in Chapter 3.1.2 and 3.2. The real load regulation of the 12 V output (linear regulator U_2 is not assembled) for different input voltages is visible in Figure 6.

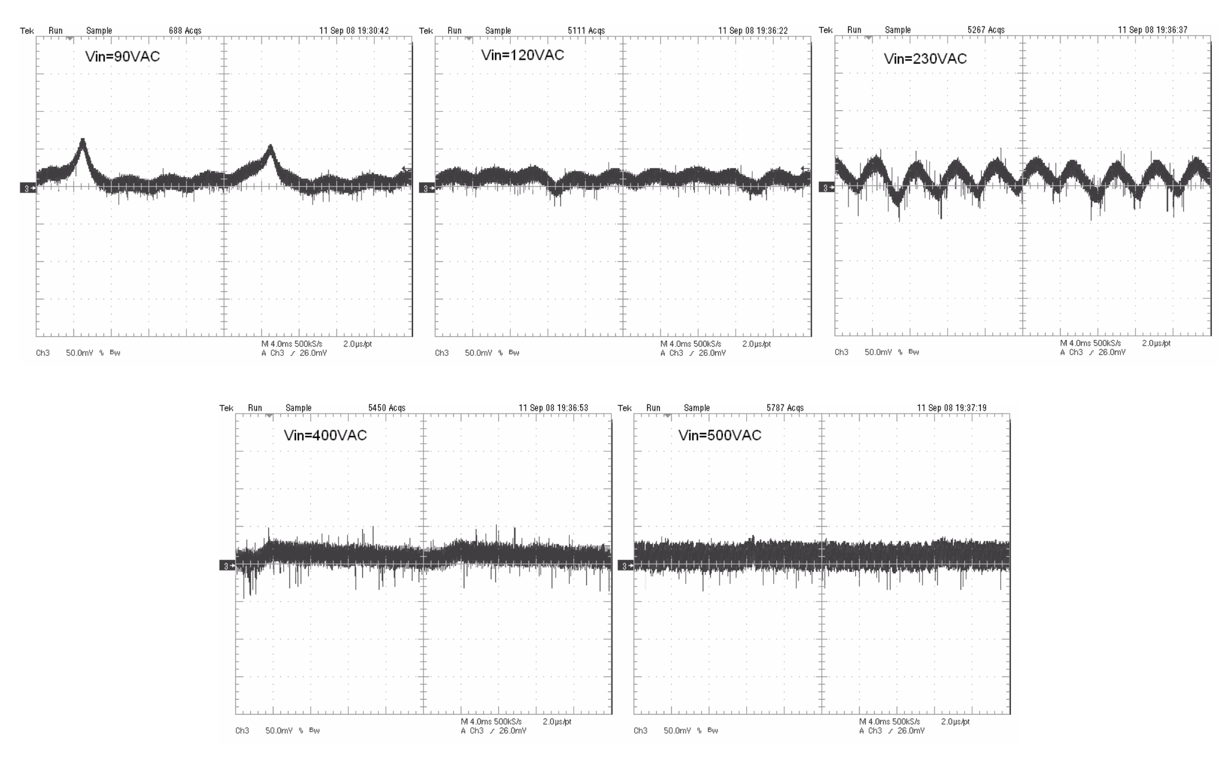
Figure 6. 12 V output load regulation for different output loads and input voltage levels (linear regulator U_2 not assembled)



The flatness of the load characteristic can be influenced mainly at light load by setting a fixed load (a resistor instead of Zener diode D_2) or assembling a linear regulator to represent light load. The behavior of the load characteristic can be influenced by the value of the auxiliary capacitor C_8 and total value of resistance of R_3 and R_4.

The output voltage ripple is very low and presents a good opportunity to use smaller capacitors with higher ESR and lower capacitance. The data measured with the demonstration board are shown in Figure 7. It is possible to see the higher 100 Hz ripple at 90 VAC on the input. This ripple can be avoided by increasing the capacitance of the input capacitors.

Figure 7. Output voltage ripple for different input voltages

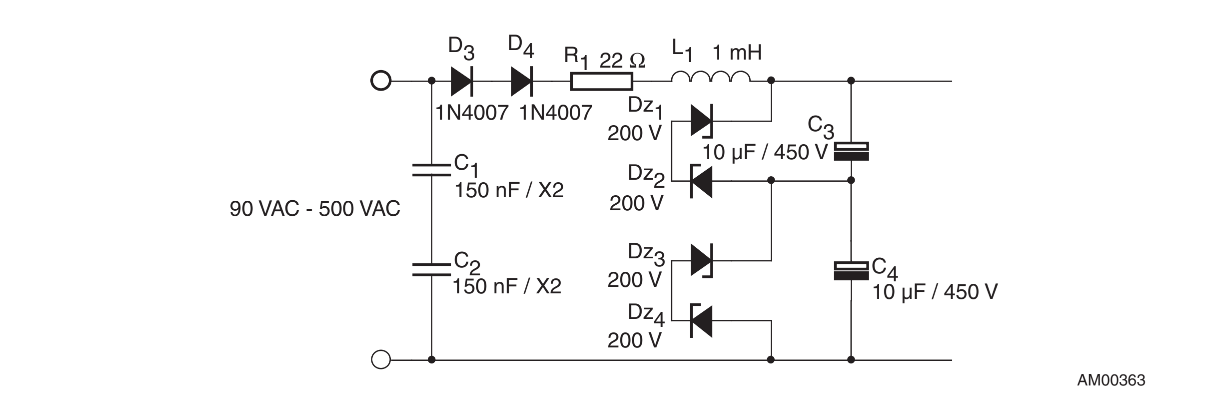


4.2 Standby

The VIPer16 is designed to operate without any external power source. The device can be supplied, thanks to its very low consumption, directly from an internal high voltage circuit (see *Section 6: References*: *3*). A major benefit of this feature is a reduction of the external component count, as well as the possibility to generate output voltages that are below voltage lockout. The buck converter based on the VIPer16 can directly generate, with a simple inductor, 5 V (for example). On the other hand, as this method of self-supply is based on the resistive principle, this method of supply increases power losses, which is mainly visible in standby power losses. If low standby power losses is a priority, it is suggested to apply an additional diode (D_1 in *Figure 4*) in cases where the output voltage is higher than 12.5 V. Diode D_1 allows the VIPer16 to be supplied from reflected voltage (C_8), used for feedback and consequently to reduce standby consumption.

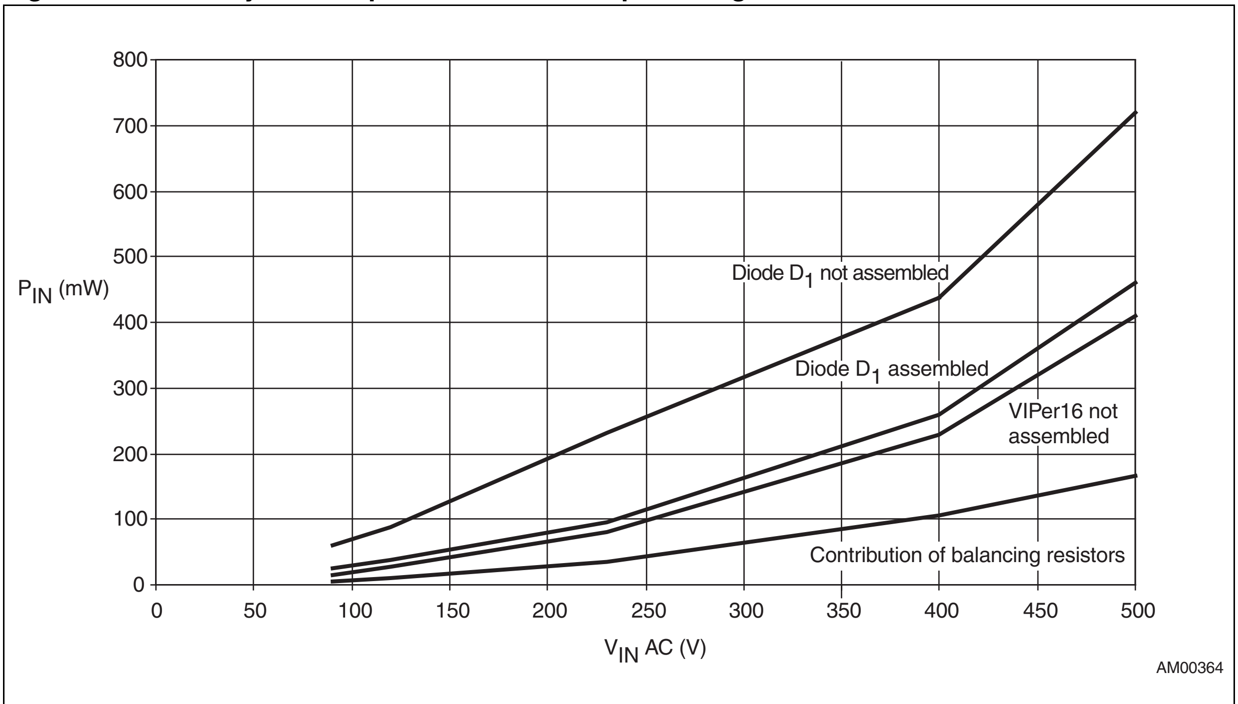
Another aspect which significantly influences standby consumption are the balancing resistors. The value of the balancing resistor was set to 1.5 MΩ, respecting the fact that there is no resolutely defined manufacturer of the capacitors, and consequently the worse case is presented for calculation of the balancing resistors. The effect of these resistors on standby consumption can be partly reduced (mainly for voltages below 400 VAC) using Zener diodes instead of resistors (see *Figure 8*).

Figure 8. Alternative schematic of the input part using balancing Zener diodes instead of resistors



The standby consumption of the demonstration board is displayed in *Figure 9*, measured without linear regulator U_2. The highest line represents the consumption of the converter in cases where diode D_1 was not assembled. The middle line is the consumption of the converter itself with diode D_1, and the lowest line represents the consumption of input part only, without the VIPer16 assembled. It is possible to observe that the contribution of the VIPer16 on standby consumption is low even at high input voltage, and most of the consumption is caused by the input stage of passive components - principally the balancing resistors, leakage of aluminum capacitors and input foil capacitors.

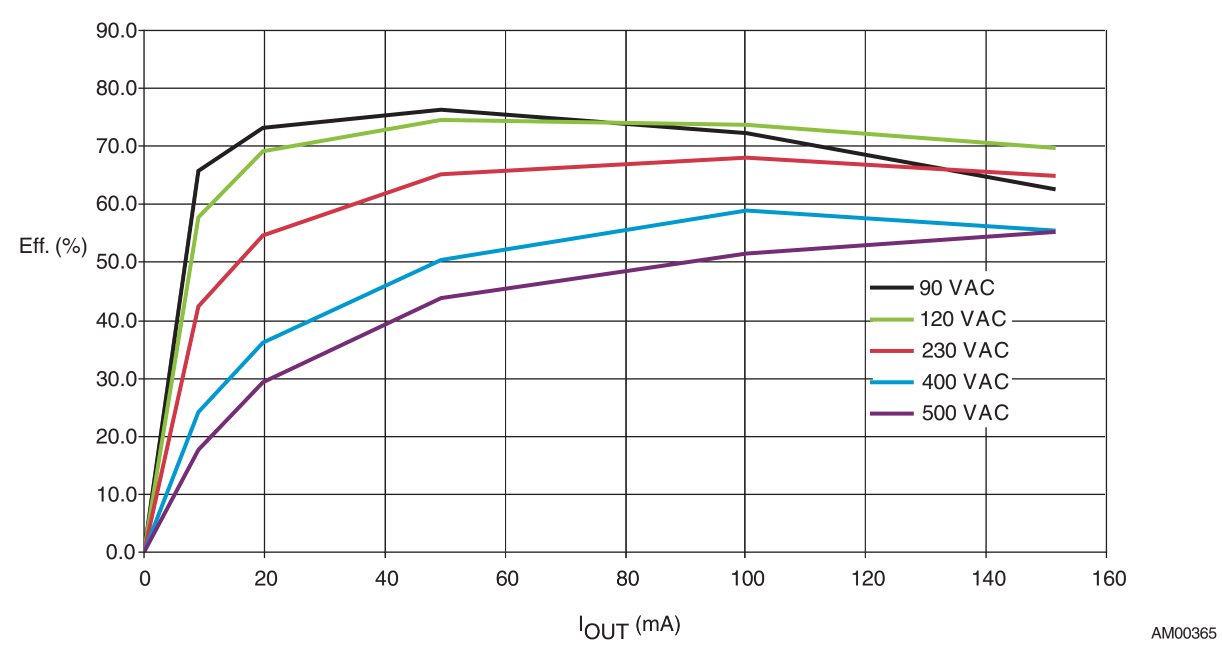
Figure 9. Standby consumption for different input voltage levels



4.3 Efficiency

The efficiency of the converter depends strictly on the input voltage. The efficiency of the tested board is about 65% full load at nominal EU voltage. Complete measurement of the efficiency is shown in *Figure 10*.

Figure 10. Efficiency of the converter

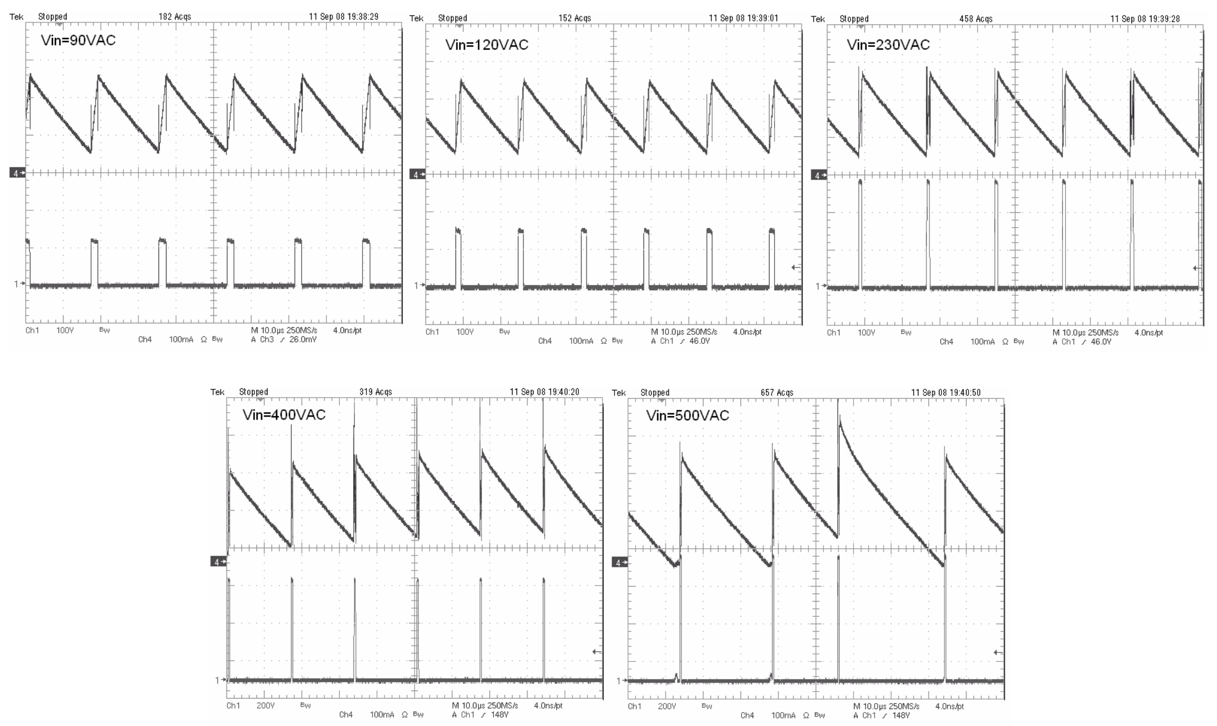


The efficiency can be slightly improved using inductors with reduced resistance and low ESR input and output capacitors.

4.4 MOSFET voltage stress

A sufficient margin between the maximum drain voltage and the real maximum operating voltage level guarantees good reliability of the converter. The drain voltage (CH1) and inductor current (CH2) is displayed in *Figure 11* at full load (150 mA). The maximum voltage drop between the drain and source is 700 V. The margin is, at worst conditions, 100 V.

Figure 11. Drain voltage (CH1) and inductor current (CH4) at different input voltages

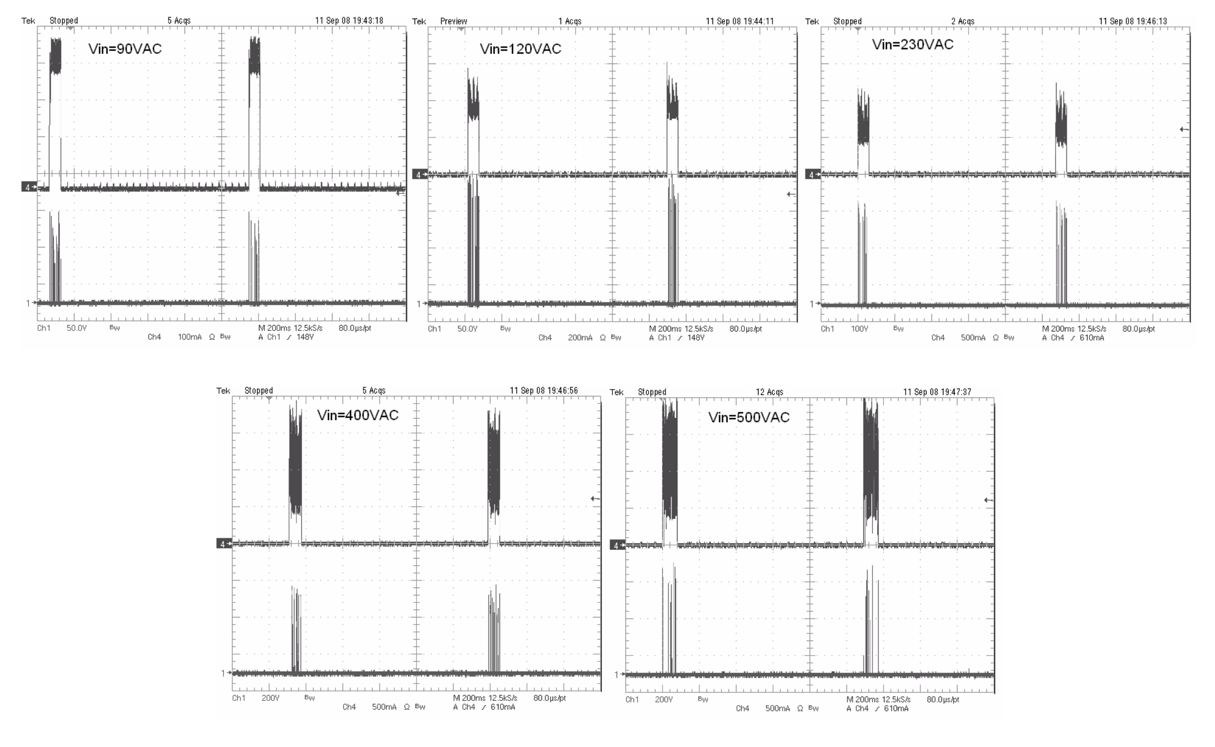


The waveforms in *Figure 10* show also the change of duty cycle (ON time) with input voltage. The converter finally operates in burst mode for highest input voltage.

4.5 Short-circuit behavior

The short-circuit protection is integrated in the VIPer16. If the peak current is limited by the internal threshold at maximum level for a duration of 50 ms (internally set), the Viper16 interprets this state as overload (short-circuit) and switches off the converter for 1 s. The typical waveforms for different input voltages are displayed in *Figure 12*.

Figure 12. Indication of current (CH4) and drain voltage (CH1) during short-circuit



4.6 EMC

The following EMC tests of the board were performed:

- EMI conducting disturbances test for 150 kHZ - 30 MHz (according to EN55022)
- Surge immunity test (IEC 61000-4-5)
- Burst immunity test (IEC 61000-4-4).

4.6.1 Surge - IEC 61000-4-5

Regulation IEC 61000-4-5 defines the so-called “Surge immunity test” (see *Section 6: References*: *8*) as high power spikes caused by large inductive devices in mains. The input of the SMPS is charged by a short (20 - 50 µs) but high voltage (0.5 - 4 kV) pulse. The pulse is applied between L-N and between L (N) - PE.

The surge pulse (typically) causes high inrush current, quickly charging the bulk capacitor in a standard SMPS. The major risk is overvoltage for input components (capacitors, diodes) and the main switch in the application. The inrush current can damage the components in series in the input section of the SMPS (rectifier, fuse, inrush current limiter).

The effect of the surge pulse can be reduced in two ways. The first is to increase the resistance of the input part (typically possible for low power applications) to reduce inrush current. Higher input resistance reduces inrush current and consequently the amount of energy charging the bulk capacitor; therefore the voltage rise over the bulk capacitor is reduced. The second way is to apply components that reduce the voltage level. Typically it is possible to use varistors or Transil™ connected to the input (to absorb part of the energy of pulse) or a bulk capacitor capable of storing enough energy from the surge pulse to reduce the voltage peak level.

The 2 kV surge test was performed on the board with no failures.

4.6.2 Burst - IEC 61000-4-4

Regulation IEC 61000-4-4 defines the so-called "Burst immunity test" (see *Section 6: References*: *9*) as fast switching disturbance presented in the mains. This test means the high frequency, high voltage (8 kV), very short pulses (50 ns) are applied between the input lines and metal plate connected to PE at a defined distance from tested device (100 mm).

This test typically does not cause any damage to the components applied for the SMPS, but it produces high current pulses flowing through the board and causes voltage spikes between different parts of PCB. These spikes can render unstable the applied integrated circuits for the SMPS (mainly the controller). The possible impact typically seen in the SMPS is unstable operation (restart of the SMPS could be allowed) or latching of the SMPS (not allowed).

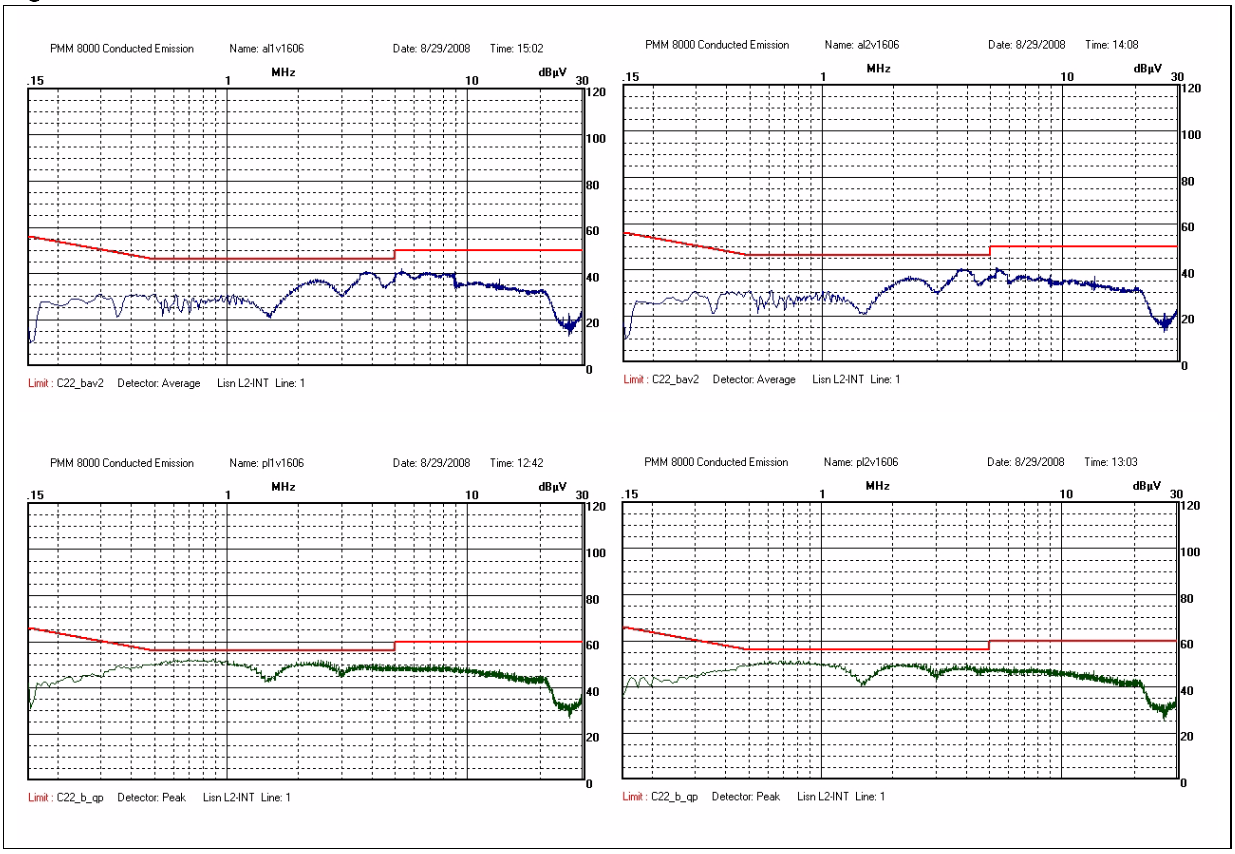
The typical protection against the effects of the burst pulses is application of small filters (capacitance in the range of 100 pF to several nF) to the sensitive inputs.

The 8 kV burst test was performed on the board with no failures.

4.6.3 EMI

The EMI was tested at an input voltage of 230 VAC for full output load. Measurements are listed for the different input connections and average and peak detector in *Figure 13*.

Figure 13. EMI measurements of the demonstration board



4.7 Thermal behavior

The temperature of the VIPer16 was measured for different input voltages at full load (12 V / 150 mA). The board was located in open area at an ambient temperature of 25 °C.

Table 2. Temperature of the VIPer16 at full load

T_{amb}	25 °C	
V_{IN} (VAC)	T (°C)	ΔT (°C)
90	52	27
120	49	24
230	60	35
400	89	64
500	77	52

5 Conclusion

This document shows that it is possible to implement a low power, non-isolated SMPS operating in a buck converter topology for super wide range (85 - 500 VAC), thanks to the new advanced monolithic converter VIPer16.

6 References

1. Application note AN1357 - VIPower: LOW COST POWER SUPPLIES USING VIPer12A IN NON ISOLATED APPLICATIONS - see www.st.com
2. Application note AN2300 - An alternative solution to Capacitive power supply using Buck converter based on VIPer12A - see www.st.com
3. Datasheet of the VIPer16 - Fixed frequency VIPer™ plus family - see www.st.com
4. General technical information - Epcos - http://www.epcos.com/web/generator/Web/Sections/ProductCatalog/Capacitors/AluminumElectrolytic/Photoflash/Page,locale=en.html - General technical information.pdf
5. Series Connection - Rubycon http://www.rubycon.co.jp/en/products/alumi/technote.html SeriesConnection.pdf
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8. IEC 61000 - 4 -5 see www.iec.ch
9. IEC 61000 - 4 -4. see www.iec.ch

7 Revision history

Table 3. Document revision history

Date	Revision	Changes
23-Apr-2009	1	Initial release.