AN2939
Application note

STSMIA832 in a remote video capture system

Introduction

Parallel-to-serial conversion is a convenient way to reduce interconnection wires, and therefore decrease cost thanks to cheaper connectors and cables, in application segments such as mobile and telecommunication.

A typical application scenario is the conversion of the serial data stream from a mobile phone camera into parallel data for its image signal processor (ISP).

Even though SerDes architectures are commonly used to cover small distances in mobile devices, the high level of immunity-to-noise arising from the use of differential pairs for serial data lanes makes them the ideal solution for data transmission over long twisted-pair cables.

This application note presents the implementation of a remote video capture system using the STSMIA832 de-serializer chip, together with cables of different lengths.

Contents

List of figures

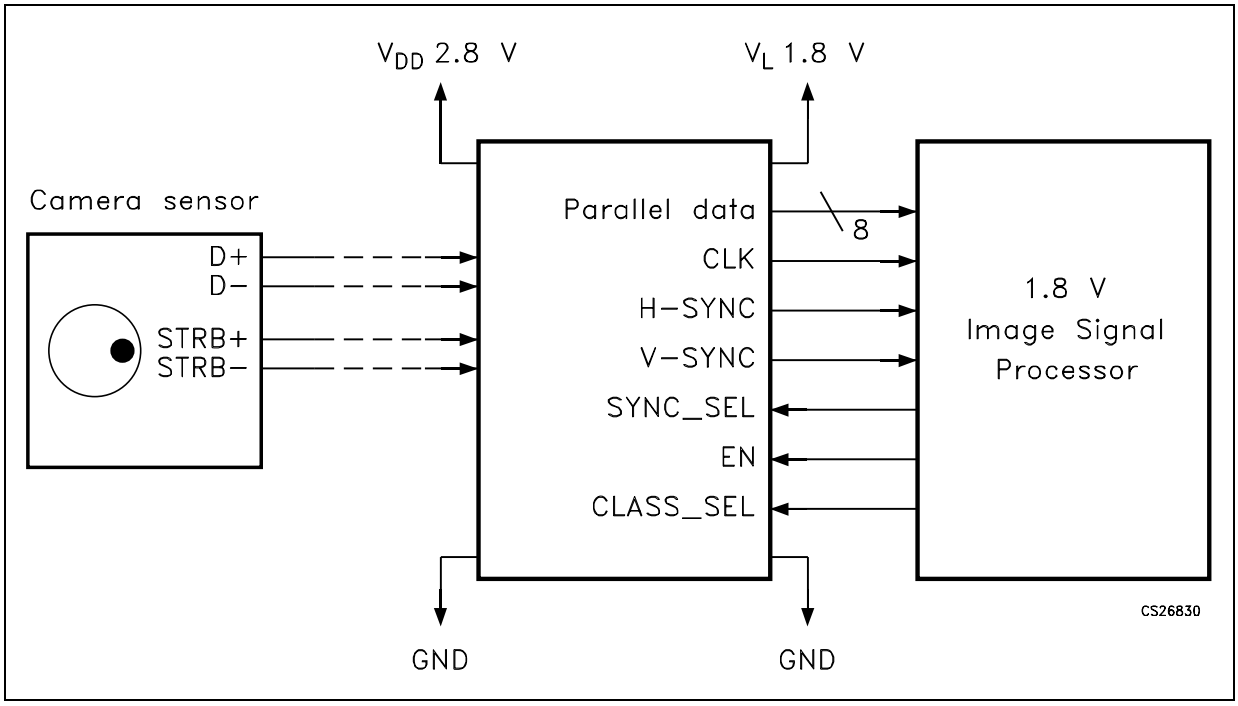
1 Description of the STSMIA832

The STSMIA832 receiver converts the subLVDS clock/data signals (up to 650 Mbps throughput bandwidth) into parallel 8-bit CMOS/LVTTL. The device recognizes the standard mobile imaging architecture (SMIA) 32-bit start-of-frame (SOF), end-of-frame (EOF), start-of-line (SOL) and end-of-line (EOL) sequences to generate the horizontal and vertical synchronization signals (H-SYNC and V-SYNC). Refer to *Appendix A* for SMIA frame structure, sync codes and timing diagrams.

The STSMIA832 supports SMIA CLASS 0 and CLASS 1, 2.

Figure 1 shows a simplified application diagram.

Figure 1. STSMIA832 application diagram



The STSMIA832 can be configured in enabled sync mode or disabled sync mode depending on the status of SYNC_SEL input pin. In enabled sync mode (SYNC_SEL = VL), synchronization codes are decoded and removed from the output data-stream; H-SYNC and V-SYNC signals are used to transmit the decoded synchronization signals to the baseband processor. When the STSMIA832 is operating in this mode, the output CLK signal is gated. This means that the CLK signal is running only when valid data is on the parallel data output; otherwise it is kept high (see *Appendix A* for example timing diagrams).

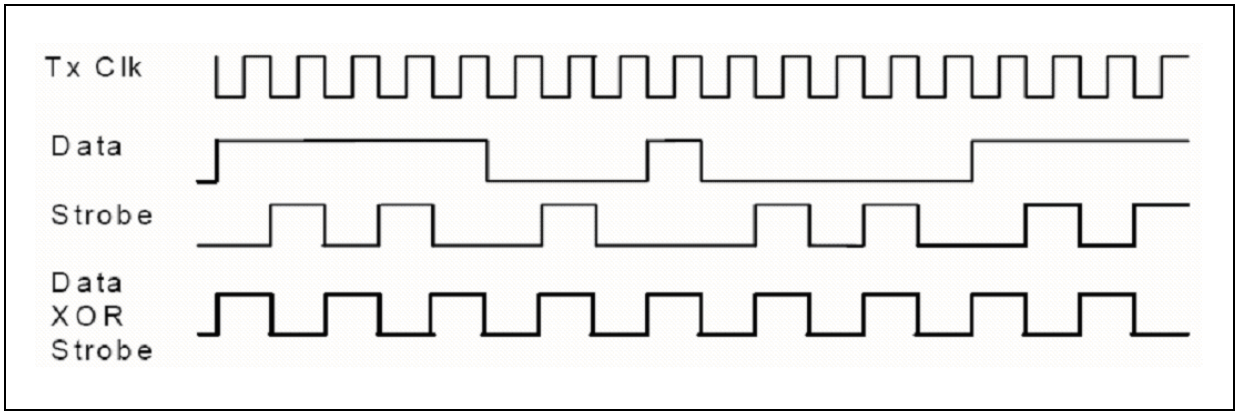
When operating in disabled sync mode, sync codes are not decoded and are therefore transparently transmitted in the parallel output data stream. H-SYNC and V-SYNC outputs are kept low. In disabled sync mode, the CLK output signal is free-running (see *Appendix A* for example timing diagrams).

In both modes, the functionality of the STRB+/ STRB- signals is defined through the CLASS_SEL input pin. If CLASS_SEL is tied low, the STRB+/ STRB- inputs are configured to accept a clock signal (compatible with SMIA CLASS 0). In this mode, data is read only on the clock's rising edge.

If CLASS_SEL is asserted high, the STRB+/ STRB- inputs are configured to accept a strobe signal (compatible with SMIA CLASS 1,2). The strobe signal toggles only when the data signal is not changing. The clock signal can be extracted through a XOR operation between data and strobe signals. Using data/strobe configuration, the frequency of the signals on the bus is reduced, resulting in lower EMI.

Figure 2 shows an example of the data/strobe signals.

Figure 2. Data/strobe signaling

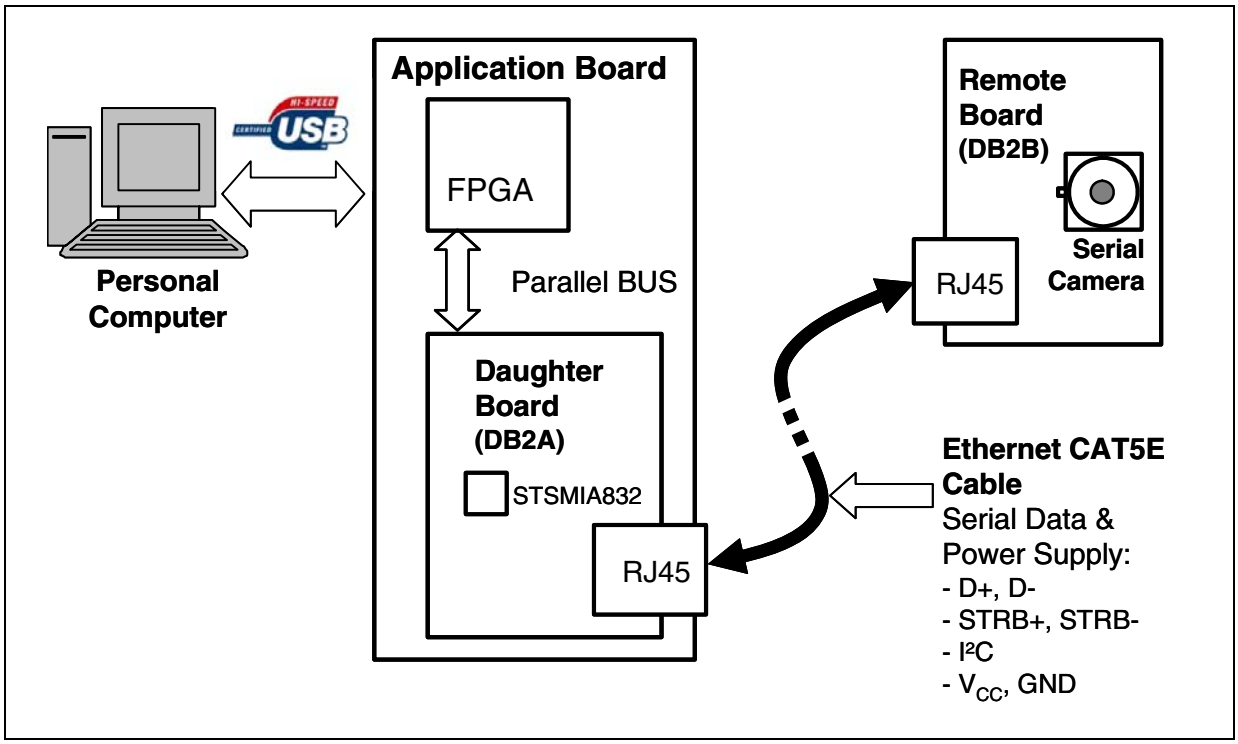


Refer to STSMIA832 datasheet for more detailed information.

2 Remote video capture system

The STSMIA832 can be used in remote video capture systems to receive subLVDS signals originating from a SMIA serial camera transmitting over long cables. *Figure 3* shows the block diagram of the architecture presented in this document.

Figure 3. Remote video capture system



The serial camera (STMicroelectronics' 1 megapixel VS6650 or 2 megapixel VS6750) is placed on a remote board (DB2B) which is connected to a daughterboard (DB2A) through a CAT5E Ethernet cable.

The daughterboard, containing the STSMIA832, is plugged into the main application board used to capture video data streams and interface to a personal computer through a standard USB2.0 bus.

All twisted pairs inside the CAT5E cable have been used (refer to *Table 1* for pair assignments). Pair numbering is in accordance with TIA/EIA-568-B.1-2001.

Signals carried by the cable are:

- I^2C for camera control (SDA-SCL)
- Differential data output (D+, D-)
- Differential clock/strobe (STRB+, STRB-)
- Ground and 5 V power supply (V_{SUPPLY})

The remote board contains a 12 MHz oscillator (input to the camera) and can also be supplied using a local voltage, up to 16 V, instead of the V_{SUPPLY} voltage coming from the main application board through the cable. The 5 V supply (either from cable or local regulator) is used to generate all the supply voltages required by the camera and the oscillator (1.8 V, 2.8 V and 3.3 V). See *Appendix B* for detailed schematics.

Table 1. Signals in the CAT5E cable twisted pairs

Pair number	Pins (1)	Signals
2	1-2	STRB+, STRB-
3	3-6	SDA, GND
1	4-5	D+, D-
4	7-8	SCL-V_{SUPPLY}

1. Pair numbering according to TIA/EIA-568-B.1-2001.

It is important to note that I^2C signals (SCL-SDA) are not transmitted using the same twisted pair, but in different pairs together with supply voltage and GND.

Using the same twisted pair for the I^2C signals would lead to distorted signals due to coupling; when using long cables the distortion would be unacceptable, causing I^2C communication failure.

Figure 4, *Figure 5* and *Figure 6* show some photos of the capture system with the daughterboard and remote board.

Figure 4. Capture system

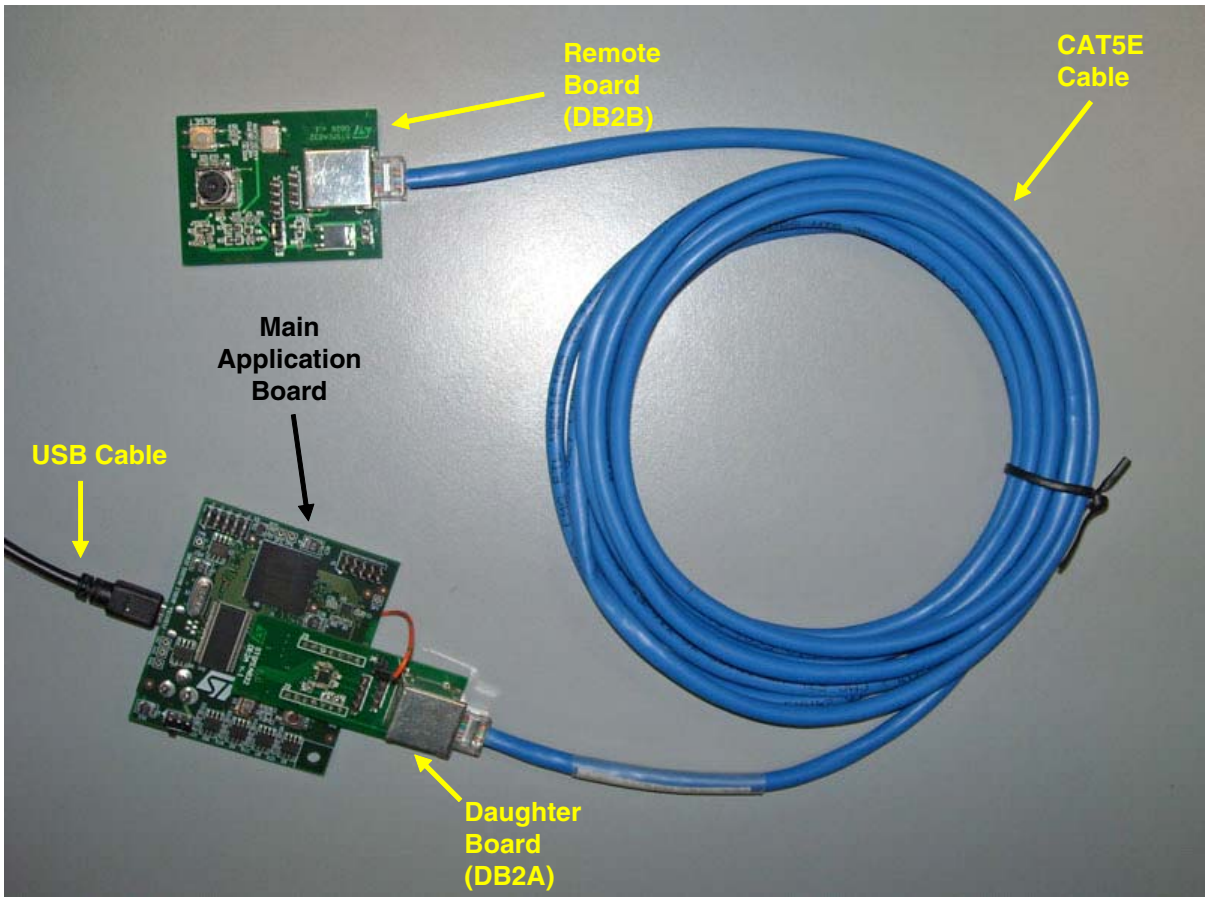


Figure 5. Daughterboard (DB2A)

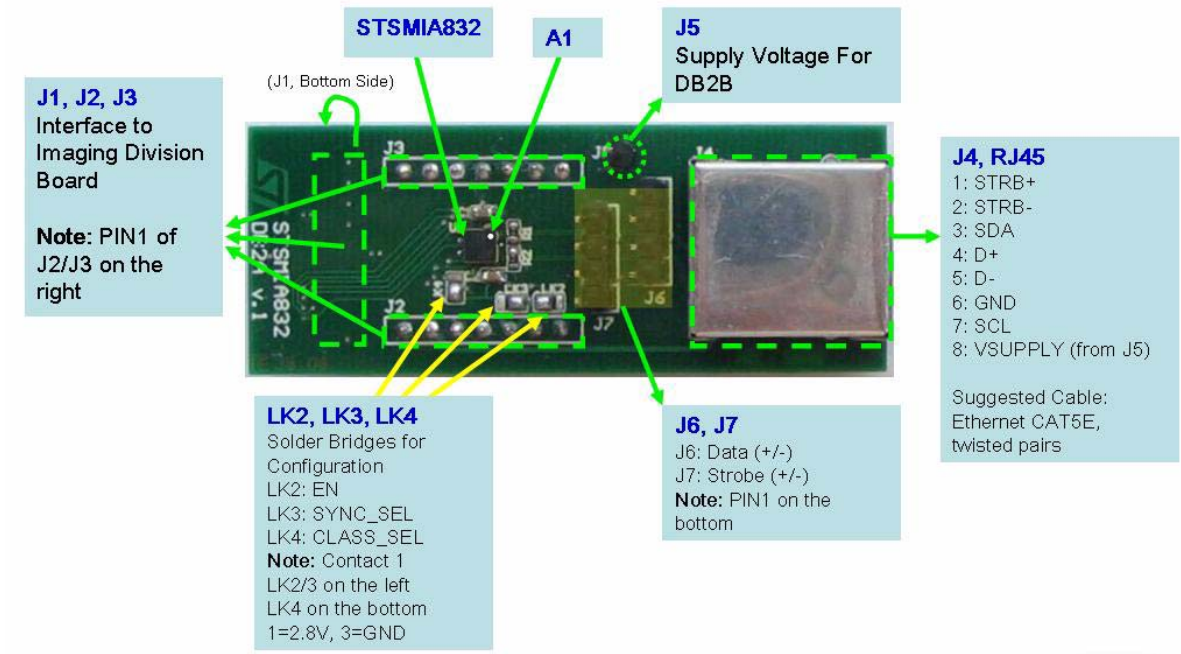
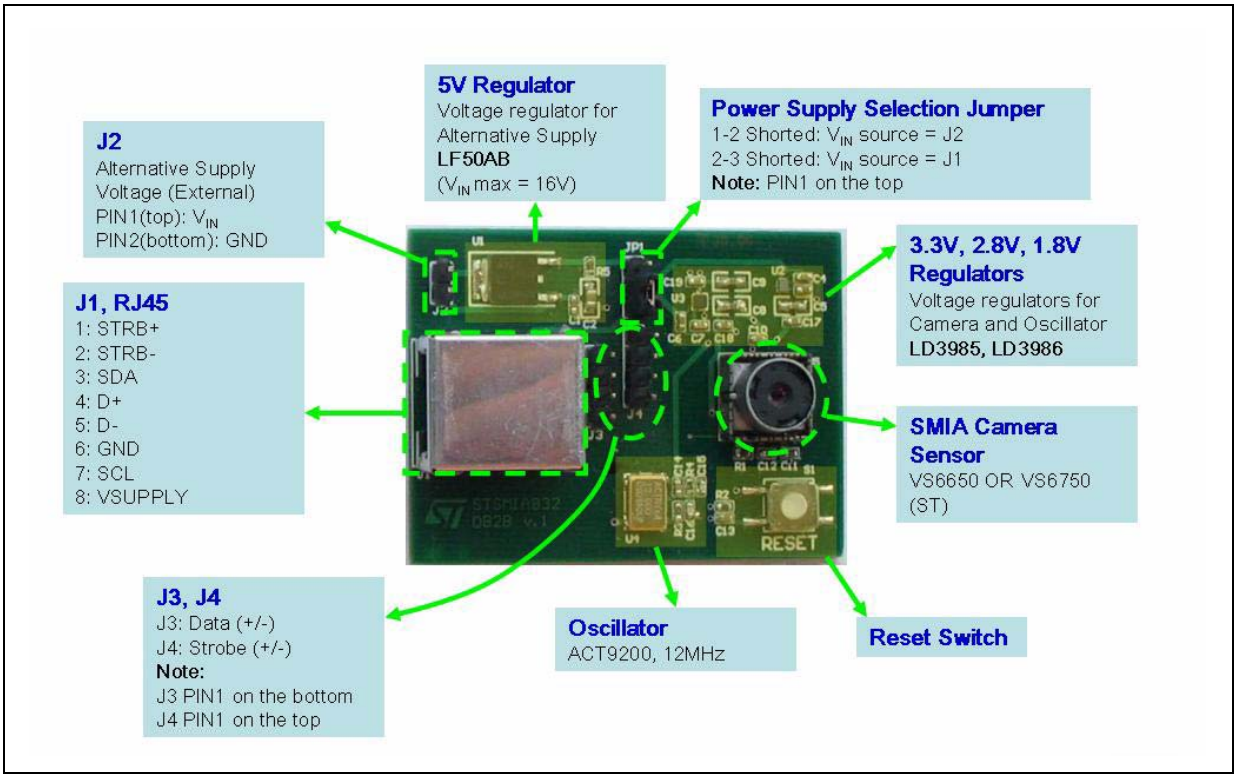


Figure 6. Remote board (DB2B)



3 PCB layout considerations

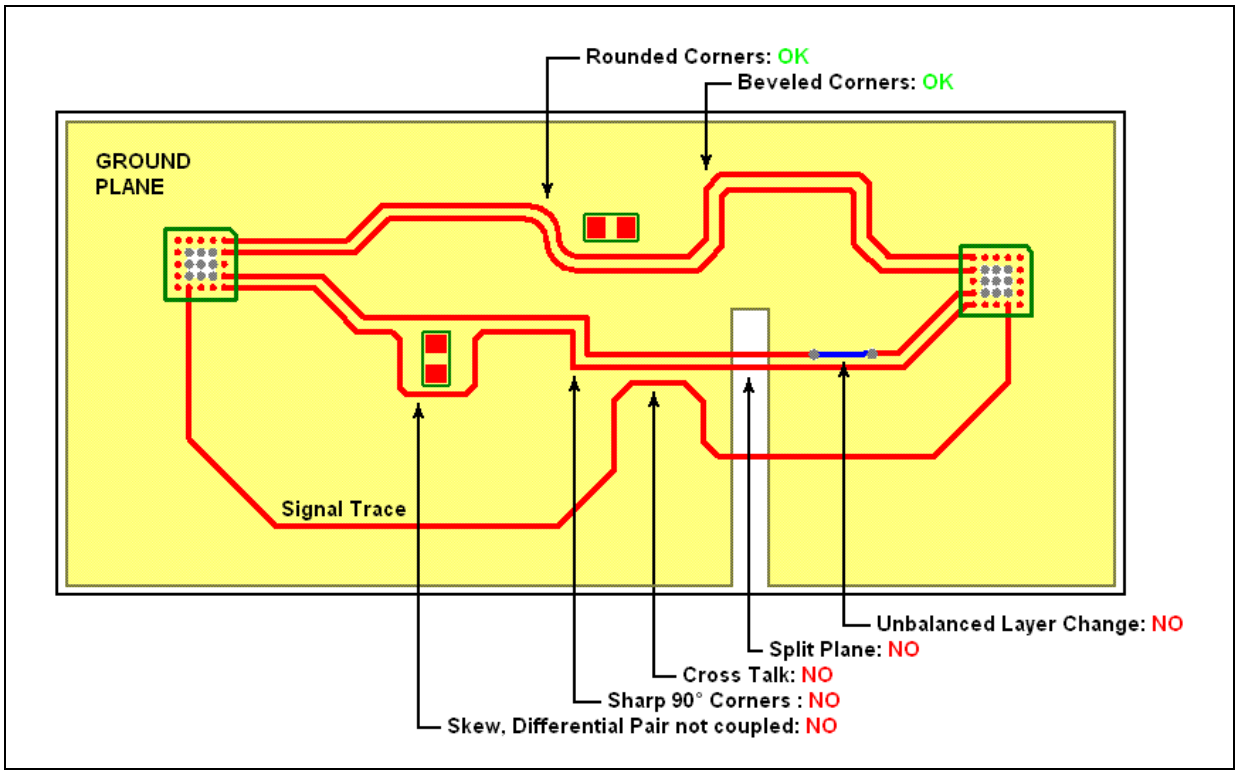
The STSMIA832 requires termination resistors on both differential lines (data and strobe) and controlled impedance tracks in order to reduce reflection of subLVDS signals and maximize signal quality.

The 100 ohm termination resistors and the power supply bypass capacitors must be placed as close as possible to the STSMIA832. Differential tracks should be routed, keeping in mind the following rules:

- Trace lengths must be equalized to reduce skew
- Traces belonging to the same differential pair should be routed as close as possible to maximize common mode noise rejection
- Differential impedance should be equal (or close to) 100 ohms
- number of discontinuities should be minimized (vias, stubs etc.)
- The reference plane (GND or VCC) under the differential traces must be continuous (no split planes)

Figure 7 shows typical routing errors for subLVDS differential pairs.

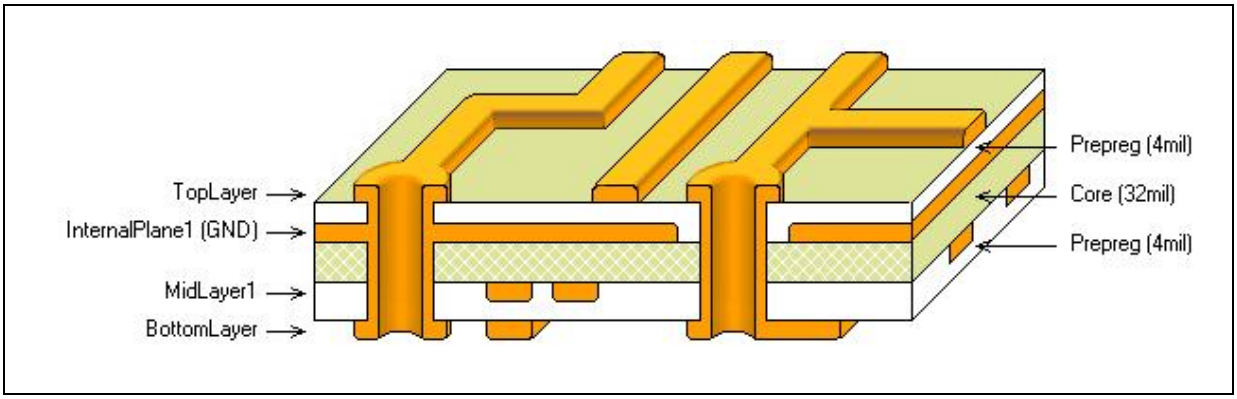
Figure 7. SubLVDS differential signal routing errors



Several tools are available on the Internet to help the PCB layout designer define the track parameters needed to obtain100 ohm differential impedance (trace thickness, trace width, distance between traces, dielectric layer thickness, dielectric constant, etc.), but it is good practice to contact the PCB manufacturer to check the impedance of differential tracks in order to achieve a more reliable result which fits the actual process and material parameters.

Figure 8 shows as an example of the layer stack used for the daughterboard (DB2A).

Figure 8. Layer stack for the DB2A



The top layer, mid layer1 and bottom layer are signal layers. The InternalPlane1 is a ground plane used as a reference plane for the differential tracks which are routed on the top layer.

Figure 9 and *Figure 10* show the PCB layout for the daughterboard and remote board (red = top layer, blue = bottom layer, brown = mid layer).

Refer to *Figure 5* and *Figure 6* for component identification.

Figure 9. Daughterboard (DB2A) layout

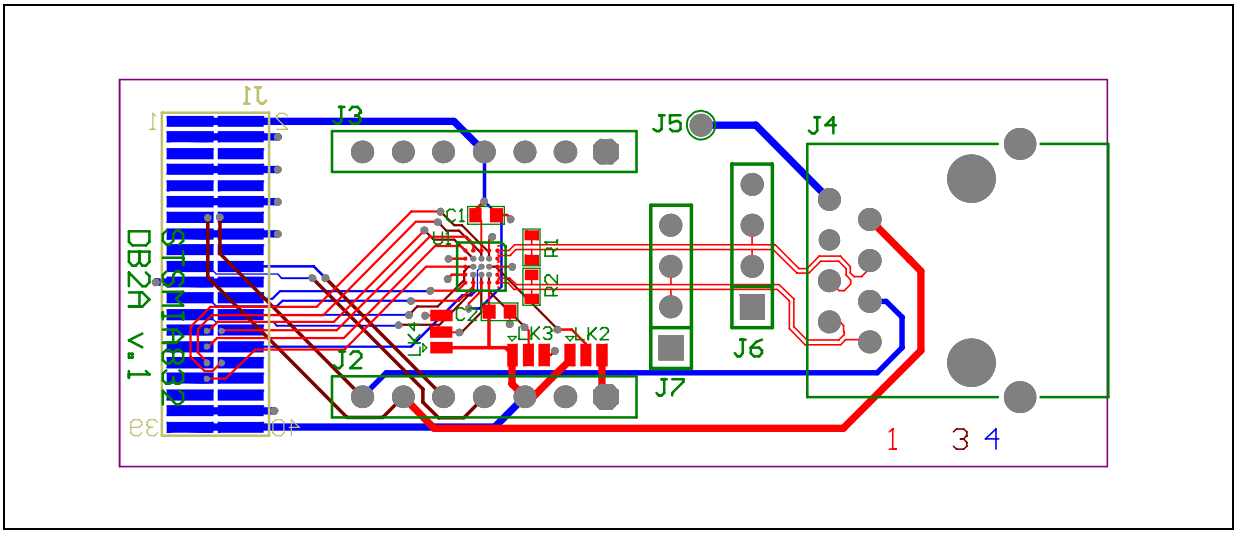
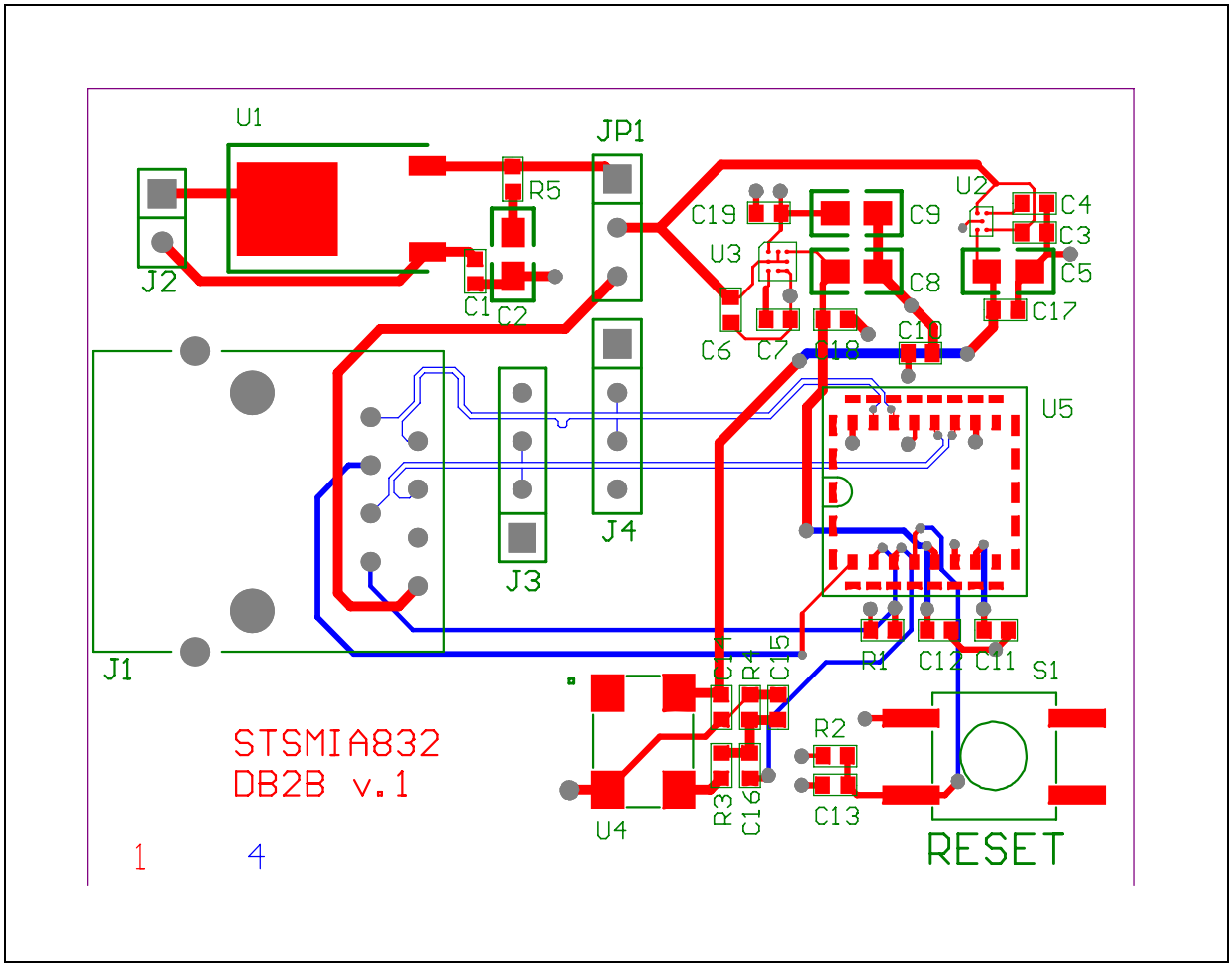


Figure 10. Remote board (DB2B) layout



4 Test results and conclusions

The application has been tested using four cables of different lengths: 2, 4, 10 and 20 meters.

The camera sensor (VS6650 or VS6750) has been set to generate a serial data stream ranging from198 to 240 Mbps.

Neither camera showed any loss in image quality over the entire range of data rate and cable length. The following pictures provide a comparison of captured serial data eye patterns at transmitter (TX - camera) and receiver (RX - STSMIA832) ends.

Figure 11. Eye patterns: 198 Mbps, 2 m cable

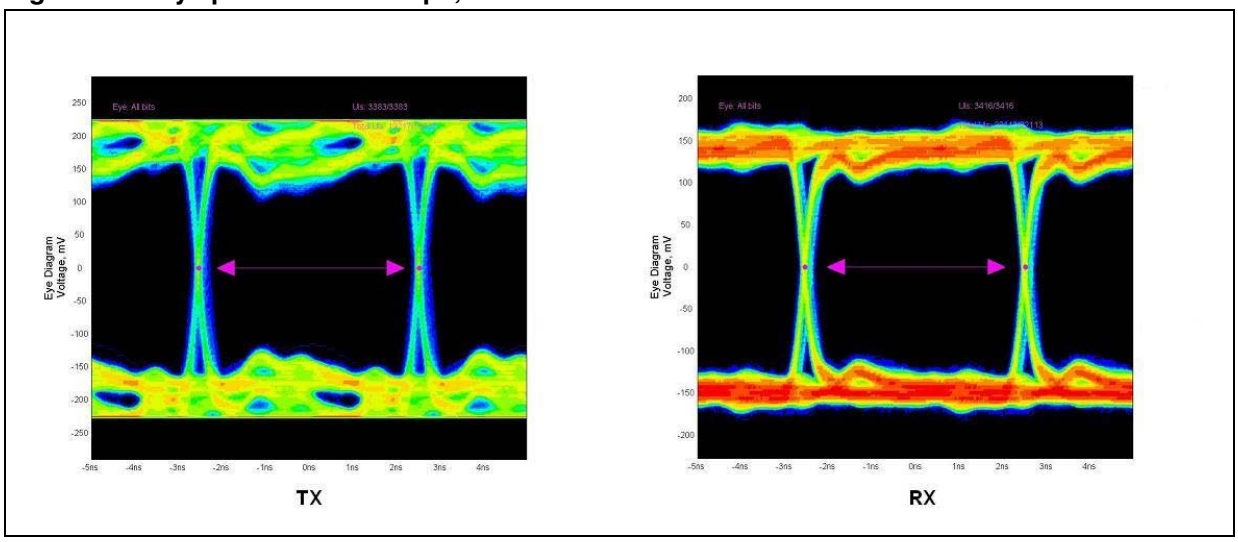


Figure 12. Eye patterns: 198 Mbps, 4 m cable

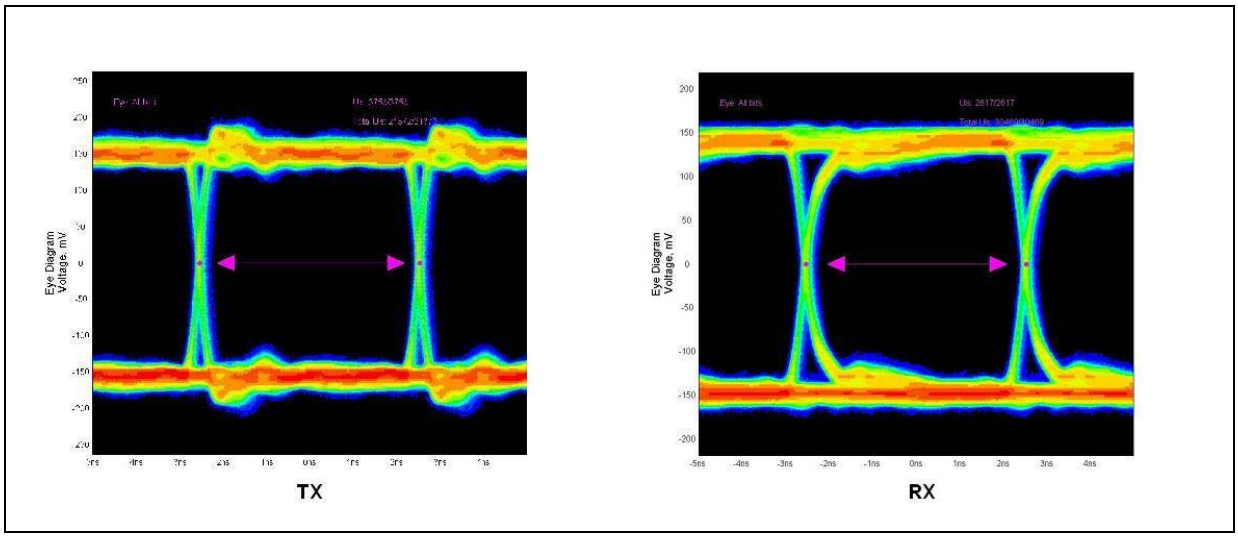


Figure 13. Eye patterns: 198 Mbps, 10 m cable

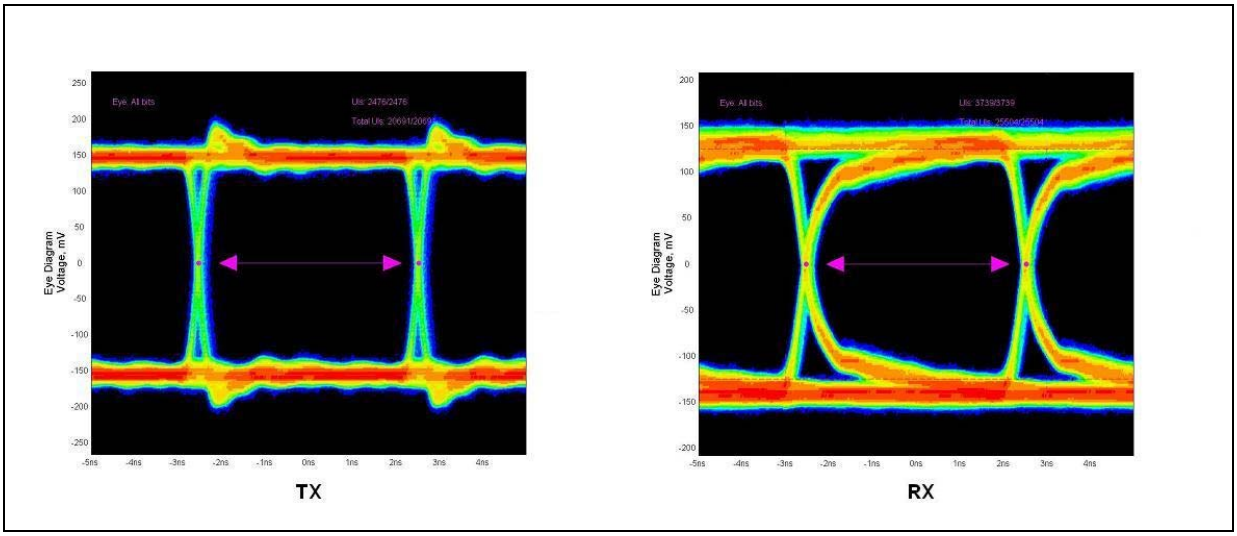
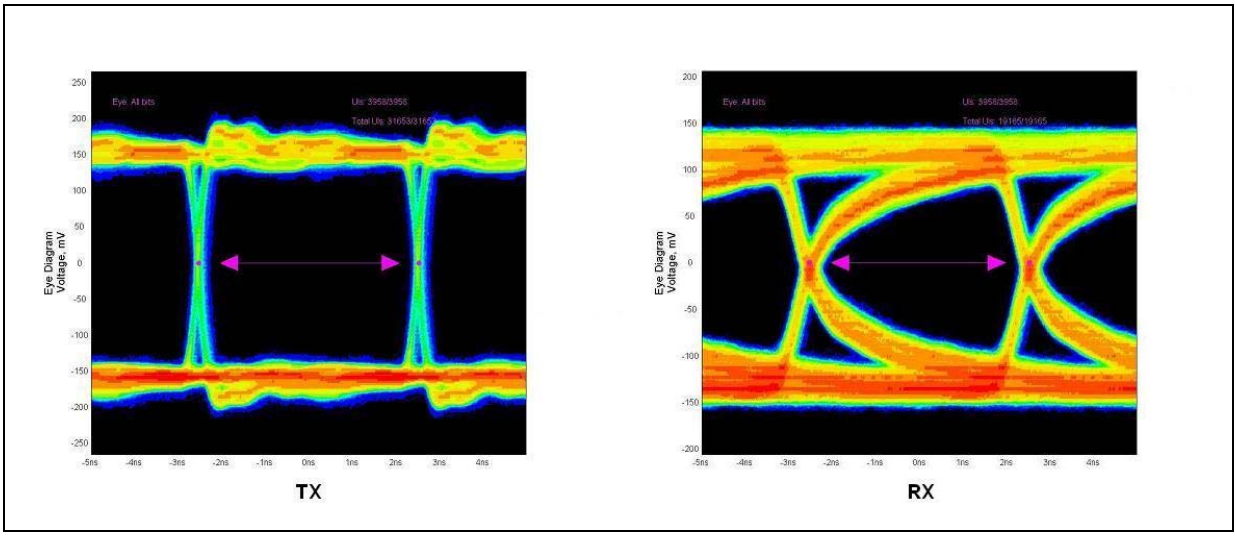


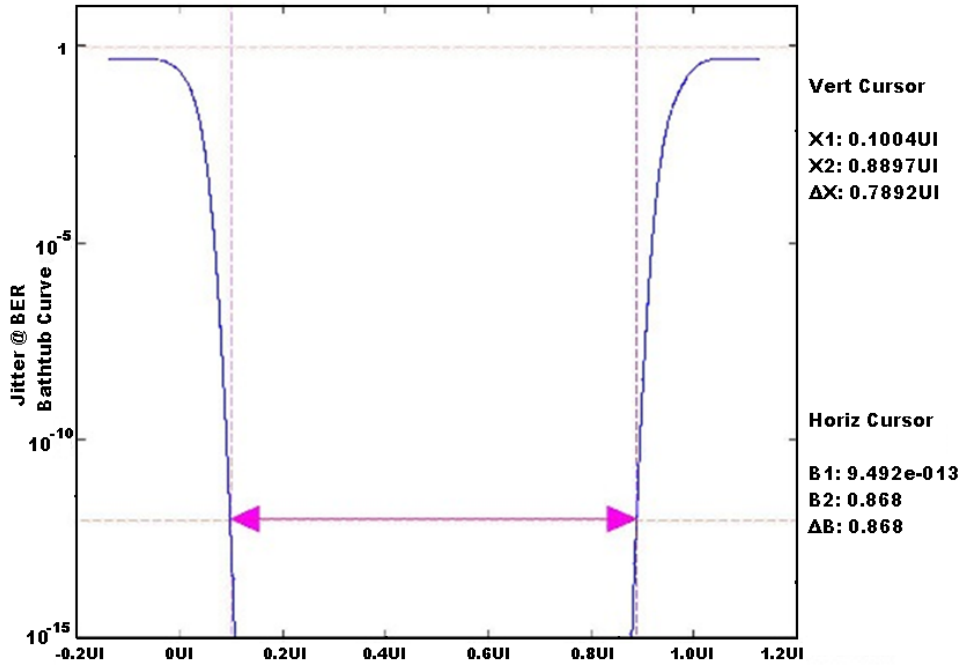
Figure 14. Eye patterns: 198 Mbps, 20 m cable



As cable length increases we can observe, as expected, slower rising and falling edges, lower differential amplitude and a slight increase in jitter. But even using 20 m CAT5 cable, the eye stays open enough to guarantee good receiving performance thanks to the high differential sensitivity of the STSMIA832.

The pink arrow indicates the sampling interval corresponding to a BER of 10^{-12} obtained from the bathtub curve generated using jitter-analysis software (see *Figure 15*).

Figure 15. Bathtub curve: 198 Mbps, 20 m cable



Results from tests at 240 Mbps are similar to the ones presented in *Figure 11* through *Figure 15*, and suggest that the application can be used well beyond this limit.

A comparison between an image received through the 2 m cable and another received through the 20 m cable is shown in figure below. Even at full resolution there is no noticeable difference in image quality.

Figure 16. Received images

2m Cable 20m Cable

5 References

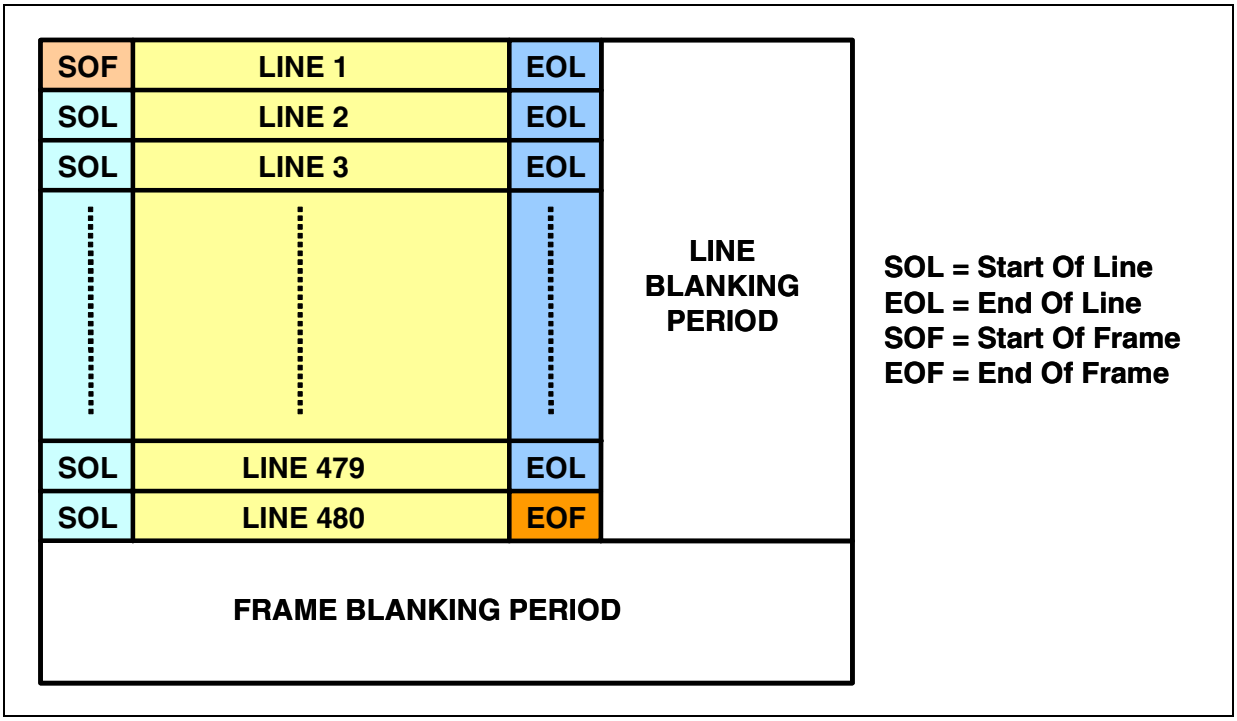
- STSMIA832 datasheet
- SMIA CCP2 specification
- TIA/EIA-568-B.1-2001 standard

Appendix A

A.1 VGA frame structure

Figure 17 shows the frame format, according to the SMIA CCP2 specification, for a VGA image. Each frame starts with a start-of-frame (SOF) synchronization code and ends with an end-of-frame (EOF). Similarly, each line starts with a start-of-line (SOL) and ends with an end-of-line (EOL). The SOL of the first line is substituted with an SOF and the EOL of the last line is replaced with an EOF. The time between the end of each line and the beginning of the following one is called “line blanking period”. The time between frames is called “frame blanking period”.

Figure 17. VGA frame structure

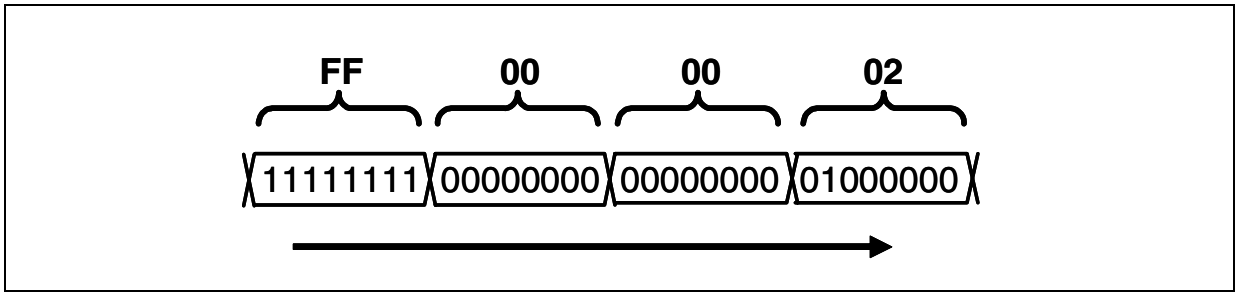


Synchronization codes are 4-byte codes and bits are transmitted bytewise LSB first (see SOF example in *Figure 18*). They contain the DMA channel number, which can range from 0 to 7. Logical channels are used only in disabled sync mode (SYNC_SEL = GND) to separate different data flows which are interleaved in the data stream. In enabled sync mode, synchronization codes are decoded, translated in H-SYNC/V-SYNC signal changes and removed from the data stream; the DMA channel information is therefore discarded.

Table 2. Synchronization codes. X = Logical channel (DMA, 0 to 7)

Name	Synchronization code (hex)
SOL	FFh 00h 00h X0h
EOL	FFh 00h 00h X1h
SOF	FFh 00h 00h X2h
EOF	FFh 00h 00h X3h

Figure 18. Bit transmission order (SOF example)



A.1.1 Timing diagram

Figure 19. Timing diagram: Enabled sync mode. Gated clock, HSYNC and VSYNC active

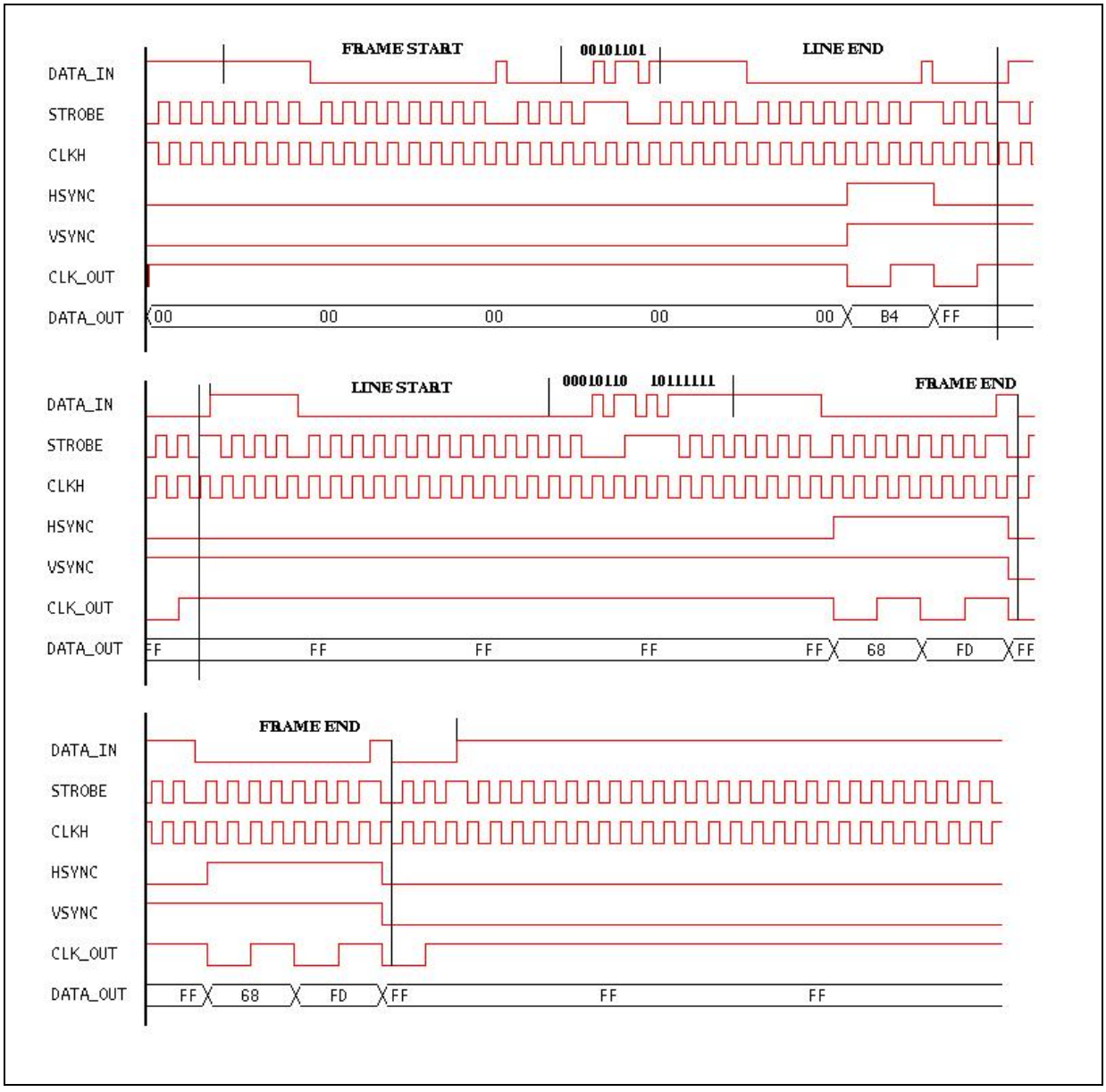
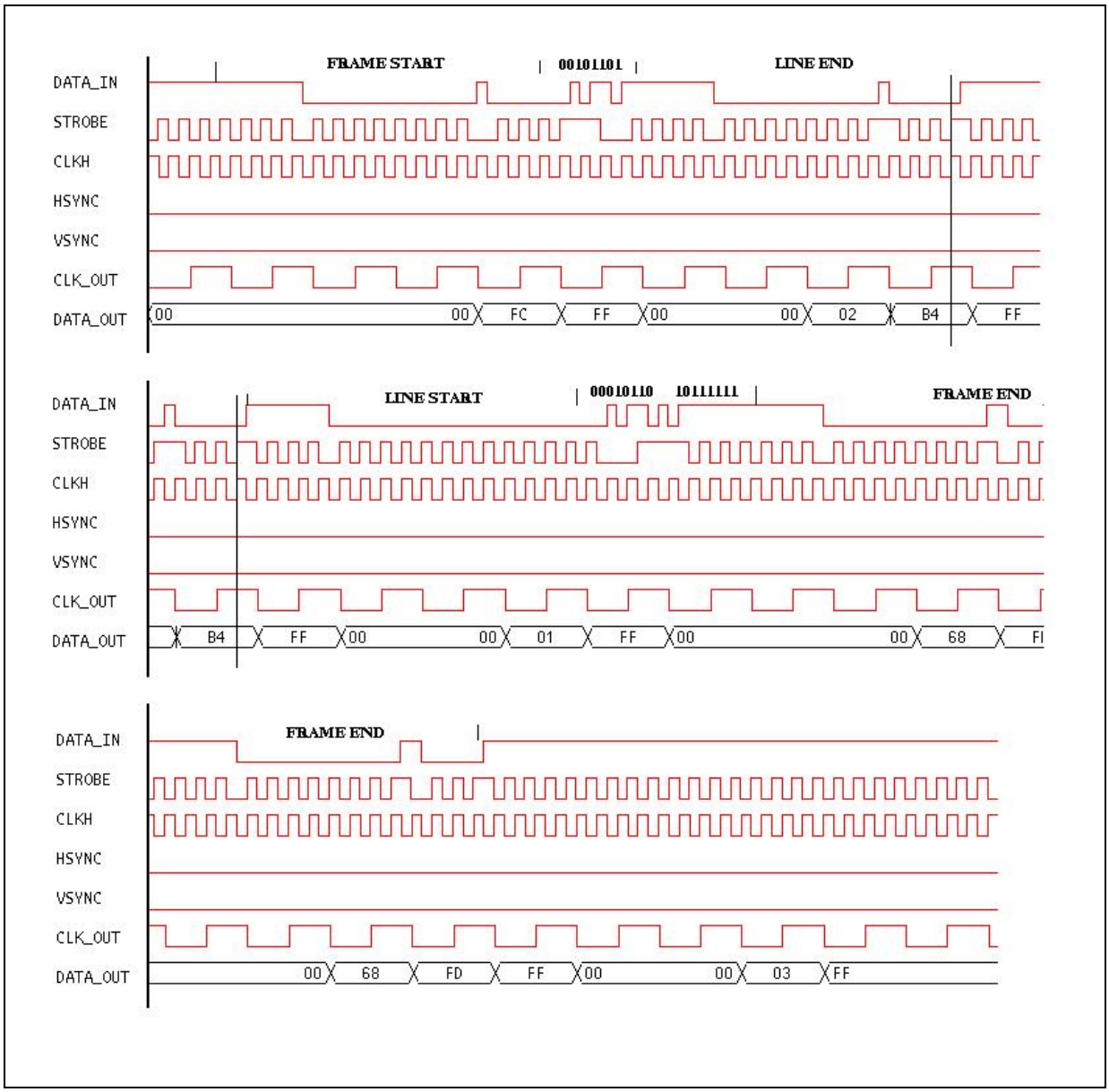


Figure 20. Timing diagram: Disabled sync mode. Free running clock, HSYNC and VSYNC disabled



Appendix B Schematic diagrams

Figure 21. Daughterboard schematic - DB2A

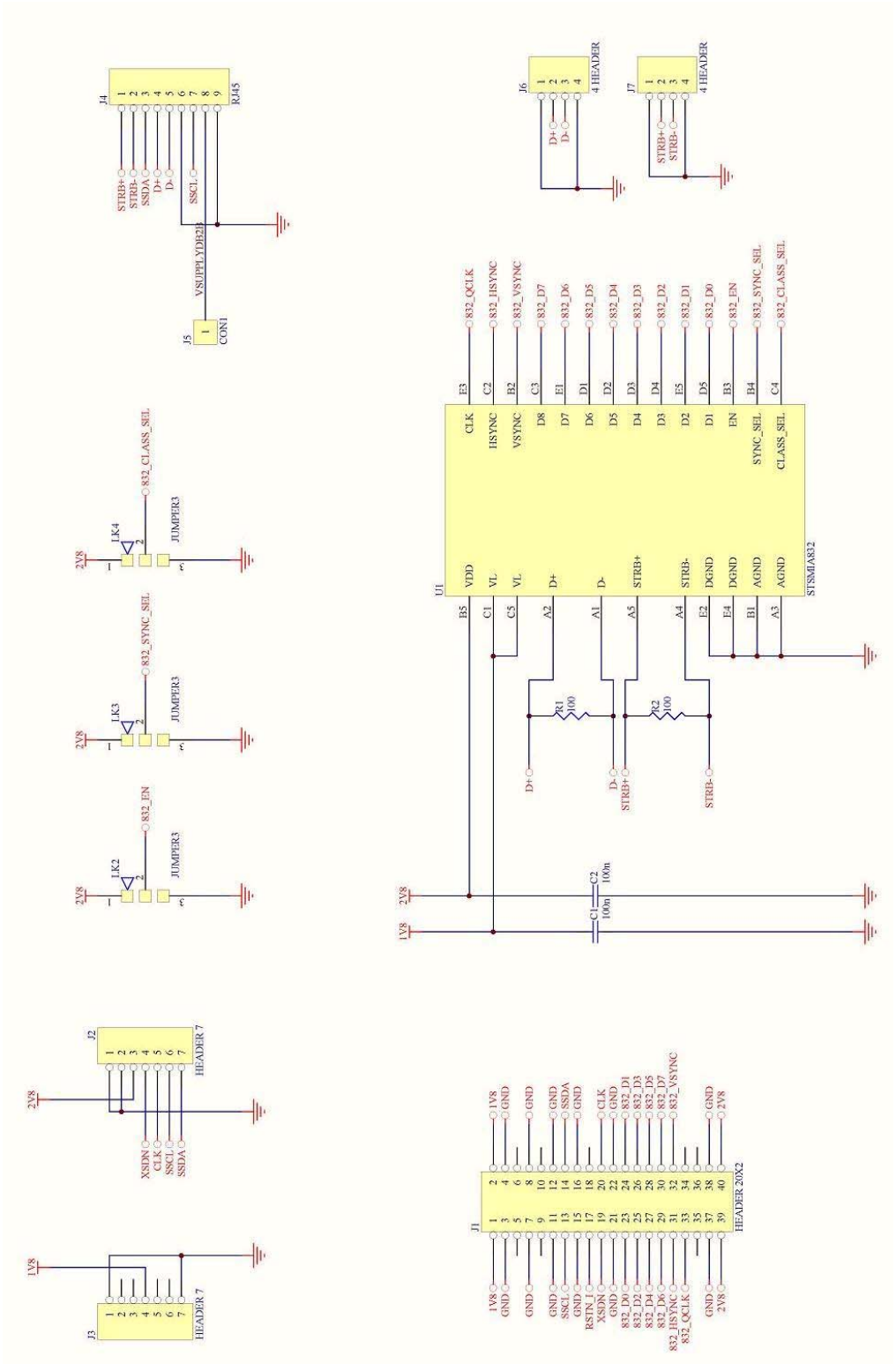
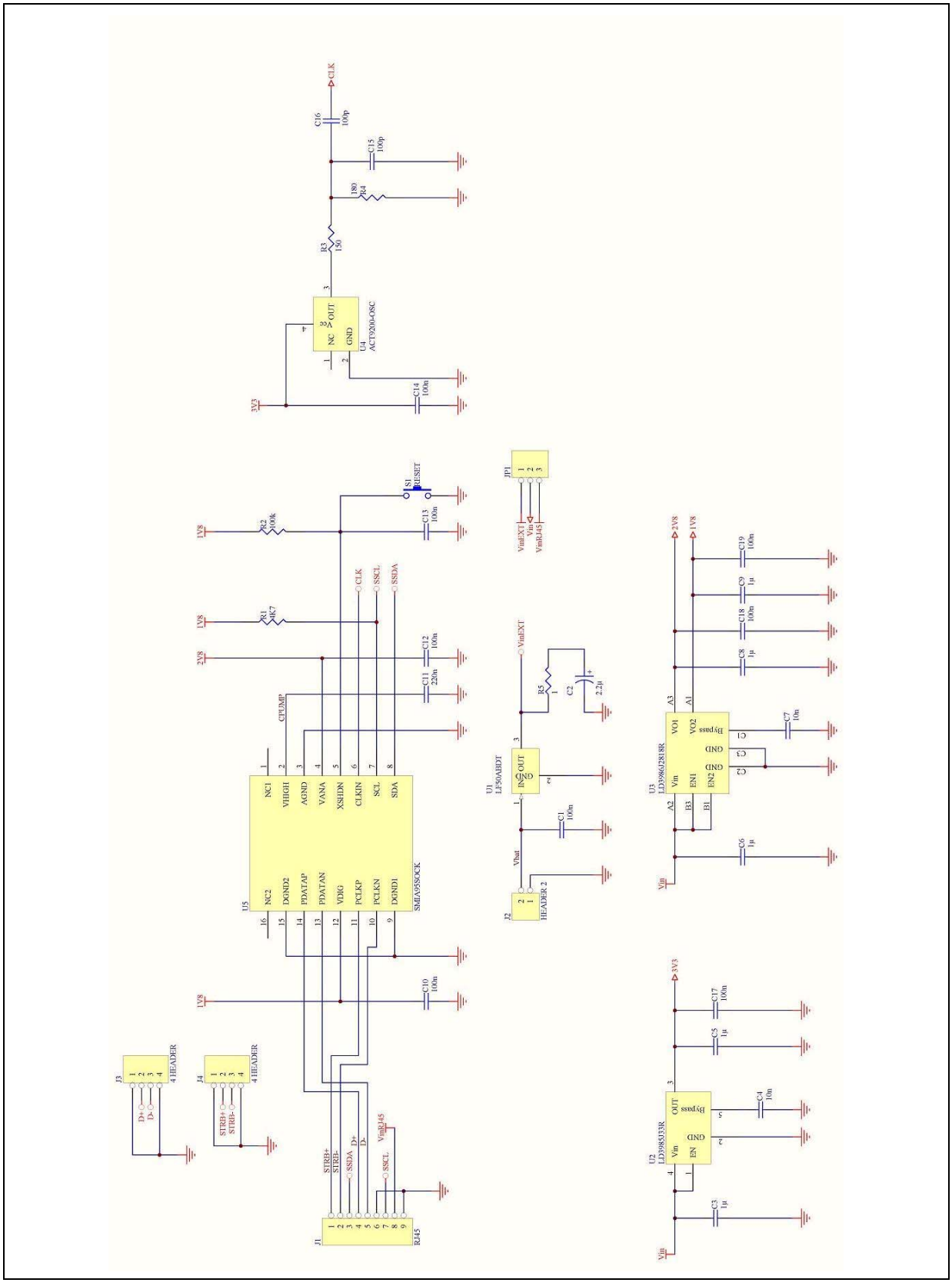


Figure 22. Remote board schematc - DB2B



6 Revision history

Table 3. Document revision history

Date	Revision	Changes
16-Mar-2010	1	Initial release.