AC switch triggering with 3.3 V power supply

Introduction

This document focuses on the calculation of gate current consumption of various types of AC switches when using a 3.3 V power supply. Until now, the standard of a 5 V power supply was used. In home appliance applications there is a bigger focus on the MCU working with a 3.3 V power supply, and a lower supply voltage brings additional constraints on gate circuitry. This application note provides a precise calculation process to correctly set the necessary parameters.

This application note concerns Q2 and Q3 operation (that is, for negative power supply) as this is the most common mode of operation for AC switches, but advice and comments for operation in Q1 and Q4 quadrants (that is, for positive power supply) are also given.

1 Gate resistor choice

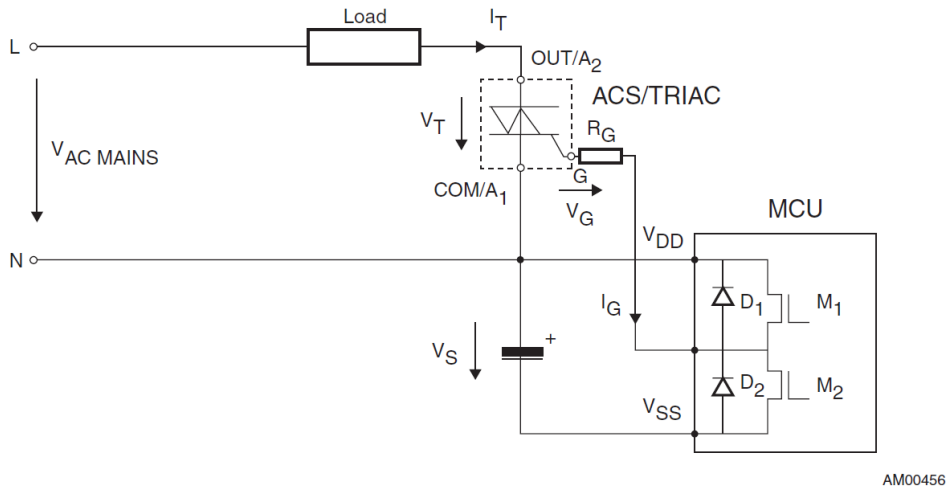
1.1 Variation of gate current with temperature

The value of the gate resistor (refer to R_G in Figure 1, where a negative power supply is used) is determined to ensure proper turn-on of the ACS/TRIAC in the temperature range specified by the application. The minimum gate current required for turn-on of the ACS/TRIAC increases as the junction temperature decreases. This variation of minimum gate current is described in the datasheet “Z01 - 1 A triacs,” see example in Figure 2. The worst case appears when junction temperature T_j is at minimum ambient temperature.

The minimum ambient temperature is set to 0 °C for most home appliance applications.

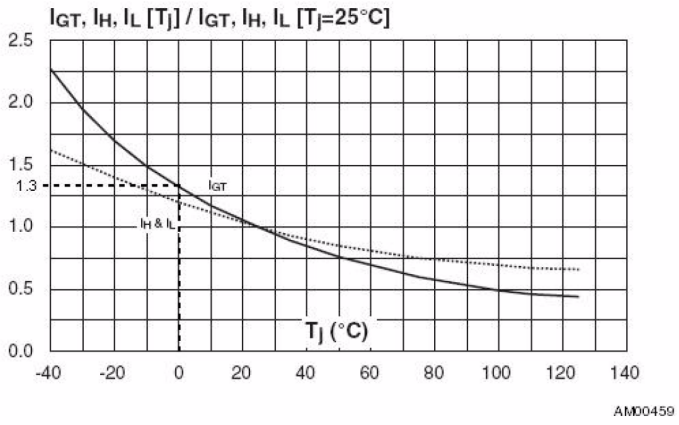
The gate current (I_{GT}) level is specified for 25 °C. At temperature 0 °C, this level is usually increased to a range 1.3 - 1.5 times as higher for most triacs and AC switches.

Figure 1. Circuit for direct driving of ACS/TRIAC from MCU



The Figure 1 also gives the references for the electrical parameters (V_T, I_T, V_G) which are used in this application note. That voltage V_G is referenced to the G terminal, not the A_1, or COM terminal to get positive values when the current is sunk from the gate.

Figure 2. Gate current variation with temperature for Z01 device



1.2 Resistor according to environment accuracy and variation

Temperature is not the only parameter influencing gate resistor choice. Other parameters have also to be considered. Parameters discussed in this section are related to the accuracy of the components used and to the working environment.

1.2.1 Parameters variations

All the different application parameters that have an impact on gate current level are listed below.

Power supply voltage (V_{DD}) variation is one of the most important parameters that has to be considered. In appliance applications a capacitive power supply is often used. The main part of this power supply is the zener diode. Stability of the zener voltage is the best at 5.1 V and 5.6 V. Accuracy of this power supply is ±10% at 5 V.

Stability of the diode at 3.3 V and 3.9 V is worse and ±0.6 V (±20%) can be achieved. This result leads to the use of switch mode power supply (SMPS) for a 3.3 V power supply.

Output voltage levels on the I/O pins of the MCU are important variable parameters. The most important parameter is the low output level (V_{OL}) which specifies the voltage on the output pin when tied to the ground. This parameter varies with the current flowing through this pin. The value is given by the MCU datasheet (for example: STM8S10xxx).

As an example, the Table 1 shows data for STM8S and STM32. The data for STM8S are taken from the high-sink pin. The data for STM32 are taken from the GPIO pin.

Table 1. Output low level voltage for STM8S and STM32

	I_G = 8 mA	I_G = 8 mA	I_G = 8 mA
STM8S (V_{DD} = 5 V) HS pin	0.35 V	0.6 V	1 V
STM8S (V_{DD} = 3.3 V) HS pin	0.55 V	0.9 V	N/A(1)
STM32 (V_{DD} = 3.3 V) GPIO pin	0.4 V	NC(2)	1.3 V

1. *Maximum current capability of high-sink I/O port for STM8S with 3.3 V power supply is 12 mA as specified in the datasheet STM8S103xx.*
2. *Information is not specified in the datasheet STM32103xx.*

It is possible to put the pins in parallel to achieve a bigger current capability. In that case the maximum current through the MCU ground pin (V_{SS}) has to be checked as it is limited to a maximum value (refer to I_{VSS} parameter on the MCU datasheet, for example: STM8S103xx).

The gate resistor (R_G) resistance varies with the accuracy of the resistor used. Standard resistor accuracy is ±5% or ±1% with a preference for ±1% accuracy. The worst case has to be taken into account for calculations.

The voltage drop of the gate junction (V_{GT}) is a parameter that varies with the load current flowing through the TRIAC/ACS and with temperature. Its value increases with a temperature drop at a rate of 2 mV / °C. Load current dependency is discussed in Section 2.1 V_{GT} variation.

1.2.2 Gate resistor calculation

The value of the gate resistor has to be calculated to deliver the proper amount of gate current under the worst condition, which is:

- Minimum ambient temperature (0 °C),
- Minimum supply voltage (V_{DD} min),
- Maximum voltage drop of the gate junction (V_{GT} max),
- Maximum output low voltage (V_{OL} max) for one high-sink I/O pin of the MCU
- Maximum resistance of the gate resistor for ±1% resistor accuracy (1.01 x R_G). The following equation summarizes all conditions for proper R_G selection:

$$R_G = \frac{V_{DD\min} - V_{GT\max} - V_{OL\max}}{I_{GT}(0°C) \times 1.01} \quad (1)$$

Two examples of calculation are shown:

1. Example 1: MCU: STM8S103K3 with ACS108-8TN for power supply 5 V ±10%
   - Specified values:
     - I_{GT_Q2} (25 °C) = 5 mA, V_{DD} = 5 V, V_{GT}(25 °C) = 1 V
   - Calculated values:
     - I_{GT_Q2} (0 °C) = 1.75 x I_{GT} (25 °C) = 8.75 mA,
     - V_{DDmin} = 0.9 x 5 V = 4.5 V,
     - V_{GT} (0 °C) = 1 + 0.05 V,
     - V_{OLmax} [25 °C, I_{GT} (0 °C)] = 0.55 V

   R_G is then given by:

$$R_G < \frac{4.5 - 1.05 - 0.55}{0.00875 \times 1.01} = 328\ \Omega \quad (2)$$

   The standard value of the resistor is 330 Ω, which is also sufficient for an accuracy of ±5%.
2. Example 2: STM32F103RB + Z0103 for 3.3 V ±5%
   - Specified values:
     - I_{GT} (25 °C)= 3 mA, V_{DD} = 3.3 V, V_{GT} (25 °C) = 1.3 V
   - Calculated values:
     - I_{GT} (0 °C) = 1.5 x I_{GT} (25 °C) = 4.5 mA,
     - V_{DDmin} = 0.95 x 3.3 V = 3.13 V,
     - V_{GT} (0 °C) = 1.3 + 0.05 V,
     - V_{OLmax} (I_G = 8 mA) = 0.4 V

   R_G is then given by:

$$R_G < \frac{3.13 - 1.35 - 0.4}{0.0045 \times 1.01} = 303\ \Omega \quad (3)$$

   The standard value of the resistor is 300 Ω. The value 270 Ω is sufficient for an accuracy of ±5%.
   We are focusing on the Q2/Q3 operation (refer to AN2703 for quadrant definition). For Q1/Q4 operation, "$V_{DDmin} - V_{OLmax}$" in Eq. (1) has to be replaced by V_{OHmin}. Usually V_{OHmin} is reached for minimum V_{DD}. Also, if a positive power supply is used (that is, the device works in Q1/Q4 quadrants), the required gate current is higher for Q4 operations (5 mA instead of 3 mA for other quadrants for Z0103), and the gate resistor has to be lower than 182 Ω (R_G < 182 Ω for $V_{OHmin} = V_{DDmin}$ –0.4 V).

2 Gate current variation

2.1 V_{GT} variation

The voltage drop of the gate junction V_{GT} varies with temperature and load current. The V_{GT} variation with temperature can be estimated as 2 mV/°C.

V_{GT} variation with load current is greater and so has a higher influence on gate current variation. For example, Figure 3 gives V_{GT} variation (dark blue curve) during an entire mains cycle for Z0103 with a 1 A 50 Hz RMS load current.

The characterization of the peak value reached by the gate to A1 (or COM) voltage (refer to "V_{GTpeak}" in Figure 3) is provided when the AC switch current reaches its peak value (refer to "I_{Tpeak}"). The measurements were taken under the following conditions:

- V_{DD} voltage level: 3.3 V
- R_G resistance: 200 Ω for Z0103 and 100 Ω for other devices

With these values and using the MCU (STM8S103K3), the gate current (for zero-load current) is 7.5 mA with the Z0103. This value is called "I_{G0}."

The V_{GT} variation with load current is larger and significant for a positive half-wave. The Figure 4 shows that V_{GT} becomes negative and its value drops to –84 mV with a 1.44 A I_T current.

This V_{GT} variation has a significant impact on the current consumption and cannot be neglected. See Figure 4 and Figure 5 for graphs of V_{GT} variation versus load current for Z0103 and ACS108-8TN.

Figure 3. V_{GT} variation with load current in quadrants 2 and 3 (0.2 A RMS) for Z0103 (T_j = 85 °C, I_{G0} = 7.5 mA)

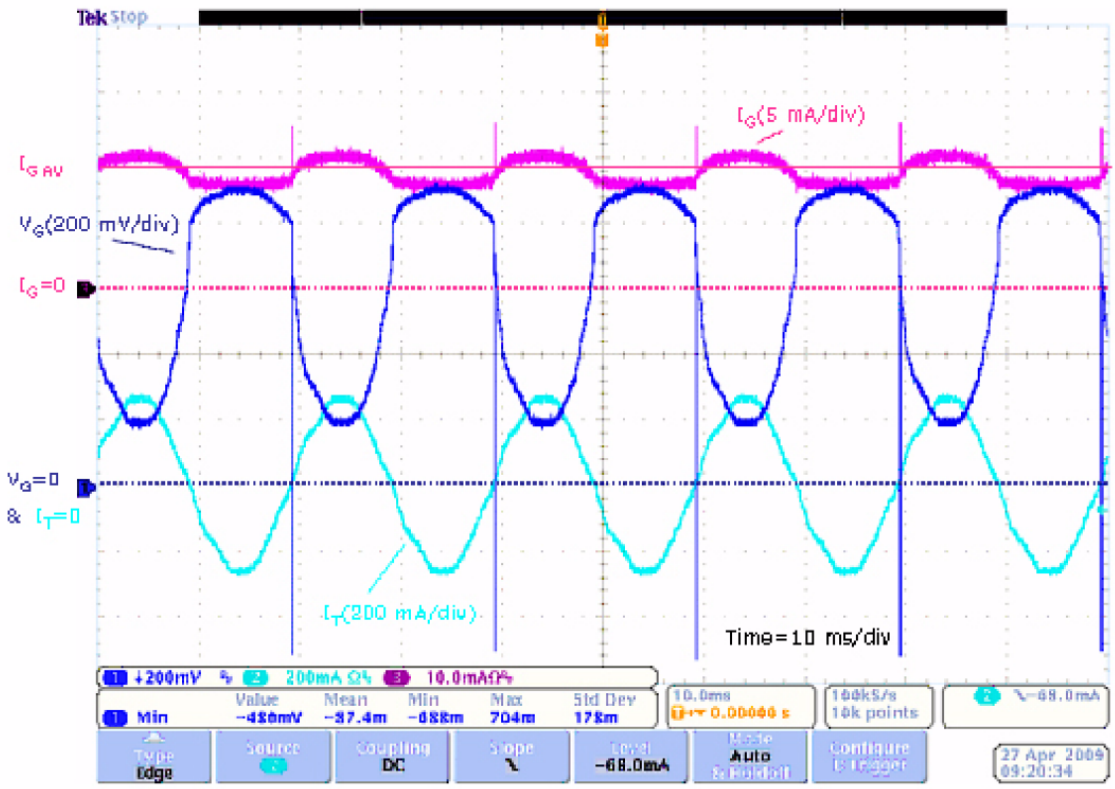


Figure 4. Typical V_{GTpeak} versus I_{Tpeak} for Z0103 (I_{G0} = 7.5 mA)

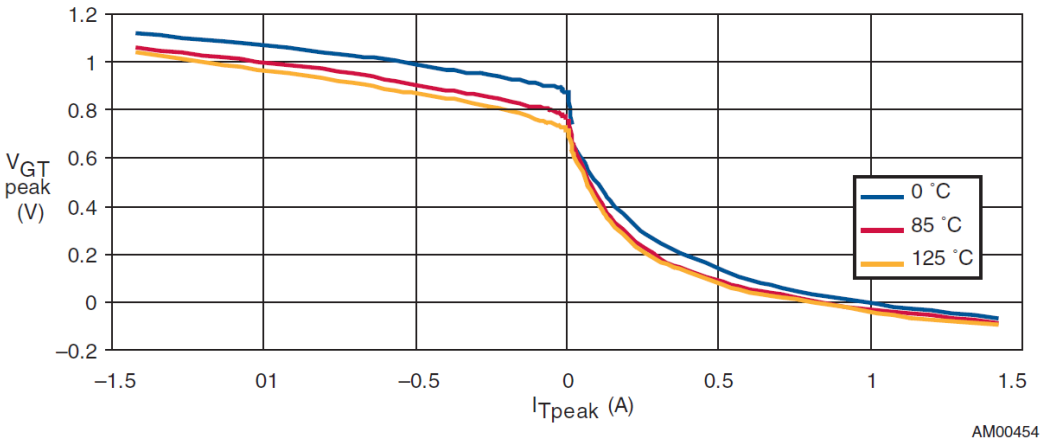
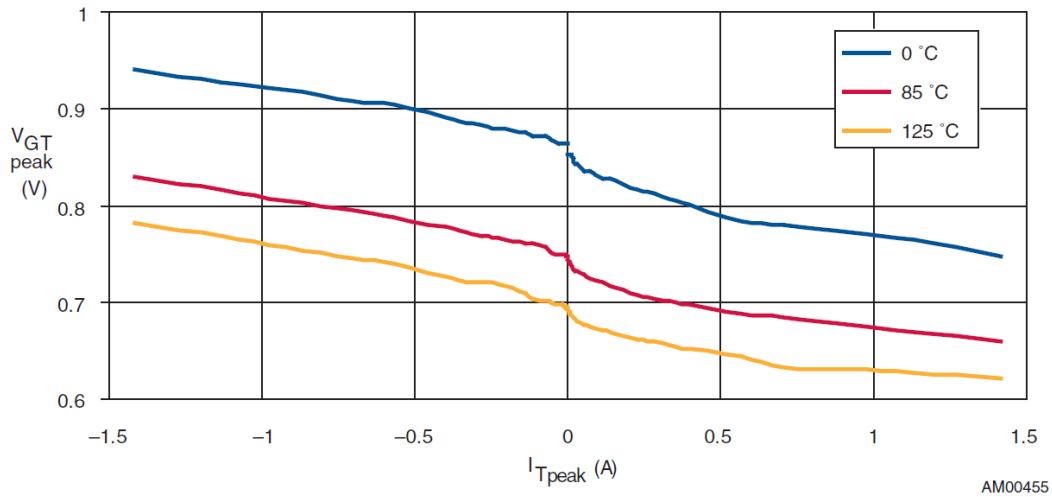


Figure 5. Typical V_{GTpeak} versus I_{Tpeak} for ACS108-8TN (I_{G0} = 15 mA)



2.2 Minimum current calculation

The minimum gate current that is applied depends on the selection of the standard value of the gate resistor (refer to Section 1.2.2) and the worst operating conditions.

The equation for estimating the minimum current is:

$$I_{G\,\min.} < \frac{V_{DD\min} - V_{GT\max} - V_{OL\max}}{1.01 \times R_G} \quad (4)$$

The maximum V_{GT} value has to be specified for the calculation. As Z0103 devices can be used with an RMS load current up to 1 A, the maximum V_{GT} value is taken into account forcurrent up to ±1.44 A. For ACS108-8TN a maximum RMS current of 0.8 A is used.

The Z01's maximum V_{GT} is then close to 1.1 V at 1.44 A peak load current in negative halfwave, for a 0 °C junction temperature (worst case). A maximum value of 1.3 V is used, as specified in the Z01 datasheet for 25 °C.

The ACS108's maximum absolute V_{GT} is close to 1 V for a 1.15 A peak load current, for a 0 °C junction temperature (worst case). A maximum value of 1 V is used, as specified in the ACS108-8TN datasheet for 25 °C.

Two examples are shown. The same components are used as those given in the Section 1.2.2. Note that different values than those specified in Table 1 could be used, especially if a different gate current is applied. Values are then taken from the MCU datasheet curves (for example.: STM8S10xxx).

1. MCU: STM8S with ACS108 -8TN for power supply 5 V ±10%
   - Specified values:
     - R_G =330 Ω, V_{DD} = 5 V, V_{GT} (25 °C) = 1 V
   - Calculated values:
     - $V_{DD\ min}$ = 0.9 x 5 V = 4.5 V
     - V_{GT} (0 °C) = 1 + 0.05 V
     - V_{OLmax} (25 °C, 16 mA) = 0.6 V

   I_{Gmin} is then given by:

   $$I_{G\min} < \frac{4.5 - 1.05 - 0.6}{1.01 \times 330} = 8.5mA \quad (5)$$

   The MCU is able to provide current that is above the minimum gate current for ambient temperature 0 °C. An estimation of V_{OLmax} has been provided for one high-sink I/O port of STM8S up to 16 mA. A standard I/O port could have lower current capability (10 mA), in which case several I/O ports have to be put in parallel.
2. STM32 + Z0103 for 3.3 V ±5%
   - Specified values:
     - R_G =300 Ω, V_{DD} = 3.3 V, V_{GT} (25 °C) = 1.3 V
   - Calculated values:
     - $V_{DD\ min}$ = 0.95 x 3.3 V = 3.13 V
     - V_{GT} (0 °C) = 0.05 + 1.3 V
     - V_{OLmax} (I_{GT} = 8 mA) = 0.4 V

   I_{Gmin} is then given by:

   $$I_{G\min} < \frac{3.13 - 1.35 - 0.4}{1.01 \times 300} = 4.6mA \quad (6)$$

   The MCU is able to provide current that is above the minimum gate current for ambient temperature 0 °C. An estimation of V_{OLmax} has been provided for one I/O port of STM32 (when 8 I/O ports are sunk with 8 mA each at the same time). If the current sunk by one I/O exceeds 8 mA, the value of 1.3 V should be used instead of 0.4 V.

2.3 Maximum current calculation

The maximum current that the MCU can handle is base on the following opposite conditions:

- Maximum supply voltage (V_{DDmax}),
- Minimum voltage drop of the gate junction (V_{GTmin}),
- Minimum gate resistor (0.99 x R_G),
- Minimum output low voltage (V_{OLmin}).

$$I_{G\,\max} < \frac{V_{DD\max} - V_{GT\min} - V_{OL\min}}{0.99 \times R_G} \quad (7)$$

As previously stated, a load RMS current of 1 A for Z0103 and 0.8 A for ACS108-8TN is used.

Z01's minimum V_{GT} is then close to –0.1 V at 1.44 A peak load current in positive half-wave and for a 125 °C junction temperature (worst case).

ACS108's minimum V_{GT} is close to 0.6 V for 1.15 A peak load current and for a 125 °C junction temperature (worst case).

Two examples are shown. The same components are used as those given in Section 1.2.2.

1. MCU: STM8S with ACS108 -8TN for power supply 5 V ±10%
   - Specified values:
     - R_G = 330 Ω, V_{DD} = 5 V, $V_{GT\ min}$(0.8 A) = 0.6 V
   - Calculated values:
     - $V_{DD\ max}$ = 1.1 x 5 V = 5.5 V
     - V_{OLmin} (I_{GT} = 20 mA) = 0.8 V

     I_{Gmax} is then given by:

$$I_{G\max} < \frac{5.5 - 0.6 - 0.8}{0.99 \times 330} = 12.5\,mA \quad (8)$$

   This result exceeds the maximum MCU current capability for one high-sink I/O port. This I_{Gmax} current can be sunk with 2 I/O ports in parallel. Estimation of V_{OLmin} has been provided for four high-sink I/O ports sinking at the same time 10 mA. V_{GTmin} depends on load current. A lower load current means higher V_{GTmin} and therefore lower I_{Gmax}.

2. STM32 + Z0103 for 3.3 V ±5%
   - Specified values:
     - RG = 300 Ω, VDD = 3.3 V, VGT min = –0.1 V
   - Calculated values:
     - $V_{DD\ max}$ = 1.05 x 3.3 V = 3.47 V
     - V_{OLmin} (I_{GT} = 8 mA) = 0.4 V

     I_{Gmax} is then given by:

$$I_{G\max} < \frac{3.47 - (-0.1) - 0.4}{0.99 \times 300} = 10.7\,mA \quad (9)$$

   The MCU is able to provide sufficient gate current. An estimation of V_{OLmin} has been provided for one I/O port of STM32 (when 8 I/O ports are sunk with 8 mA each at the same time).

2.4 Summary of calculations

This section summarizes the calculations for devices used in all examples.

ΔIG describes the difference between the maximum and minimum gate current, which has an impact on the power supply rating.

$$\Delta I_G = I_{G\max} - I_{G\min} \quad (10)$$

Average current consumption is based on the hypothesis that the maximum value is reached continuously during the half-cycle, that is, as if the gate current were a squared form. The maximum average gate current is then the average of the maximum values for a positive and negative half-wave:

$$I_{Gav\max} = \frac{1}{2}\left(I^{+}_{G\max} - I^{-}_{G\max}\right) \quad (11)$$

Where I^{+}_{Gmax} is the maximum gate current for a positive half-wave according to Eq. (7).

I^{-}_{Gmax} is the maximum gate current for negative half-wave and is calculated according to Eq. (7), using the V_{GTmin} value estimated in Section 2.2 Minimum current calculation for negative half-wave. It means that a V_{GTmin} of 1.05 V for Z0103 and 0.75 V for ACS108-8TN are used for calculating the maximum gate current in the negative half-wave.

Table 2. Current consumption of different devices and MCUs

	R_G (Ω) ±1%	I_{Gmin} (mA)	I_{Gmax} (mA)	ΔI_G (mA)	I_{Gavmax} (mA)
STM8S + ACS108-8, 5 V	330	8.6	12.5	4.0	12.3
STM8S + ACS108-8, 3.3 V	150	8.9	15.0 (1)	6.1	14.5
STM8S + Z0103, 5 V	590	4.6	8.9	4.3	7.9
STM8S + Z0103, 3.3 V	300	4.6	9.6	5.0	7.6
STM32 + ACS108-8, 3.3 V	150	9.2	17.7	8.5	17.2
STM32 + Z0103, 3.3 V	300	4.6	11.3	6.8	9.3

1. *This value exceeds the maximum allowed current capability for one high-sink I/0 port of STM8S with 3.3 V power supply (12 mA). Two pins must be used instead.*

MCUs with negative 3.3 V supply voltage can be used for triggering ACS/TRIACs, but this puts additional constraints on the power supply design. V_{GT} peak variation is already around 30% of V_{DD}, so it is mandatory to reduce V_{DD} ripple by precise control. For example a ±5% precision of the power supply has been taken into account and is appropriate according to our results. An SMPS + linear voltage regulator have to be used to achieve this accuracy (example VIPER16 + LM337).

MCUs with negative 5 V power supply have some advantages concerning power supply. Precision of ±10% is enough and can be achieved using a capacitive power supply or SMPS without additional regulation (example VIPER16, assuming a minimum output current 2 mA).

It should be noted that ACS devices are the better candidates for operation with a 3.3 V supply as the V_{GTpeak} variation is much lower than with triacs. Combined with a lower V_{DD} ripple, this helps to decrease the current consumption (maximum average gate current is 14.5 mA with 3.3 V).

Placing the pins in parallel is necessary to control the 10 mA gate current AC switches with a 3.3 V supply as the maximum gate current is 60 to 80% above the maximum allowed sunk current for the I/O MCU pin (for example: STM8S103xx).

For a 5 V supply, the maximum calculated gate current (around 12 mA) is below the maximum allowed I/O pin current. So, according to application conditions (min. ambient temperature, V_{DD} accuracy, etc.), a single pin could be used.

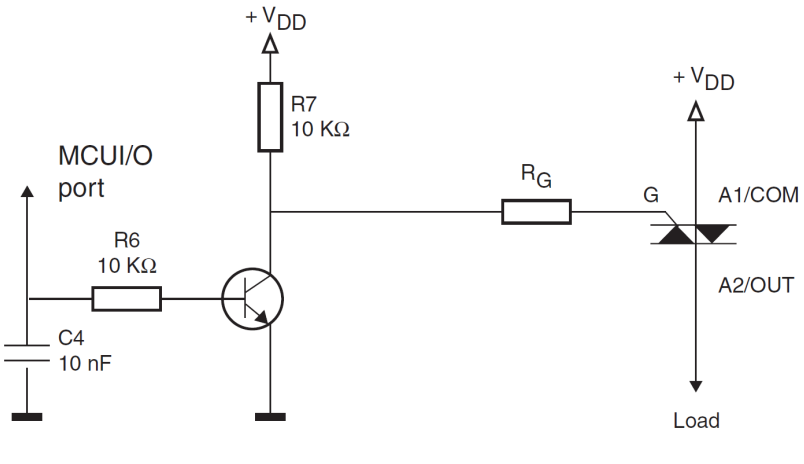
3 Proposed solutions

3.1 MCU current capability

The maximum current through the I/O port of the MCU can exceed the maximum current capability of the MCU. This is a hazardous state for the MCU and has to be prevented.

There are two principal solutions. The first solution is to use a buffer transistor (refer to Figure 6). This transistor takes over the gate current and the MCU I/O port controls only the base with current that is 50 to 100 times lower than the ACS/TRIAC gate current.

Figure 6. Schematics of using buffer transistor



The second solution is to put the I/O ports in parallel. The maximum number of I/O ports that can be paralled is limited by the application and MCU pin count. The maximum current must also not exceed the maximum current capability of the MCU through the GND pin (150 mA for STM32, 80 mA for STM8S with 3.3 V power supply or 160 mA for STM8S with 5 V power supply).

3.2 Average current consumption

The average consumption shown in Table 2 is given for gate control lasting an entire period. The consumption is in this case high. Contrary to the use of relay, it is possible to decrease current consumption by reducing the gate pulse length, which is useful when several ACS/TRIACs are controlled at the same time (for example several small pumps or valves). Refer to AN302 and AN303 for more information on triac pulse gate control.

4 Conclusion

MCUs supplied from negative 3.3 V power supplies are good replacements of 5 V supplied MCUs for the control of ACS/TRIACs.

It is possible to design gate control circuits that provide enough current for triggering the ACS/TRIAC. Calculations of proper gate resistors have been provided.

The variation of V_{GT} has a significant influence on circuit behavior for a 3.3 V power supply. The ACS devices have a lower V_{GT} variation and so are preferred for operation with a 3.3 V supply. They do indeed allow the power supply consumption to be reduced compared to triacs.

The design of a 3.3 V power supply has to achieve a good accuracy (±5%) to reduce gate current variation. A capacitive power supply cannot provide the accuracy required. An SMPS with additional regulation has to be used.

The maximum gate current must meet MCU operating conditions. Refer to the maximum I/O port current capability. The maximum current capability for any I/O of the STM32 port is 20 mA. One I/O pin to control the Z0103 is sufficient. Putting the I/O ports in parallel to control the less sensitive devices is possible and could also be implemented.

The maximum MCU GND current capability is another parameter that has to be met. The STM32's current capability is 150 mA. The STM8S has different current capabilities for different power supply ratings: 160 mA for a 5 V power supply, and 80 mA for a 3.3 V power supply.

The average gate current consumption has to meet the capability of the power supply current. The average gate current can be reduced using pulse gate control. This is especially efficient for boards where several ACSs or triacs are controlled at the same time.

Revision history

Table 3. **Document revision history**

Date	Revision	Changes
15-Jul-2009	1	Initial release.
06-Sep-2023	2	Updated Section 1.2.2 Gate resistor calculation, and Section 2 Gate current variation. Minor text changes.

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