

## Introduction

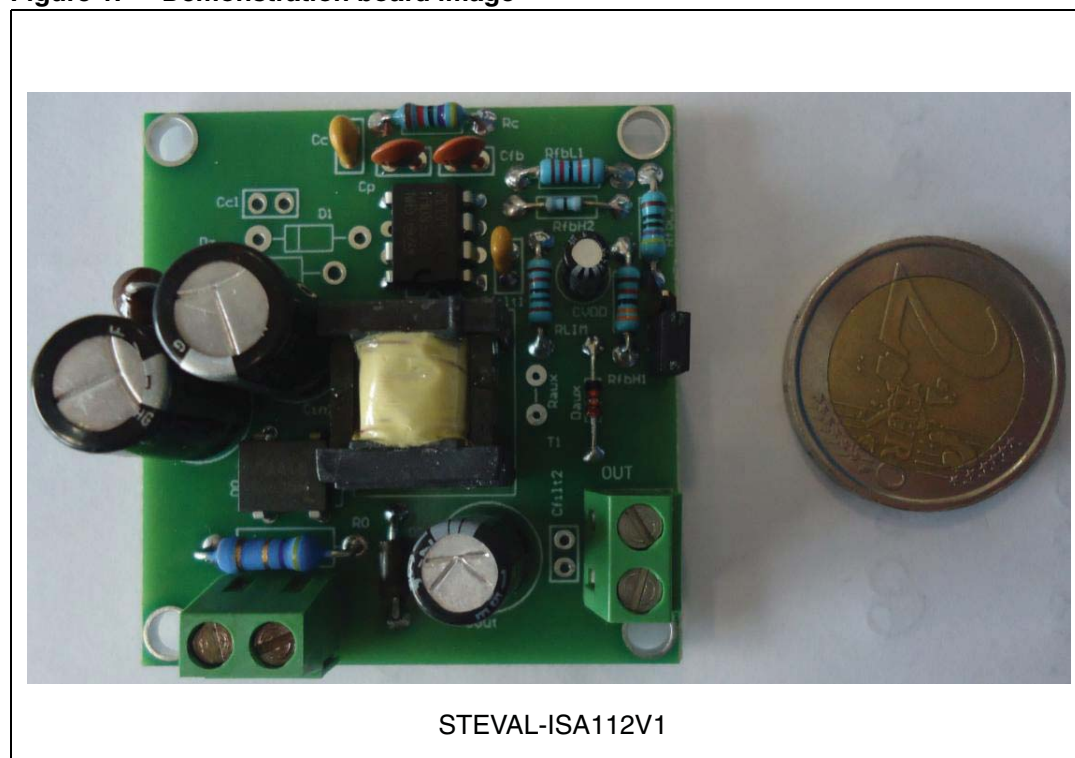
This document describes a 12 V-350 mA power supply set in non-isolated flyback topology with the VIPER06, a new offline high voltage converter by STMicroelectronics.

The features of the device are:

- 800 V avalanche rugged power section
- PWM operation at 115 kHz with frequency jittering for lower EMI
- limiting current with adjustable set point
- onboard soft-start
- safe auto-restart after a fault condition (overload, short-circuit)

The VIPER06 does not require a biasing circuit to operate because the IC can be supplied by an internal current generator, therefore saving the cost of the transformers auxiliary winding. If the device is biased through an auxiliary winding, the demonstration board can reach very low standby consumption (< 30 mW at 230 V<sub>AC</sub>, with output load disconnected). Both cases are treated in the present document. The available protections are: thermal shutdown with hysteresis, delayed overload protection, open loop failure protection (the last is available only if self-biasing is excluded).

**Figure 1. Demonstration board image**



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# 1 Adapter features

The electrical specifications of the demonstration board are listed below in [Table 1](#).

**Table 1. Electrical specifications**

Parameter	Symbol	Value
Input voltage range	$V_{IN}$	[90 V <sub>AC</sub> ; 265 V <sub>AC</sub> ]
Output voltage	$V_{OUT}$	12 V
Max. output current	$I_{OUT}$	0.35 A
Precision of output regulation	$\Delta V_{OUT\_HF}$	± 5%
High frequency output voltage ripple	$\Delta V_{OUT\_HF}$	50 mV
Max. ambient operating temperature	$T_{AMB}$	60 °C

## 2 Circuit description

The power supply is set in flyback topology. The schematic is given in [Figure 2](#) and the bill of materials in [Table 2](#). The input section includes a resistor R0 for inrush current limiting and a diode bridge (D0) and Pi filter for EMC suppression (Cin1, Lin, Cin2). The transformer core is a standard E13. The output voltage value is set in a simple way through the RfbH-RfbL voltage divider between the output terminal and the FB pin, according to the following formula:

**Equation 1**

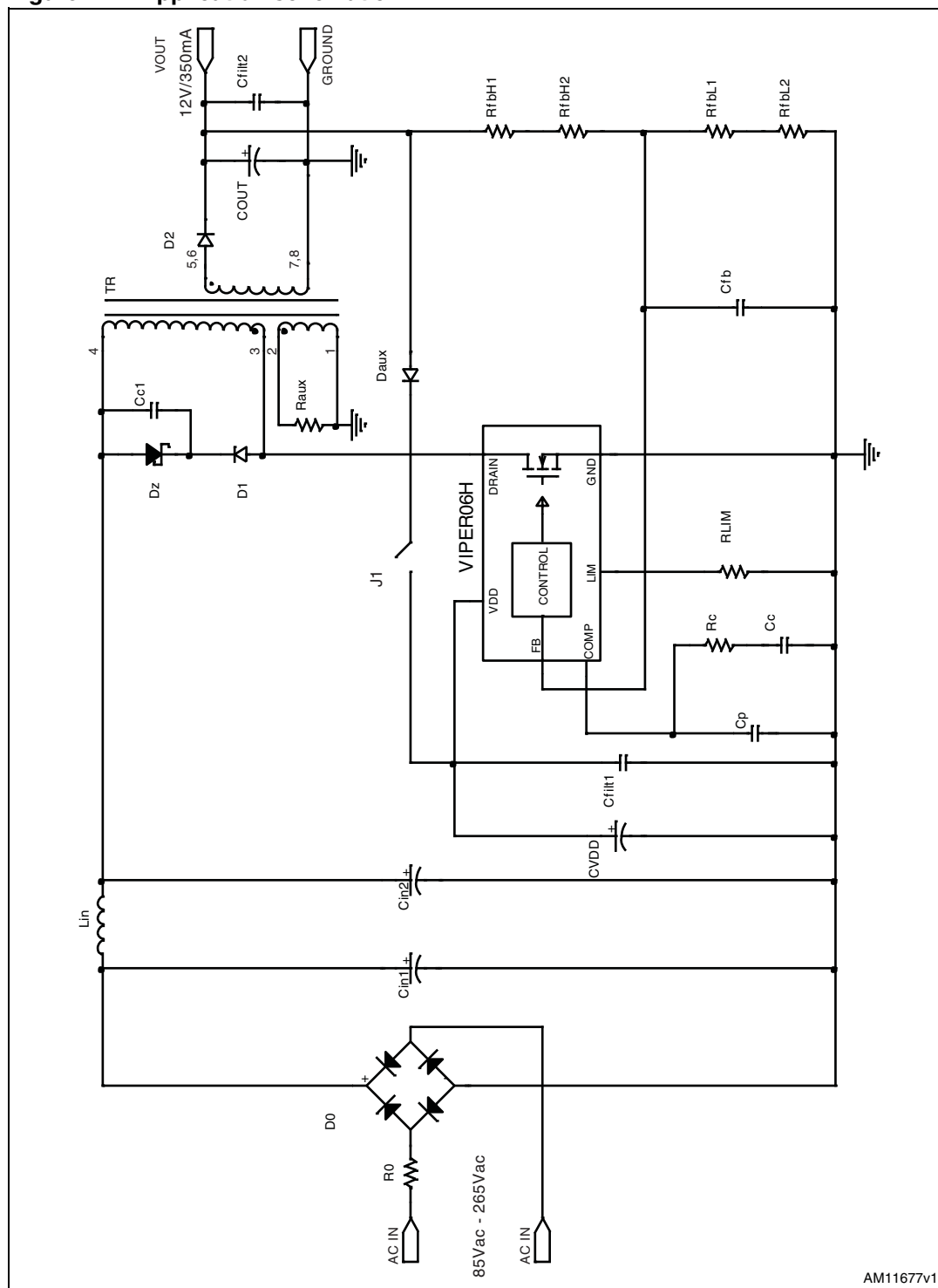
$$V_{OUT} = 3.3 \cdot \left( 1 + \frac{R_{fbH}}{R_{fbL}} \right)$$

In fact, the FB pin is the input of an error amplifier and is an accurate 3.3 V voltage reference. In the schematic the upper resistor RfbH has been split into RfbH1 and RfbH2; and the lower resistor RfbL into RfbL1 and RfbL2 in order to allow a better tuning of the output voltage value. The compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin and is made up of Cp, Cc and Rc. The resistor RLIM, placed between the LIM and GND pins, has the purpose of reducing the drain current limitation, from IDLIM to about 250 mA in order to limit the deliverable output power of the converter and keep the power components safe. At power-up, as the rectified input voltage rises over the V<sub>DRAINSTART</sub> threshold, the high voltage current generator starts charging the VDD capacitor, CVDD, from 0 V up to VDD<sub>ON</sub>. At this point the Power MOSFET starts switching, the HV current generator is turned off and the IC is biased by the energy stored in CVDD. In this demonstration board, if jumper J1 is not selected, the IC is biased through the internal high voltage startup current generator, which is automatically turned on as the VDD voltage drops to VDD<sub>CS\_ON</sub> and switched off as VDD is charged up to VDD<sub>ON</sub> (self-biasing). The use of self-biasing means higher power dissipation and must be avoided if low standby consumption is required. Self-biasing is excluded by keeping the VDD pin voltage always above the VDD<sub>CS\_ON</sub> threshold. In this board, since the output voltage is higher than VDD<sub>CS\_ON</sub>, this is obtained selecting jumper J1, which

connects the output terminal to the VDD through a small signal diode. If the output voltage is lower than  $VDD_{CS\_ON}$ , the self-biasing can be excluded only using an auxiliary winding. The IC biasing through auxiliary winding or through the output is referred to as external biasing. In [Figure 3](#) the VDD waveforms for both cases (IC external biased and self-biased) are shown.

### 3 Schematic and bill of material

**Figure 2. Application schematic**



**Table 2. Bill of material**

Ref.	Part	Description	Manufacturer
Cin1		3.3 $\mu$ F, 400 V NHG series electrolytic capacitor	
Cin2		3.3 $\mu$ F, 400 V NHG series electrolytic capacitor	
CVDD		1 $\mu$ F, 50 V electrolytic capacitor	
Cfilt1		100 nF, 50 V ceramic capacitor	
Cc		10 nF, 50 V ceramic capacitor	
Cp		1 nF, 50 V ceramic capacitor	
Cfb		1 nF, 50 V ceramic capacitor	
Cout		330 $\mu$ F, 16 V ZL series ultra-low ESR electrolytic capacitor	Rubycon
Ccl	Not mounted		
Cfilt2	Not mounted		
D0	DF06M	600 V, 1 A diode bridge	Vishay
D1	Not mounted		
D2	STPS2H100	100 V, 2 A, power Schottky rectifier	ST
Daux	1N4148	Small signal diode	
Dz	Not mounted		
R0		4.7 $\Omega$ 3/4 W resistor	
RLIM		15 k $\Omega$ 5% 1/4 W resistor	
Rc		47 k $\Omega$ 5% 1/4 W resistor	
RfbH1		33 k $\Omega$ 1% 1/4 W resistor	
RfbH2		0 $\Omega$	
RfbL1		12 k $\Omega$ 1% 1/4 W resistor	
RfbL2		0.47 k $\Omega$ 1% 1/4 W resistor	
Raux	Not mounted		
IC1	VIPer06HN	Offline high voltage PWM controller	ST
T1	1921.0040	Transformer	Magnetica
Lin	B82144A2105J000	1 mH inductor LBC series	Epcos

Figure 3. VDD waveforms IC externally biased (J1 selected)

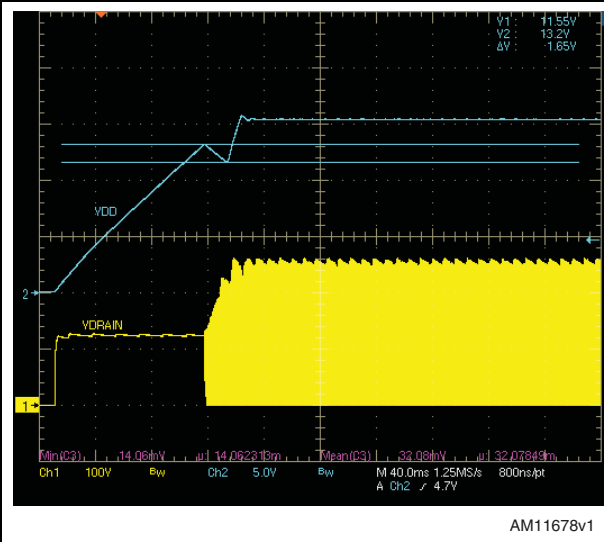
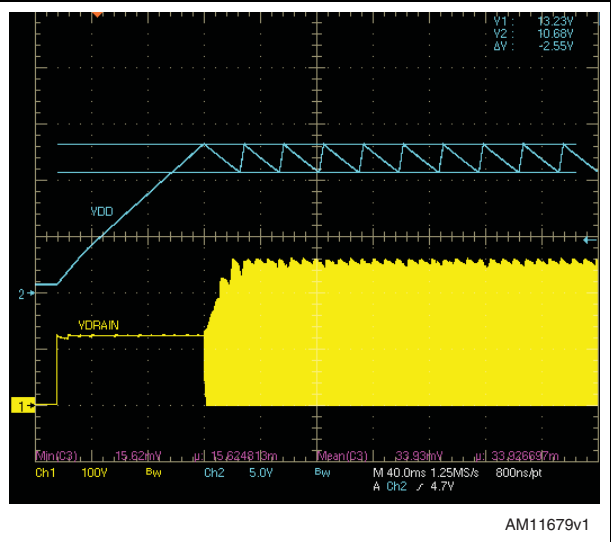


Figure 4. VDD waveforms IC self-biased (J1 not selected)



# 4 Transformer

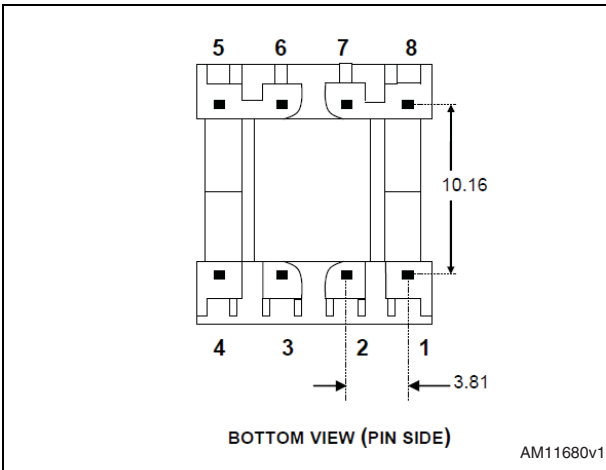
The transformer characteristics are listed in the table below.

**Table 3. Transformer characteristics**

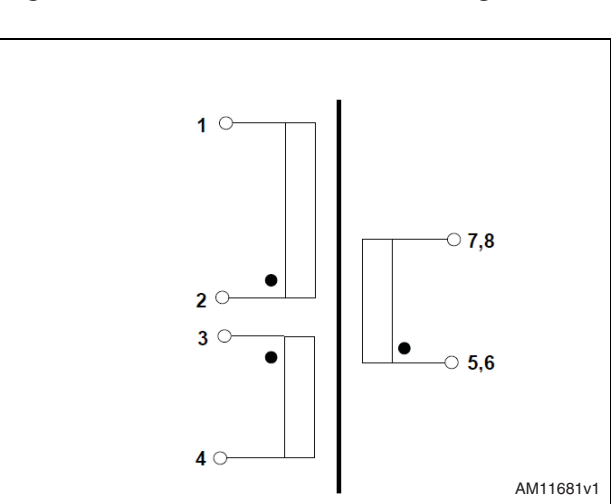
Parameter	Value	Test conditions
Manufacturer	Magnetica	
Part number	1921.0040	
Primary inductance (pins 3 - 4)	1.2 mH $\pm$ 15%	Measured at 1 kHz 0.1 V
Leakage inductance	2.8%	Measured at 10 kHz 0.1 V
Primary to secondary turn ratio (3 - 4)/(5 - 8)	6.11 $\pm$ 5%	Measured at 10 kHz 0.1 V
Primary to auxiliary turn ratio (3 - 4)/(2 - 1)	5 $\pm$ 5%	Measured at 10 kHz 0.1 V

The following figures show size and pin distances ([mm]) of the transformer.

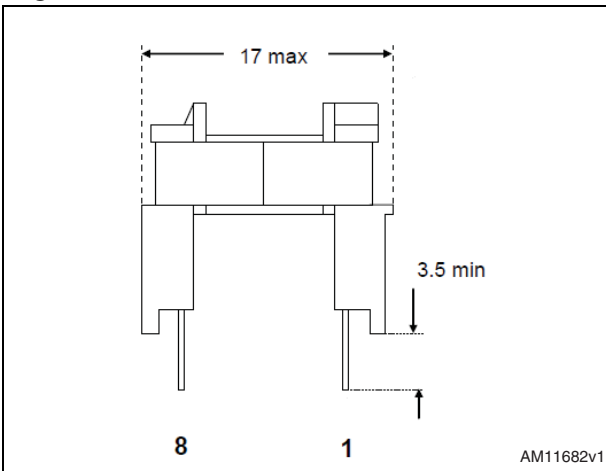
**Figure 5. Transformer size and pin diagram pin distances**



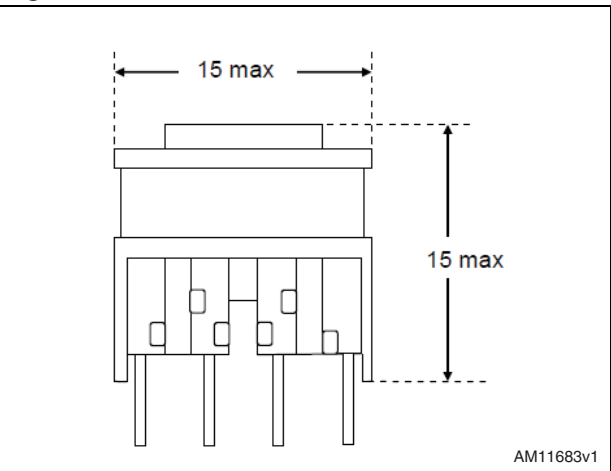
**Figure 6. Transformer electrical diagram**



**Figure 7. Transformer side view 1**



**Figure 8. Transformer side view 2**

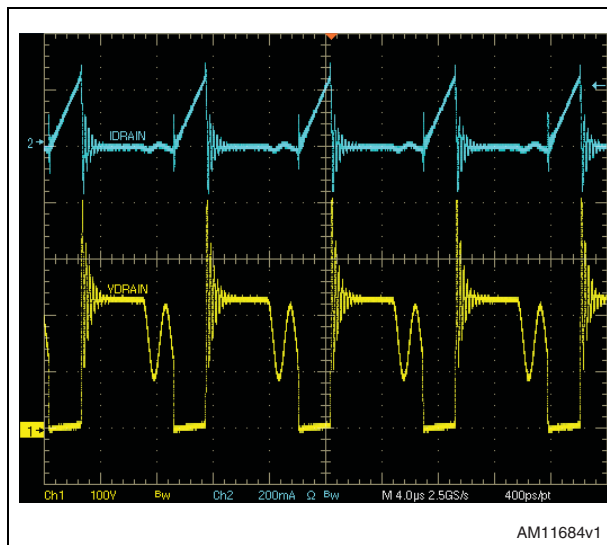


## 5 Testing the board

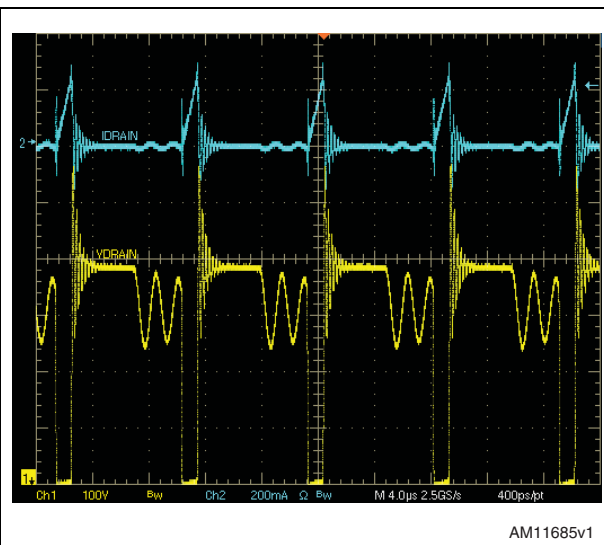
### 5.1 Typical waveforms

Drain voltage and current waveforms in full load condition are reported for the two nominal input voltages in [Figure 9](#) and [10](#), and for minimum and maximum input voltage in [Figure 11](#) and [12](#) respectively.

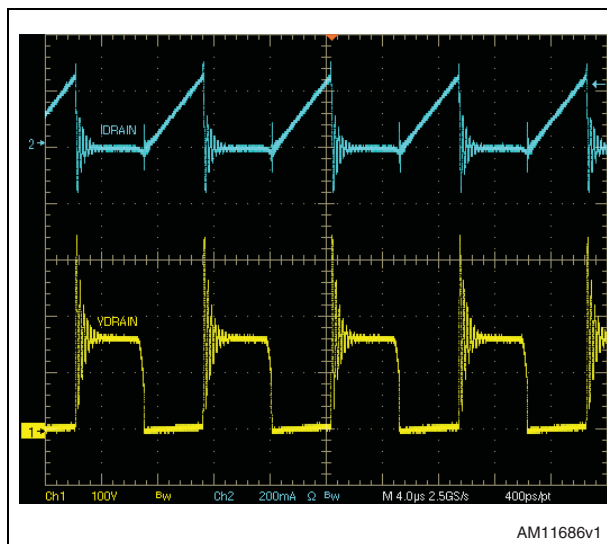
**Figure 9. Drain current/voltage @ 115 V<sub>AC</sub> max. load**



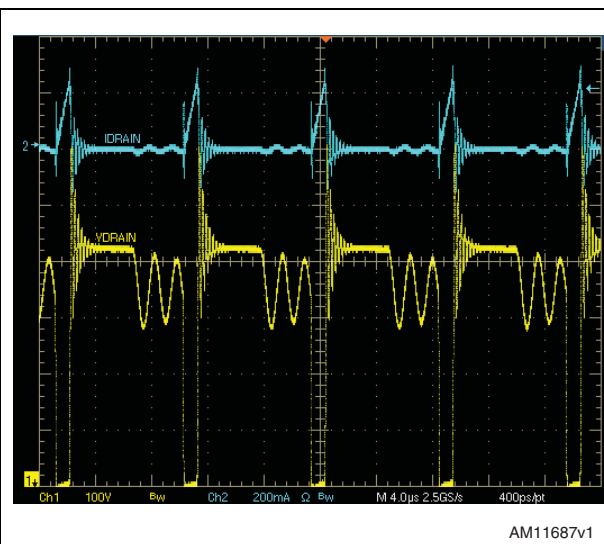
**Figure 10. Drain current/voltage @ 230 V<sub>AC</sub> max. load**



**Figure 11. Drain current/voltage @ 90 V<sub>AC</sub> max. load**



**Figure 12. Drain current/voltage @ 265 V<sub>AC</sub> max. load**



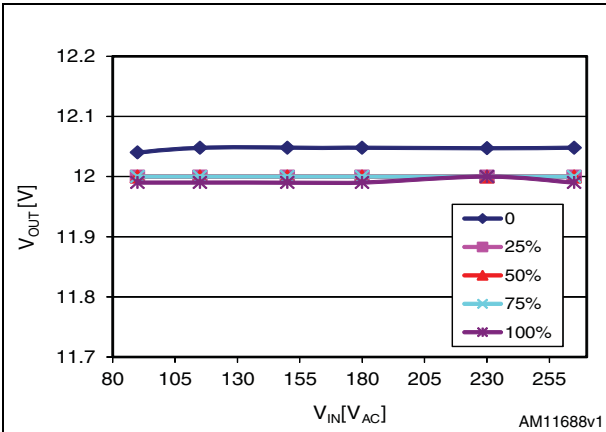
# 5.2 Precision of the regulation and output voltage ripple

The output voltage of the board has been measured in different line and load conditions with the results shown in [Table 4](#). The output voltage is practically not affected by the line condition and by the IC biasing (self-supply or not).

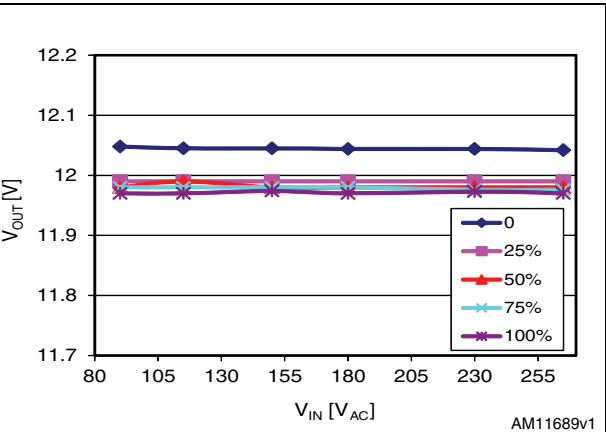
**Table 4. Output voltage line-load regulation**

$V_{IN}$ [V <sub>AC</sub> ]	$V_{OUT}$ [V]							
	No load		50% load		75% load		100% load	
	IC externally biased	IC self-biased	IC externally biased	IC self-biased	IC externally biased	IC self-biased	IC externally biased	IC self-biased
90	12.04	12.05	12.00	11.98	12.00	11.98	11.99	11.97
115	12.05	12.05	12.00	11.99	12.00	11.98	11.99	11.97
150	12.05	12.05	12.00	11.98	12.00	11.98	11.99	11.97
180	12.05	12.04	12.00	11.98	12.00	11.98	11.99	11.97
230	12.05	12.04	12.00	11.98	12.00	11.98	11.99	11.97
265	12.05	12.04	12.00	11.98	12.00	11.98	11.99	11.97

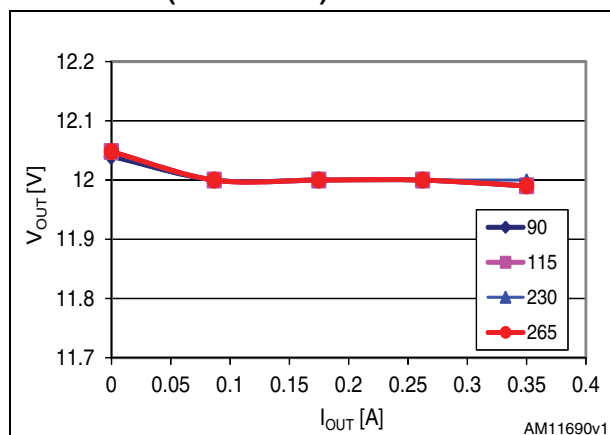
**Figure 13. Line regulation at different loads; IC externally biased (J1 selected)**



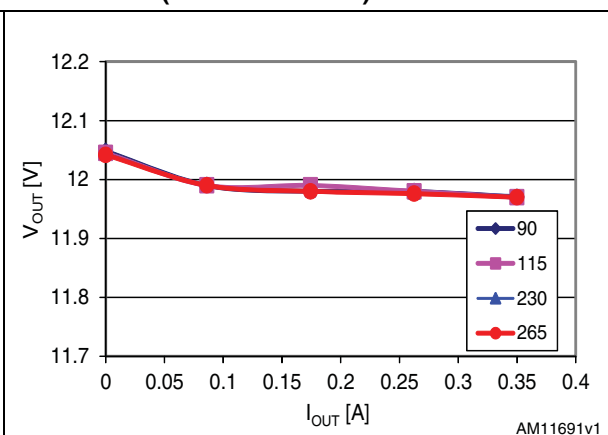
**Figure 14. Line regulation at different loads; IC self-biased (J1 not selected)**



**Figure 15. Load regulation at different input voltages; IC externally biased (J1 selected)**



**Figure 16. Load regulation at different input voltages; IC self-biased (J1 not selected)**

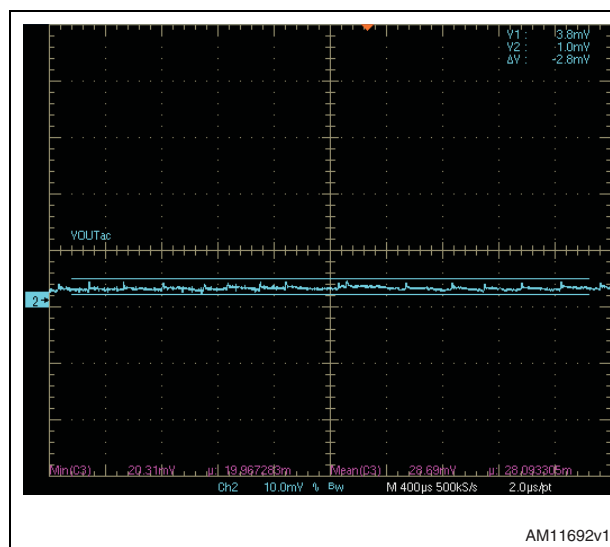


### 5.3 Burst mode and output voltage ripple

When the converter is lightly loaded, the COMP pin voltage decreases. As it reaches the shutdown threshold,  $V_{COMPL}$  (1.1 V, typical), the switching is disabled and no more energy is transferred to the secondary side. So, the output voltage decreases and the regulation loop makes the COMP pin voltage increase again. As it rises 40 mV above the  $V_{COMPL}$  threshold, the normal switching operation is resumed. This results in a controlled on/off operation which is referred to as “burst mode”. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected, making it easier to comply with energy saving regulations.

The figures below show the output voltage ripple when the converter is no/lightly loaded and supplied with 115 V<sub>AC</sub> and 230 V<sub>AC</sub> respectively.

**Figure 17. Output voltage ripple @ 115 V<sub>AC</sub> no load**



**Figure 18. Output voltage ripple @ 230 V<sub>AC</sub> no load**

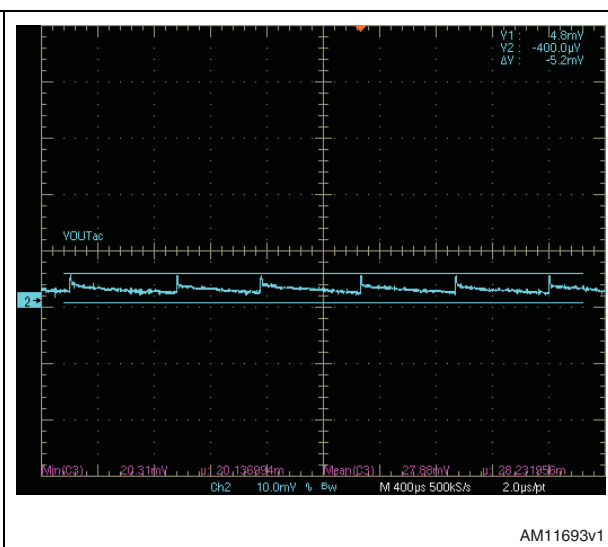


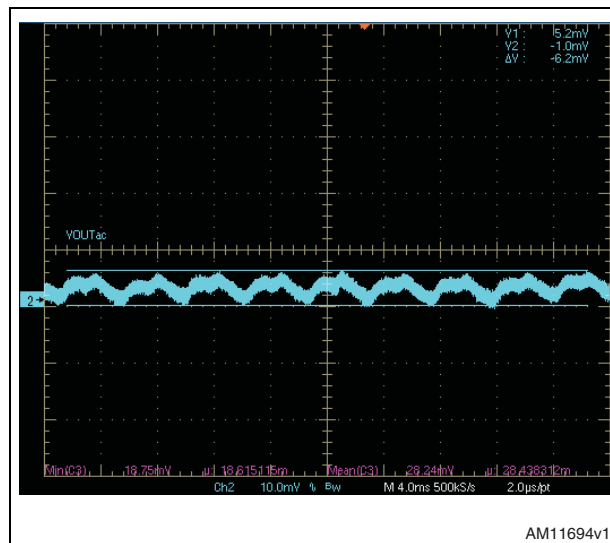
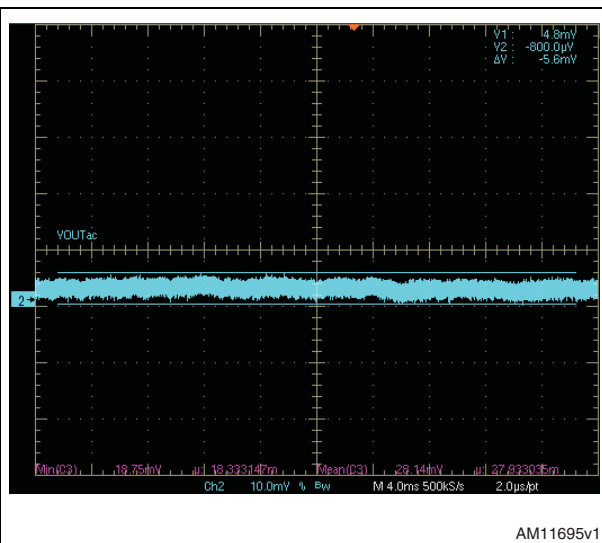
Figure 19. Output voltage ripple @ 115 V<sub>AC</sub>  
25 mAFigure 20. Output voltage ripple @ 230 V<sub>AC</sub>  
25 mA

Table 5 shows the measured value of the burst mode frequency ripple measured in different operating conditions. The ripple in burst mode operation is very low.

Table 5. Output voltage ripple at no/light load

V <sub>IN</sub> [V <sub>AC</sub> ]	V <sub>OUT</sub> [mV]	
	No load	25 mA load
90	2	7
115	2	7
230	4	8
265	4	9

## 5.4 Efficiency

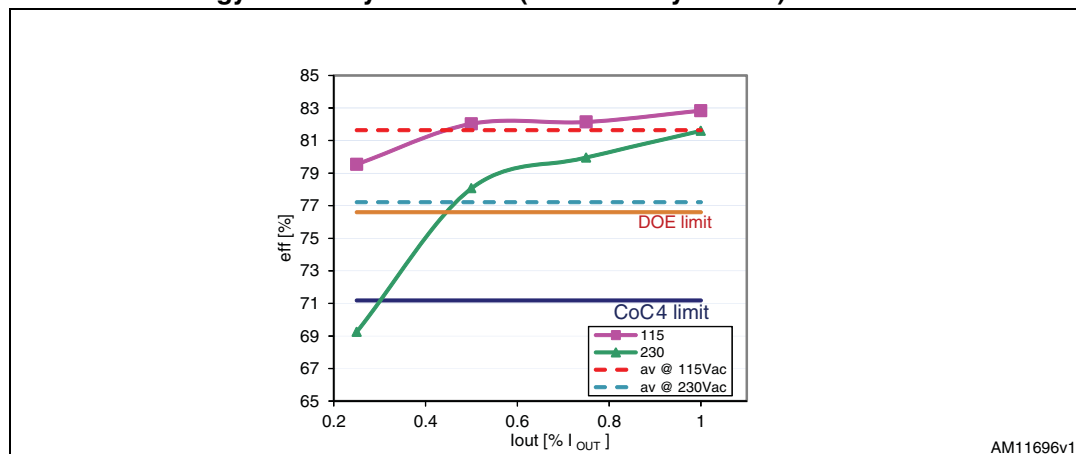
The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltage ( $V_{IN} = 115 V_{AC}$  and  $V_{IN} = 230 V_{AC}$ ).

External power supplies (the power supplies which are contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct (version 4) “Active Mode Efficiency” criterion, which states an active mode efficiency higher than 71.18% for a power throughput of 4.2 W.

Another standard to be applied to external power supplies in the coming years is the DOE (Department of Energy) recommendation, whose active mode efficiency requirement for the same power throughput is 76.6%.

If the IC is externally biased, the presented demonstration board is compliant with both standards, as can be seen from Figure 21, where the average efficiencies of the board at 115 V<sub>AC</sub> (81.6%) and at 230 V<sub>AC</sub> (77.2%) are plotted with dotted lines, together with the above limits. In the same figure the efficiency at 25%, 50%, 75% and 100% of output load for both input voltages is also shown.

**Figure 21. Active mode efficiency of the demonstration board and comparison with energy efficiency standards (IC externally biased)**



## 5.5 Light load performance

The input power of the converter has been measured in no load condition for different input voltages and the results are reported in [Table 6](#).

**Table 6. No load input power**

$V_{IN}$ [V <sub>AC</sub> ]	$P_{IN}$ [mW]	
	IC externally biased	IC self-biased
90	17.2	108
115	18.3	137
150	20.2	178
180	22.1	213
230	25.9	273
265	28.5	314

In version 4 of the Code of Conduct, also the power consumption of the power supply when it is no loaded is considered. The criteria to be compliant with are reported in [Table 7](#) below:

**Table 7. Energy consumption criteria for no load**

Nameplate output power ( $P_{no}$ )	Maximum power in no load for AC-DC EPS
$0\text{ W} \leq P_{no} \leq 50\text{ W}$	$< 0.3\text{ W}$
$50\text{ W} < P_{no} < 250\text{ W}$	$< 0.5\text{ W}$

The performance of the presented board (when the self-supply function is not used) is much better than required; the power consumption is more than ten times lower than the limit fixed by version 4 of the Code of Conduct. Even though the performance seems to be

disproportionally better than requirements, it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirements about no load consumption and if the converter is used as an auxiliary power supply, the line filter is often the big line filter of the entire power supply that increases greatly the standby consumption.

Even though version 4 of the Code of Conduct does not have other requirements regarding light load performance, in order to give a more complete overview, we report the input power and efficiency of the demonstration board also in two other low load cases. [Table 8](#) and [14](#) show the performance when the output load is 25 mW and 50 mW respectively.

**Table 8. Light load performance  $P_{OUT}=25$  mW**

$V_{IN}$ [V <sub>AC</sub> ]	$P_{OUT}$ [mW]	$P_{IN}$ [mW]		Efficiency (%)	
		IC externally biased	IC self-biased	IC externally biased	IC self-biased
90	25	49.7	128	50.30	19.6
115	25	51.5	157	48.54	15.9
150	25	54.7	200	45.70	12.5
180	25	57.3	236	43.63	10.6
230	25	61.7	296	40.52	8.4
265	25	64.8	337	38.58	7.4

**Table 9. Light load performance  $P_{OUT}=50$  mW**

$V_{IN}$ [V <sub>AC</sub> ]	$P_{OUT}$ [mW]	$P_{IN}$ [mW]		Efficiency (%)	
		IC externally biased	IC self-biased	IC externally biased	IC self-biased
90	50	82.4	167	60.71	29.94
115	50	85.0	198	58.82	25.25
150	50	89.3	242	55.99	20.66
180	50	93.0	280	53.76	17.86
230	50	98.0	341	51.02	14.66
265	50	101.1	384	49.46	13.02

The input power vs. input voltage for no and light load conditions ([Table 7](#), [8](#) and [14](#)) are reported in the diagrams below.

Figure 22.  $P_{IN}$  vs.  $V_{IN}$  at no load and light load; IC externally biased (J1 selected)

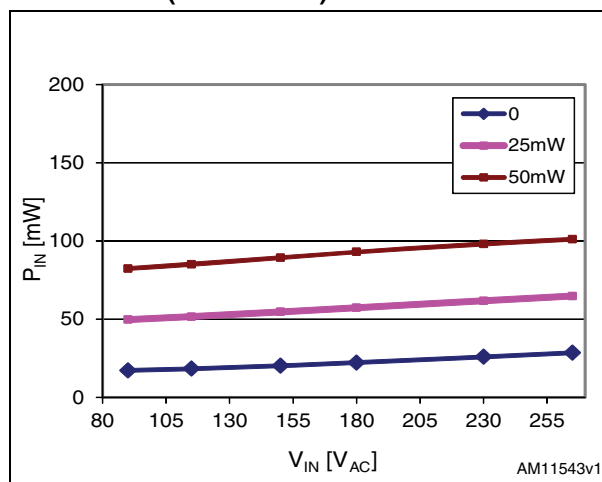
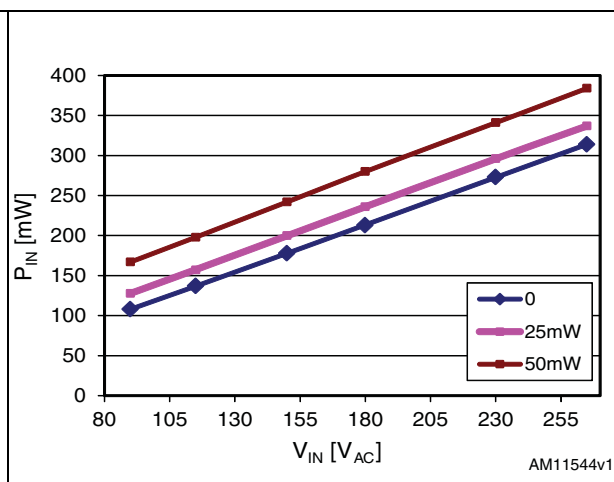


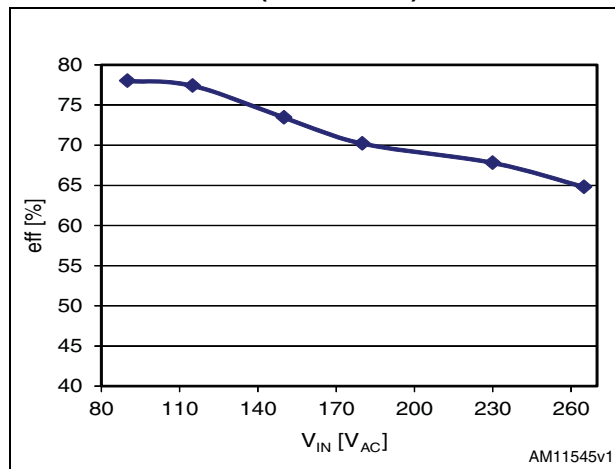
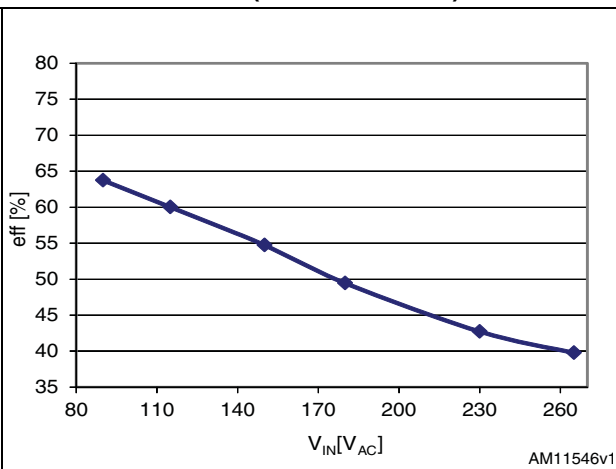
Figure 23.  $P_{IN}$  vs.  $V_{IN}$  at no load and light load, IC self-biased (J1 not selected)



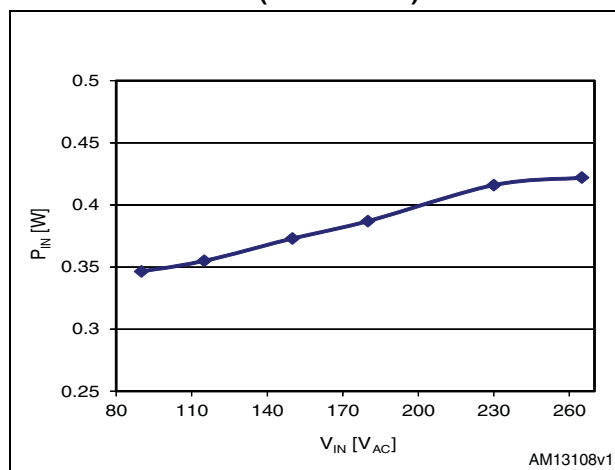
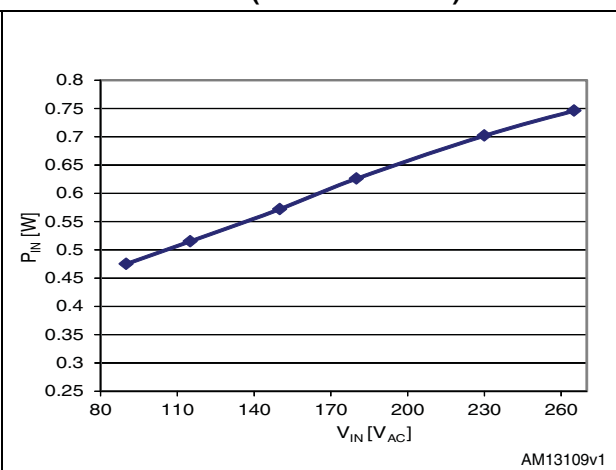
Depending on the equipment supplied, we can have several criteria to measure the standby or light load performance of a converter. One of these is the measurement of the output power when the input power is equal to one watt. In [Table 10](#) the output power needed to have 1 W of input power in different line conditions is reported. [Figure 24](#) and [25](#) show the diagram of the output powers corresponding to  $P_{IN} = 1$  W for different values of the input voltage.

Table 10.  $P_{OUT}$  @  $P_{IN}=1$  W

$V_{IN}$ [V <sub>AC</sub> ]	$P_{IN}$ [W]	$P_{OUT}$ [W]		Efficiency (%)	
		IC externally biased	IC self-biased	IC externally biased	IC self-biased
90	1	0.78	0.64	78	64
115	1	0.77	0.60	77	60
150	1	0.73	0.55	73	55
180	1	0.70	0.49	70	49
230	1	0.68	0.43	68	43
265	1	0.65	0.40	65	40

**Figure 24. Efficiency @  $P_{IN}=1$  W; IC externally biased (J1 selected)****Figure 25. Efficiency @  $P_{IN}=1$  W; IC self-biased (J1 not selected)**

Another requirement (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The performance is shown in [Figure 26](#) for IC externally biased and in [Figure 27](#) for self-biasing.

**Figure 26.  $P_{IN}$  @  $P_{OUT} = 250$  mW; IC externally biased (J1 selected)****Figure 27.  $P_{IN}$  @  $P_{OUT} = 250$  mW; IC self-biased (J1 not selected)**

## 6 Functional check

### 6.1 Soft-start

At startup the current limitation value reaches IDLIM after an internally fixed time,  $t_{SS}$ , whose typical value is 8.5 msec. This time is divided into 16 time intervals, each corresponding to a current limitation step progressively increasing. In this way the drain current is limited during the output voltage increase, therefore reducing the stress on the secondary diode.

The soft-start phase is shown in [Figure 28](#) and [29](#).

Figure 28. Soft-start at startup

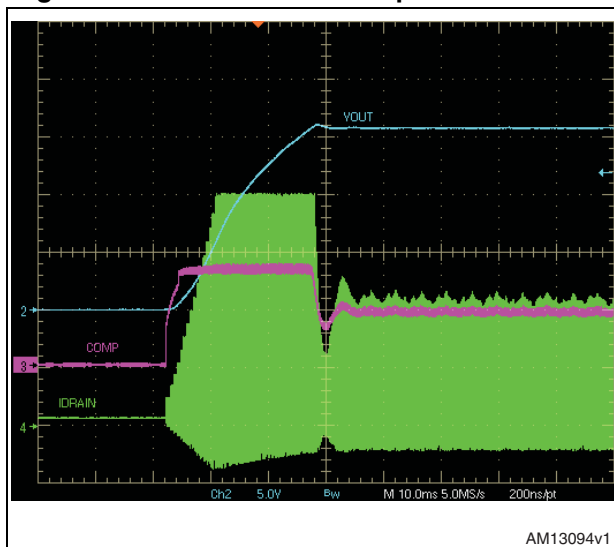
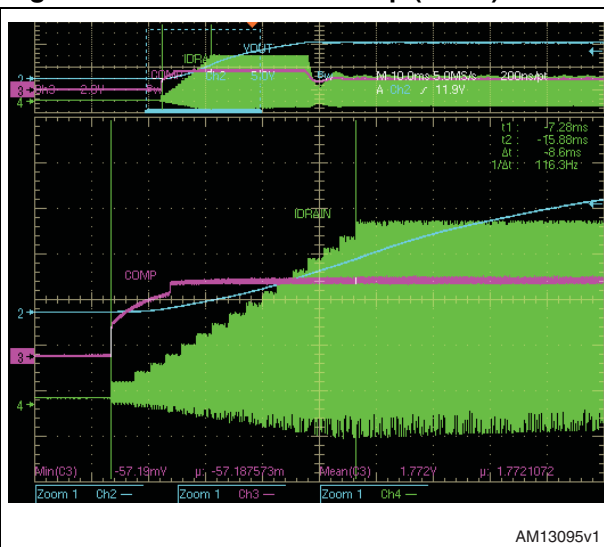


Figure 29. Soft-start at startup (zoom)



### 6.2 Overload protection

In the case of overload or short-circuit (see [Figure 38](#)), the drain current reaches the IDLIM value (or the one set by the user through the RLIM resistor). In every cycle where this condition is met, a counter is incremented; if it is maintained continuously for the time  $t_{OVL}$  (50 msec typical, internally fixed), the overload protection is tripped, the power section is turned off and the converter is disabled for a  $t_{RESTART}$  time (1sec typical). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way ([Figure 31](#)). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoids the IC overheating in the case of repeated overload events.

Furthermore, every time the protection is tripped, the internal soft startup function is invoked ([Figure 32](#)), in order to reduce the stress on the secondary diode.

After the short removal, the IC resumes normal working. If the short is removed during  $t_{SS}$  or  $t_{OVL}$ , i.e. before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during  $t_{RESTART}$ , the IC must wait for the  $t_{RESTART}$  period to elapse before switching is resumed ([Figure 33](#)).

Figure 30. Output short-circuit applied: OLP tripping

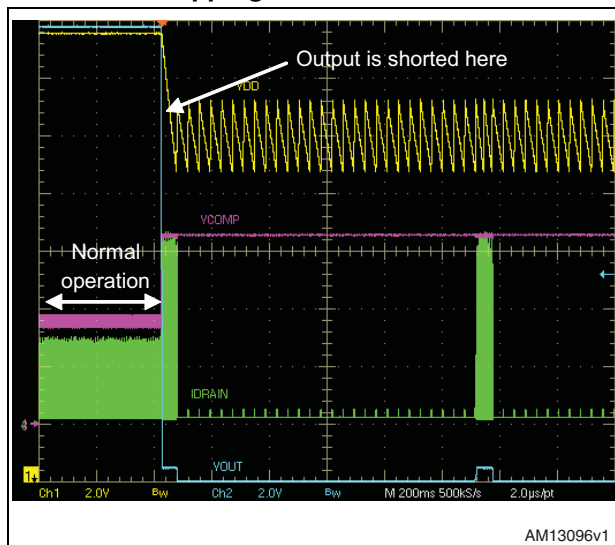


Figure 31. Output short-circuit maintained: OLP steady-state

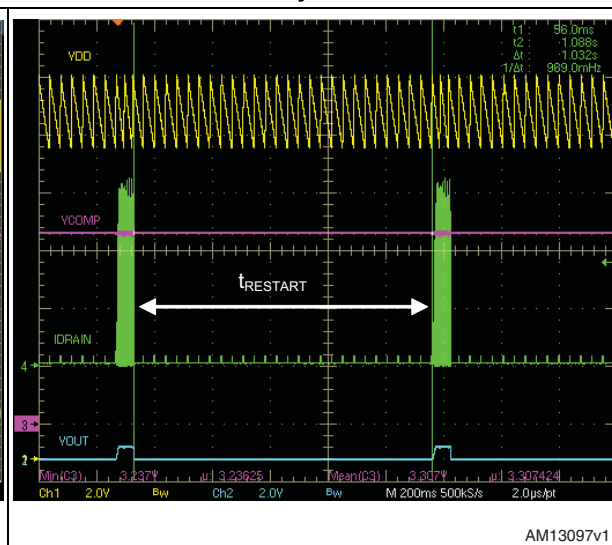


Figure 32. Output short-circuit maintained: OLP steady-state (zoom)

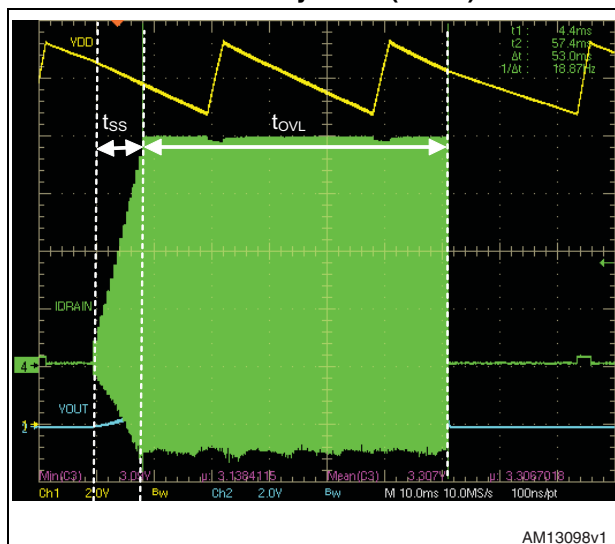
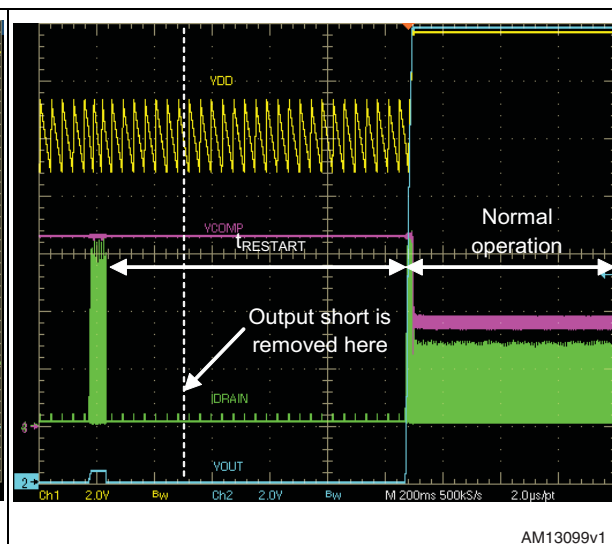


Figure 33. Output short-circuit removal and converter restart



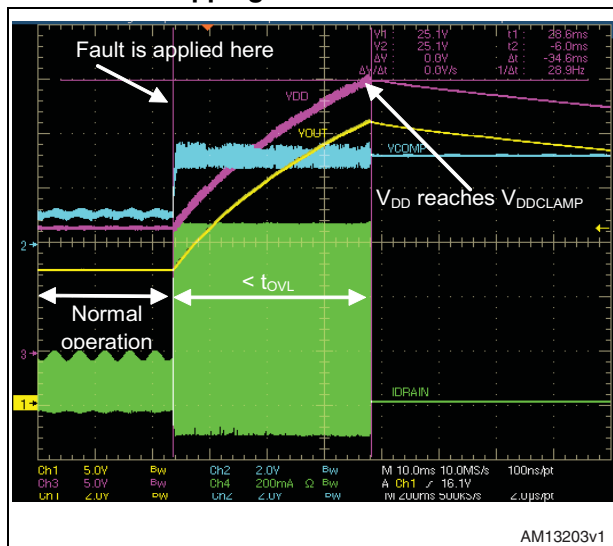
## 6.3 Feedback loop failure protection

This protection is available any time the IC is not self-biased. As the loop is broken ( $R_{fbL}$  shorted or  $R_{fbH}$  open), the output voltage  $V_{OUT}$  increases and the VIPER06 runs at its maximum current limitation. The VDD pin voltage increases as well, because it is linked to the  $V_{OUT}$  voltage either directly or through the auxiliary winding, depending on the cases.

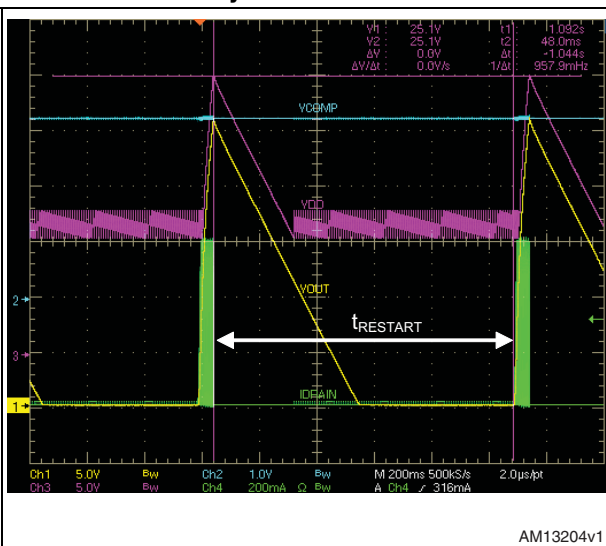
If the VDD voltage reaches the VDD clamp threshold (23.5 V min.) in less than 50 msec, the IC is shut down by open loop failure protection (see [Figure 34](#) and [35](#)), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low side resistor of the output voltage divider,  $R_{fbL} = R_{fbL1} + R_{fbL2}$ . The same behavior can be induced opening the high side resistor,  $R_{fbH} = R_{fbH1} + R_{fbH2}$ .

The protection acts in auto-restart mode with  $t_{\text{RESTART}} = 1\text{sec}$  (Figure 35). As the fault is removed, normal operation is restored after the last  $t_{\text{RESTART}}$  interval has been completed (Figure 37).

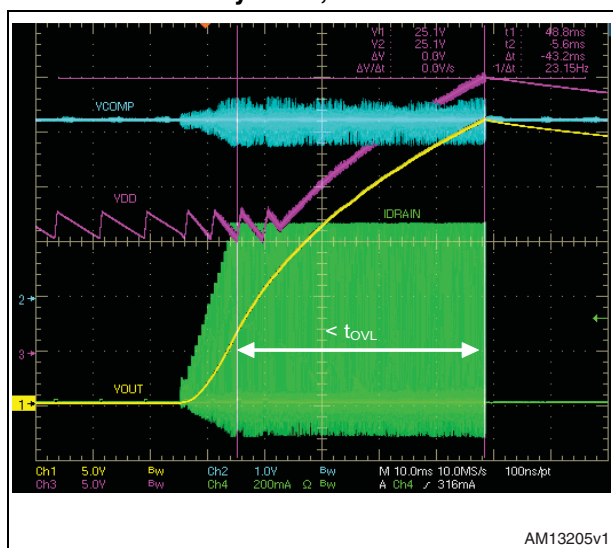
**Figure 34. Feedback loop failure protection: tripping**



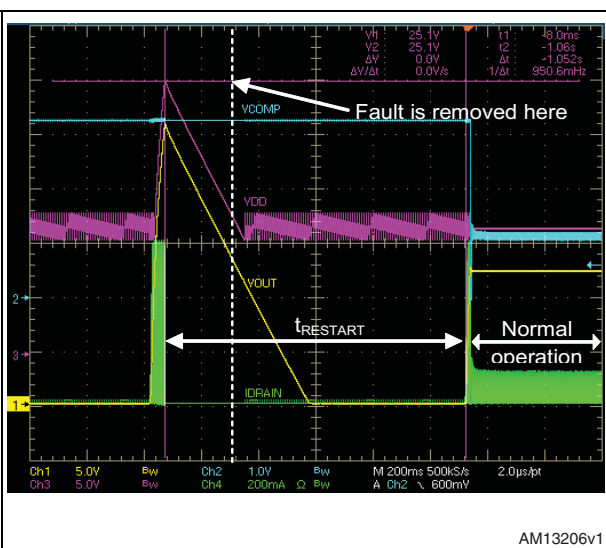
**Figure 35. Feedback loop failure protection: steady-state**



**Figure 36. Feedback loop failure protection: steady-state, zoom**



**Figure 37. Feedback loop failure protection: converter restart**

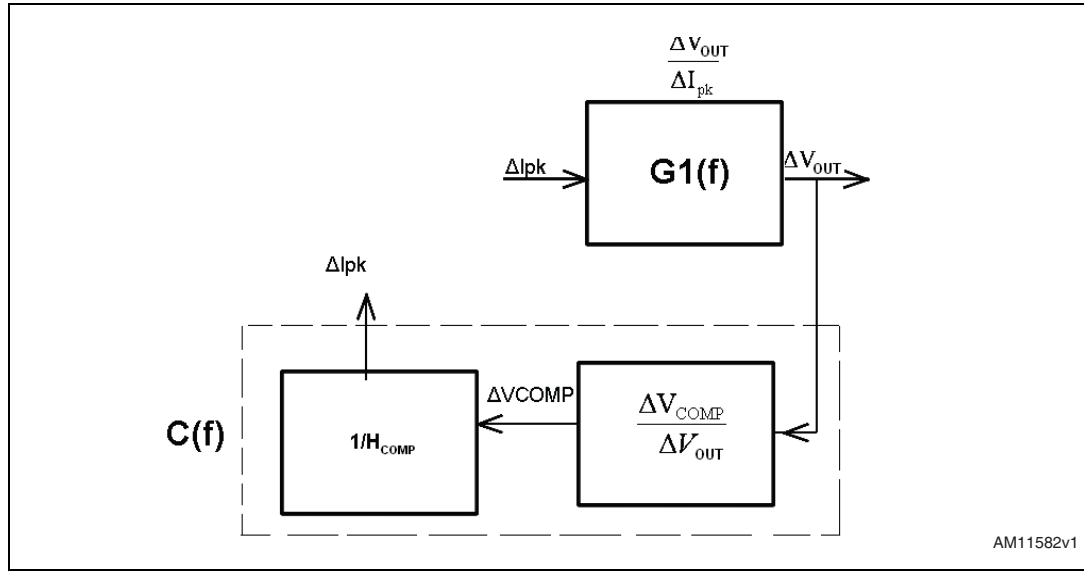


## 7 Feedback loop calculation guidelines

### 7.1 Transfer function

The set PWM modulator + power stage is indicated with  $G_1(f)$ , while  $C(f)$  is the “controller”, i.e. the network which is in charge to ensure the stability of the system.

**Figure 38. Control loop block diagram**



AM11582v1

The mathematical expression of the power plant  $G_1(f)$  is the following:

**Equation 2**

$$G_1(f) = \frac{\Delta V_{OUT}}{\Delta I_{pk}} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z})}{I_{pkp}(f_{sw}, V_{dc}) \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p})} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot f}{f_z})}{I_{pkp}(f_{sw}, V_{dc}) \cdot (1 + \frac{j \cdot f}{f_p})}$$

where  $f_p$  is the pole due to the output load and  $f_z$  the zero due to the ESR of the output capacitor:

**Equation 3**

$$f_p = \frac{1}{\pi \cdot C_{OUT} \cdot (R_{OUT} + 2ESR)}$$

**Equation 4**

$$f_z = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR}$$

The mathematical expression of the compensator  $C(f)$  is:

**Equation 5**

$$C(f) = \frac{\Delta I_{pk}}{\Delta V_{OUT}} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{2 \cdot \pi \cdot f \cdot j \cdot \left(1 + \frac{f \cdot j}{fPc}\right)}$$

where:

**Equation 6**

$$C_0 = -\frac{G_m}{C_c + C_p} \cdot \frac{R_{fbL}}{R_{fbL} + R_{fbH}}$$

**Equation 7**

$$fZc = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

**Equation 8**

$$fPc = \frac{C_c + C_p}{2 \cdot \pi \cdot R_c \cdot C_c \cdot C_p}$$

are chosen in order to ensure the stability of the overall system.  $G_m = 2 \text{ mA/V}$  (typical) is the VIPER06 transconductance.

## 7.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency, for instance:

- $fZc = f_p/2$
- $fPc = f_z$
- $f_{cross} = f_{cross\_sel} \leq f_{sw}/10$

$G_1(f_{cross\_sel})$  can be calculated from [Equation 2](#) and, since by definition it is  $|C(f_{cross\_sel}) \cdot G_1(f_{cross\_sel})| = 1$ ,  $C_0$  can be calculated as follows:

**Equation 9**

$$C_0 = \frac{\left| 2 \cdot \pi \cdot f_{cross\_sel} \cdot j \right| \cdot \left| 1 + \frac{f_{cross\_sel} \cdot j}{fPc} \right|}{\left| 1 + \frac{f_{cross\_sel} \cdot j}{fZc} \right|} \cdot \frac{H_{COMP}}{|G_1(f_{cross\_sel})|}$$

At this point the bode diagram of  $G1(f) \cdot C(f)$  can be plotted, in order to check the phase margin for the stability. If the margin is not high enough, an alternative choice should be made for  $fZc$ ,  $fPc$  and  $f_{cross\_sel}$ , and the procedure repeated. When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated, using the above formulas, as follows:

**Equation 10**

$$RfbL = \frac{RfbH}{\frac{Vout}{3.3V} - 1}$$

**Equation 11**

$$Cp = \frac{fZc}{fPc} \cdot \frac{Gm}{|C0|} \cdot \frac{RfbL}{RfbL + RfbH}$$

**Equation 12**

$$Cc = Cp \cdot \left( \frac{fPc}{fZc} - 1 \right)$$

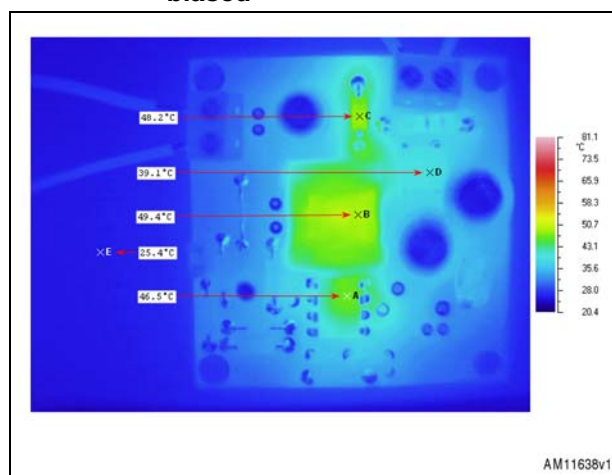
**Equation 13**

$$Rc = \frac{Cc + Cp}{2 \cdot \pi \cdot fPc \cdot Cc \cdot Cp}$$

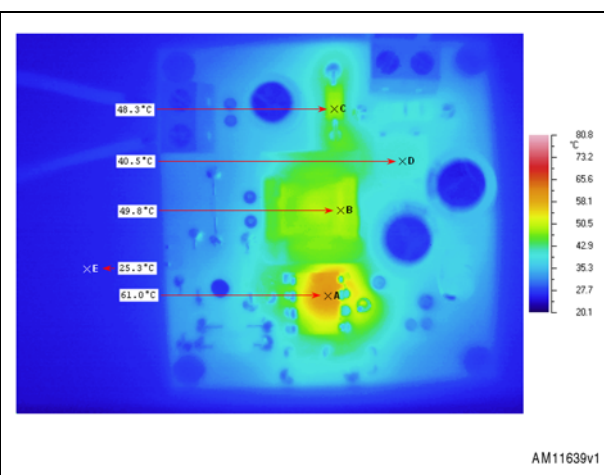
## 8 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for 85 V<sub>AC</sub>, 115 V<sub>AC</sub>, 230 V<sub>AC</sub> and 265 V<sub>AC</sub> mains input, full load condition, both with and without the self-biasing function. The results are shown in the following figures. When the self-biasing function is used, the VIPER06 temperature is higher, due to the power dissipated by the HV-startup generator.

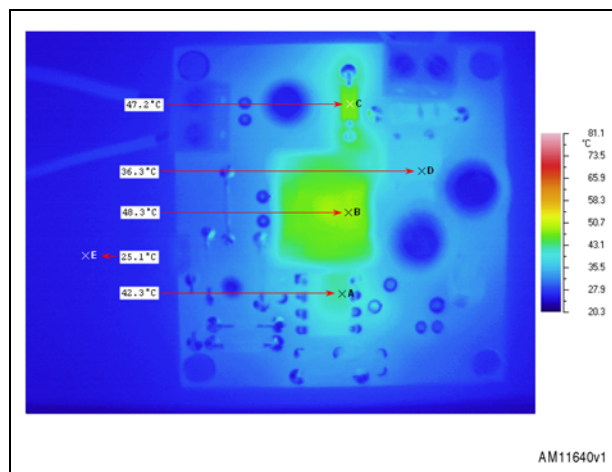
**Figure 39.** Thermal map at V<sub>IN</sub>=85 V<sub>AC</sub>, T<sub>AMB</sub>=25 °C, full load; IC externally biased



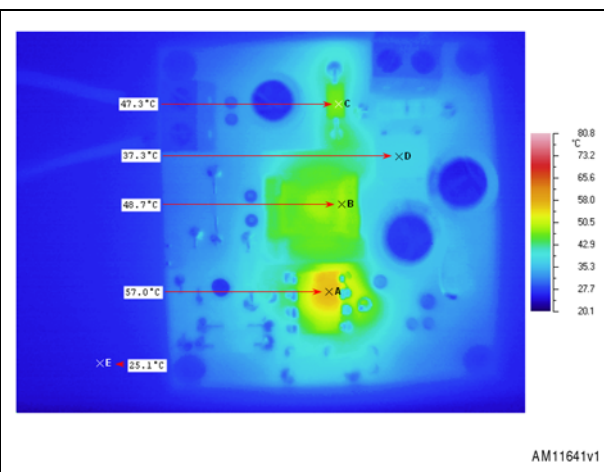
**Figure 40.** Thermal map at V<sub>IN</sub>=85 V<sub>AC</sub>, T<sub>AMB</sub>=25 °C, full load; IC self-biased



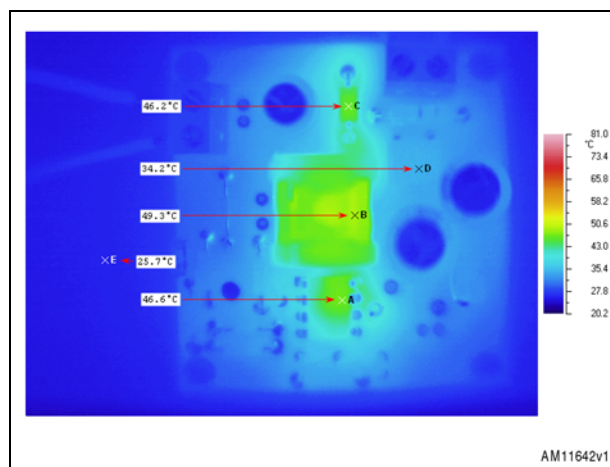
**Figure 41.** Thermal map at V<sub>IN</sub>=115 V<sub>AC</sub>, full load, T<sub>AMB</sub>=25 °C; IC externally biased



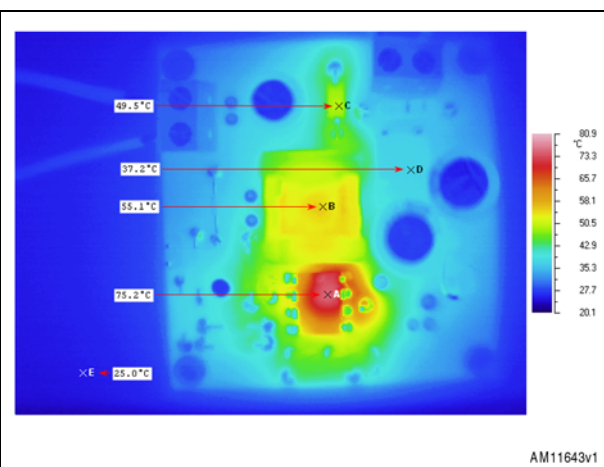
**Figure 42.** Thermal map at V<sub>IN</sub>=115 V<sub>AC</sub>, full load, T<sub>AMB</sub>=25 °C; IC self-biased



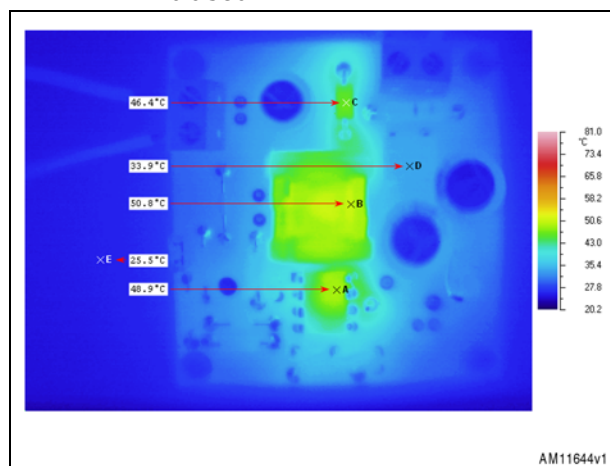
**Figure 43.** Thermal map @  $V_{IN}=230\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ; IC externally biased



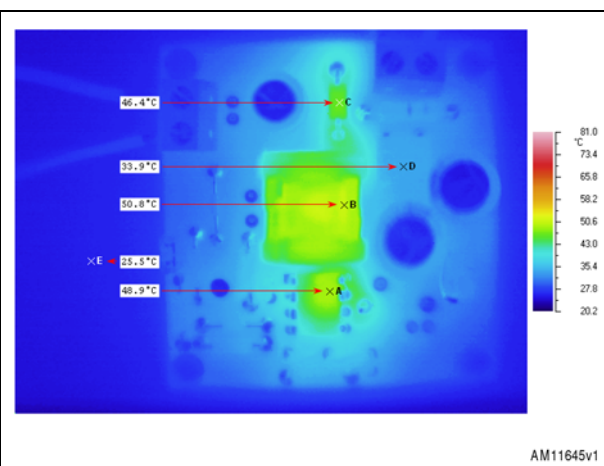
**Figure 44.** Thermal map @  $V_{IN}=230\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ; IC self-biased



**Figure 45.** Thermal map @  $V_{IN}=265\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ; IC externally biased



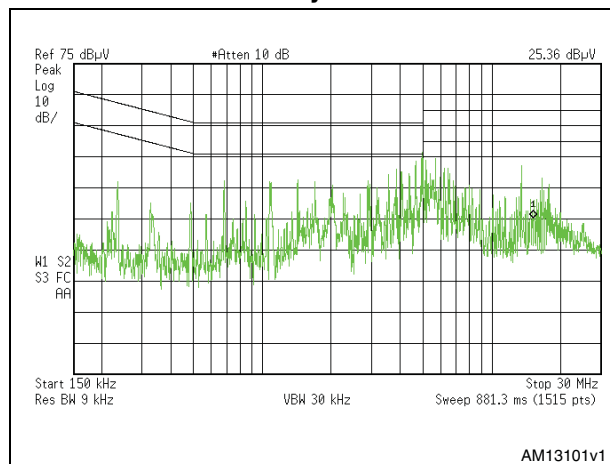
**Figure 46.** Thermal map @  $V_{IN}=265\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ; IC self-biased



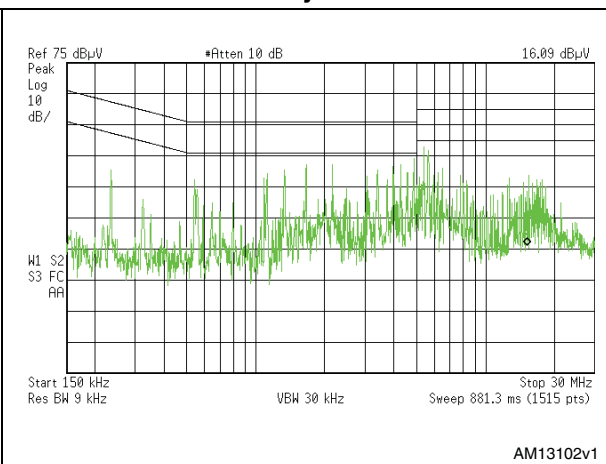
## 9 EMI measurements

A pre-compliant test of the EN55022 (Class B) European standard has been performed using an EMC analyzer and an LISN. Peak, quasi-peak and average measurements have been conducted as reported in the following figures.

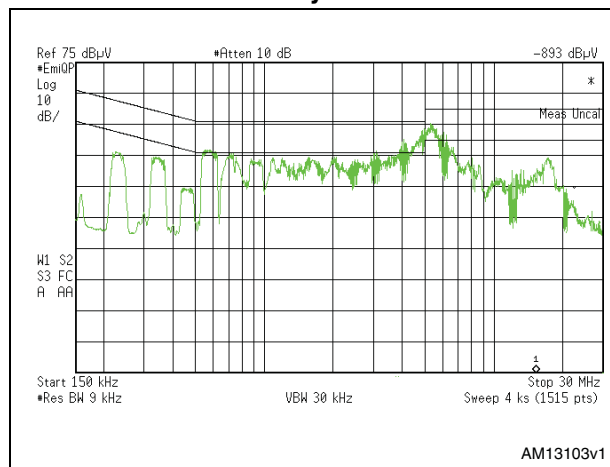
**Figure 47. Peak measurements @**  
 $V_{IN}=115\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ;  
 IC externally biased



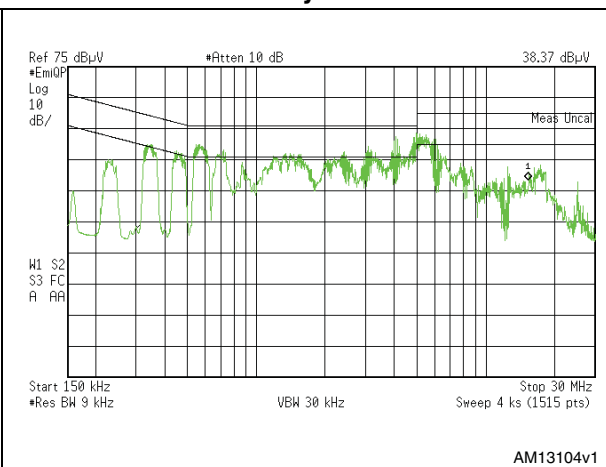
**Figure 48. Peak measurements @**  
 $V_{IN}=230\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ;  
 IC externally biased



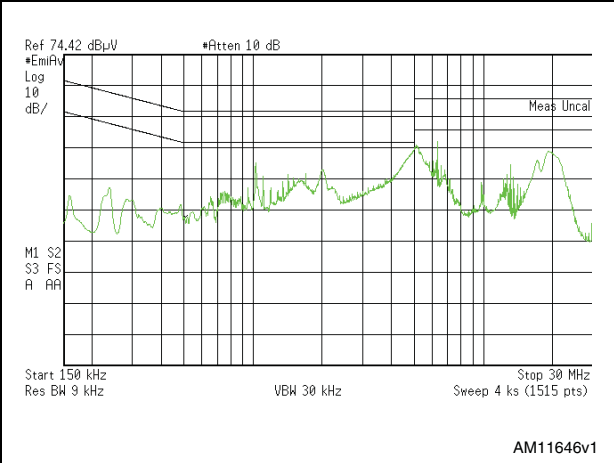
**Figure 49. Quasi-peak measurements @**  
 $V_{IN}=115\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ;  
 IC externally biased



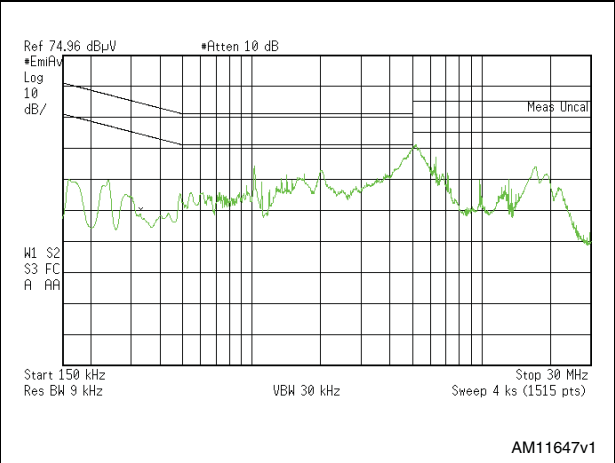
**Figure 50. Quasi-peak measurements @**  
 $V_{IN}=230\text{ V}_{AC}$ , full load,  $T_{AMB}=25\text{ }^{\circ}\text{C}$ ;  
 IC externally biased



**Figure 51. Average measurements @  $V_{IN}=115$  V<sub>AC</sub>, full load, T<sub>AMB</sub>=25 °C; IC externally biased**

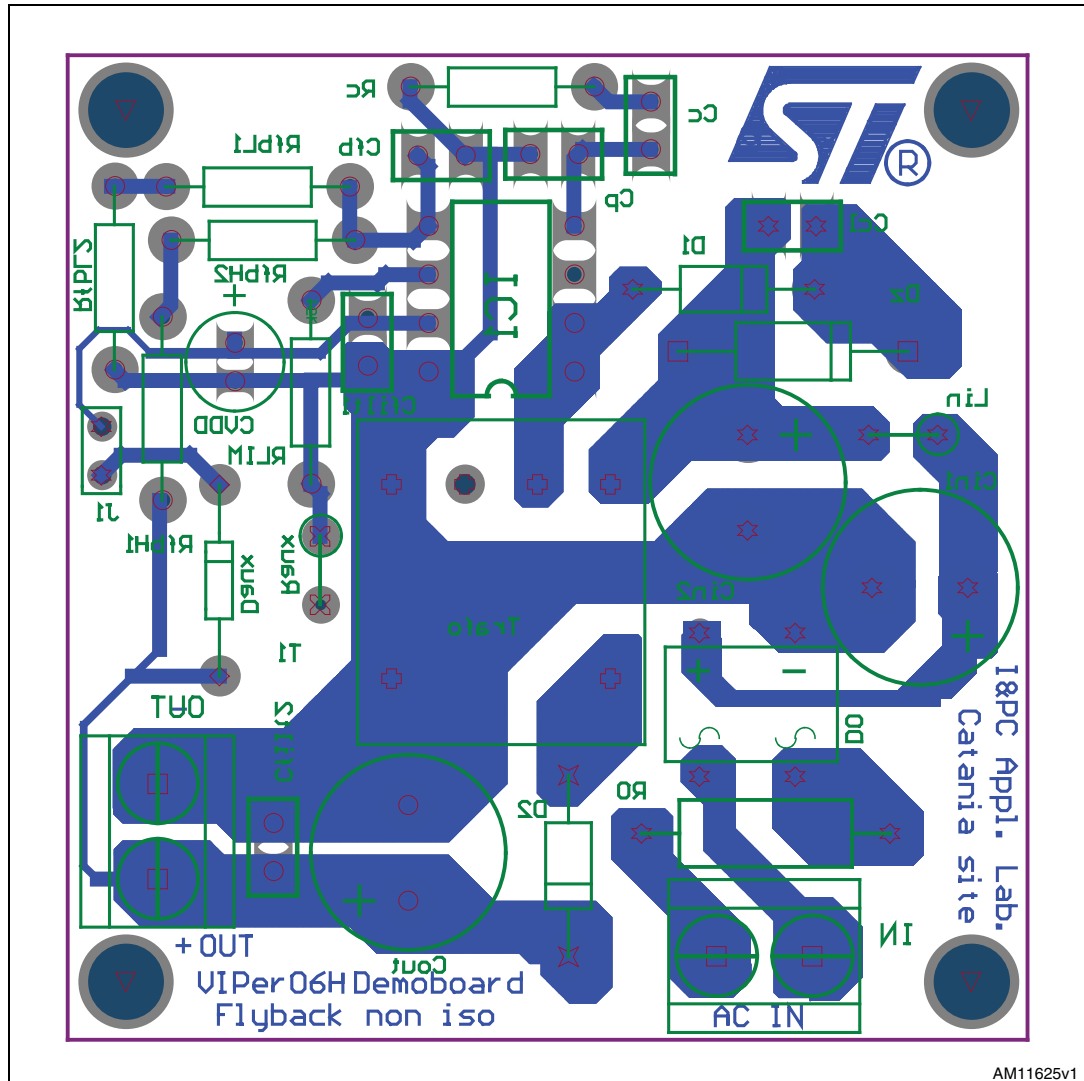


**Figure 52. Average measurements @  $V_{IN}=230$  V<sub>AC</sub>, full load, T<sub>AMB</sub>=25 °C; IC externally biased**



## 10 Board layout

Figure 53. Board layout



## 11 Conclusions

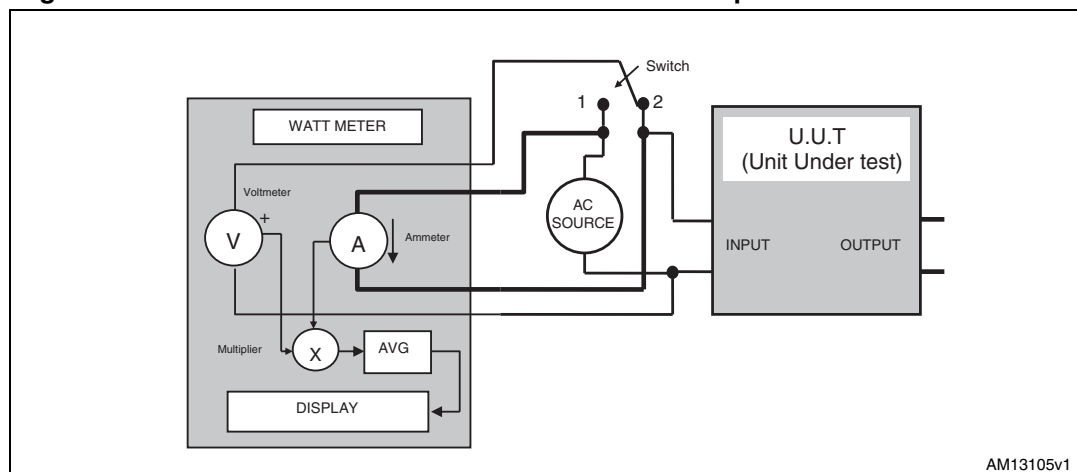
The VIPER06 allows a non-isolated converter to be designed in a simple way and with few external components. In this document a flyback has been described and characterized. Special attention has been given to light load performance. The efficiency performance has been compared to the requirements of the Code of Conduct (version 4) for an external AC-DC adapter with very good results, the measured active mode efficiency is always higher with respect to the minimum required.

## Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

Figure 54 shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

**Figure 54. Connections of the UUT to the wattmeter for power measurements**

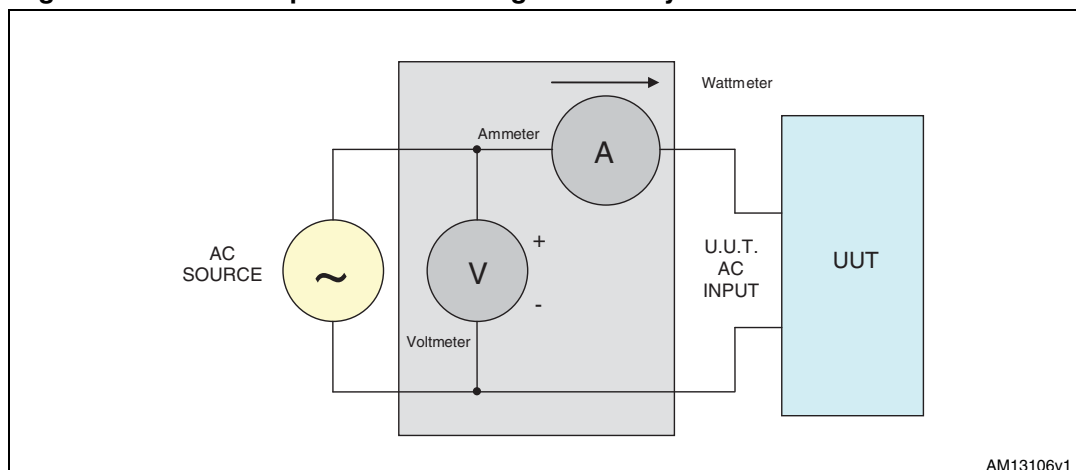


An electronic load has been connected to the output of the power converter (UUT), allowing to set and measure the converter load current, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter's efficiency, which has been measured in different input/output conditions.

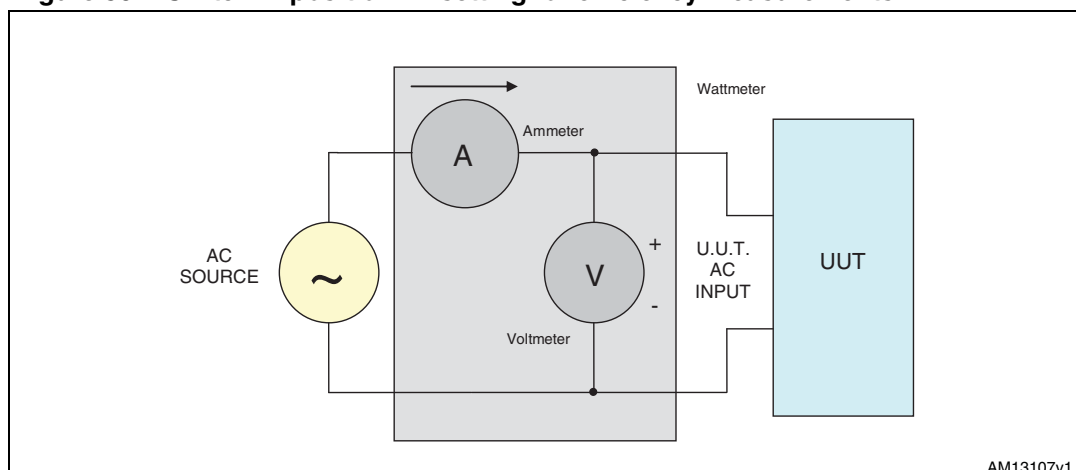
### A.1 Measuring input power

With reference to Figure 54, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal as it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

If the switch of Figure 54 is in position 1 (see also the simplified scheme of Figure 55), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example, when measuring the input power of UUT in light load condition).

**Figure 55. Switch in position 1 - setting for standby measurements**

In the case of high UUT input current (i.e. for measurements in heavy load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in [Figure 54](#) can be changed to position 2 (see simplified scheme of [Figure 56](#)), where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

**Figure 56. Switch in position 2 - setting for efficiency measurements**

On the other hand, the position of [Figure 56](#) may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is why it is recommended to use the setting of [Figure 55](#) for light load measurements and the setting of [Figure 56](#) for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements. After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value

observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured over time for both AC input and DC output.

Some wattmeter models allow the measured input power to be integrated in a time range and then the energy absorbed by the UUT to be measured during the integration time. The average input power is calculated by dividing by the integration time itself.

## 12 References

- [1] Code of Conduct on Energy Efficiency of External Power Supplies, Version 4.
- [2] VIPER06 datasheet.

## 13 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
23-Jan-2013	1	Initial release.

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