AN4163
Application note

EVL4984-350W: 350 W CCM PFC pre-regulator with the L4984D

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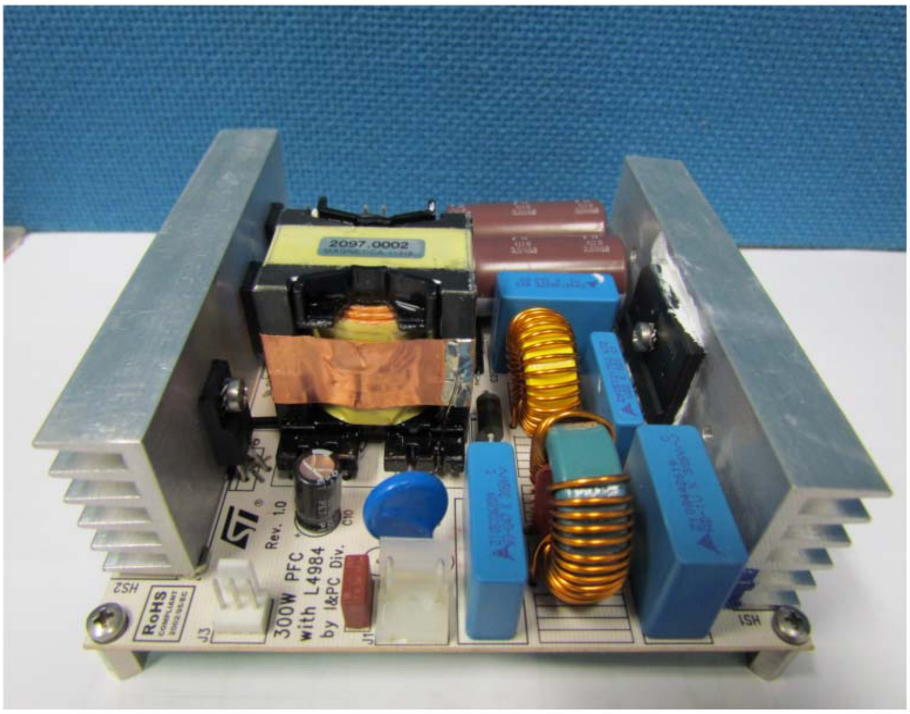
Introduction

This application note describes the demonstration board EVL4984-350W, based on the “Continuous Conduction Mode” PFC (CCM) controller, the L4984D, and presents the results of its bench evaluation. The board implements a 350 W, wide-range input, PFC pre-conditioner suitable for all SMPS from 150 W to those in the kilowatt range which must meet the IEC61000-3-2 or the JEITA-MITI regulation.

Figure 1. EVL4984-350W demonstration board



EVL4984-350W

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1 Main characteristics and circuit description

The main characteristics of the SMPS are listed below:

- Input mains range: 90 to 265 V_{ac}
- Minimum line frequency (f_L): 47 Hz
- Regulated output voltage: 400 V
- Rated output power: 350 W
- Maximum $2f_L$ output voltage ripple: 12.5 V (peak- to-peak)
- Hold-up time: 20 ms (VDROP after hold-up time: 300 V)
- Switching frequency: 70 kHz
- Minimum efficiency: 94% (at V_{in} = 90 V_{ac}, P_{out} = 350 W)
- PCB: single-sided, 70 µm, CEM-1, 112 x 114 mm

The power stage of the PFC is a traditional boost PFC converter, connected to the output of the rectifier bridge D2. It is comprised of the boost inductor L3, the power switch, formed by the parallel of MOSFETs Q1 and Q2, the diode D3 and the output capacitors C3 and C4.

The 300 V varistor RV1, connected between the line and the neutral, protects the circuit against high input voltage transients while the fuse F1 disconnects the mains in case of short-circuit.

To meet the EMC standards, the board is equipped with an input EMI filter cutting the switching noise coming from the boost stage. In particular L2 filters the common-mode emissions while L1, C1, C2 reduce the differential-mode emissions.

The L4984D has to be supplied by an external power supply, connected between pin #1 (VCC) and pin #2 (GND) of J3.

The capacitor C14 connected to the TIMER (#7) pin determines the switching frequency. The resistor divider R12, R16, R22 and R24 provides to the L4984D multiplier (MULT, pin #3) the information of the instantaneous mains voltage that is used to modulate the peak current of the boost, the T_{OFF} duration and is fed to the VFF block.

The resistors R6, R8, R13 with R17 and R18 are dedicated to sense the output voltage and feed to the inverting input of the error amplifier (INV, pin #1) the feedback information necessary to keep the output voltage regulated. Between the INV (#1) and COMP (#2) pins, the components C8, R21 and C11 form the error amplifier compensation network in order to keep the required loop stability.

The inductor peak current is sensed by resistors R27, R30, R31 placed in series to the MOSFETs' source and the derived signal is fed into the current sense pin (CS, #4) of the L4984D via the filter by R29 and C13. C15 and R28, connected to the VFF pin (#5), complete an internal peak-holding circuit providing the information on the RMS mains voltage, deriving a DC voltage equal to the peak of the MULT pin (#3) voltage, which is fed to the multiplier to compensate the control loop gain dependence on the mains voltage.

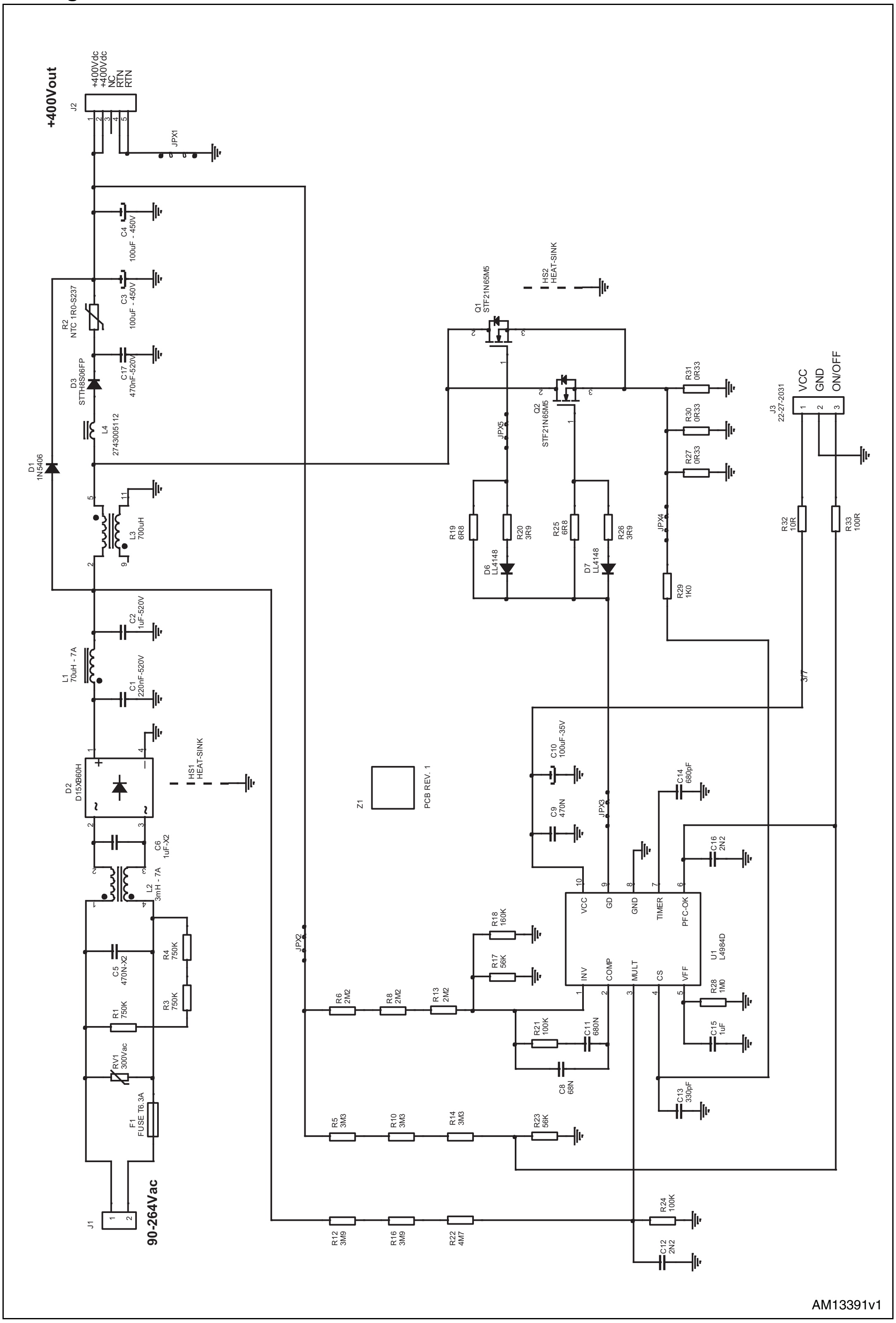
The brownout function is also implemented using the VFF pin. A voltage below 0.8 V on the VFF pin (#5) shuts down (no latch) the IC and brings its consumption to a considerably lower level. The L4984D starts as the voltage at the pin rises above 0.88 V.

The divider R5, R10, R14 and R23 provides to the L4984D PFC_OK pin (#7) the information of the output voltage level, to trigger the dynamic OVP protection, preventing the output voltage from excessive values during the load transients due to the slow response caused by the intrinsic narrow bandwidth of PFC systems. If the voltage on the PFC_OK pin (#7) exceeds 2.5 V, the L4984D stops switching and restarts as the voltage on the pin falls below 2.4 V.

The open-loop protection (also called feedback failure protection) monitors the PFC_OK (#7) and INV (#1) pins. If the voltage of the PFC_OK pin (#7) exceeds 2.5 V, and at the same time the voltage on INV pin (#1) falls below 1.66 V, a feedback failure is assumed and the device is latched off. Normal operation can be resumed only by cycling Vcc (pin #10), bringing its value lower than $V_{CCrestart}$ (6 V, typ.), before rising up to the turn-on threshold V_{CCon} (12 V, typ.).

Additionally a remote on/off control input is present. If the voltage on the PFC_OK pin (#7) is tied below the PFC_OK disable threshold ($V_{PFC\_OK\_D}$, 0.23 V typ.), the L4984D is shut down and the operation is restarted when the voltage on the PFC_OK pin (#7) increases above the PFC_OK enable threshold ($V_{PFC\_OK\_E}$, 0.27 V typ.). The L4984D operation can be also disabled or enabled to manage properly light load or failure by the D2D via the PFC_OK pin (#7), using pin #3 of J3 (ON/OFF).

Figure 2. EVL4984-350W CCM PFC demonstration board electrical schematic



2 Test results and significant waveforms

2.1 Harmonic content measurement

One of the main purposes of a PFC pre-conditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this demonstration board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI class-D, at full load at both the nominal input voltage mains.

As shown in *Figure 3* to *Figure 6*, the circuit can reduce the harmonics well below the limits of both regulations from full load down to light load. An output power of 70 W has been chosen because it is close to the lower power limit at which the harmonics have to be limited according to the above-mentioned standards.

Figure 3. EVL4984-350W: compliance to EN61000-3-2 standard at full load

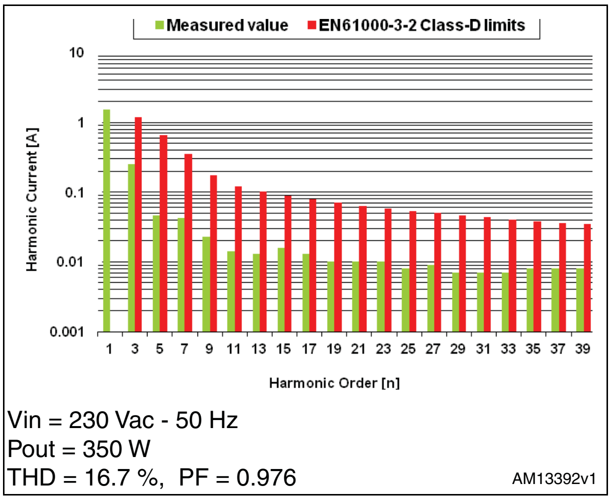


Figure 4. EVL4984-350W: compliance to JEITA-MITI standard at full load

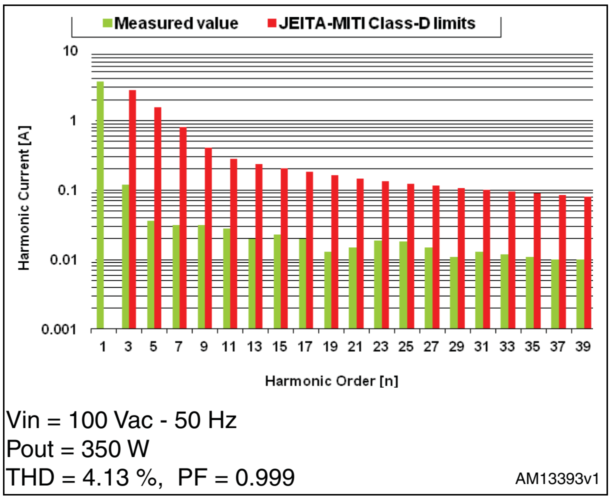


Figure 5. EVL4984-350W: compliance to EN61000-3-2 standard at 70 W load

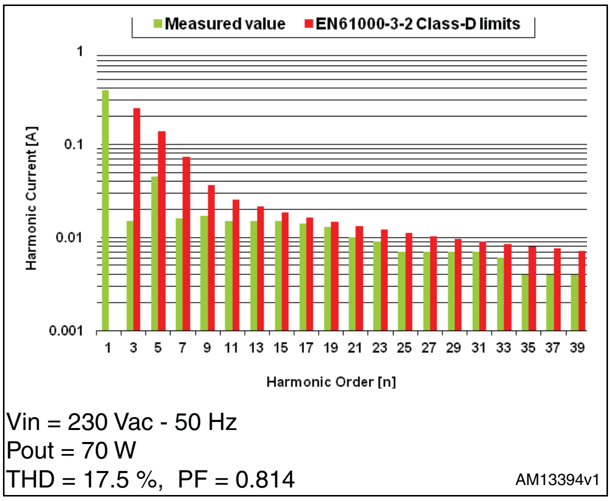
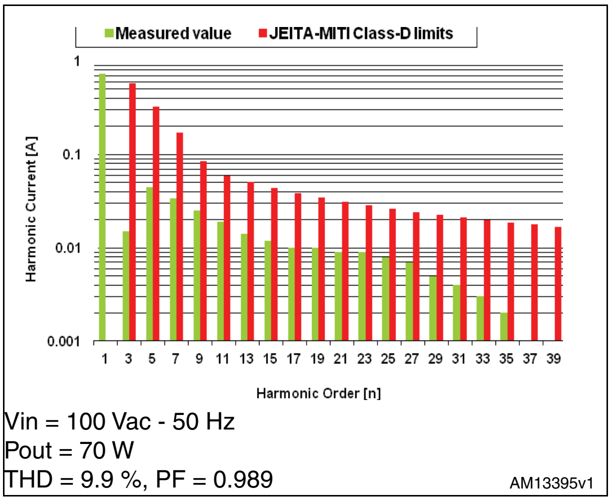


Figure 6. EVL4984-350W: compliance to JEITA-MITI standard at 70 W load



For user reference, waveforms of the input current and voltage at the nominal input voltage mains and different load conditions are shown in *Figure 7* to *Figure 10*.

Figure 7. EVL4984-350W input current waveform at 100 V - 60 Hz - 350 W load

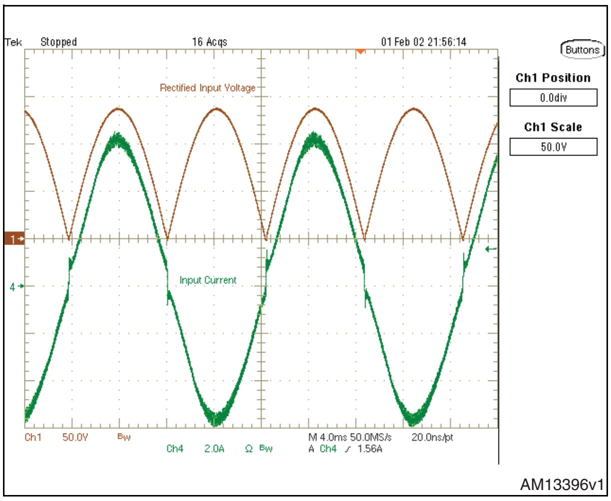


Figure 8. EVL4984-350W input current waveform at 230 V - 50 Hz - 350 W load

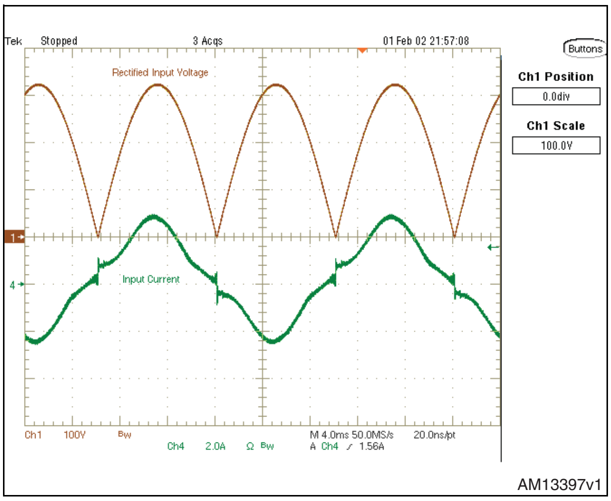


Figure 9. EVL4984-350W input current waveform at 100 V - 60 Hz - half load

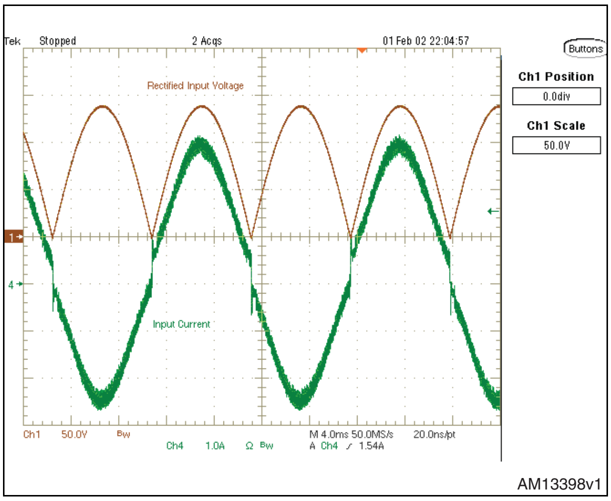


Figure 10. EVL4984-350W input current waveform at 230 V - 50 Hz - half load

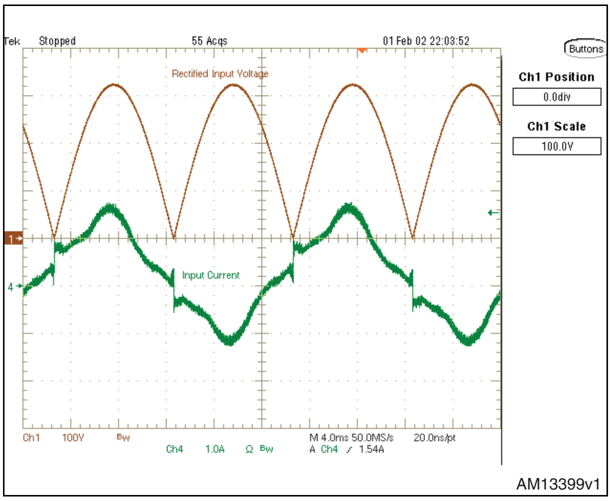


Figure 11. EVL4984-350W input current waveform at 100 V - 60 Hz – 70 W load

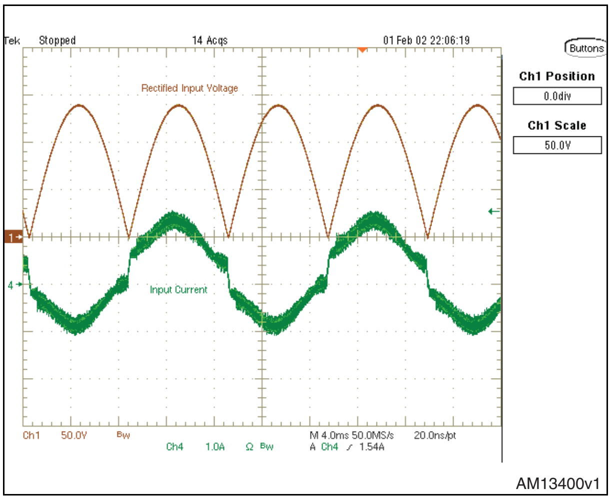
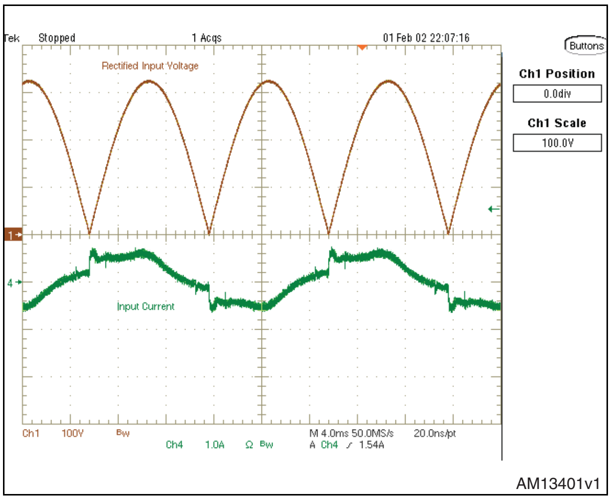


Figure 12. EVL4984-350W input current waveform at 230 V - 50 Hz – 70 W load



The Power Factor (PF) and the Total Harmonic Distortion (THD) have also been measured with the results given in *Figure 13* and *Figure 14*. As shown, the PF at full load and half load remains above 0.9 over the input voltage mains range, while when the circuit is delivering 70 W, it decreases at high mains range. THD is within 20% until 230 V and at the maximum mains voltage (265 V_{ac}) it increases at the maximum input voltage.

Figure 13. Power factor vs. V_{in} and load

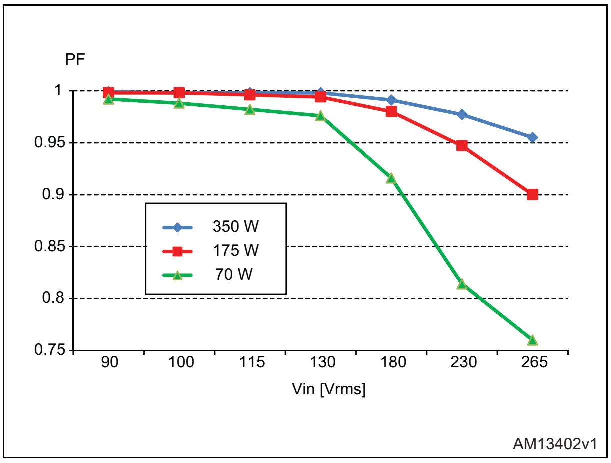
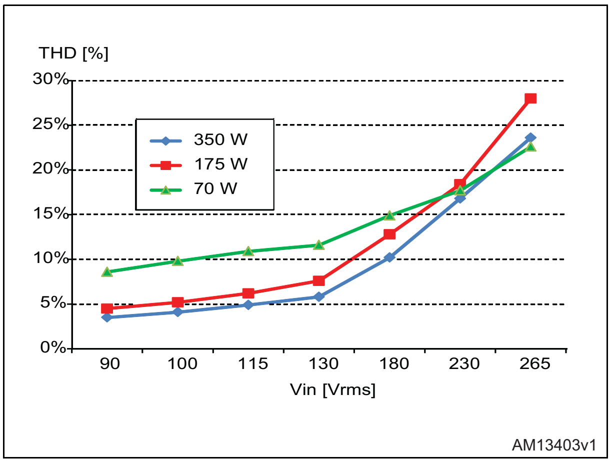


Figure 14. THD vs. V_{in} and load



The measured efficiency is shown in *Figure 15*, measured according to the ES-2 requirements: it is very good at all load and line conditions. At full load it is always higher than 94%, making this design suitable for high-efficiency power supplies. The average efficiency calculated according to the ES-2 requirements at different nominal mains voltages are shown in *Figure 16*.

Figure 15. Efficiency vs. output power

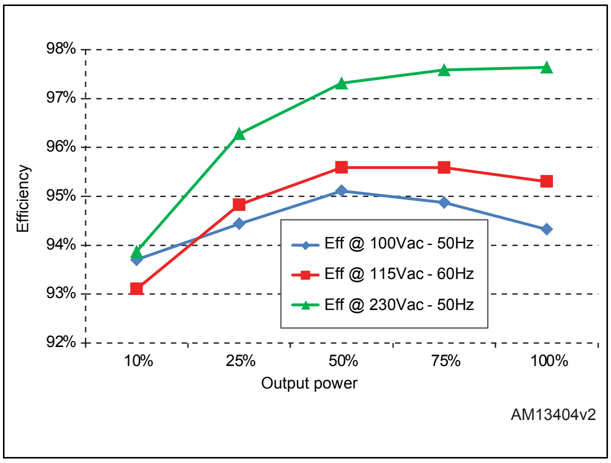
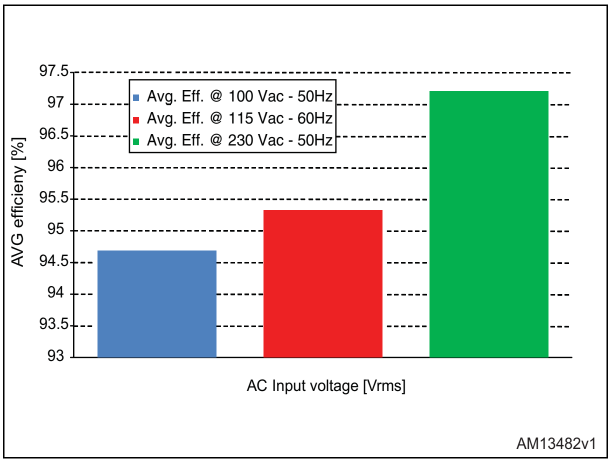
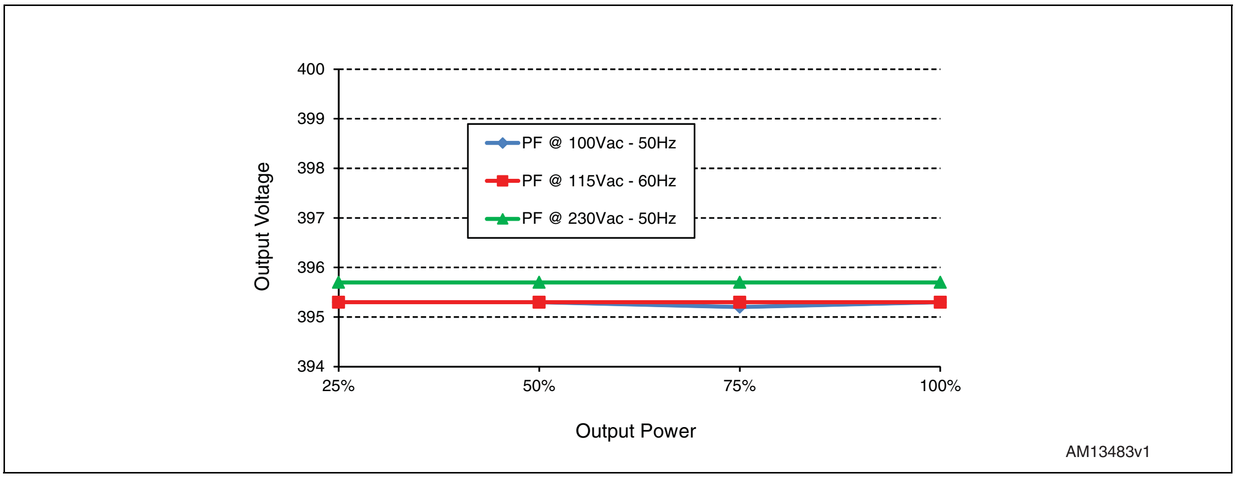


Figure 16. Average efficiency acc. to ES-2



The measured output voltage at different lines and static load is given in *Figure 17*. As shown, the voltage is very stable over the entire input voltage and output load range.

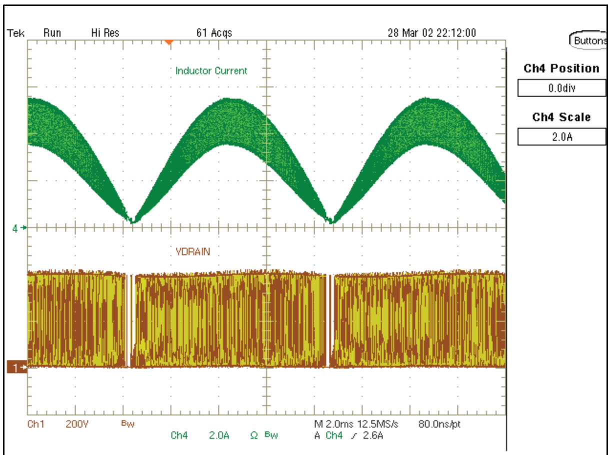
Figure 17. Static V_{out} regulation vs. output power



2.2 Inductor current in FOT and L4984D THD optimizer

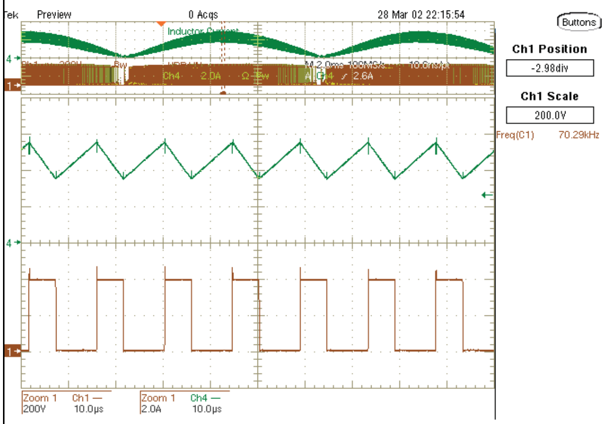
Figure 18 through *Figure 21* represent the waveform of the inductor current at different voltage mains. As shown in *Figure 18* and *Figure 20*, the inductor current waveform over a line half-period is very similar to that of an average CCM PFC. Comparing *Figure 18* to *Figure 20* showing the inductor ripple envelope at 115 V_{ac} and 230 V respectively, it is possible to notice the different ripple currents and how the converter operates in either CCM or DCM depending on the input voltage and the load. At 115 V_{ac} the borderline between DCM and CCM occurs close to the zero-crossing of the current sine wave, so the inductor is working in CCM for almost all the line period while at 230 V_{ac} the borderlines between DCM and CCM move toward the top of the circuit and the boost inductor works in CCM only in a portion centered around the peak of the sine wave.

Figure 18. EVL4984-350W inductor current ripple envelope at 115 V_{ac} - 60 Hz - full load



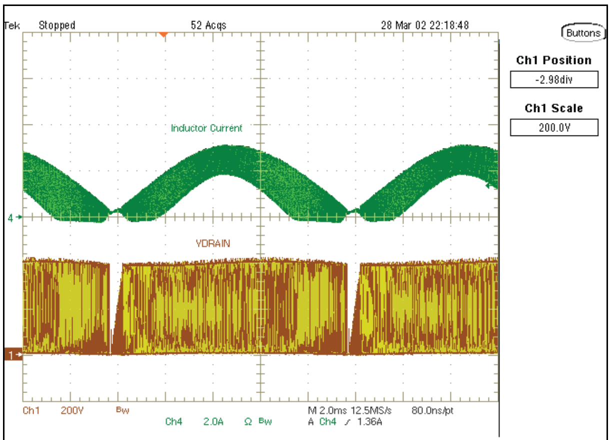
CH1: Q1/Q2 drain voltage
CH4: L4 inductor current ripple envelope
AM13405v1

Figure 19. EVL4984-350W inductor current ripple (detail) at 115 V_{ac} - 60 Hz - full load



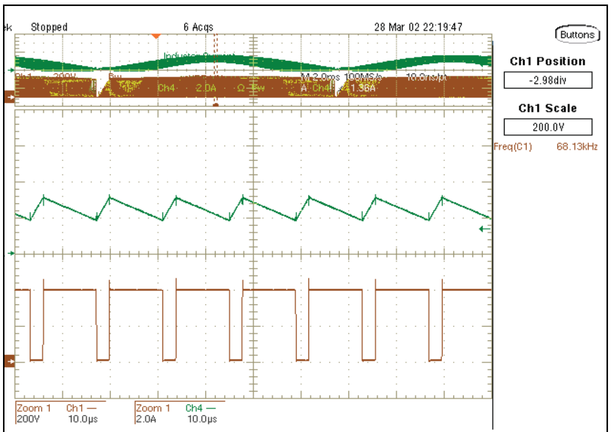
CH1: Q1/Q2 drain voltage
CH4: L4 inductor current ripple envelope
AM13406v1

Figure 20. EVL4984-350W inductor current ripple envelope at 230 V_{ac} - 50 Hz - full load



CH1: Q1/Q2 drain voltage
CH4: L4 inductor current ripple envelope
AM13407v1

Figure 21. EVL4984-350W inductor current ripple (detail) at 230 V_{ac} - 50 Hz - full load



CH1: Q1/Q2 drain voltage
CH4: L4 inductor current ripple envelope
AM13408v1

On both the drain voltage traces shown in *Figure 19* and *Figure 20*, close to the zero-crossing points of the sine wave, it is possible to note the action of the THD optimizer embedded in the L4984D, minimizing the conduction dead-angle occurring on the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way, the THD (Total Harmonic Distortion) of the current is considerably reduced. A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high-frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop.

To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This will result in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid and it is modulated by the voltage on the VFF pin, so as to have little offset at low line, where energy transfer at zero-crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse.

To derive maximum benefit from the THD optimizer circuit, the high-frequency filter capacitors after the bridge rectifier should be minimized, compatible with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current in itself, thus reducing the effectiveness of the optimizer circuit.

2.3 Switching frequency and TIMER pin

With the L4984D the switching frequency is determined by a capacitor connected between the TIMER pin and ground, charged by an accurate internal generator (I_{TIMER}) of 156 A (typ.) during the OFF-time, generating a voltage ramp. As shown in *Figure 22* when the voltage ramp on TIMER equals the voltage on the MULT pin, connected through a resistive divider to the rectified mains to get a sinusoidal voltage reference, the OFF-time of the power MOSFET is terminated, the gate driver (GD) pin is driven high and the ramp resets at zero. The timing capacitor C_T is then selected with the following formula described in the L4984D datasheet:

Equation 1

$$C_T = \frac{I_{TIMER}}{k_P \, Vout \, f_{sw}}$$

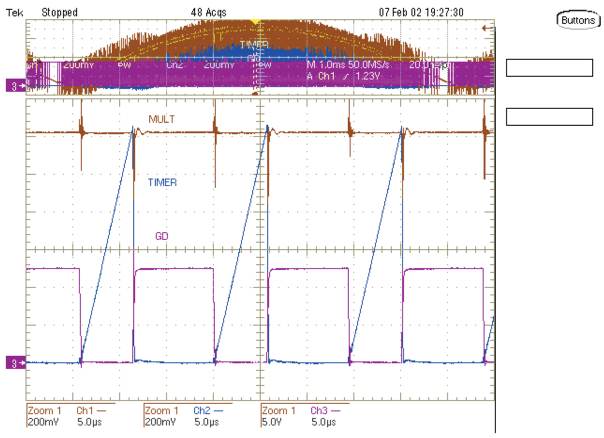
where f_{SW} is the switching frequency and k_p the ratio of the resistive divider on the MULT pin, calculated considering the maximum value of the multiplier input, that is the voltage measured on the MULT pin at maximum mains voltage. The switching frequency f_{SW} is not constant but is modulated at twice the line frequency ripple $2f_L$ appearing across the output capacitor C_{out}, spreading the spectrum of the electrical noise injected back into the power line and facilitating the compliance with conducted EMI emission regulations. The switching frequency chosen for this design is around 70 kHz, so the capacitor on the TIMER pin needed to obtain the desired frequency is:

Equation 2

$$C_T = \frac{156\mu A}{8 \cdot 10^{-3} \cdot 400V \cdot 70kHz} = 695pF$$

An NP0 capacitor with commercial value of 680 pF has been selected for the TIMER capacitor. For further details on the calculation procedure of the entire converter, please refer to AN4149, “Designing a CCM PFC pre-regulator based on the L4984D”.

Figure 22. EVL4984-350W 115 V_{ac} - 60 Hz - normal working condition



2.4 Voltage feed-forward

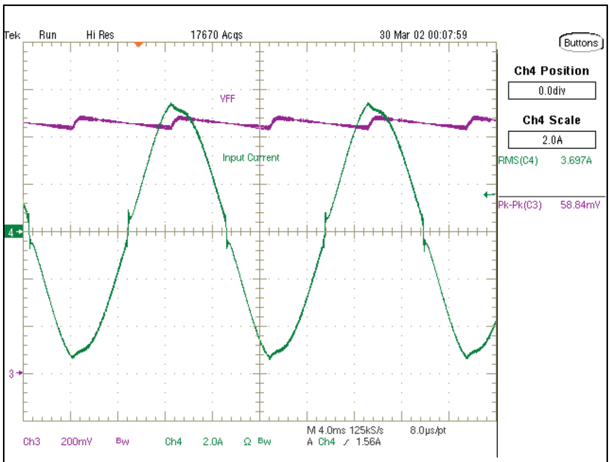
The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. This applies as well to the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get fc = 20 Hz at 264 V_{ac} means having fc = 4 Hz at 88 V_{ac}, resulting in sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. However, a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

The voltage feed-forward function can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop. In this way a change of the line voltage will cause an inversely proportional change of the half sine amplitude at the output of the multiplier so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain will be constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

The L4984D implements voltage feed-forward with a technique that makes use of just two external parts and that limits the feed-forward time constant trade-off issue to only one direction. A capacitor C_{FF} (C15) and a resistor R_{FF} (R28), both connected to the V_{FF} pin (#5), complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on the MULT pin (#3). R_{FF} provides a means to discharge C_{FF} when the line voltage decreases.

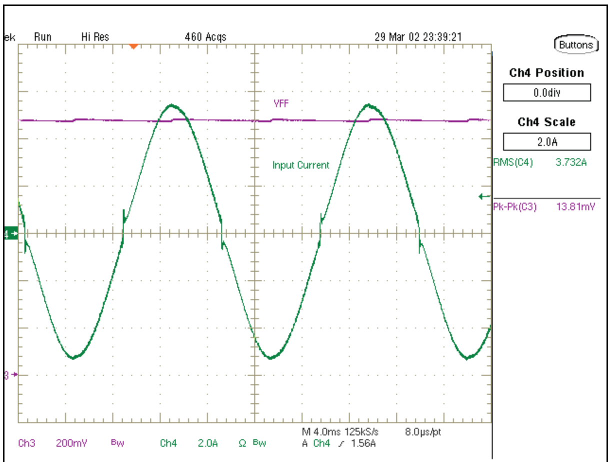
However, a drawback of the V_{FF} technique is an increase of the harmonics. Deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small, the voltage generated will be affected by a considerable amount of ripple at twice the mains frequency causing distortion of the current reference (resulting in high THD and poor PF). If it is too large, there will be a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly, a trade-off is required. For reference, in *Figure 23* and *Figure 24* the comparison of the input current shape and the measurement of the THD and 3rd harmonic amplitude for different C_{FF} values taken from a similar board using the former L4984D are shown.

Figure 23. EVL4984-350W input current shape at 100 V_{ac} - 60 Hz - C_{FF} = 470 nF, R_{FF} = 390 kΩ



THD [%]: 3.6 % - 3RD harmonic: 0.07 A
CH3: VFF - pin #5
CH4: input current
AM13410v1

Figure 24. EVL4984-350W input current shape at 100 V_{ac} - 60 Hz - C_{FF} = 1 µF, R_{FF} = 1 MΩ

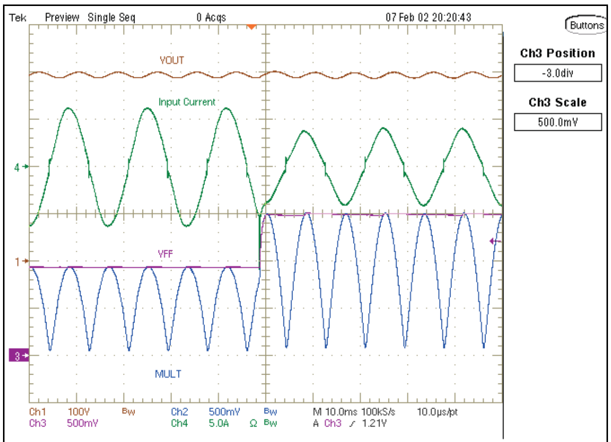


THD [%]: 2.8 % - 3RD harmonic: 0.057 A
CH3: VFF - pin #5
CH4: input current
AM13411v1

To overcome this issue the new L4984D has integrated an innovative circuitry which allows getting a fast transient response for whichever voltage change occurs on the mains, both surges and drops. Thus, in case of sudden line voltage rise, C_{FF} will be rapidly charged through the low impedance of the internal diode and no appreciable overshoot will be visible at the pre-regulator's output. In case of line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges C_{FF} avoiding a long settling time before reaching the new voltage level. Consequently an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the pre-regulator’s output like in systems with no feed-forward compensation.

In *Figure 25* the behavior of the EVL4984-350W demonstration board in case of an input voltage surge from 90 to 140 V_{ac} has been analyzed. As shown the V_{FF} function provides for the stability of the output voltage which is not affected by the input voltage surge. Thanks to the V_{FF} function, the compensation of the input voltage variation is very fast and the output voltage remains stable at its nominal value, as opposed to *Figure 26*, which shows the behavior of a PFC using the L6562 working in FOT and delivering 400 W in case of a mains surge. The controller cannot compensate it and the output voltage stability depends on the feedback loop only. Unfortunately, as previously stated, its bandwidth is narrow and thus the output voltage has a significant deviation from the nominal value.

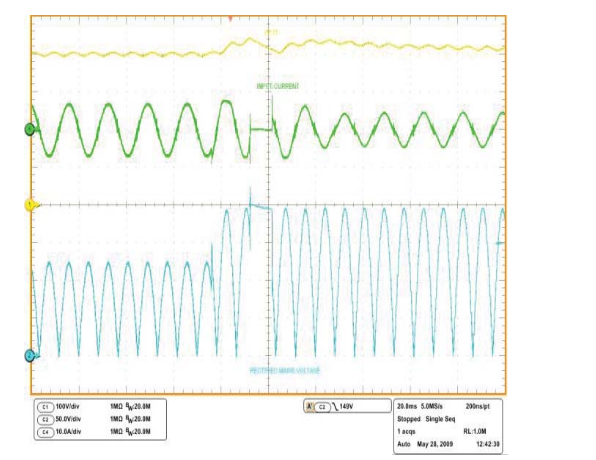
Figure 25. EVL4984-350W input mains surge from 90 V_{ac} to 140 V_{ac} - full load - C_{FF} = 1 µF



CH1: output voltage
CH2: MULT - pin #3
CH3: VFF - pin #5
CH4: input current

AM13412v1

Figure 26. L6562 FOT input mains surge from 90 V_{ac} to 140 V_{ac} - full load - NO V_{FF} input

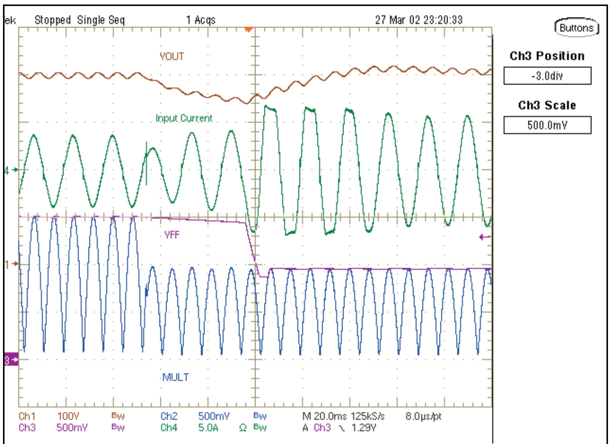


CH1: output voltage
CH2: input rectified mains voltage
CH4: input current

AM13413v1

Figure 27 shows the circuit behavior in case of mains dip: as previously described, the internal circuitry detects the drop of the mains voltage and it activates the C_{FF} internal fast discharge. As visible, in that case the output voltage changes, but after few mains cycle it comes back to the nominal value. The situation is different if we check the behavior of a PFC using the L6562A with FOT and delivering 400 W: in case of a mains dip from 140 Vac to 90 Vac, the output voltage requires a longer time to restore the original value. Testing with a wider voltage variation (e.g. 265 V_{ac} to 90 V_{ac}), the output voltage variation of a PFC without the voltage feed-forward fast discharging is much more emphasized.

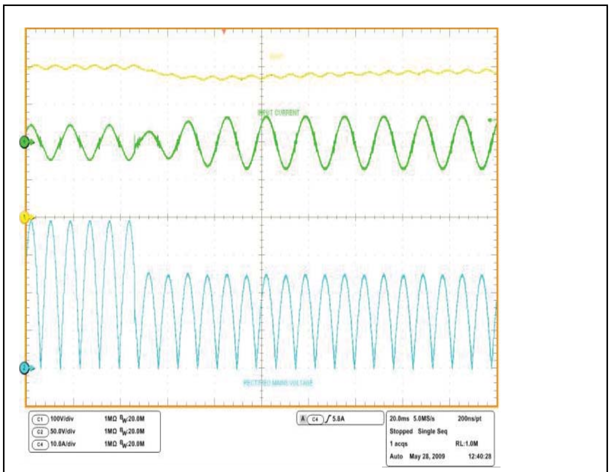
Figure 27. EVL4984-350W input mains dip from 140 V_{ac} to 90 V_{ac} - full load - C_{FF} = 1 µF



CH1: output voltage
CH2: MULT - pin #3
CH1: VFF - pin #5
CH4: input current

AM13414v1

Figure 28. L6562 FOT input mains dip from 140 V_{ac} to 90 V_{ac} - full load - NO V_{FF} input



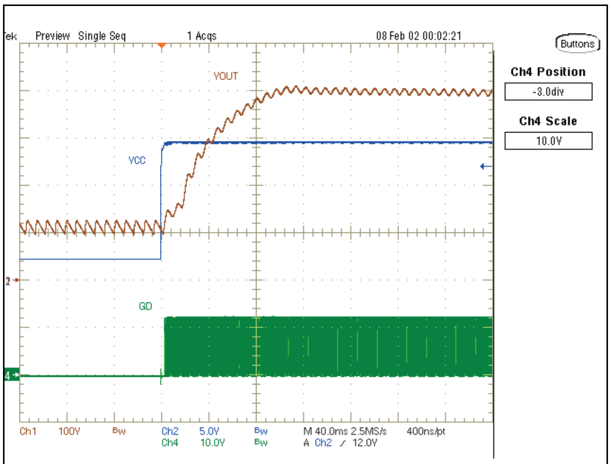
CH1: output voltage
CH2: input rectified mains voltage
CH4: input current

AM13415v1

2.5 Startup

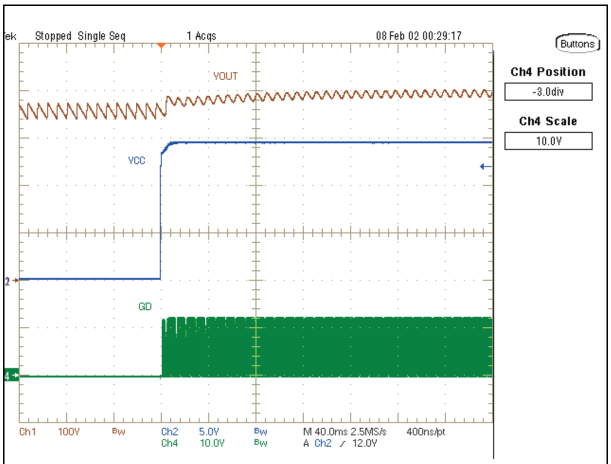
Figure 29 and *Figure 30* represent the output voltage waveform during the startup of the circuit when the mains is plugged in and the external V_{CC} voltage is applied between pin 3 (V_{CC}) and pin 1 (GND) of J3. When the V_{CC} voltage rises up to the turn-on threshold, the L4984D starts the operation. The good phase margin of the compensation network allows a clean startup, without overshoots.

Figure 29. EVL4984-350W start-up at 90 V_{ac} -60 Hz - full load



CH1: PFC output voltage
CH2: VCC - pin #10
CH4: GD - pin #9
AM13416v1

Figure 30. EVL4984-350W start-up at 265 V_{ac} -50 Hz - full load



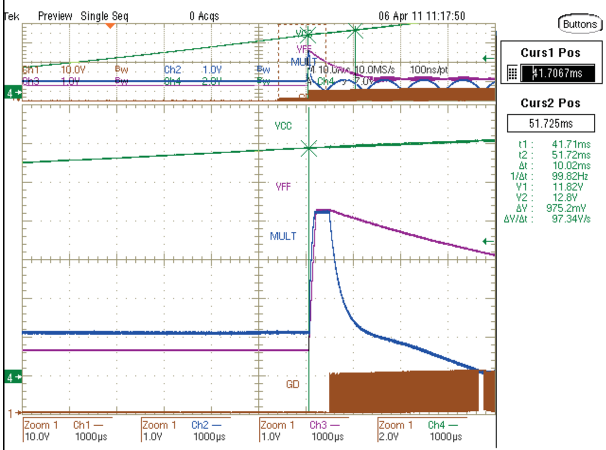
CH1: PFC output voltage
CH2: VCC - pin #10
CH4: GD - pin #9
AM13417v1

To reduce inrush energy at startup or after an auto-restart protection tripping, the L4984D uses an internal soft-start function.

The function is performed by internally pulling the voltage on pin MULT towards an asymptotic level located at about 4.1 V as the device wakes up. This has a twofold effect: on one hand, the output of the multiplier will be lowered through the voltage feed-forward function, thus programming a lower peak current; on the other hand, the off-time of the power switch is considerably prolonged with respect to the normal values programmed by the capacitor connected to pin TIMER. In this way, both the current inrush and the risk of saturating the boost inductor at startup are minimized.

After 300 µs from its activation the pull-up is released. The voltage on pin MULT decays with the time constant determined by the resistor divider that biases the pin and the bypass capacitor typically connected between the pin and ground. At the same time C_{FF} is discharged by turning on the low impedance discharge switch. In this way the programmed current by the multiplier is minimized and increases according to the previously mentioned V_{FF} time constant.

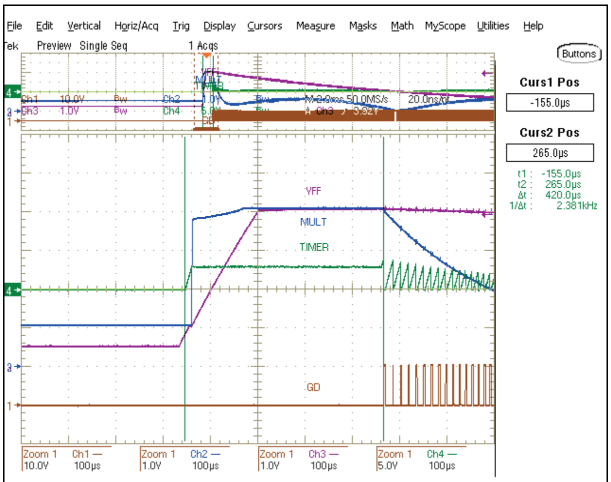
Figure 31. V_{in} 115 V_{ac} - startup by V_{CC}



CH1: GD - pin #9
CH2: MULT - pin #3
CH2: VFF - pin #5
CH4: VCC - pin #10

AM13418v1

Figure 32. V_{in} 115 V_{ac} - startup by V_{CC} - details

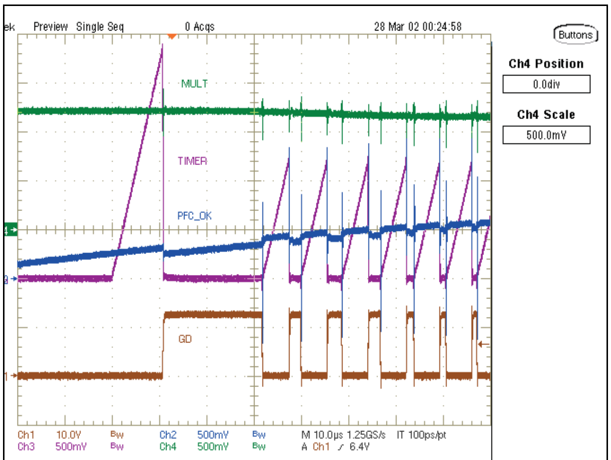


CH1: GD - pin #9
CH2: MULT - pin #3
CH2: VFF - pin #5
CH4: VCC - pin #10

AM13419v1

As shown in *Figure 31* and *Figure 32*, once V_{CC} reaches the V_{ccON} voltage, the MULT pin is pulled up to 4.2 V (4.1V typ. in the datasheet). After 300 us, the V_{FF} capacitor starts discharging and the MOSFET starts switching. After startup T_{off} is properly extended as long as the MULT voltage is higher than the steady state value, then progressively decreased to the value determined by the TIMER capacitance and MULT instantaneous voltage. When the device is disabled and enabled more than one time (burst mode), the PFC_OK is released after the first startup. In this condition, the L4984D does not activate the soft-start procedure, as required in case the burst mode pulses are enabled by a downstream converter via the PFC_STOP pin. The L4984D restarts almost immediately after releasing the PFC_OK pin and GD begins operation just after a T_{off} period.

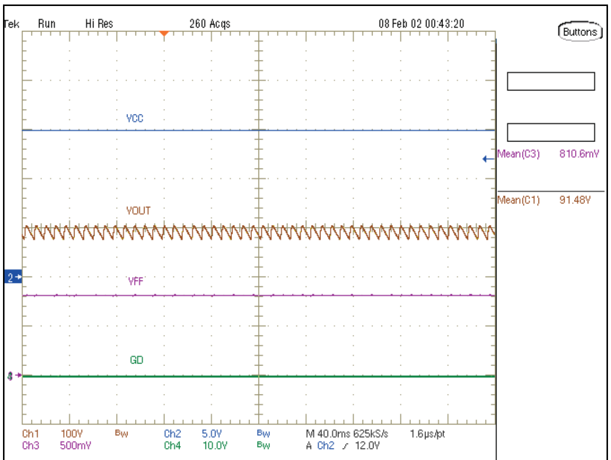
Figure 33. V_{in} 115 V_{ac} startup by VPFC_OK_E (burst mode like) on L4984D



CH1: GD - pin #9
CH2: PFC_OK - pin #6
CH2: VFF - pin #5
CH4: MULT - pin #3

AM13420v1

Figure 34. EVL4984-350W startup attempt at 80 V_{ac} - 60 Hz - full load

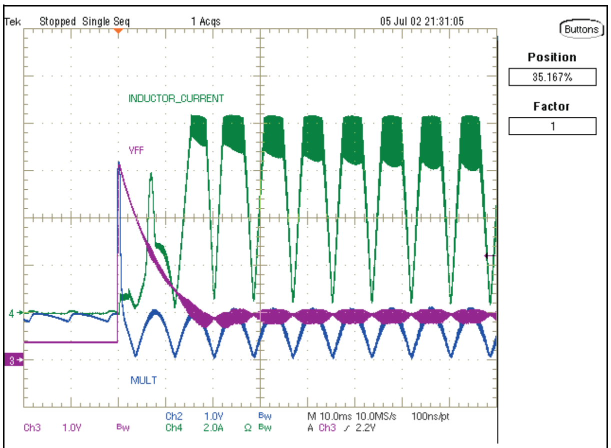


CH1: PFC output voltage
CH2: VCC - pin #10
CH2: VFF - pin #5
CH4: GD - pin #9

AM13421v1

For reference, the waveform of the inductor current during startup has been captured at 90 Vac and full load (*Figure 35* and *Figure 36*). As can be noted, the inductor current does not exhibit any flux accumulation, which sometimes may occur working in CCM. In that case, a higher margin in the PFC inductor calculation has to be considered.

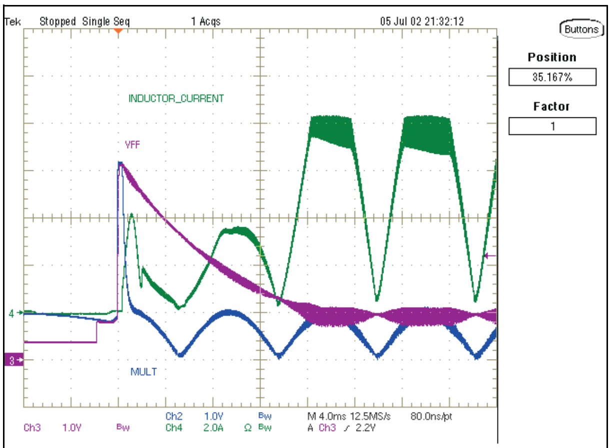
Figure 35. V_{in} 90 V_{ac} - startup at full load



CH2: MULT - pin #3
CH2: VFF - pin #5
CH4: INDUCTOR CURRENT

AM13482v2

Figure 36. V_{in} 115 V_{ac} - startup at full load

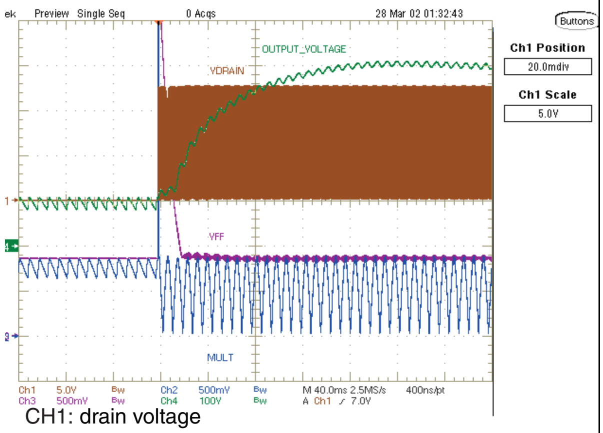


CH2: MULT - pin #3
CH2: VFF - pin #5
CH4: INDUCTOR CURRENT

AM13483v2

A dangerous event for any PFC is operating with an insufficient input voltage. This condition may cause overheating of the power section due to an excess of RMS current. To prevent the PFC from this abnormal operation a brownout protection is needed. It is basically an unlatched shutdown function that has to be activated when a condition of mains undervoltage is detected.The brownout function is implemented in the L4984D by the VFF pin (#5). A voltage below the disable threshold (V_{DIS}, 0.8 V typ.) on the VFF shuts down (no latch) the IC and brings its consumption to a considerably lower level. The L4984D restarts as the voltage at the pin rises above 0.88 V which is the enable threshold (V_{EN}, 0.88 V typ.). As shown in *Figure 34* the startup is inhibited as the voltage on VFF is below 0.8 V, and the PFC is not allowed to start up. In *Figure 37* and *Figure 38* the waveforms of the circuit during operation of the brownout protection are captured. In both cases the mains voltage was increased or decreasing slowly: as visible, both at turn-on or turn-off there are no bouncing or starting attempts by the converter.

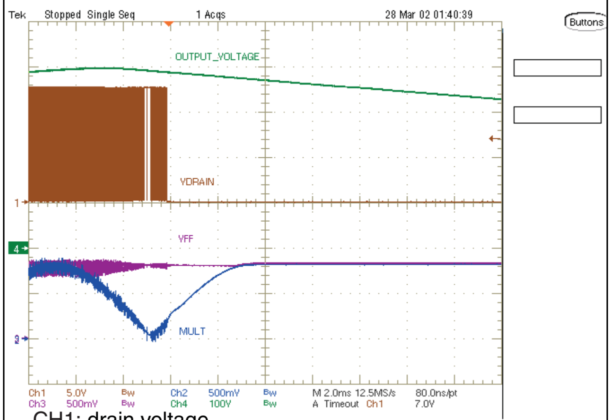
Figure 37. EVL6563S-400W startup with slow input voltage increasing - full load



CH1: drain voltage
CH2: VCC - pin #10
CH2: MULT - pin #3
CH4: output voltage

AM13422v1

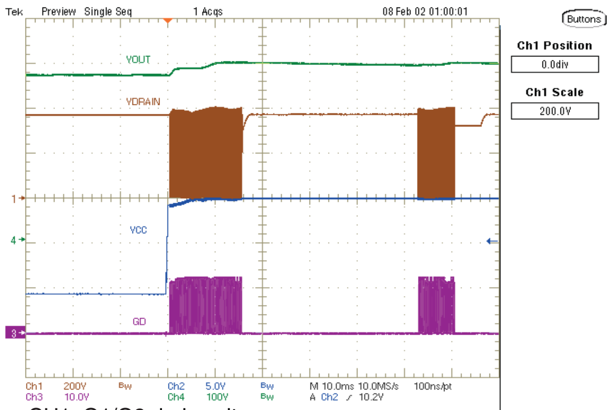
Figure 38. EVL6563S-400W turn-off with slow input voltage decreasing - full load



CH1: drain voltage
CH2: VCC - pin #10
CH2: MULT - pin #3
CH4: output voltage

AM13423v1

Figure 39. EVL4984-350W startup at 265 V -50 Hz - 30 mA load



CH1: Q1/Q2 drain voltage
CH2: VCC - pin #10
CH2: GD - pin #9
CH4: PFC output voltage

AM13424v1

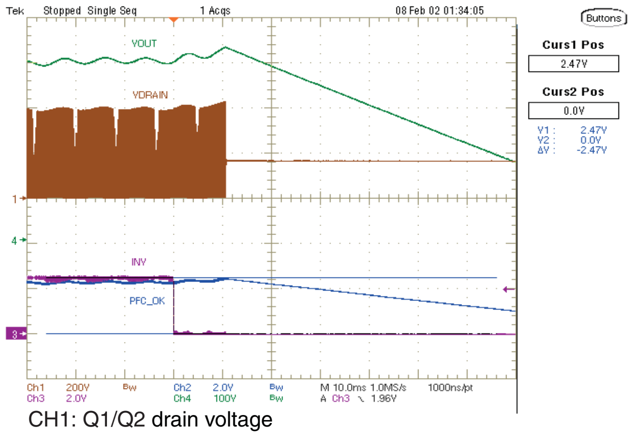
The startup behavior at light load (10 W), powering the L4984D by an external V_{cc} (15 V), is shown in *Figure 39*. It can be noted that the L4984D is working in burst-mode and the PFC keeps the output voltage regulated.

2.6 Overvoltage and open-loop protection

Normally, the voltage control loop keeps the output voltage V_{out} of the PFC pre-regulator close to its nominal value, set by the ratio of the resistors of the output divider (the resistors R6, R8, R13 with R17 and R18). The pin PFC_OK (#6) of the device has been dedicated to monitor the output voltage V_{OUT} with a separate resistor divider (R5+R10+R14 and R23) in order to detect the OVP condition. This divider is selected so that the voltage at the pin reaches 2.5 V when the output voltage exceeds a preset value, usually larger than the maximum V_{OUT} that can be expected, also including worst-case load/line transients.

When the OVP condition is detected, the gate drive activity is immediately stopped until the voltage on the pin PFC_OK drops below 2.4 V. Notice that R5, R10, R14 and R23 can be selected without any constraints. The unique criterion is that both dividers have to sink a current from the output bus which needs to be significantly higher than the current biasing the error amplifier and PFC_OK comparator.

Figure 40. EVL4984-350W open loop at 115 V_{ac} - 60 Hz - full load



CH1: Q1/Q2 drain voltage
CH2: INV - pin #1
CH2: PFC_OK - pin #6
CH4: PFC output voltage

AM13425v1

The OVP function described above is able to handle “normal” overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. In case the overvoltage is generated by a feedback disconnection, for instance, when the upper resistor of the output divider (R6) fails open, the open-loop protection is needed.

The open-loop protection is implemented by the PFC_OK (#6) and INV (#1) pins. If the voltage of the PFC_OK pin exceeds 2.5 V, and at the same time the voltage on INV pin (#1) falls below 1.66 V a feedback failure is assumed, and the device is latched off, stopping the gate drive activity.

The pin PFC_OK doubles its function as a non-latched IC disable: a voltage below 0.23 V will shut down the IC, reducing its consumption below 2 mA. To restart the L4984D simply let the voltage at the pin rise above 0.27 V.

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a PFC_OK pin floating will result in shutting down the L4984D and stopping the pre-regulator.

The event of an open loop is captured in *Figure 40*, we can notice the protection intervention latching the operation of the L4984D. The operation can be resumed by recycling V_{CC}.

2.7 Power management/housekeeping functions

A communication line with the control IC of the cascaded DC-DC converter can be established via the disable function included in the PFC_OK pin. Typically this line is used to allow the PWM controller of the cascaded DC-DC converter to shut down the L4984D in case of light load and to minimize the no-load input consumption. Should the residual consumption of the chip be an issue, it is also possible to cut down the supply voltage. Interface circuits like those are shown in *Figure 41*. Needless to say, this operation assumes that the cascaded DC-DC converter stage works as the master and the PFC stage as the slave or, in other words, that the DC-DC stage starts first, it powers both controllers and enables/disables the operation of the PFC stage.

Figure 41. Interface circuits that let DC-DC converter's controller IC disable the L4984D

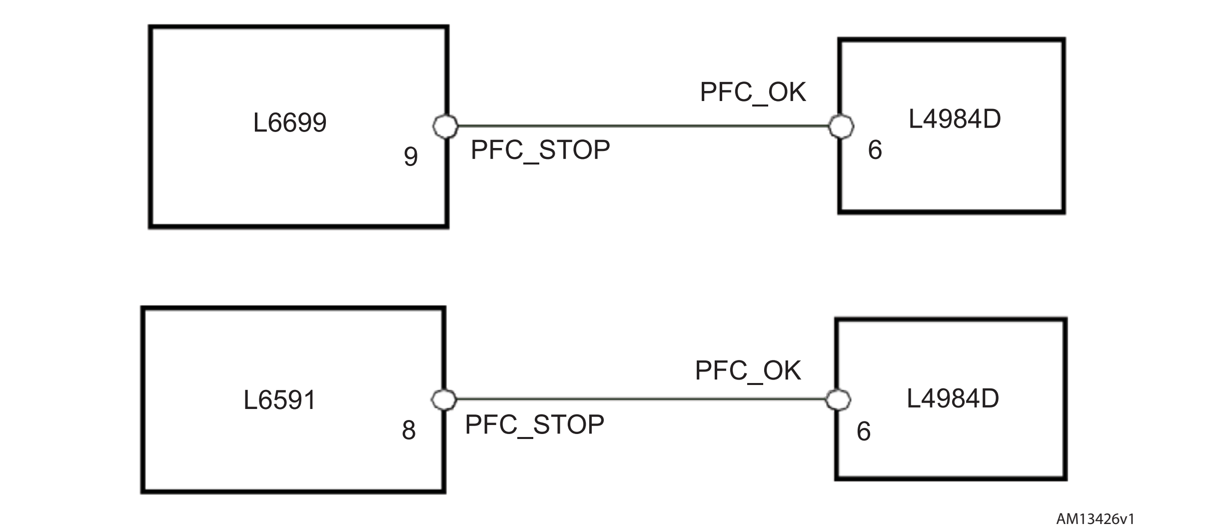


Table 1 summarizes all the operating conditions that cause the device to stop working.

Table 1. Summary of L4984D idle states

Condition	Caused or revealed by	IC behavior	Restart condition	Typical IC consumption	SS activation
UVLO	$V_{cc} < V_{ccOff}$	Disabled	$Vcc > V_{ccOn}$	65 µA	Yes
Standby	$V_{PFC\_OK} < V_{PFC\_OK\_D}$	Stop switching	$V_{PFC\_OK} > V_{PFC\_OK\_E}$	2.2 mA	No
AC brownout	$V_{VFF} < V_{DIS}$	Stop switching	$V_{VFF} > V_{EN}$	1.5 mA	Yes
OVP	$V_{PFC\_OK} > V_{PFC\_OK\_S}$	Stop switching	$V_{PFC\_OK} < V_{PFC\_OK\_R}$	2.2 mA	No
Feedback failure	$V_{PFC\_OK} > V_{PFC\_OK\_S}$ and $V_{INV} < 1.66$ V	Latched-off	$Vcc < Vcc_{restart}$ then $Vcc > Vcc_{On}$	180 µA	Yes
Low consumption	$V_{COMP} < 2.4V$	Burst mode	$V_{COMP} > 2.4V$	2.2 mA	No
Saturated boost inductor	$Vcs > V_{CS\_th}$	Stop switching	Auto restart after 300 s	4 mA	No

3 Thermal measurements

In order to check the design reliability, a thermal mapping by means of an IR camera was done. *Figure 42* and *Figure 43* show thermal measurements of the on-board components at nominal input voltages and full load. Some pointers visible on the pictures placed across key components show the relevant temperature. *Table 2* provides the correlation between the measured points and components, for both thermal maps. The ambient temperature during both measurements was 25 °C. According to these measurement results, all components of the board are working within their temperature limits.

Figure 42. Thermal map at 115 V_{ac} - 60 Hz - full load

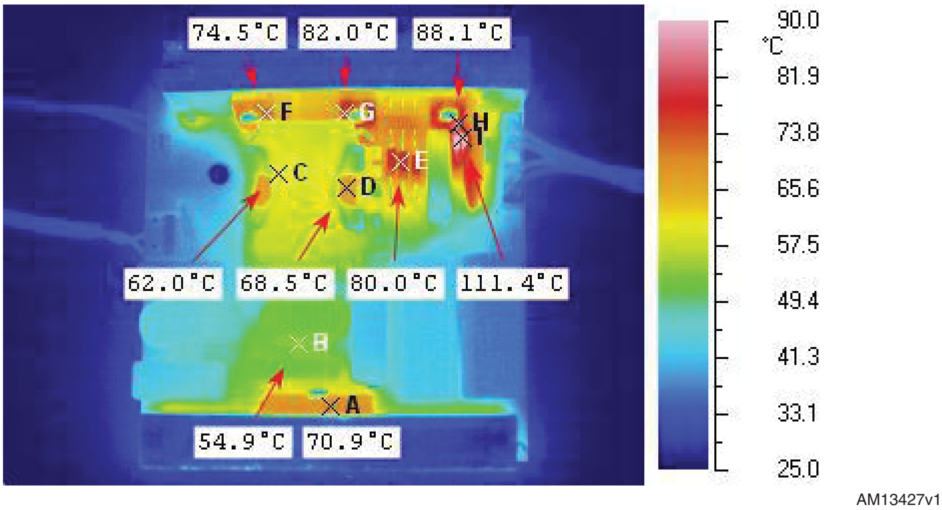


Figure 43. Thermal map at 230 V_{ac} - 50 Hz - full load

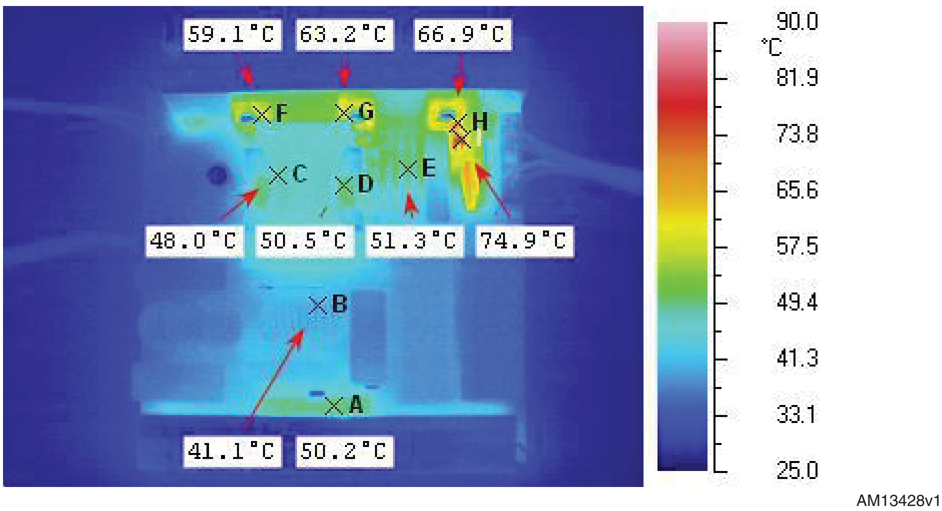


Table 2. Measured temperature table at 115 V_{ac} and 230 V_{ac} - full load

Point	Component	Temperature at 115 V_{ac}	Temperature at 230 V_{ac}
A	D2	70.9 °C	50.2 °C
B	L1	54.9 °C	41.1 °C
C	L3 – CORE	62.0 °C	48.0 °C
D	L3 – Winding	68.5 °C	50.5 °C
E	Rsense	80.0 °C	51.3 °C
F	Q1	74.5 °C	59.1 °C
G	Q2	82.0 °C	63.2 °C
H	D3	88.1 °C	66.9 °C
I	R2	111.4 °C	74.9 °C

4 Conducted emission pre-compliance test-peak detection

In *Figure 44* to *Figure 47* the peak measurements of the conducted noise at full load and nominal mains voltages are given. The limits shown on the diagrams are relevant to the EN55022 Class-B, the most popular standard for European equipment using a two-wire mains connection. As visible in the diagrams, in all test conditions there is a good margin of the measurements with respect to the limits.

Figure 44. 115 V_{ac} and full load - phase

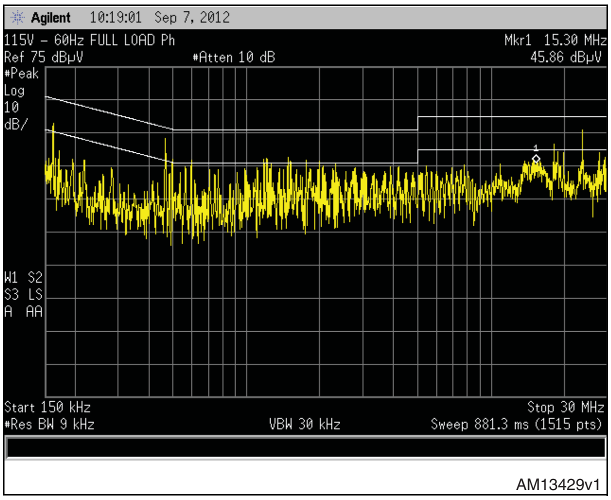


Figure 45. 115 V_{ac} and full load - neutral

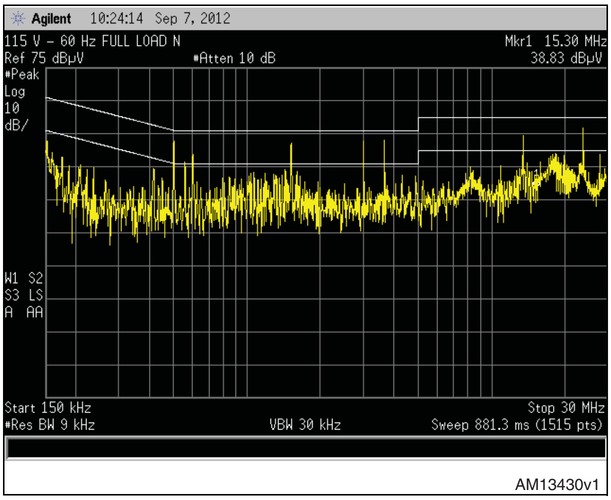


Figure 46. 230 V_{ac} and full load - phase

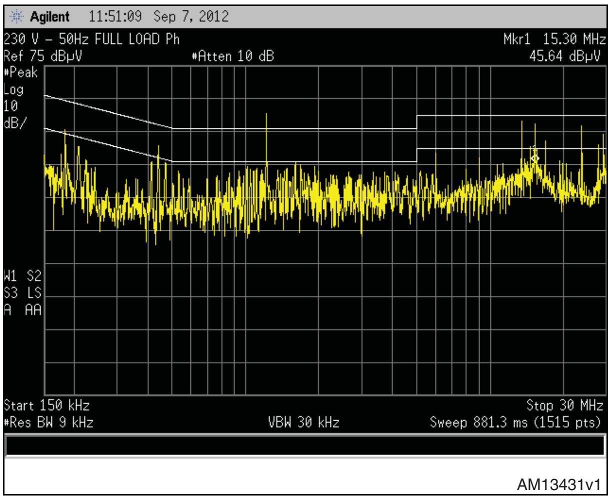
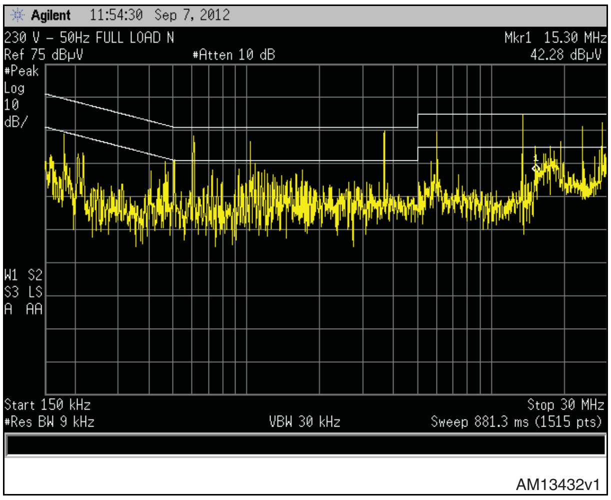


Figure 47. 230 V_{ac} and full load - neutral



5 Bill of material

Table 3. EVL4984-350W CCM PFC demonstration board bill of material

Description	Part type/ part value	Case style/ package	Description	Supplier
C1	220 nF - 520 V	7.5 x 26.5 mm	520 V - FLM cap - B32673T5224	Epcos
C2	1 µF - 520 V	10.5 x 26.5 mm	520 V - FLM cap - B32673Z5105	Epcos
C3	100 µF - 450 V	Dia. 18 x 40 mm	450 V - aluminium elcap - KXG series - 105 °C	Nippon Chemi-Con
C4	100 µF - 450 V	Dia. 18 x 40 mm	450V - aluminium elcap - KXG series - 105 °C	Nippon Chemi-Con
C5	470N - X2	10.5 x 26.5 mm	X2 - FLM cap - B32923A3474M	Epcos
C6	1 µF - X2	11 x 26.5 mm	X2 - FLM cap - B32923C3105	Epcos
C8	68N	0805	100 V cercap - general purpose - X7R - 10%	AVX
C9	470N	1206	100 V cercap - general purpose - X7R - 10%	Kemet
C10	100 µF-35 V	Dia. 8 x 11 mm	50 V - aluminium elcap - YXF SERIES - 105 °C	Rubycon
C11	680N	0805	25 V cercap - general purpose - X7R - 10%	Kemet
C12	10N	0805	50 V cercap - general purpose - X7R - 10%	Kemet
C13	330 pF	0805	50 V cercap - general purpose - COG - 5%	Epcos
C14	680 pF	0805	50 V cercap - general purpose - COG - 5%	Epcos
C15	1 µF	1206	50 V cercap - general purpose - X7R - 10%	TDK
C16	2N2	0805	50 V cercap - general purpose - X7R - 10%	Kemet
C17	470 nF - 520 V	7 x 26.5 mm	520 V - FLM cap - B32673Z5474K***	Epcos
D1	1N5406	DO-201	Rectifier - general purpose	Vishay
D2	D15XB60H	DWG	Single phase bridge rectifier	Shindengen
D3	STTH8S06FP	TO-220	Ultrafast high-voltage rectifier	ST
D6	LL4148	Minimelf	High-speed signal diode	Vishay
D7	LL4148	Minimelf	High-speed signal diode	Vishay
F1	Fuse T6.3A	4 x 8.5 mm pitch 5.08 mm	Subminiature fuse 392/TE5 - time delay 6.3 A	Littelfuse
HS1	Heatsink	DWG	Heatsink for D2	Meccal
HS2	Heatsink	DWG	Heatsink for Q1, Q2 and D3	Meccal
J1	09-65-2038	DWG	KK PCB conn. - straight - pitch 3.96 mm - 3 pins (central removed)	Molex
J2	10-16-1051	DWG	KK PCB conn. - straight - pitch 5.08 mm - 5 pins (central removed)	Molex
J3	22-27-2031	DWG	KK PCB connector, straight, pitch 2.54 mm - 3 pins	Molex

Table 3. EVL4984-350W CCM PFC demonstration board bill of material (continued)

Description	Part type/ part value	Case style/ package	Description	Supplier
JPX1	Shorted	WIRE	Wire jumper	
JPX2	Shorted	WIRE	Wire jumper	
JPX3	Shorted	WIRE	Wire jumper	
JPX4	Shorted	WIRE	Wire jumper	
JPX5	Shorted	WIRE	Wire jumper	
L1	70 µH - 7 A	DWG	DM inductor - 1119.0013	Magnetica
L2	3 mH - 7 A	DWG	EMI FILTER - 1606.0007	Magnetica
L3	700 µH	DWG	PFC inductor - 2097.0002	Magnetica
L4	2743005112	DWG	Ferrite bead dia. 3.5 x 6 mm vertical	Fair rite
Q1	STF21N65M5	TO-220FP	N-channel Power MOSFET	ST
Q2	STF21N65M5	TO-220FP	N-channel Power MOSFET	ST
R1	750K	1206	SMD standard film res. - 1/4 W - 5% - 250 ppm/°C	Vishay
R2	NTC 1R0-S237	dia. 15 x 7 p. 7.5 mm	NTC resistor P/N B57237S0109M000	Epcos
R3	750K	1206	SMD standard film res. - 1/4 W - 5% - 250 ppm/°C	Vishay
R4	750K	1206	SMD standard film res. - 1/4 W - 5% - 250ppm/°C	Vishay
R5	3M3	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R6	2M2	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R8	2M2	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R10	3M3	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R12	1M0	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R13	2M2	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R14	3M3	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R16	1M0	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R17	56 K	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R18	160 K	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R19	6R8	0805	SMD standard film res. - 1/8 W - 5% - 250 ppm/°C	Vishay
R20	3R9	0805	SMD standard film res. - 1/8 W - 5% - 250 ppm/°C	Vishay
R21	100 K	0805	SMD standard film res. - 1/8 W - 5% - 250 ppm/°C	Vishay
R22	1M0	1206	SMD standard film res. - 1/4 W - 1% - 100 ppm/°C	Vishay
R23	56 K	0805	SMD standard film res. - 1/8 W - 1% - 100 ppm/°C	Vishay
R24	24 K	0805	SMD standard film res. - 1/8 W - 5% - 250 ppm/°C	Vishay
R25	6R8	0805	SMD standard film res. - 1/8 W - 5% - 250 ppm/°C	Vishay
R26	3R9	0805	SMD standard film res. - 1/8 W - 5% - 250 ppm/°C	Vishay

Table 3. EVL4984-350W CCM PFC demonstration board bill of material (continued)

Description	Part type/ part value	Case style/ package	Description	Supplier
R27	0R33	PTH	RSMF1TB - metal film res. - 1 W - 2% - 250 ppm/°C	Akaneohm
R28	1M0	0805	SMD standard film res - 1/8 W - 1% - 100 ppm/°C	Vishay
R29	1 K0	0805	SMD standard film res - 1/8 W - 5% - 250 ppm/°C	Vishay
R30	0R33	PTH	RSMF1TB - metal film res - 1 W - 2% - 250 ppm/°C	Akaneohm
R31	0R33	PTH	RSMF1TB - metal film res - 1 W - 2% - 250 ppm/°C	Akaneohm
R32	10R	0805	SMD standard film res - 1/8 W - 5% - 250 ppm/°C	Vishay
R33	100R	1206	SMD standard film res - 1/4 W - 5% - 250 ppm/°C	Vishay
RV1	300 V_{ac}	dia. 15 x 5 p. 7.5 mm	300 V metal oxide varistor - B72214S0301K101	Epcos
U1	L4984D	SSOP10	CCM PFC controller	ST
Z1	PCB rev. 1			

6 PFC coil specification

6.1 General description and characteristics

- Application type: consumer, home appliance
- Inductor type: open
- Coil former: vertical type, 6 + 6 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temp.: 60 °C
- Unit finishing: varnished

6.2 Electrical characteristics

- Converter topology: CCM boost PFC preregulator
- Core type: pq35/35-PC44 or equivalent (center-leg gapped)
- Operating freq. range: 70 kHz - 135 kHz
- Primary inductance: 700 µH ±15% at 1 kHz-0.25 V (measured between pins 5 - 2)
- Primary rms current 3.5 A
- Primary peak current 7.5 A

Figure 48. Electrical diagram

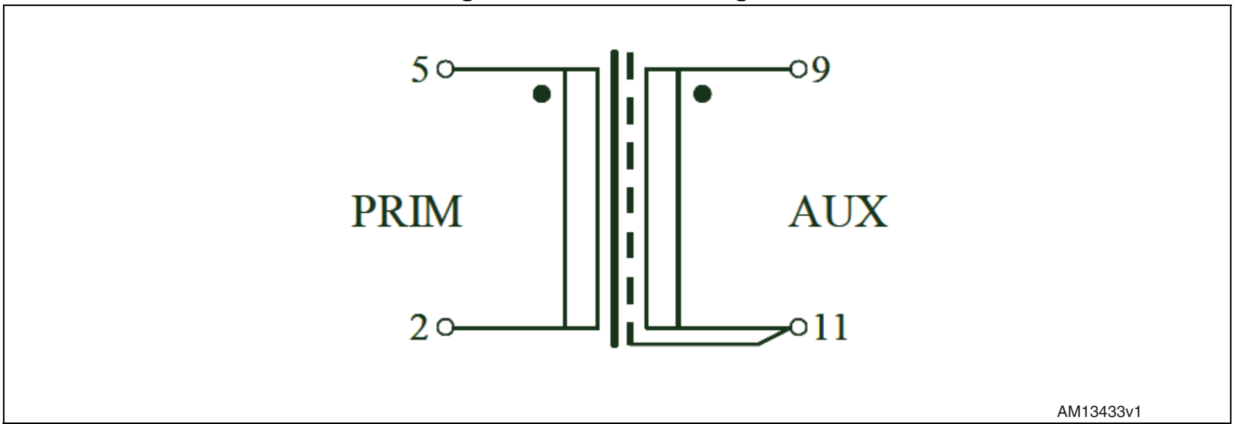


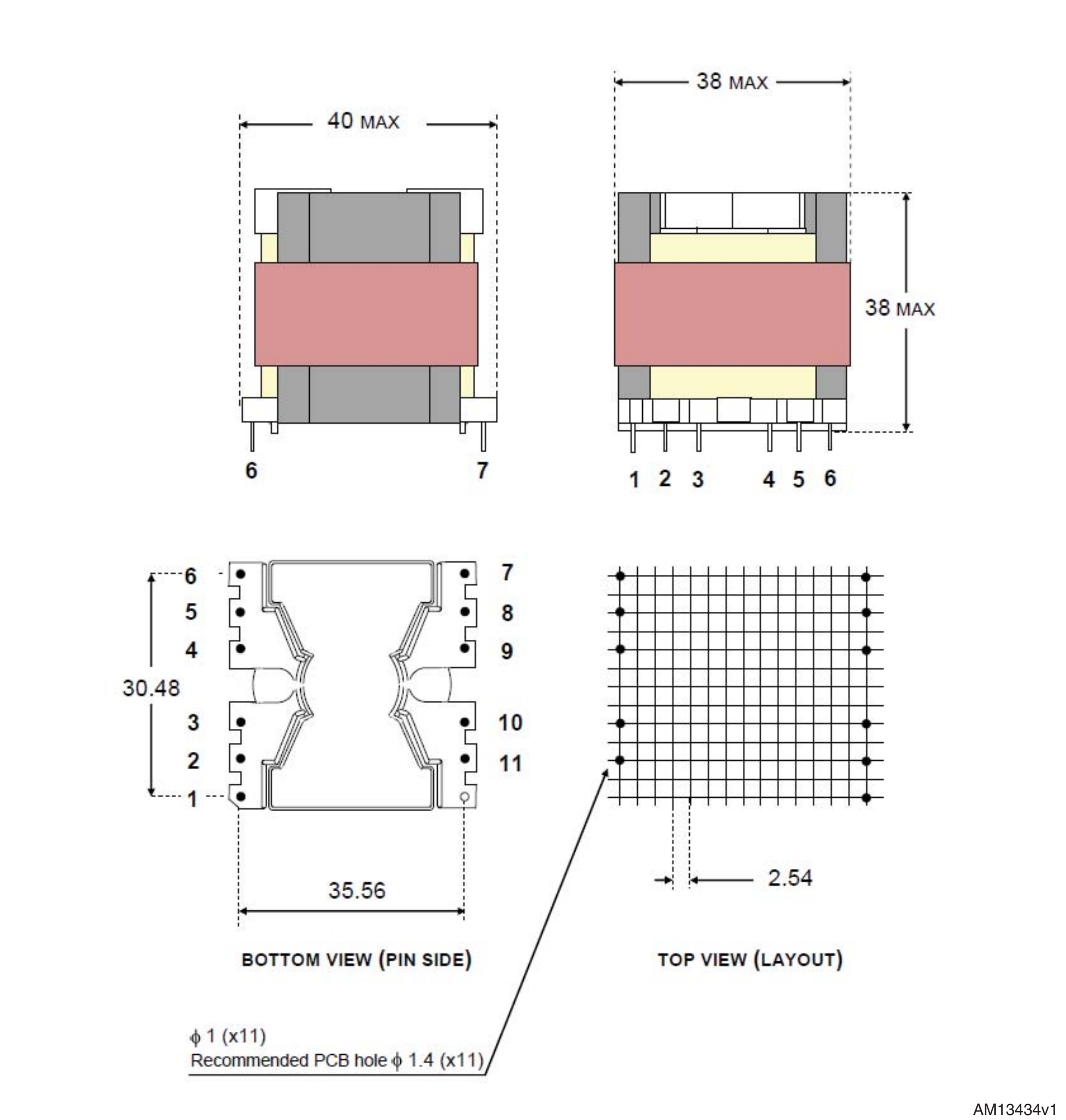
Table 4. Winding characteristics

Windings	Start pins	End pins	Number of turns	Wire type	Wire diameter
AUX	9	11	5 (spaced)	Litz – G2	0.28 Ø
PRIM	5	2	70	Single – G2	Litz 0.2 Ø x 30

6.3 Mechanical aspect and pin numbering

- Maximum height from PCB: 38 mm
- Coil former type: vertical, 6 + 6 pins (pin 12 is removed)
- Pin distance: 5.08 mm
- Row distance: 30.48 mm
- External copper shield: not insulated, wound around the ferrite core and including the coil former; it is connected to pin 11 by a soldered solid wire

Figure 49. PFC coil mechanical aspect



6.4 Manufacturer

- MAGNETICA di R. Volpini - Italy
- PFC Inductor P/N: 2097.0002

7 References

- L4984D - CCM PFC controller datasheet
- AN4149 - Designing a CCM PFC pre-regulator based on the L4984

8 Revision history

Table 5. Document revision history

Date	Revision	Changes
05-Mar-2013	1	Initial release.
20-Jun-2013	2	Updated title in cover page. Added cross-references to *Section 2.1* and *Section 4*. Updated *Figure 15*. Corrected units in *Section 6.1*. Minor corrections throughout document.