AN4214
Application note

High power factor flyback converter using the L6564

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Introduction

This application note describes the example of single stage high power factor (HPF) flyback topology using ST's L6564 PFC controller. The L6564 is a current mode PFC controller operating in transition mode (TM). The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide range mains operation with an extremely low THD, even over a large load range. The main drawback of such flyback topology with HPF is that it has significant magnitude of twice the mains frequency ripple at output DC voltage because there is no electrolytic capacitor after bridge rectification. But there are some applications like lighting for LED driving, battery chargers, where ripple voltage is not a big concern, since in these applications the loads are mostly constant-current driven with acceptable ripple or any kind of load which is powered through followed DC-DC downstream converters connected to output of HPF flyback.

The output voltage is controlled by means of a voltage mode error amplifier and an accurate (1% at Tj = 25 °C) internal voltage reference. The loop stability is optimized by the voltage feedforward function ($1/V^2$ correction), which in this IC uses a proprietary technique that considerably improves line transient response as well in case of both drops and surges ("bidirectional") of the mains.

In addition to overvoltage protection being capable of controlling the output voltage in the PFC stage during transient conditions, the IC also provides protection against feedback loop failures or erroneous settings. The feature is quite useful in case of flyback operation to detect output voltage for any primary auxiliary winding and trigger the protection to shutdown the converter in case output voltage exceeds the nominal value.

Other on-board protection functions allow brownout conditions and magnetic saturation to be safely handled. The brownout is sensed through the MULT pin to shut down the converter in case the input mains supply drops below the minimum operating voltage level.

The L6564 main features are:

- Fast "bidirectional" input voltage feedforward ($1/V^2$ correction)
- Accurate adjustable output overvoltage protection
- Protection against feedback loop disconnection (latched shutdown)
- Inductor saturation protection
- AC brownout detection
- Low (100 µA) start-up current
- 6 A max. operating bias current
- 1% (at T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SSOP10 package

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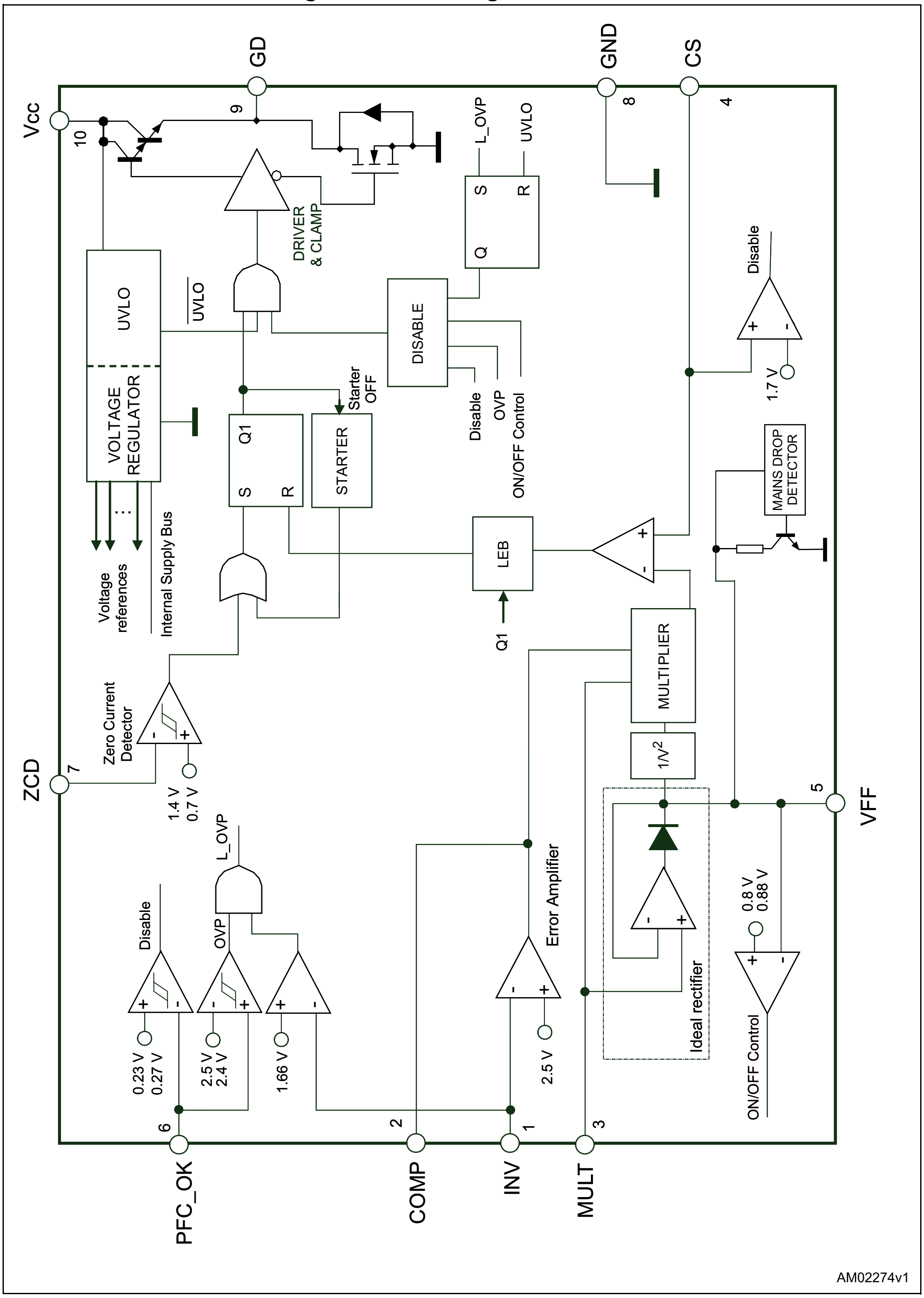
1 Block diagram

Figure 1. Block diagram of L6564



2 SMPS description

The main feature of this converter is that the input current is almost in phase with the mains voltage, therefore the power factor is close to unity and hence the low current harmonics. This is achieved using the L6564 TM PFC controller, which shapes the input current as a sine wave in phase with the mains voltage. The power supply utilizes a typical flyback converter topology, using a transformer to provide the required insulation between the primary and secondary side. The converter is connected after the mains rectifier and the capacitor filter, which in this case is quite small to prevent damage to the shape of the input current. The flyback switch is represented by the power MOSFET M1, and driven by the L6564.

At startup, the L6564 is powered by the VCC capacitor (C16), which is charged via resistors R4 and R8. As the capacitor C16 charges to the turn-on threshold of the L6564 (typically at 12 V), the transformer T1 auxiliary winding (pins 5-6) generates the VCC voltage, rectified by D8 and R13, that powers the L6564 during normal operation. R12 is also connected to the auxiliary winding to provide the transformer demagnetization signal to the L6564 ZCD pin, turning on the MOSFET at any switching cycle. The MOSFET used is the STP7N80K5, a ST's K5 high voltage MOSFET series device housed in a TO-220 package, and needing only a small heat sink. The transformer is layer type, using a standard ferrite size ER28. The flyback reflected voltage is close to 180 V, providing enough room for the leakage inductance voltage spike still within the reliability margin of the MOSFET even at 300 V_{ac} input.

The RCD snubber circuit using R5, C5 and D6 clamps the peak of the leakage inductance voltage spike at MOSFET turn-off. Resistor R3 is usually inserted in series with subbing capacitor C5 to kill the spike and reduces further the EMI generated due to leakage spikes. The resistors R33 and R34 sense the current flowing into the transformer primary side. Once the signal at the current sense pin has reached the level programmed by the internal multiplier of the L6564, the MOSFET turns off. The divider R11, R14 and R18 provides the L6564 multiplier pin with instantaneous voltage information which is used to modulate the current flowing into the transformer primary side. C17 is a small noise suppression capacitor, of course the purpose of this capacitor is to prevent disturbance to the actual sinusoidal mains information.

The output regulation is done by means of an isolated voltage loop by the optocoupler U2, and using an inexpensive TL431 to drive the optocoupler. For an LED driving application, additional constant current drive circuitry using the SEA05 can be implemented as described in the schematic, whereas the current signal is detected by sensing resistors R9, R10. The opto-transistor modulates the input voltage of the L6564 internal amplifier, thus closing the voltage loop. The output rectifier is a fast recovery type, selected according to its maximum reverse voltage, forward voltage drop and power dissipation. A small LC filter is added on the output, filtering the high frequency ripple.

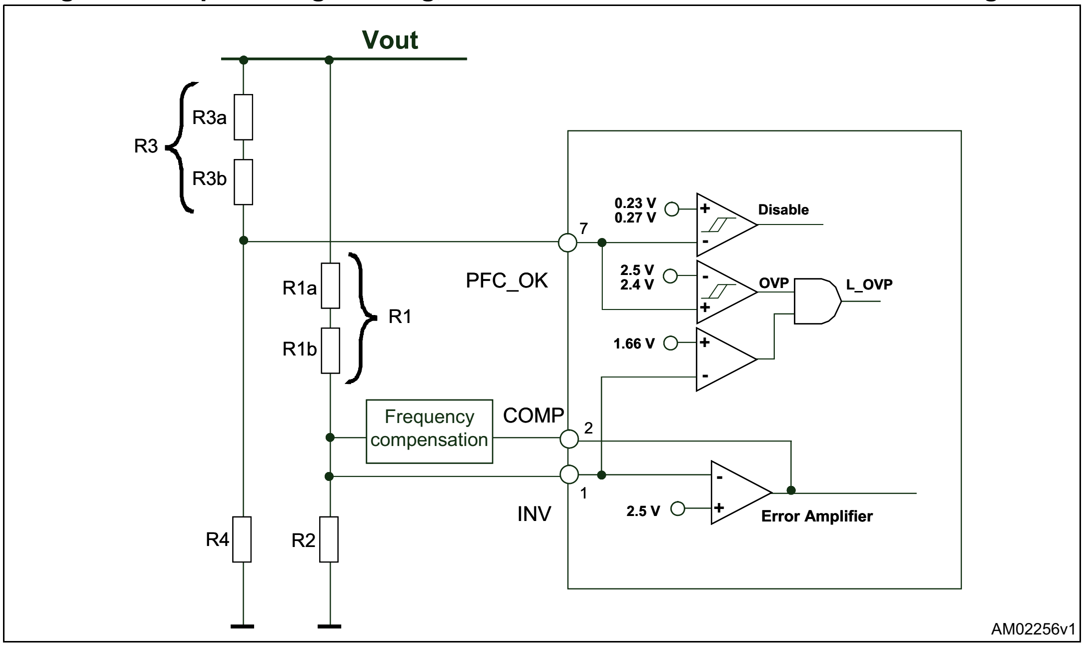
Compared to the L6562A (8-pin TM PFC controller), the L6564 has some additional features and hence there is additional circuitry incorporated in the schematic for utilizing the features of the L6564. The L6564 also has two additional pins: VFF and PFC_OK. The functions of these pins are described in the following paragraphs.

2.1 PFC_OK

2.1.1 PFC_OK function in PFC operation

PFC pre-regulator output voltage monitoring/disable function: This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage on the pin exceeds 2.5 V the IC stops switching and restarts as the voltage on the pin falls below 2.4 V. However, if the voltage of the INV pin falls 40 mV below that of the pin PFC_OK, a feedback failure is assumed. In this case the device is latched off due to feedback failure protection (FFP). Normal operation can be resumed only by cycling V_{CC}, bringing its value lower than 6 V before moving up to the turn-on threshold. If the voltage on this pin is brought below 0.23 V, the IC is shut down. To restart the IC the voltage on the pin must go above 0.27 V. This can also be used as a remote on/off control input. Referring to the circuit portion below, R3 and R4 composes the network to activate PFC output overvoltage shutdown.

Figure 2. Output voltage setting, OVP and FFP functions: internal block diagram

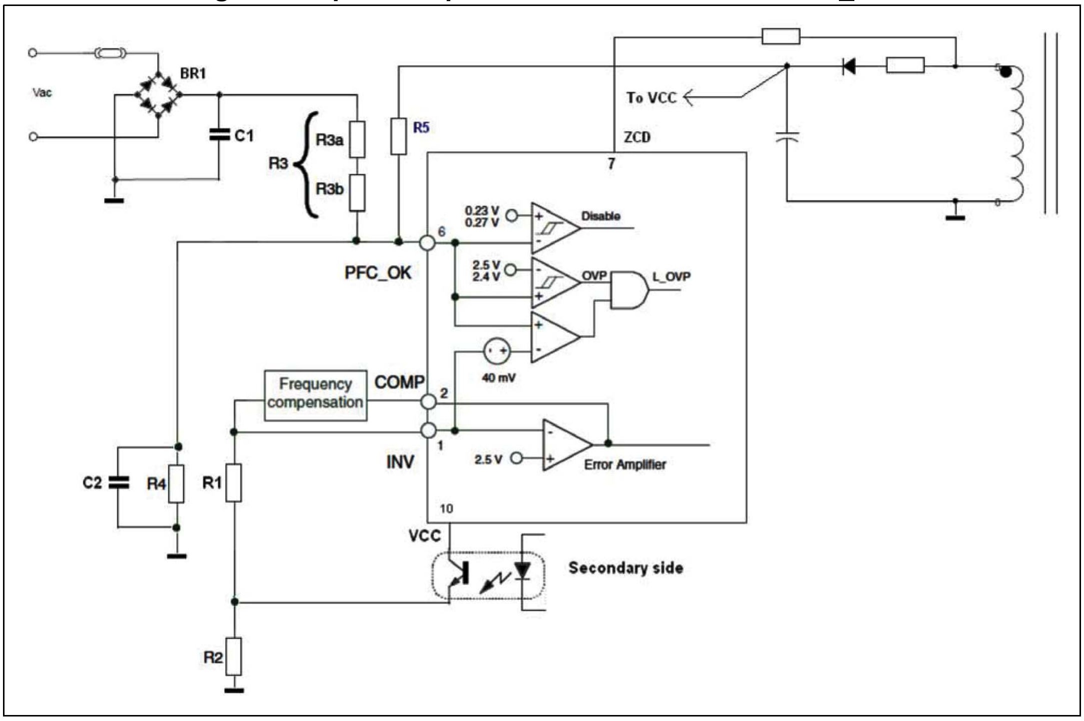


2.1.2 PFC_OK function in flyback operation

The same pin can be also be used in case of flyback converter to shut down the converter in case of either input overvoltage or output overvoltage. For input overvoltage protection, one can bias the pin using resistor divider network at rectified DC voltage to activate input overvoltage protection at the required mains OVP level. Referring to the circuit portion below, R3, R4 composes the network to activate mains overvoltage shutdown, where the small capacitor C2 is used to average the DC value of sensing voltage at the PFC_OK pin. In the schematic, the biasing components R2, R6, R7 and R22 comprise the input OVP detection circuit. The divider ratio is selected to provide 2.5 V at required mains OVP level.

If output overvoltage protection is preferred instead of mains OVP, we can utilize the auxiliary winding output used to provide the operating voltage to the controller as well as demagnetization input to ZCD. Since we get the reflection of output voltage at auxiliary output supply, we can simply tap the signal for PFC_OK which is programmed to 2.5 V using the resistor divider network at the desired output OVP. This is achieved using resistor divider network R5 and R4 at auxiliary output supply. In the schematic (see Figure 36 on page 30) we have implemented an input OVP protection network to bias PFC_OK.

Figure 3. Input OVP protection network to bias PFC_OK



2.1.3 VFF pin and brownout function

This is second input to the multiplier block for 1/V² function. A capacitor and a parallel resistor must be connected from this pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a DC level equal to the peak voltage on the pin MULT (3), compensates the control loop gain dependence on the mains voltage. The variation of internal current reference signal VCSX versus the mains voltage level detected at MULT input (VFF = VMULT) is shown in the graph in Figure 4. This is the last signal which is compared with the error signal to output the required gate signal ON time. Never connect the pin directly to GND, but with a resistor ranging from 100 kΩ (minimum) to 2 MΩ (maximum). This pin is internally connected to a comparator in order to provide the brownout (AC mains under voltage) protection. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The IC restarts as the voltage at this pin goes above 0.88 V.

Note: This is one of the important features of the L6564 where we can manage the overload condition and prevent excessive current from flowing through the input section at worst low mains operating condition. So as the mains voltage drops below a programmed level, the IC stops as the VFF pin detects the brownout level.

Figure 4. Voltage feedforward: squarer-divider ($1/V^2$) block diagram and transfer characteristic

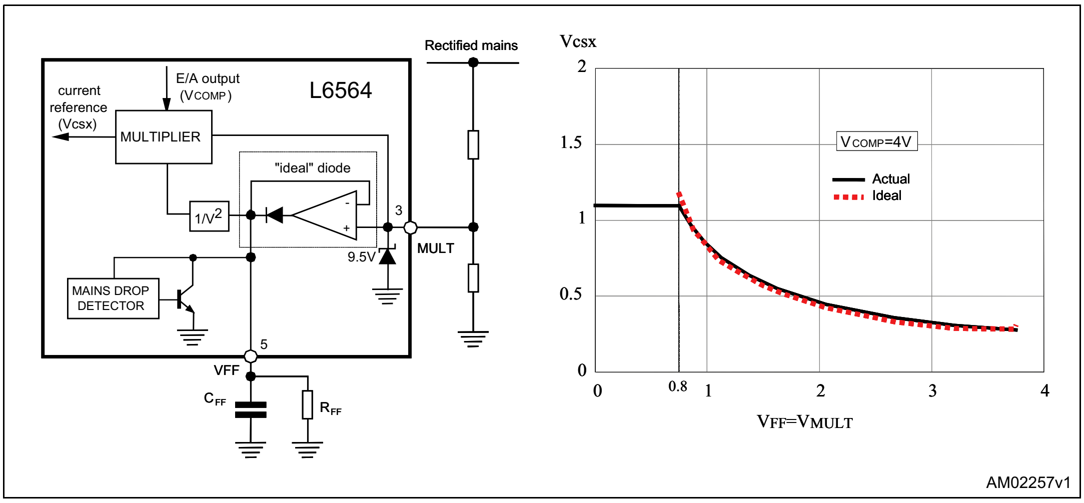
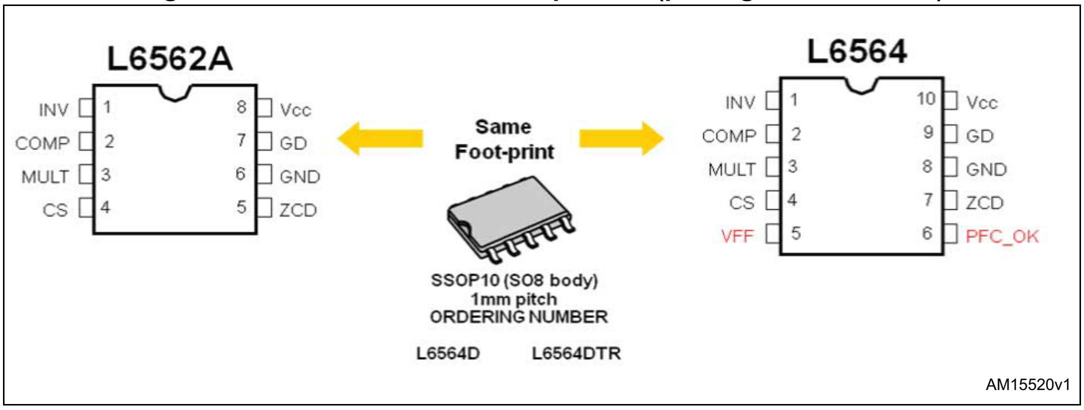


Figure 5. L6562A and L6564 comparison (package and features)



The L6564 is the same as the L6562A, but with the followings additional features:

- Brownout protection: prevents bridge inductor and MOSFET damage
- Inductor saturation protection: prevents MOSFET damage
- Feedback disconnection protection: prevents bulk capacitor burn
- Improved noise immunity: easier PCB layout
- Voltage feedforward: high line/load transient rejection
- Remote ON/OFF control: to easy communicate with PWM stage

3 Basic specifications

Table 1. Basic specifications of SMPS

Parameters	Limits
Rated input voltage range	190 - 265 V_{ac}
Minimum voltage operation (in case of line sag)	140 V_{ac}
Input overvoltage shutdown	> 275 V_{ac}
Input supply frequency (fL)	47 - 63 Hz
Input / output isolation	Yes, > 2.7 kV
Power factor correction	Yes, > 0.95
THD	< 20%
Nominal output voltage	75 V ± 1.5 V
Load current	0.7 A
No load input power at 230 V_{ac}(1)	< 0.75 W
Total output power	55 W
Efficiency (full load for wide mains variations)	> 85%
Output voltage pk-pk ripple(2.fL)	< 20%
Topology	Single stage HPF flyback
Maximum ambient temperature	50 °C

1. The no load power consumption is measured after removing the resistors used for input OVP (R2, R6, R7).

Table 2. Transformer specification

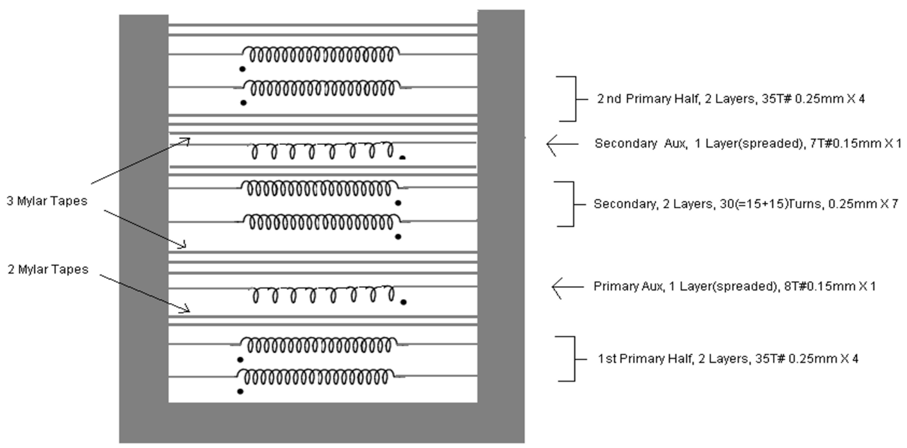
Parameters	Limits
Max. output power	Max. 55 W
Primary inductance	0.62 ± 0.01 mH at 50 KHz
Primary side leakage inductance	< 10 µH at 50 KHz
Peak primary current	2.8 A
Average primary current	0.9 A
Saturation current	3.5 A
Operating switching frequency	50 KHz min. to 125 KHz max.
Core size	ER28/17/11
Ferrite material	N87, EPCOS
Bobbin	12 pins, horizontal
Dielectric strength	> 2.7 kV
Approx air gap (central limb)	0.8 mm

Table 3. Winding details

Winding name	Start	Stop	No. of turns	Wire gauge	Order of windings
Np1	3	2	35	4 x 0.25 mm	Bottom
Naux1	5	6	8	0.15 mm	Above Np1
Nsec	12	10	30	7 x 0.2 5 mm	Above Naux
Naux2	8	7	7	0.15 mm	Above Nsec
Np2	2	1	35	4 x 0.25 mm	Topmost

4 Transformer construction

Figure 6. Transformer construction



5 Test results

The converter is tested at full load conditions from 140 Vac to 265 Vac and following are the test results as shown in *Table 4*.

Table 4. Test results

Vinac (Vrms)	Arms	PF	%ITHD	Pin (W)	Vo (Vdc)	Io (Adc)	Po (W)	% efficiency	Ior (mA)(1)
140	0.449	0.999	5.16	64.08	76.4	0.72	55.00	85.84	122
150	0.417	0.999	5.52	63.13	76.2	0.72	54.86	86.91	120
190	0.321	0.996	9.78	61.30	76.1	0.71	54.26	88.51	116
230	0.263	0.991	13.3	60.23	75.9	0.72	54.27	90.10	112
265	0.231	0.973	15.9	59.57	75.5	0.71	53.76	90.24	112

1. Ior = load current peak-peak ripple.

Figure 7. Current THD vs. mains voltage

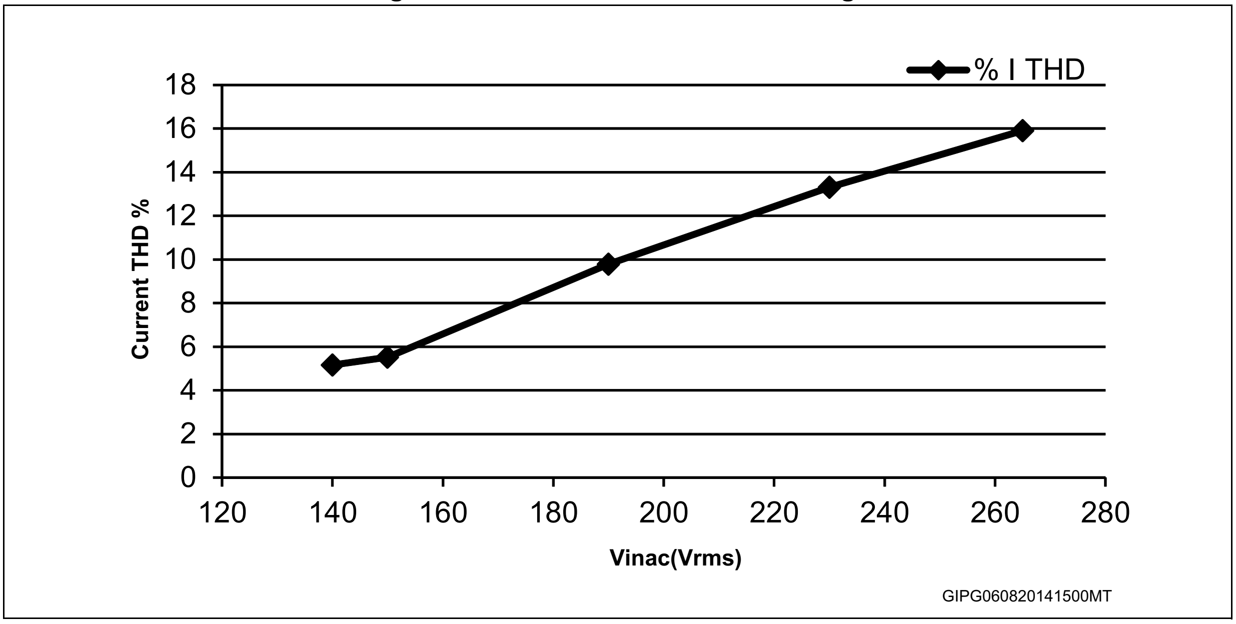


Figure 8. Power factor vs. mains voltage

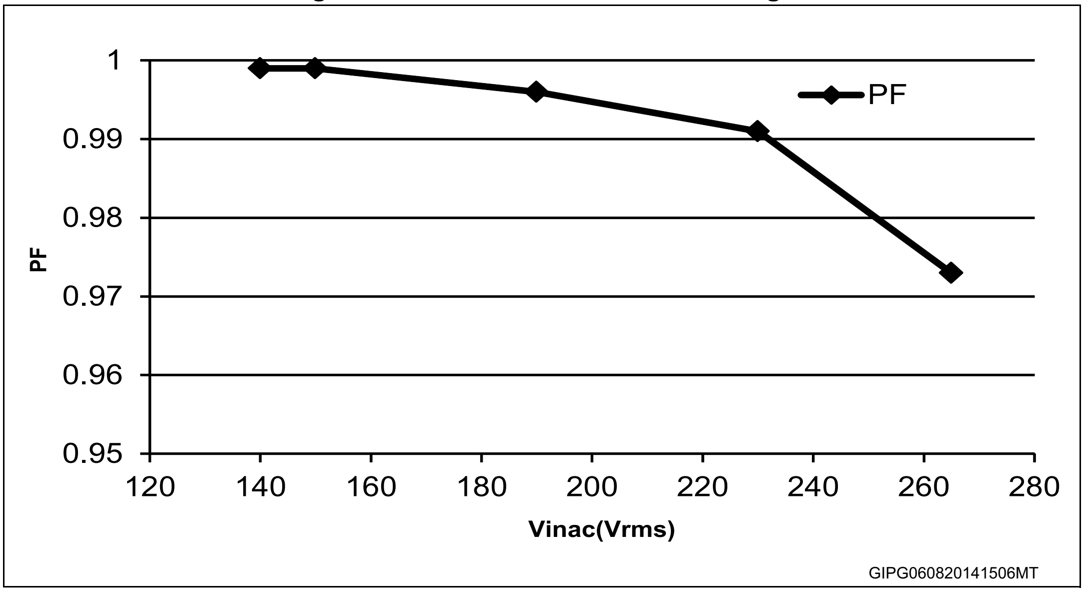
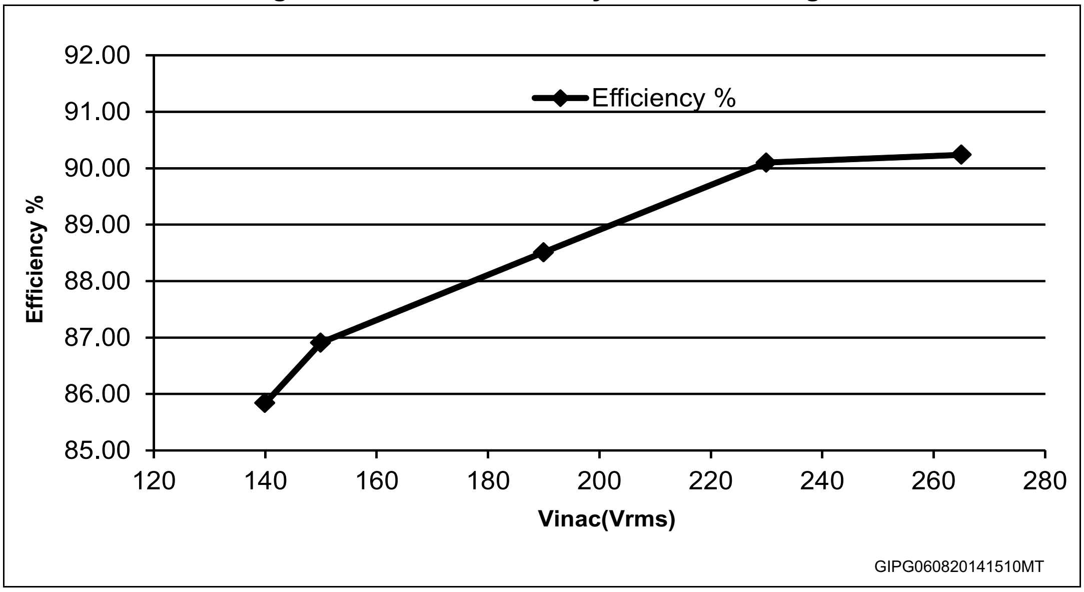


Figure 9. Full load efficiency vs. mains voltage



6 Waveforms

6.1 Mains voltage and input current waveforms

The converter is loaded at full load at input mains current is captured at different line conditions: 140 Vac, 190 Vac, 220 Vac and 265 Vac as shown from *Figure 10* to *14*.

Figure 10. Ch: 4-input voltage; Ch: 2-input current waveforms at 140 V_{ac}

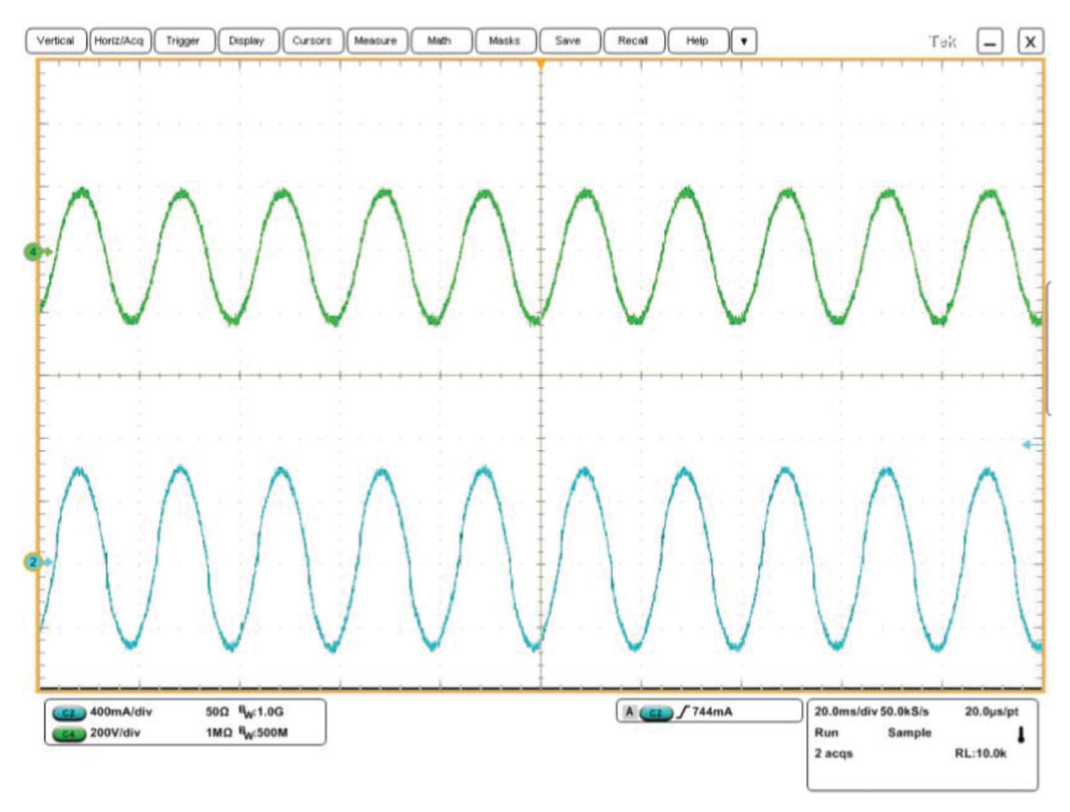


Figure 11. Ch: 4-input voltage; Ch: 2-input current waveforms at 190 V_{ac}

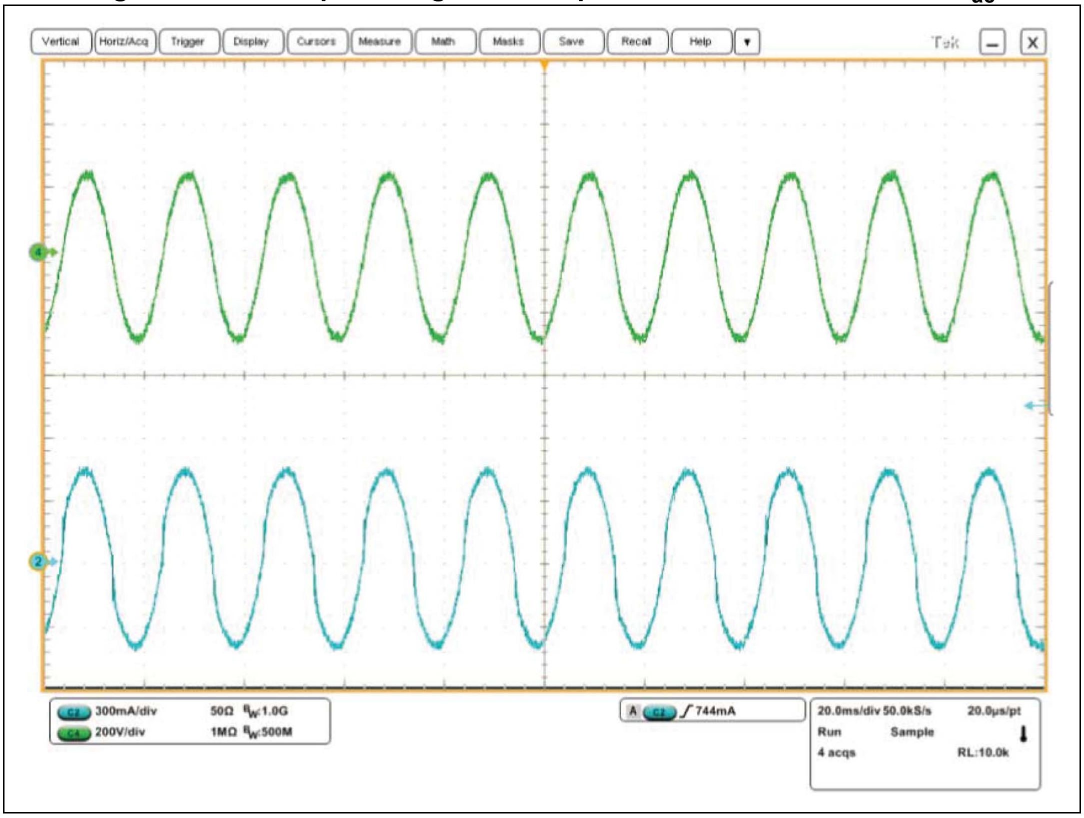


Figure 12. Ch: 4-input voltage; Ch: 2-input current waveforms at 220 V_{ac}

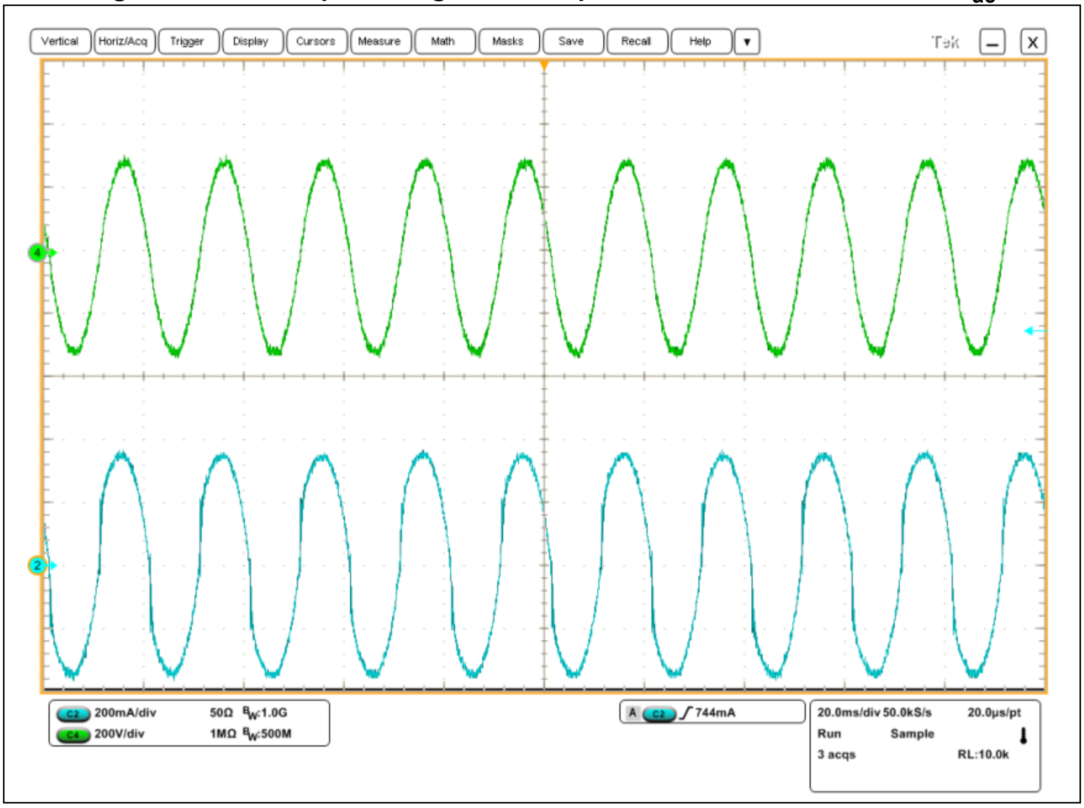
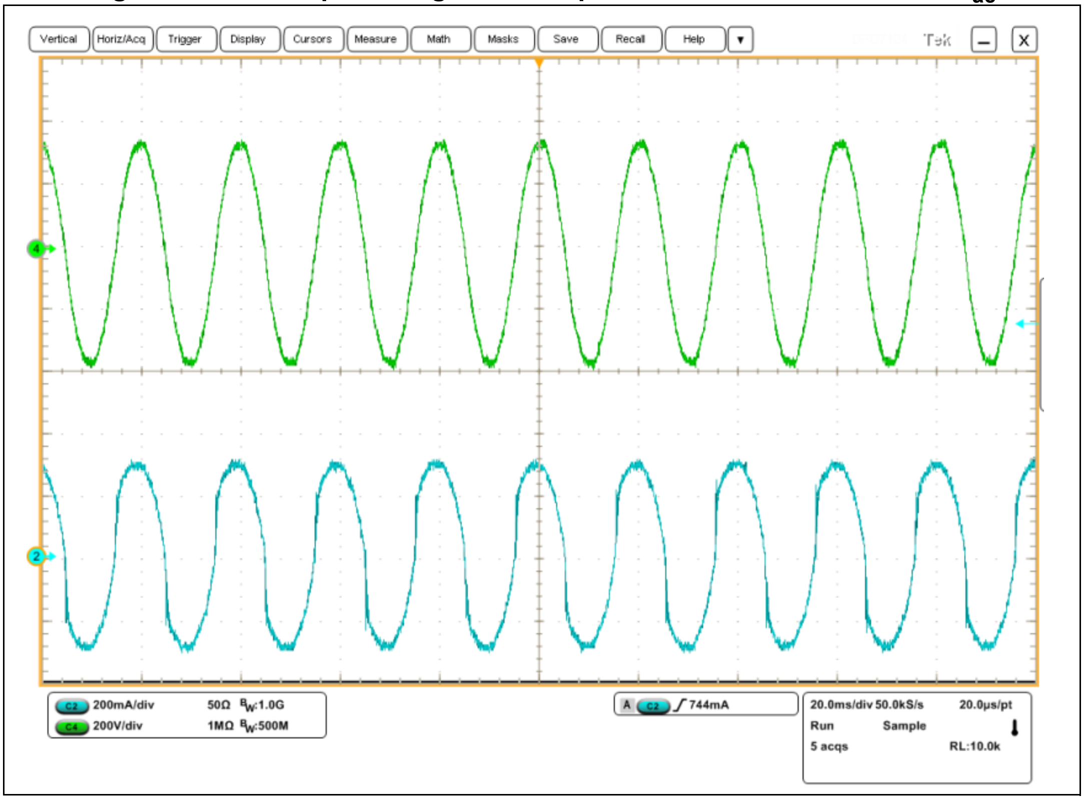


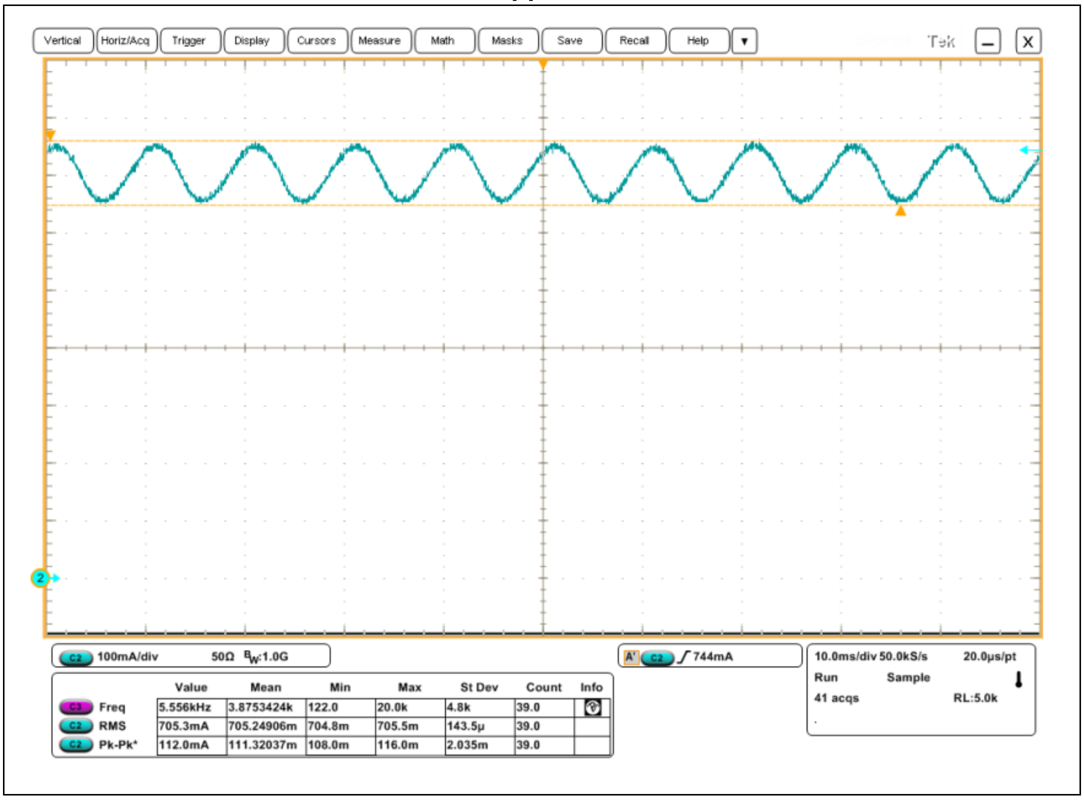
Figure 13. Ch: 4-input voltage; Ch: 2-input current waveforms at 265 V_{ac}



6.2 Output load current waveform

The full load current waveform is captured at 220 Vac. The current pattern shows 100 Hz line ripple reflected at output. The typical peak to peak ripple is 15% of rated load current.

Figure 14. Ch: 2-output load current waveform at 220 V_{ac} pk-pk current ripple = 112 mA



6.3 Steady state switching waveforms

The converter is powered at full load conditions and typical switching waveforms are captured as shown from *Figure 15* to *20*.

Figure 15. Ch: 4-drain-source voltage; Ch: 1-drain current; Ch: 2-COMP at 140 V_{ac}

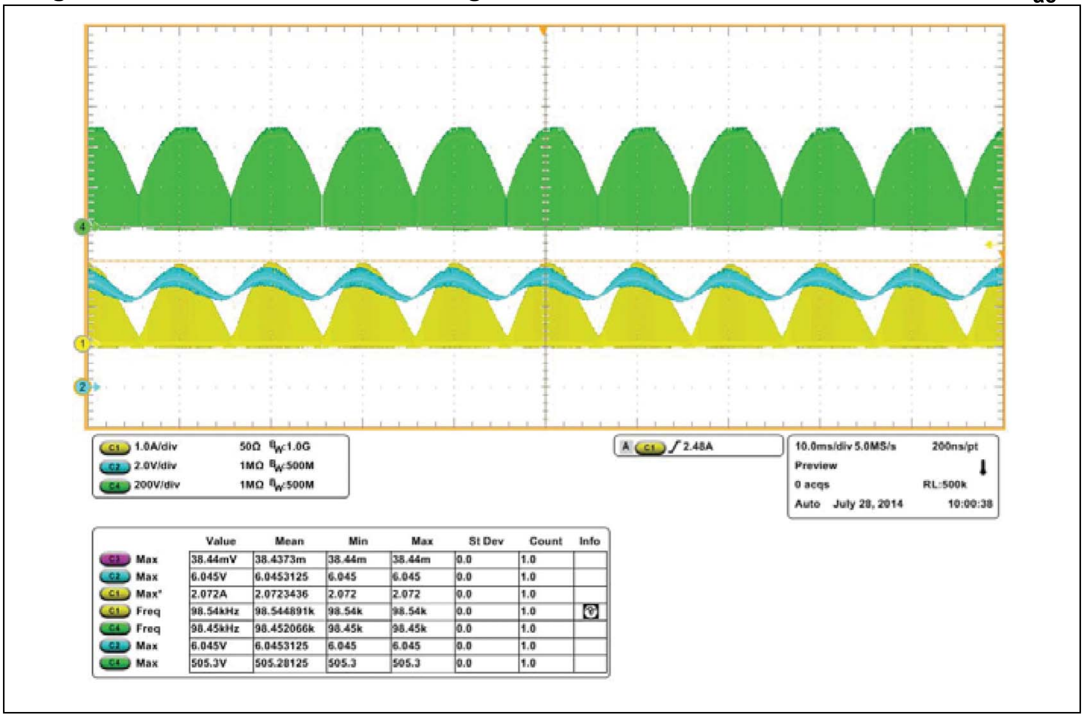


Figure 16. Ch: 4-drain-source voltage; Ch: 1-drain current; Ch: 2-COMP at 140 V_{ac} (zoom view)

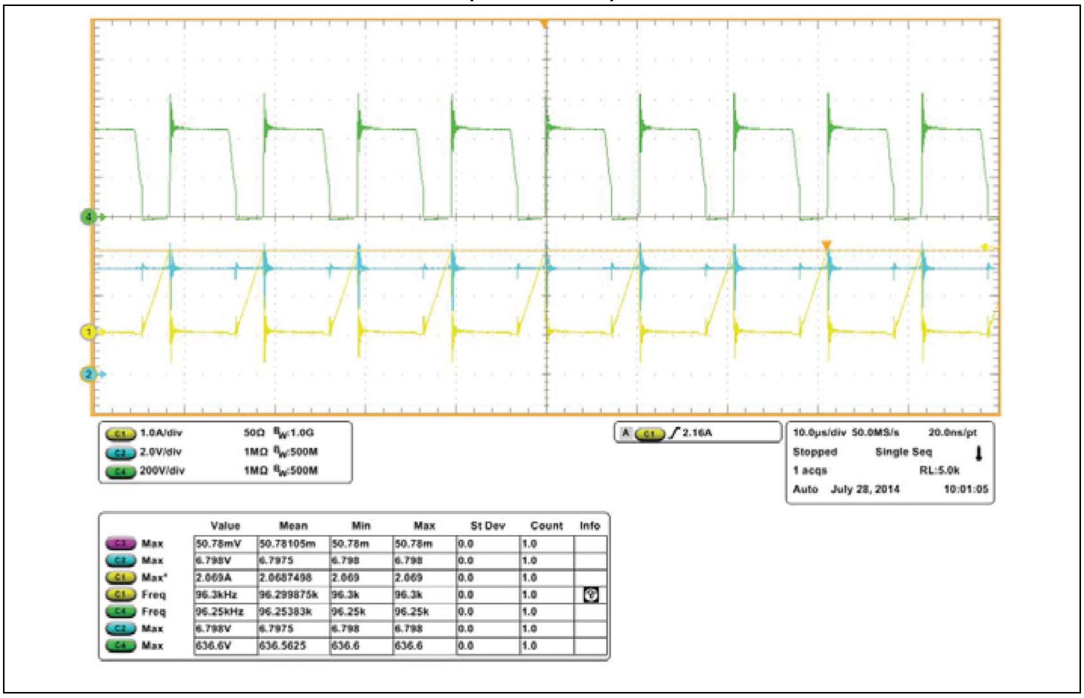


Figure 17. Ch: 4-drain-source voltage; Ch: 1-drain current; Ch: 2-COMP at 230 V_{ac}

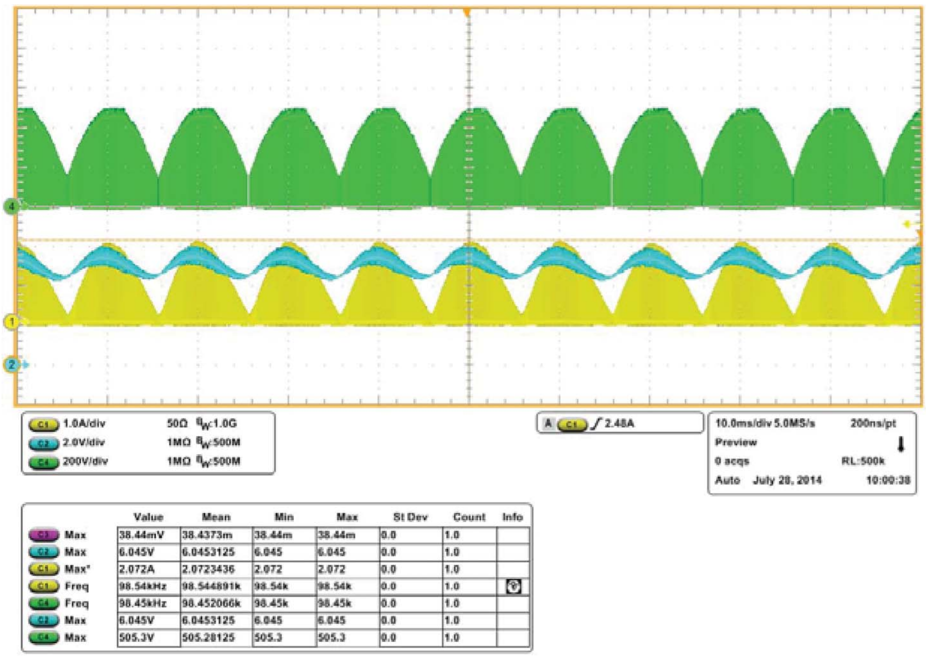


Figure 18. Ch: 4-drain-source voltage; Ch: 1-drain current; Ch: 2-COMP at 230 V_{ac} (zoom view)

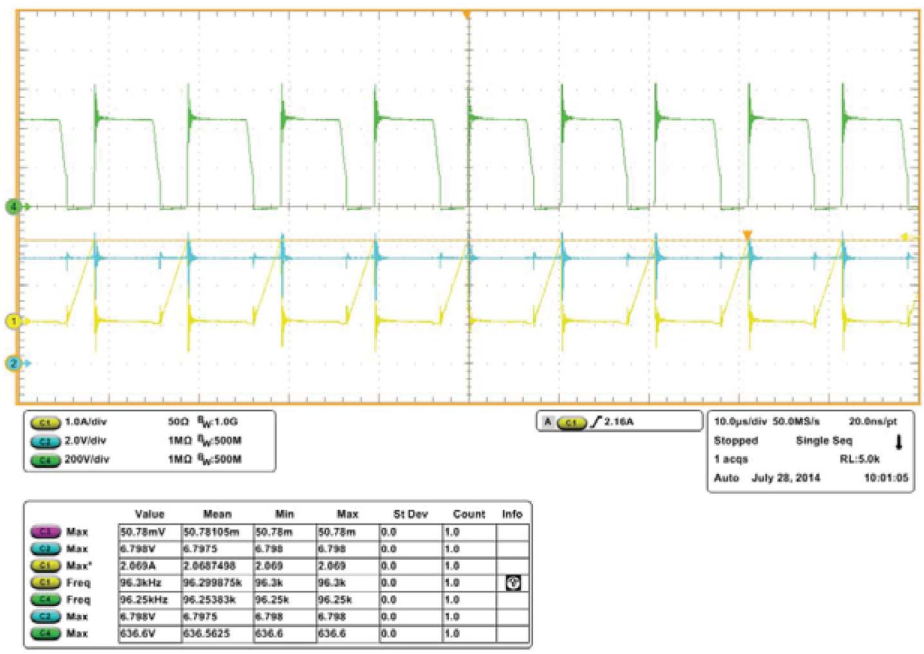


Figure 19. Ch: 4-drain-source voltage; Ch: 1-drain current; Ch: 2-COMP at 265 V_{ac}

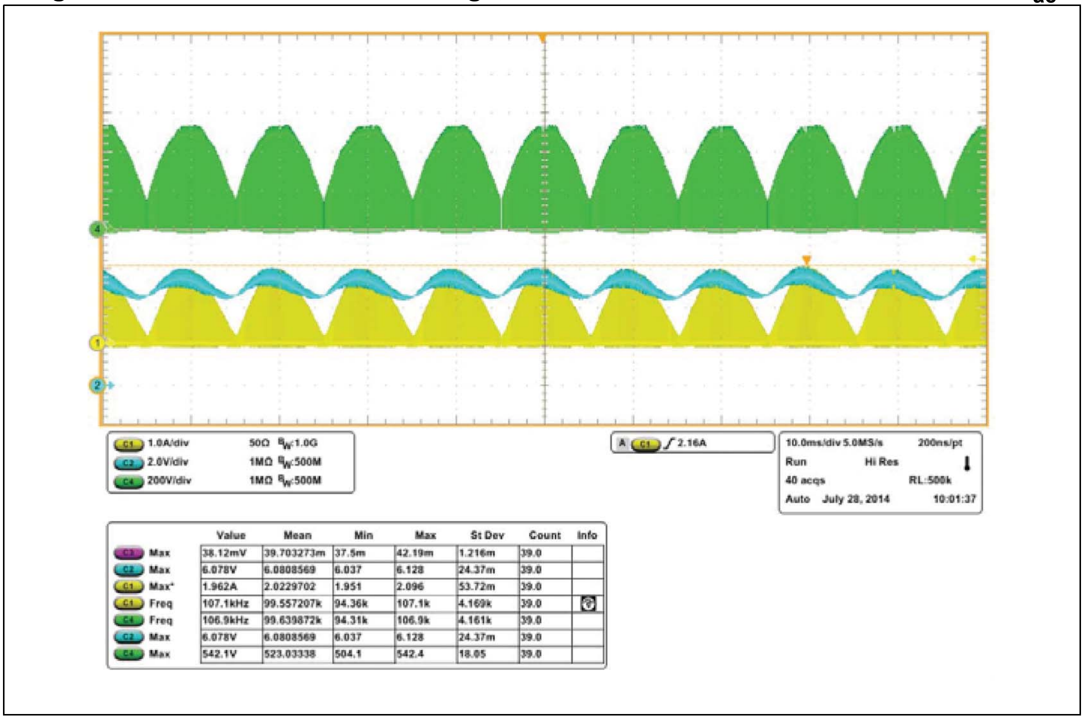
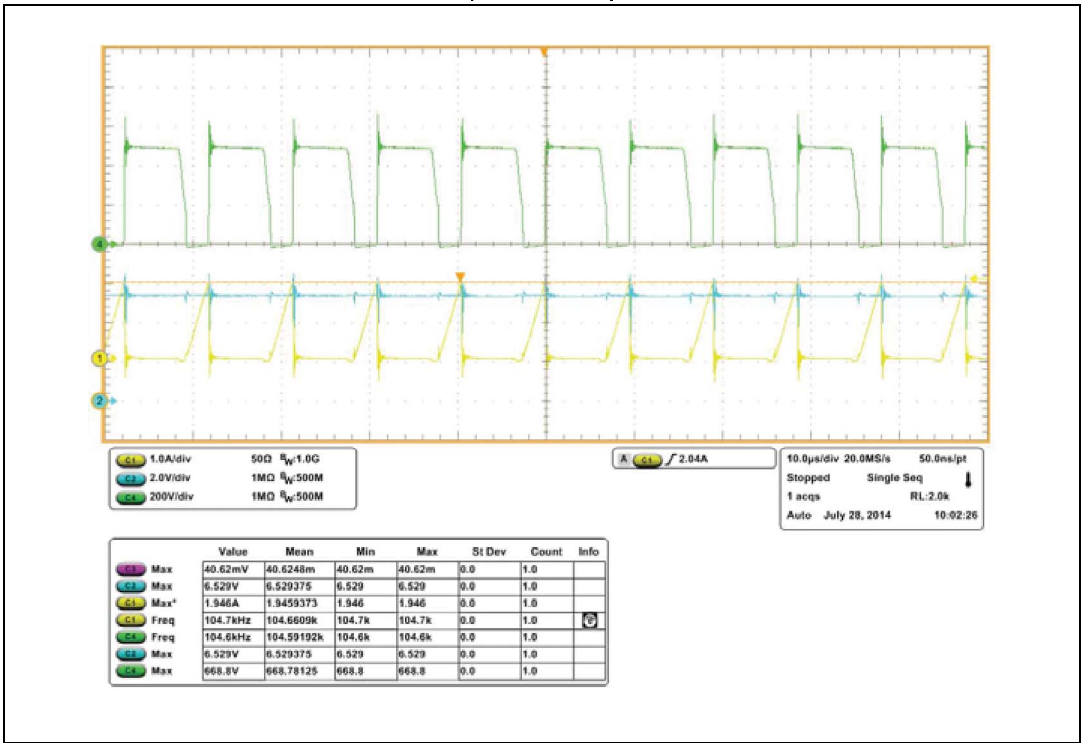


Figure 20. Ch: 4-drain-source voltage; Ch: 1-drain current; Ch: 2- COMP at 265 V_{ac} (zoom view)



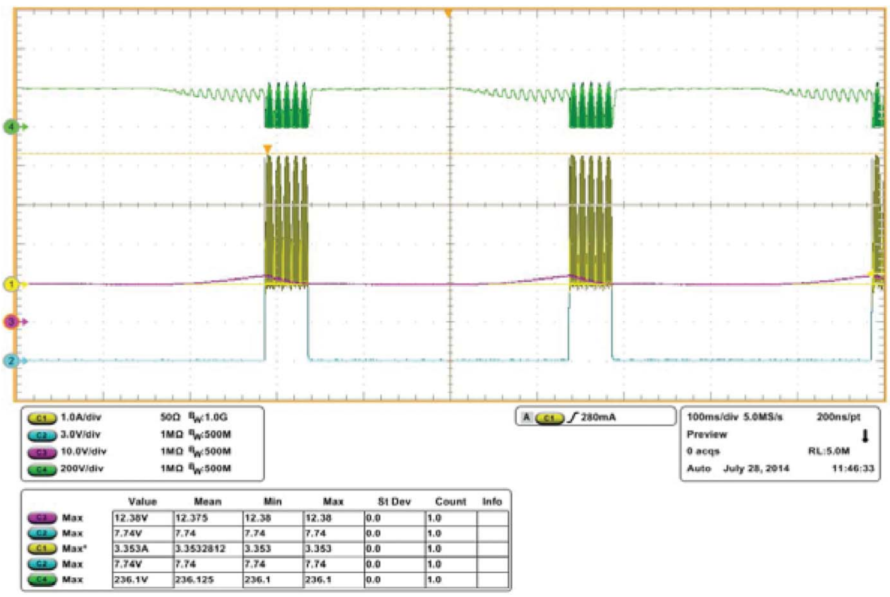
7 Short-circuit test

The short-circuit of output terminals of the converter is performed to analyze the safe operation of the converter in case of overload and short-circuit. The test is performed at 140 Vac, 230 Vac and 265 Vac in order to observe for any malfunction or failure.

In particular the waveforms of drain switching voltage, drain current and Vcc of the device is observed when attempting the short-circuit.

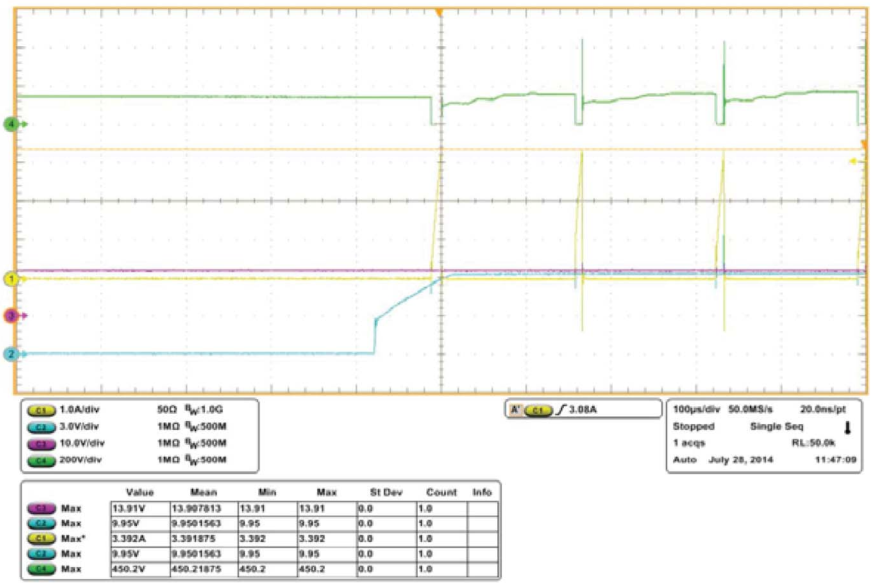
Looking into figures from 21 to 23, we can notice that there is no stress condition observed in power as well as control stage. The L6564 enters into protection mode with very low switching frequency of switching burst and MOSFET is well protected.

Figure 21. Output short-circuit at 140 V_{ac}



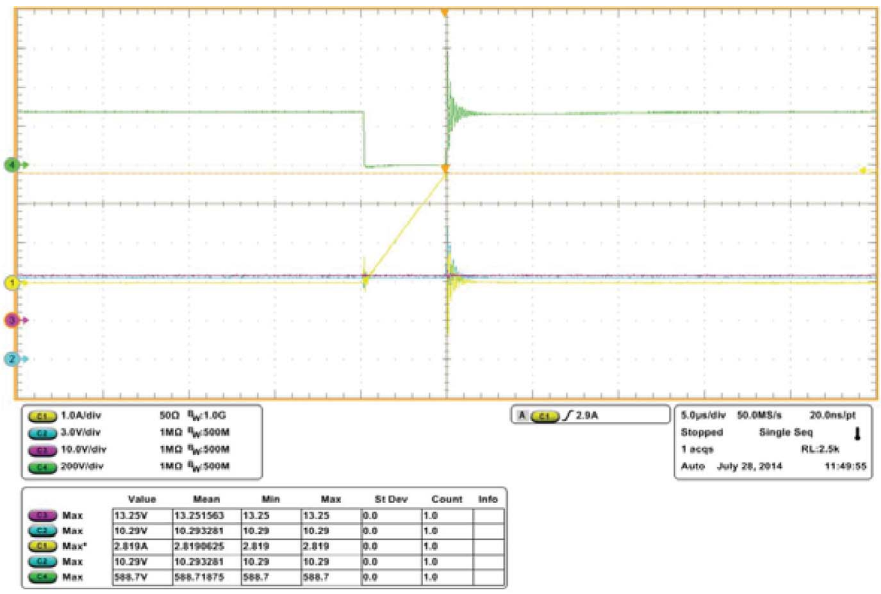
(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 22. Output short-circuit at 140 V_{ac} (zoom view 1)



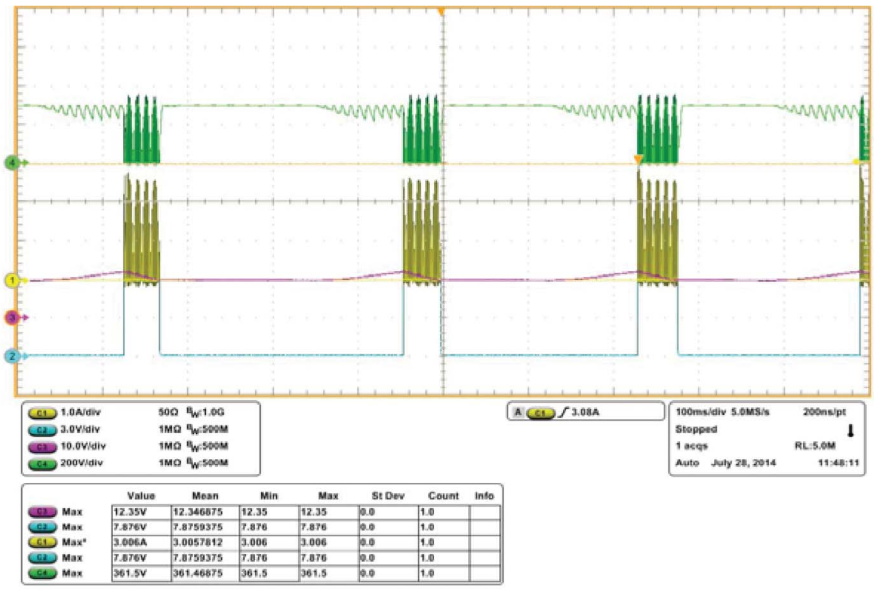
(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 23. Output short-circuit at 140 V_{ac} (zoom view 2)



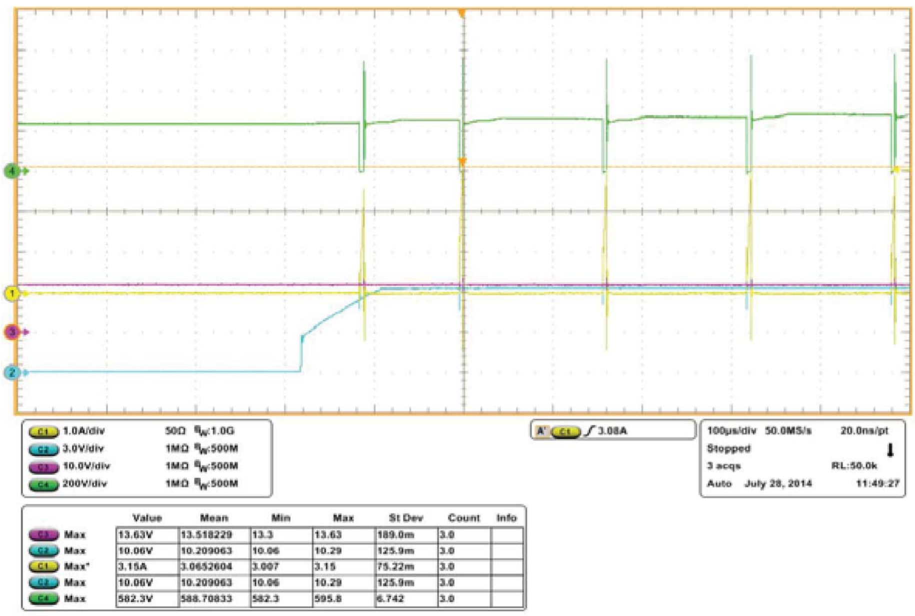
(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 24. Output short-circuit at 230 V_{ac}



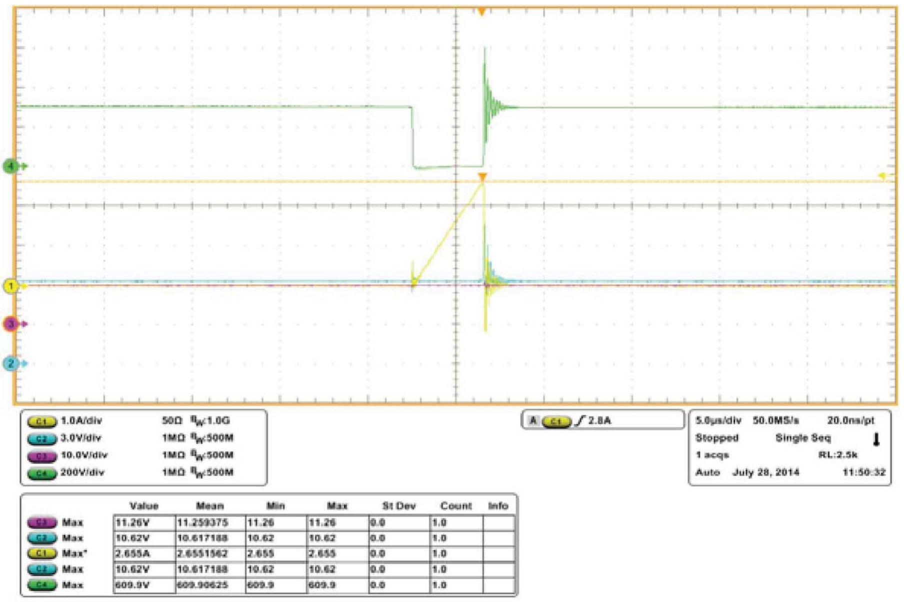
(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 25. Output short-circuit at 230 V_{ac} (zoom view 1)



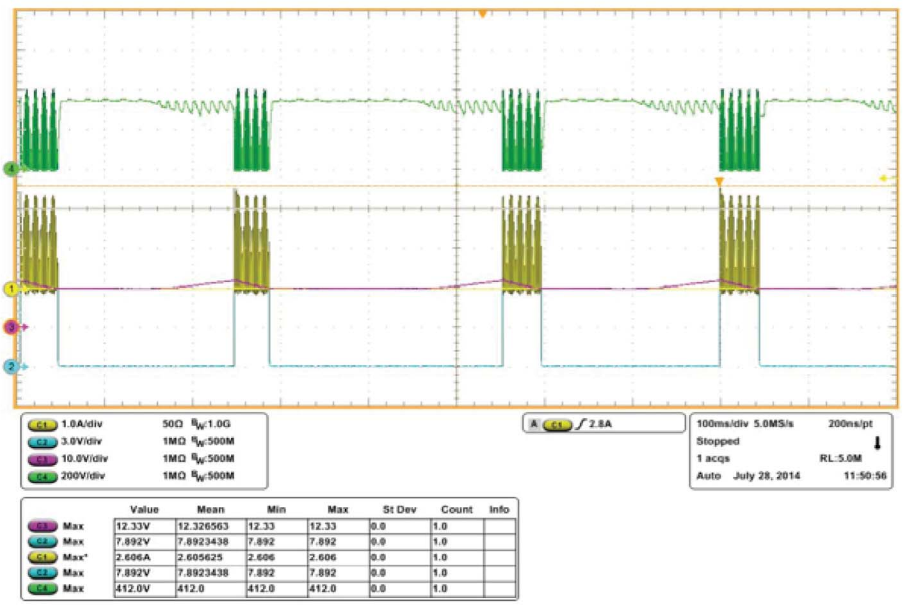
(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 26. Output short-circuit at 230 V_{ac} (zoom view 2)



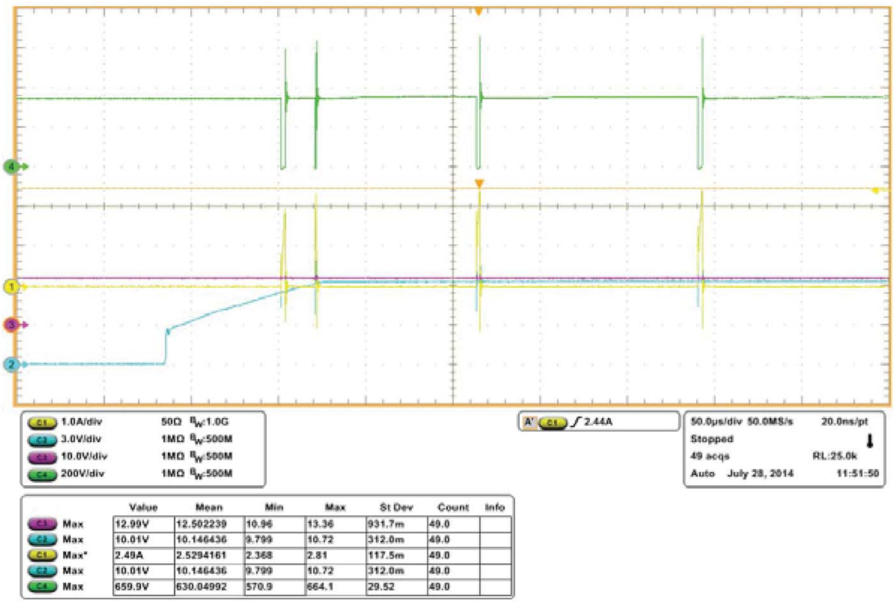
(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 27. Output short-circuit at 265 V_{ac}



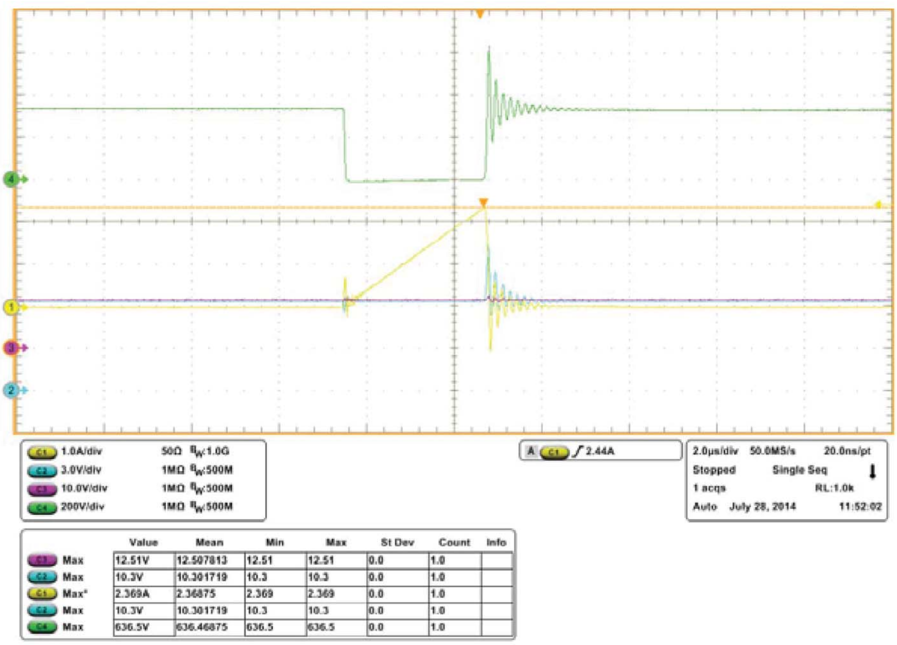
(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 28. Output short-circuit at 265 V_{ac} (zoom view 1)



(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

Figure 29. Output short-circuit at 265 V_{ac} (zoom view 2)

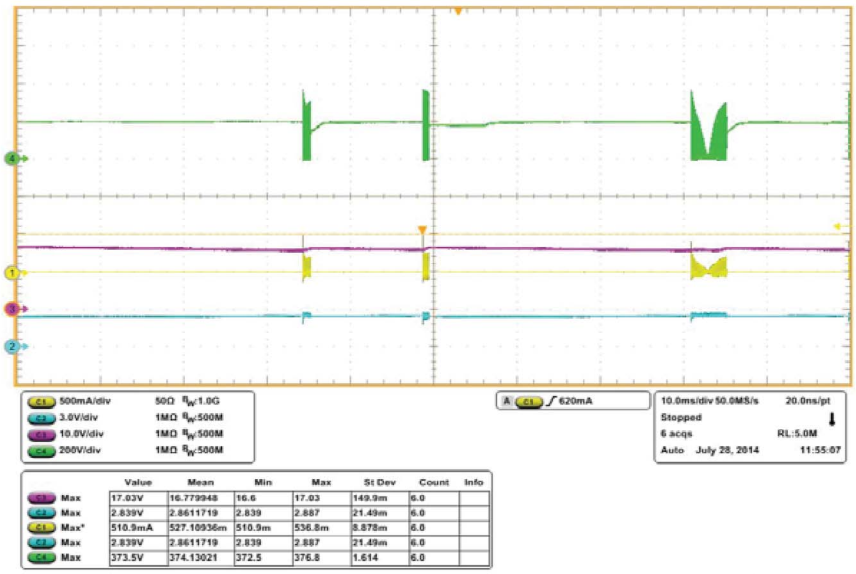


(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : COMP; Ch-3-Vcc)

8 No load

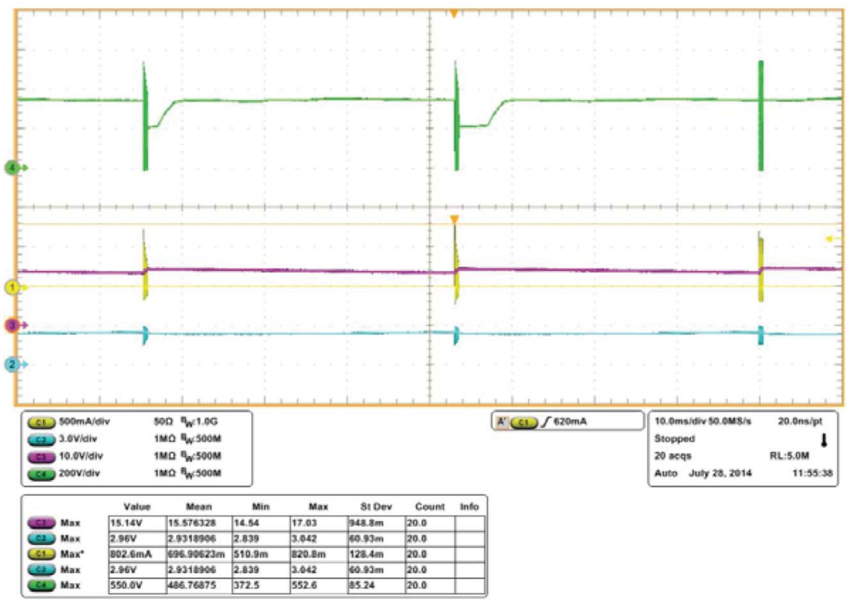
In *Figure 30* and *Figure 31*, some no load waveforms of the circuit are captured. When the control voltage on the COMP pin decreases below the Burst mode threshold of the L6564 (2.4 V typ.), IC gate driver output is inhibited and its consumption reduced.

Figure 30. No load waveforms at 140 V_{ac}



(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : Vcc; Ch-3-COMP)

Figure 31. No load waveforms at 265 V_{ac}



(Ch:4- Drain-source voltage ; Ch-1- Drain current ; Ch-2 : Vcc; Ch-3-COMP)

9 Harmonics measurements

At different mains voltage levels, the harmonic contents in mains current and its total harmonic distortion (THD) are noted to compare with the IEC61000-3-2 mainly for Class-C equipment.

Figure 32. Current THD at 150 V_{ac} mains

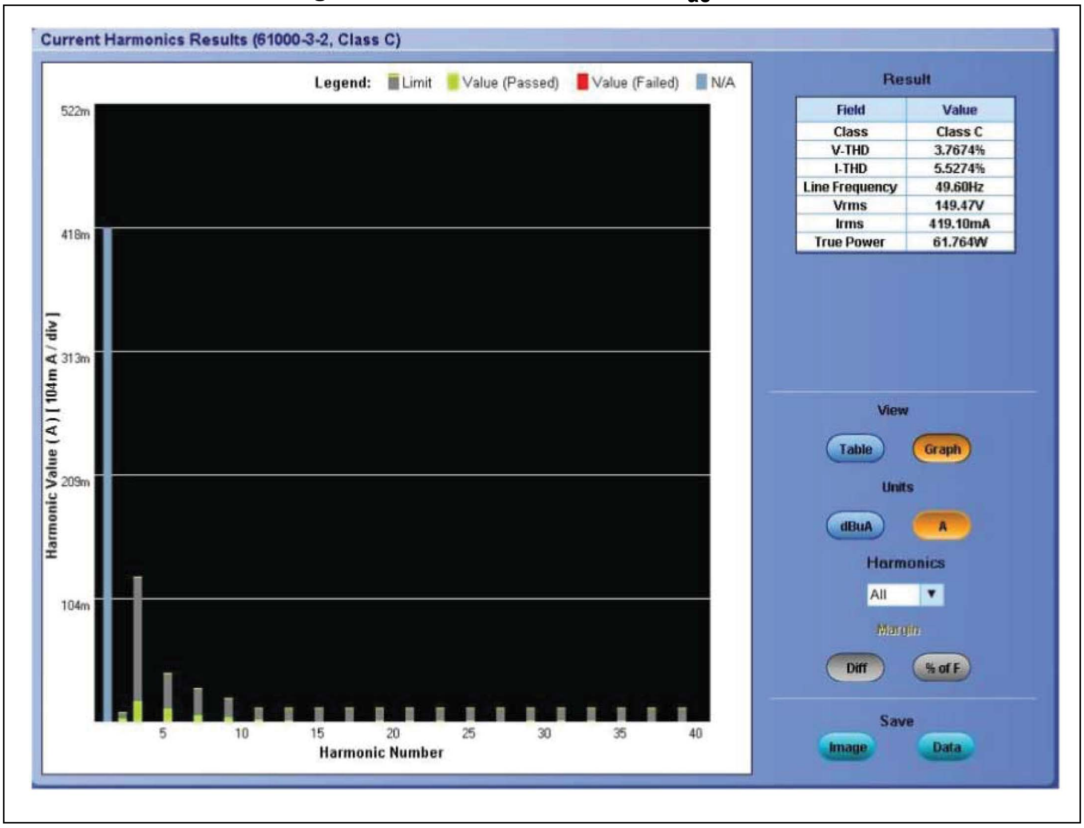


Figure 33. Current THD at 190 V_{ac} mains

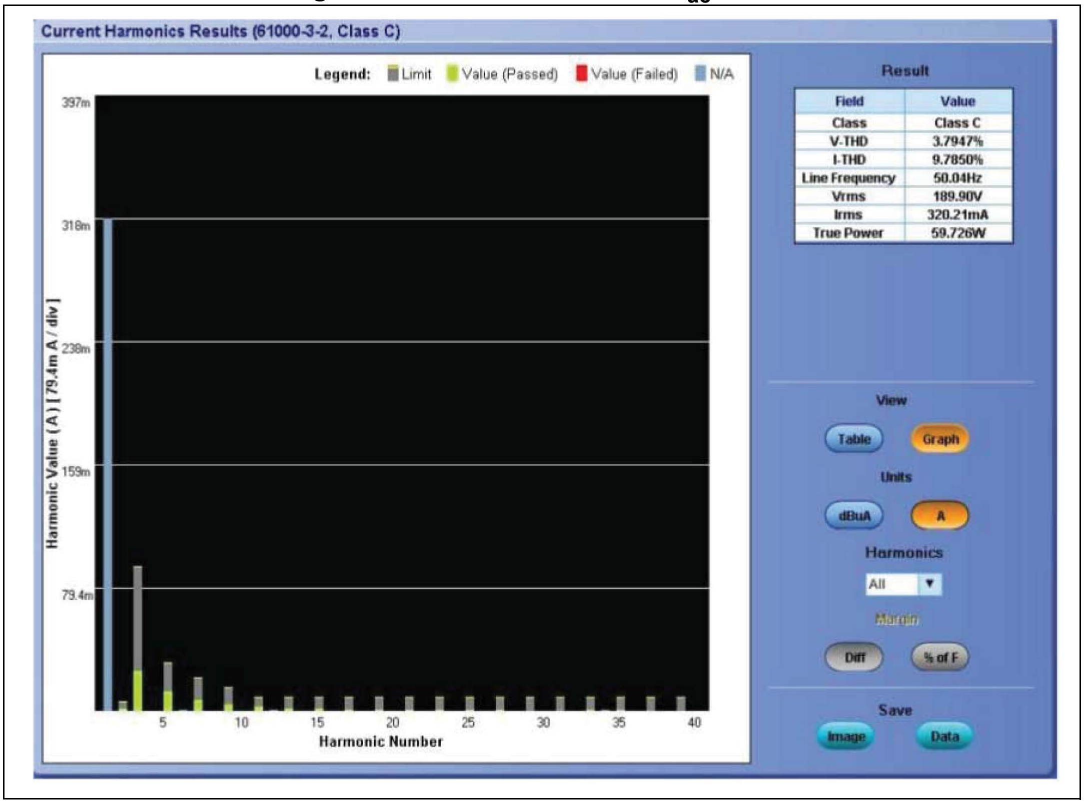


Figure 34. Current THD at 230 V_{ac} mains

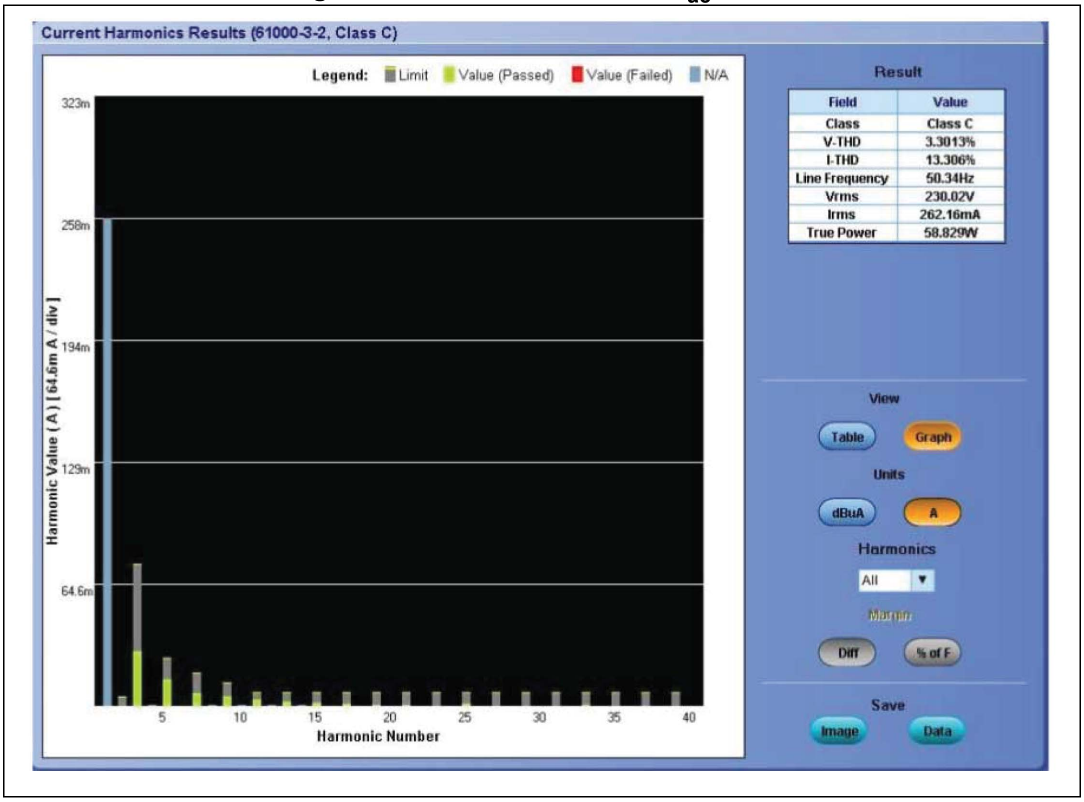
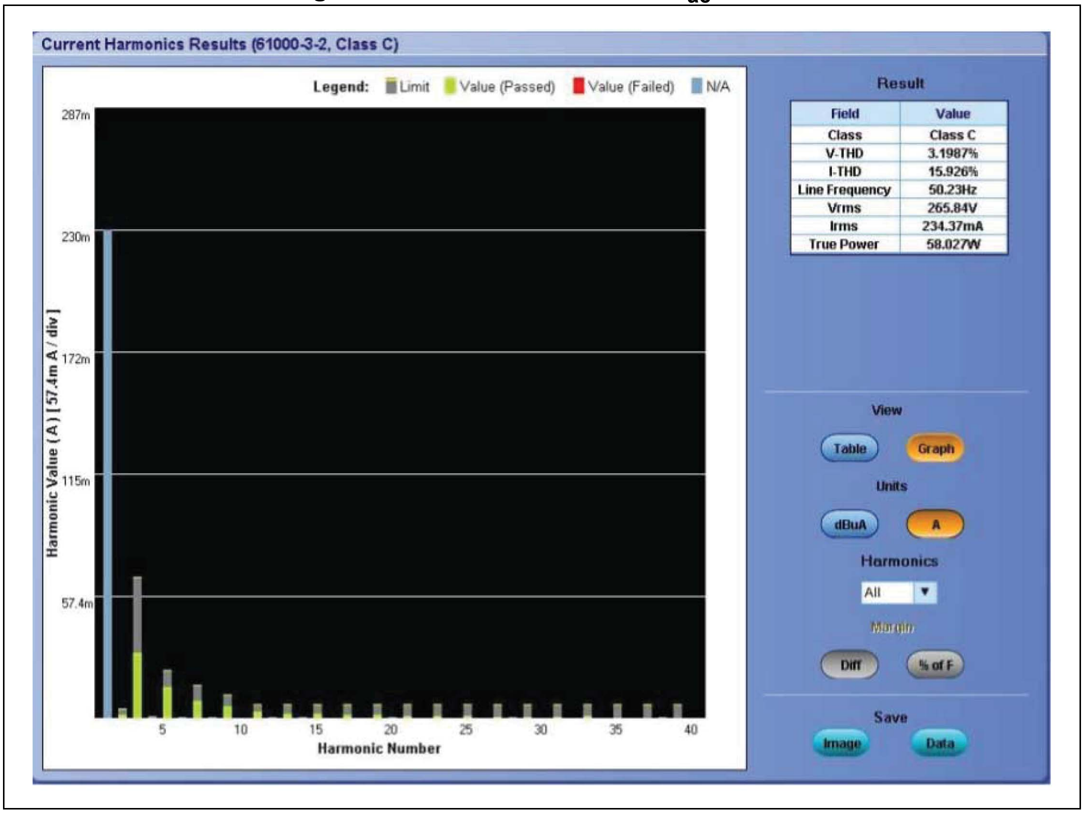
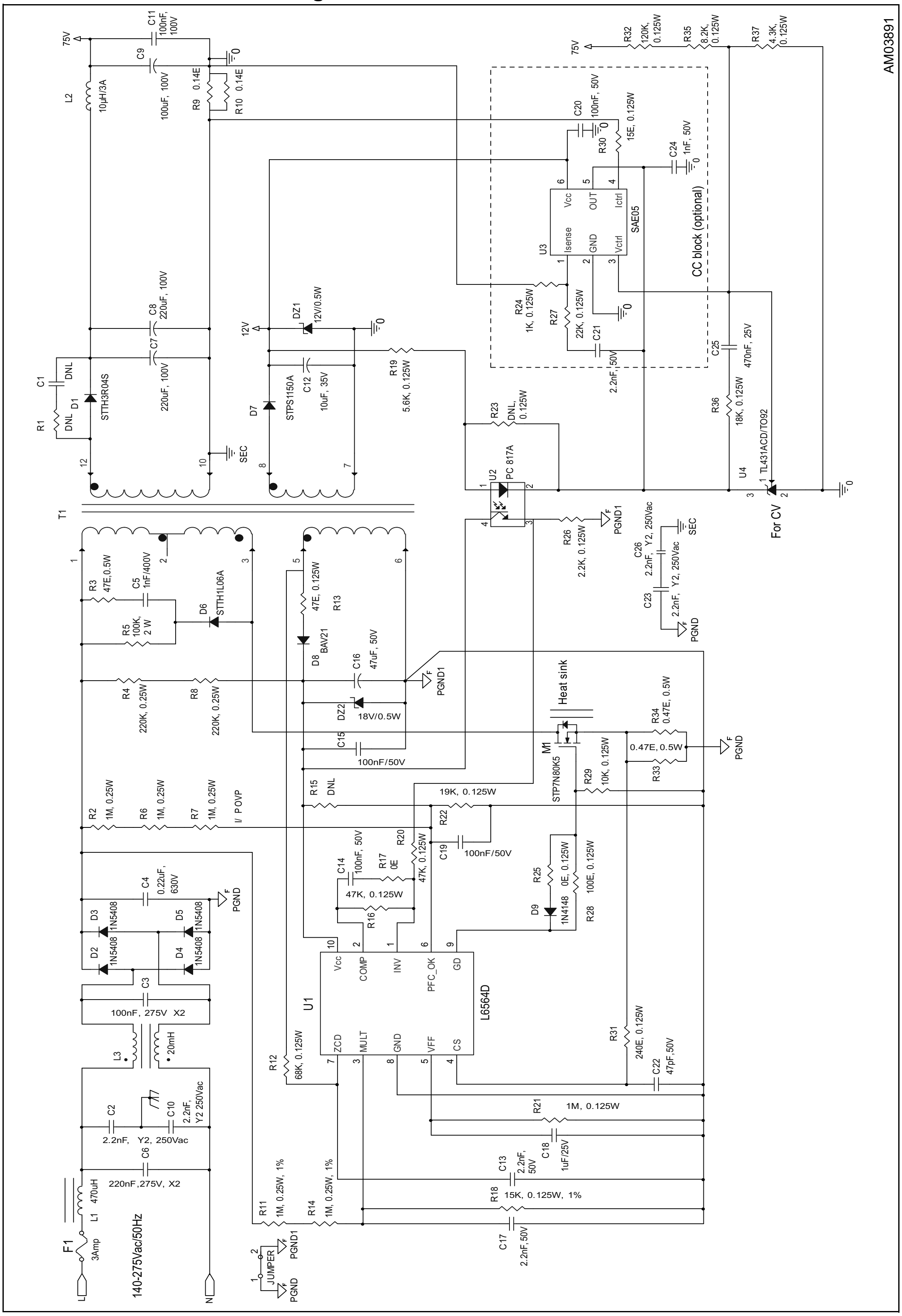


Figure 35. Current THD at 265 V_{ac} mains



10 Schematic of SMPS

Figure 36. Schematic of SMPS



11 Bill of material

Table 5. Bill of material

Sr. no.	Part reference	Part description	Qty.	Package	Manufacturer
1	R2, R8, R7, R11, R14	Resistor 1 MΩ	5	SMD 1206	
2	R4, R8	Resistor 220 KΩ	2	SMD 1206	
3	R3	Resistor CFR, 47 Ω/0.5 W	1	TH	
4	R5	Resistor 100 KΩ/2 W	1	TH, axial	
5	R13	Resistor 47 Ω	1	SMD 0805	
6	R21	Resistor 1 MΩ	1	SMD 0805	
7	R31	Resistor 240 Ω	1	SMD 0805	
8	R25, R17	Resistor 0 Ω	2	SMD 0805	
9	R28	Resistor 100 Ω	1	SMD 0805	
10	R22	Resistor 19 KΩ	1	SMD 0805	
11	R16	Resistor 47 KΩ	1	SMD 0805	
12	R29	Resistor 10 KΩ	1	SMD 0805	
13	R33, R34	Resistor 0.47 Ω	2	SMD 1206/TH	
14	R18	Resistor 15 KΩ, 1%	1	SMD 0805	
15	R12	Resistor 68 KΩ	1	SMD 0805	
16	R26	Resistor 2.2 KΩ	1	SMD 0805	
17	R19	Resistor 5.6 KΩ	1	SMD 0805	
18	R9, R10	Resistor 0.14 Ω, 1%	2	SMD 1206	
19	R24	Resistor 1 KΩ	1	SMD 0805	
20	R27	Resistor 22 KΩ	1	SMD 0805	
21	R30	Resistor 15 Ω	1	SMD 0805	
22	R36	Resistor 18 KΩ	1	SMD 0805	
23	R32	Resistor 120 KΩ, 1%	1	SMD 0805	
24	R35	Resistor 8.2 KΩ, 1%	1	SMD 0805	
25	R37	Resistor 4.3 KΩ, 1%	1	SMD 0805	
26	R1	Resistor, DNL	1	SMD 0805	
27	R15	Resistor, DNL	1	SMD 0805	
28	R23	Resistor, DNL	1	SMD 0805	
29	C6	Capacitor X2 type, 220 nF/275 Vac	1	TH	
30	C3	Capacitor X2 type, 100 nF/275 Vac	1	TH	

Table 5. Bill of material (continued)

Sr. no.	Part reference	Part description	Qty.	Package	Manufacturer
31	C2,C10, C23, C26	Capacitor Y2 type, 2.2 nF/250 Vac	4	TH	
32	C4	Capacitor polyester type 220 nF/630 Vdc	1	TH	
33	C13, C17, C21	Capacitor ceramic 2.2nF/50V	3	SMD 0805	
34	C18	Capacitor ceramic 1 µF/25 V	1	SMD 0805	
35	C22	Capacitor ceramic 22 pF/50 V	1	SMD 0805	
36	C14,C19, C20, C15	Capacitor ceramic 100 nF/50 V	4	SMD 0805	
37	C5	Capacitor film type 1 nF/400 Vdc or 1 KV disc	1	TH	
38	C1	Capacitor film type - DNL	1	TH	
39	C11	Capacitor ceramic 100 nF/100 V	1	SMD 1206	
40	C24	Capacitor ceramic 1 nF/50 V	1	SMD 0805	
41	C25	Capacitor ceramic 470 nF/25 V	1	SMD 0805	
42	C16	Capacitor electrolytic 47 µF/50 V	1	TH	
43	C7, C8	Capacitor electrolytic 220 µF/100 V	2	TH	
44	C12	Capacitor electrolytic 10 µF/35 V	1	TH	
45	F1	Fuse 3 A glass	1	Axial	
46	L1	Line inductor 470 µH	1	TH, drum type - dia. = 6 mm	
47	L3	Common mode inductor 20 mH, EF20 type	1	TH, 8 pins horizontal	
48	L2	DC filter inductor, 10 µH/3 Amp	1	TH, drum type - dia. = 6 mm	
49	T1	Transformer ER28/17/11	1	TH, 12 pins horizontal	
50	D2, D3, D4, D5	Diode 1N5408	4	CASE 267-05, axial lead	ON Semiconductor
51	D9	Diode 1N4148	1	SOD27; DO-35	NXP Semiconductors
52	D8	Diode BAV21	1	SOD27; DO-35	NXP Semiconductors
53	D6	Diode STTH1L06A	1	SMD - SMA package	STMicroelectronics
54	DZ2	Zener diode 18 V/0.5 W	1	TH	
55	DZ2	Zener diode 12 V/0.5 W	1	TH	
56	D1	Fast rectifier STTH3R04S	1	SMD - SMC package	STMicroelectronics

Table 5. Bill of material (continued)

Sr. no.	Part reference	Part description	Qty.	Package	Manufacturer
57	D7	Fast rectifier STPS1150	1	SMD - SMA package	STMicroelectronics
58	U1	PFC controller, L6564D	1	SMD - SSO-10 package	STMicroelectronics
59	U2	Optocoupler PC817A	1	SMD - SO-4	
60	U3	SEA05	1	SMD- SOT23-6L	STMicroelectronics
61	M1	MOSFET STP7N80K5	1	TO-220	STMicroelectronics

12 CVCC controller

The SEA05 is ST's advanced constant voltage, constant current driver designed for secondary side control for SMPS, battery charging and LED driving applications. One can implement the secondary side CVCC control using the SEA05 to achieve good stability in terms of temperature variations and better efficiency.

The SEA05 is a highly integrated solution for SMPS applications requiring a dual control loop to perform CV (constant voltage) and CC (constant current) regulation. The device integrates a voltage reference, two op-amps (with OR-ed open-drain outputs), and a low side current sensing circuit. The voltage reference, along with one op-amp, is the core of the voltage control loop; the current sensing circuit and the other op-amp make up the current control loop. The external components needed to complete the two control loops are: a resistor divider that senses the output of the power supply and fixes the voltage regulation set-point at the specified value; a sense resistor that feeds the current sensing circuit with a voltage proportional to the DC output current (this resistor determines the current regulation set-point and must be adequately rated in terms of power dissipation), and the frequency compensation components (R-C networks) for both loops. The device, housed in one of the smallest available packages, is ideal for space-limited applications such as adapters and chargers. Some of the features of this device are as follows:

- Constant voltage and constant current control
- Wide operating V_{CC} range: 3.5 - 36 V
- Low quiescent consumption: 200 µA
- Voltage reference: 2.5 V
- Voltage control loop accuracy: ± 0.5%
- Current sense threshold: 50 mV
- Open-drain output stage
- Low external component count
- SOT23-6L micro package

The pin diagram, typical application schematic and package are show in figures 37 and 38.

Figure 37. SEA05 internal circuit and its application in flyback topology

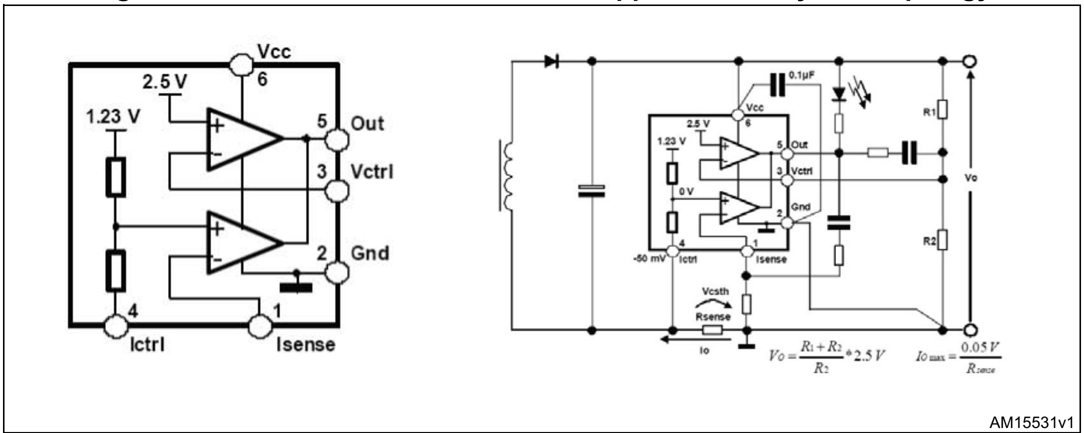
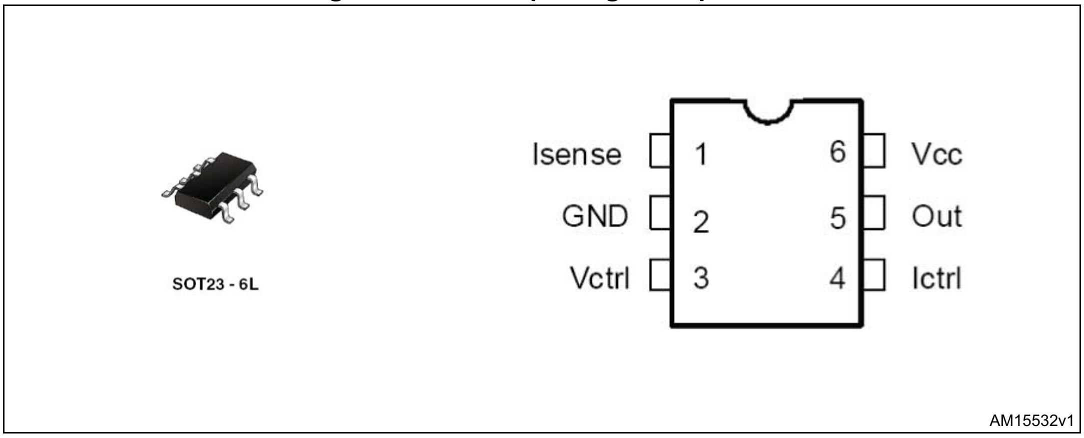


Figure 38. SEA05 package and pinout



13 References

- AN1059: Design equations of high-power-factor flyback converters based on the L6561
- AN2838: 35 W wide-range high power factor flyback converter evaluation board using the L6562A
- L6564 datasheet
- SEA05 datasheet

14 Revision history

Table 6. Document revision history

Date	Revision	Changes
02-Dec-2014	1	Initial release.
12-Jan-2015	2	Updated *Section 2: SMPS description on page 6* (updated device and package name). Updated *Table 1: Basic specifications of SMPS on page 10* (updated parameters and limits, added note *1.*). Updated *Figure 36: Schematic of SMPS on page 30* (replaced by new figure). Updated *Table 5: Bill of material on page 31* (replaced by new table). Minor modifications throughout document.