# AN4259
# Application note

## STEVAL-ISA117V1 12 V / 4.2 W, 60 kHz flyback isolated with VIPer16LN

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## Introduction

This document describes a 12 V - 350 mA power supply set in isolated flyback topology with VIPER16, a new off-line high voltage converter by STMicroelectronics.

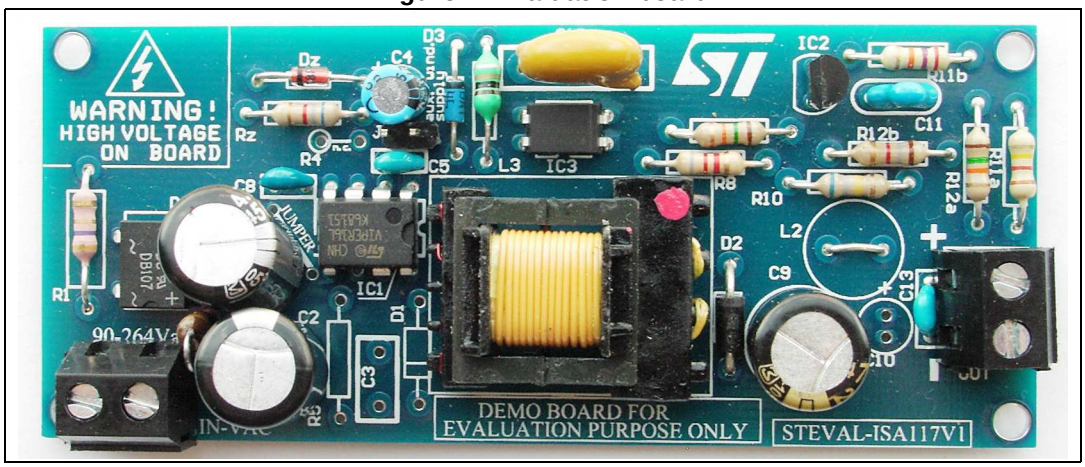
The features of the device are:

- 800 V avalanche rugged power section
- PWM operation at 60 kHz with frequency jittering for lower EMI
- current limiting with adjustable set point
- on-board soft-start
- safe auto-restart after a fault condition (overload, short-circuit)
- low standby power consumption

The VIPER16 does not require a biasing circuit to operate because the IC can be supplied by an internal current generator, therefore saving the cost of the transformers auxiliary winding. If the device is biased through an auxiliary winding, the evaluation board can reach very low standby consumption (< 30 mW at 230 $V_{AC}$, with output load disconnected).

Both cases are treated in the present document. The available protections are: thermal shutdown with hysteresis, delayed overload protection, open loop failure protection (the last one available only if VIPER16 is biased through the auxiliary winding).

**Figure 1. Evaluation board**



# Contents

# 1 Adapter features

The electrical specifications of the evaluation board are listed in *Table 1*.

**Table 1. Electrical specification**

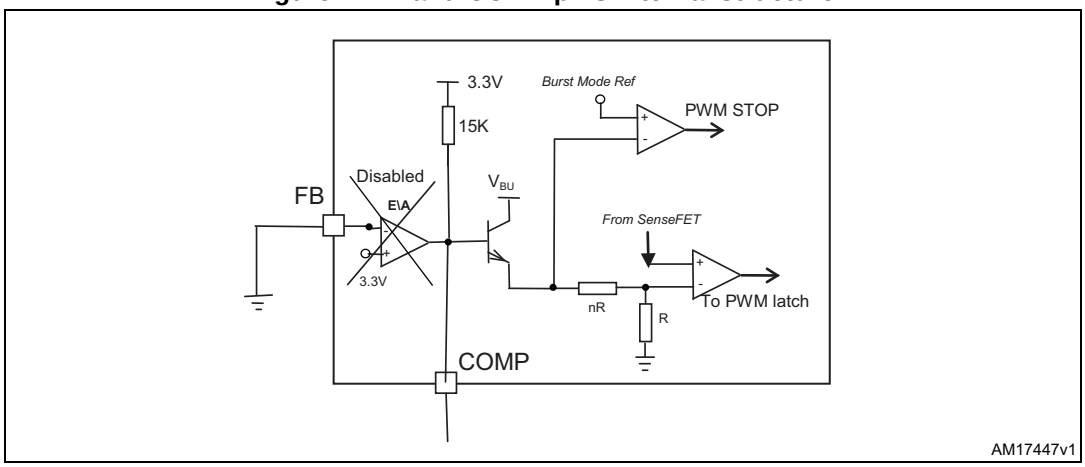
| Parameter | Symbol | Value |
|---|---|---|
| Input voltage range | $V_{IN}$ | [90 $V_{AC}$; 265 $V_{AC}$] |
| Output voltage | $V_{OUT}$ | 12 V |
| Max output current | $I_{OUT}$ | 0.35 A |
| Precision of output regulation | $\Delta V_{OUT\_LF}$ | ± 5% |
| High frequency output voltage ripple | $\Delta V_{OUT\_HF}$ | 50 mV |
| Max ambient operating temperature | $T_{AMB}$ | 60 °C |

# 2 Circuit description

The power supply is set in flyback topology. The schematic is given in *Figure 5* and the bill of materials in *Table 2*. The input section includes a resistor R1 for inrush current limiting, a diode bridge (D0) and a Pi filter for EMC suppression (C1, L1, C2). The transformers core is a standard E16. A transil clamp network (D1, D5) is used for leakage inductance demagnetization.

The output voltage value is set through the voltage reference IC2 and the voltage divider from the output, made up of R11 and R12, each of them split into two in order to allow a better tuning of the output voltage value. The FB pin of the VIPER16 is shorted to GND, which disables the internal error amplifier. In this case, a 15 kΩ internal resistor is connected between an internal 3.3 V generator and the COMP pin, as shown in *Figure 2*. The feedback signal is transferred to the primary side through an optocoupler, connected in parallel with the compensation network to COMP pin. The optocoupler modulates the voltage of the pin (and so the primary peak current) according to the current sunk, thus setting the right drain peak current value to keep the output voltage regulated.

**Figure 2. FB and COMP pins internal structure**




The LIM pin has been left open, thus the current limitation is set to the default value, $I_{DLIM}$. If a lower value is required, a resistor of the right value should be connected between LIM and GND pins, according to the $I_{DLIM}$ vs $R_{LIM}$ graphic reported in the datasheet. In this evaluation board, $R_{LIM}$ = R4.

A 100 nF capacitor has been placed very close to the output connector solder points, to limit the spike amplitude.

At power-up, as the rectified input voltage rises over the $V_{DRAINSTART}$ threshold, the high voltage current generator starts charging the $V_{DD}$ capacitor, C4, from 0 V up to $V_{DDON}$. At this point the power MOSFET starts switching, the HV current generator is turned off and the IC is biased by the energy stored in C4.

If the jumper J is not selected, the VIPER16 is self-biased, i.e. supplied by the input line voltage through the internal high-voltage startup current generator, which is turned on as the $V_{DD}$ voltage falls down to $V_{DDCSON}$ and is switched off as it reaches $V_{DDON}$ (see *Figure 3*). The use of self-biasing means higher power dissipation and must be avoided if low standby consumption is required.

If the jumper J is selected, the IC is biased by the auxiliary winding, through D3 and L3, (see *Figure 4*). The IC biasing through auxiliary winding is referred to as external biasing and allows the converter to reach very low input power consumption in no load condition.

The auxiliary winding voltage, and then the $V_{DD}$ voltage, increases with the output load. In order to avoid that the $V_{DD}$ operating range is exceeded, an external clamp (Dz and Rz) has been added between $V_{DD}$ and GND pins.

**Figure 3. $V_{DD}$ waveform (IC self-biased)**

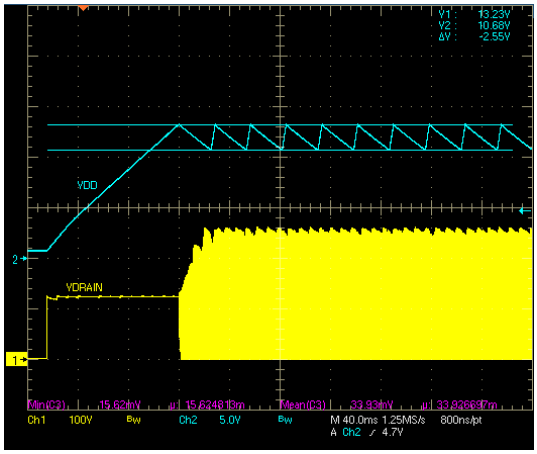



**Figure 4. $V_{DD}$ waveform (IC externally biased)**

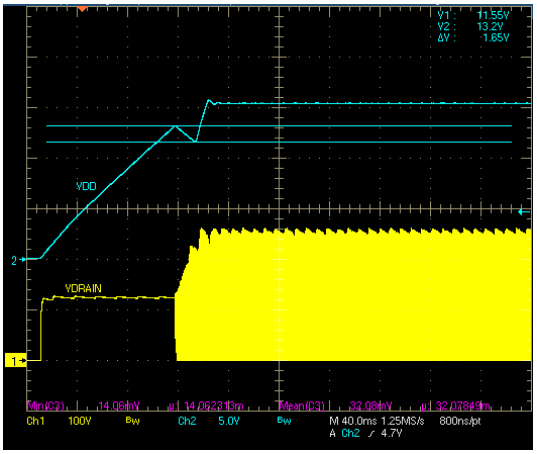


**Figure 5. Application schematic**

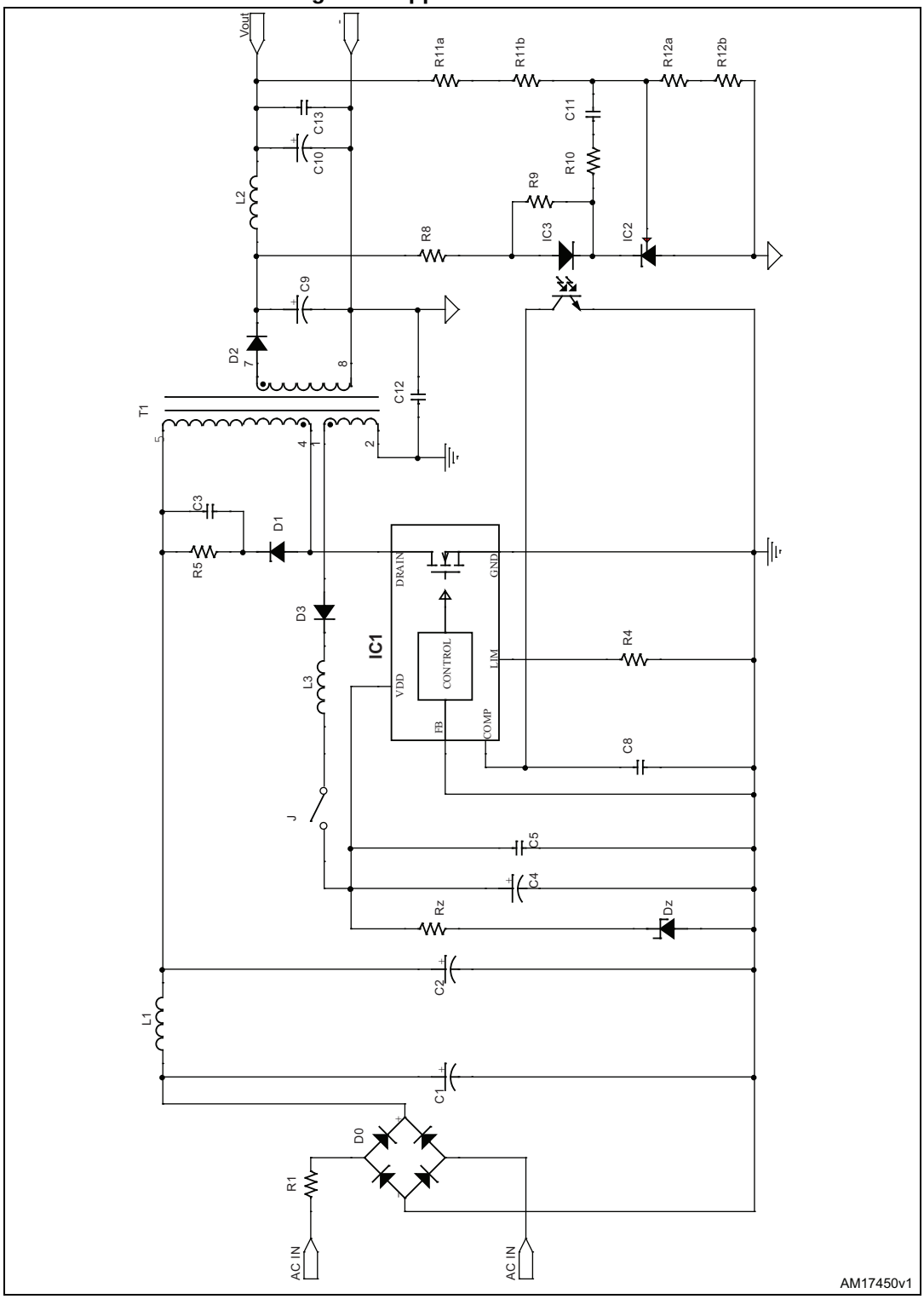


**Table 2. Bill of material**

| Ref. | Part | Description | Manufacturer |
|---|---|---|---|
| D0 | DF06M | Diode bridge | Vishay |
| C1, C2 | 4.7µF, 400 V | Electrolytic capacitor, NHG series | Panasonic |
| C3 | not mounted | | |
| C4 | 10 µF, 35 V | Electrolytic capacitor, G series | Panasonic |
| C5 | 100 nF, 50 V | Ceramic capacitor, SR series | AVX |
| C8 | 3.3 nF, 100 V | Ceramic capacitor | |
| C9 | 470 µF, 25 V | Ultra-low ESR electrol. cap., ZL series | Rubycon |
| C10 | not mounted | Electrolytic capacitor | |
| C11 | 33 nF, 50 V | Ceramic capacitor B3798X series | EPCOS |
| C12 | 2.2 nF | Y1 capacitor 440L series | Vishay |
| C13 | 100 nF, 50 V | Ceramic capacitor, SR series | AVX |
| D1 | not mounted | Clamp diode | |
| D2 | STPS2H100 | Output diode 2 A, 100 V | ST |
| D3 | BAT46 | Small signal diode | ST |
| Dz | 18 V | Zener diode | |
| Rz | 6.8 kΩ | 1/4 W resistor | |
| R1 | 4.7 Ω | 1 W resistor | Tyco electronics |
| R4 | not mounted | 1/4 W resistor | |
| R5 | not mounted | 1/2 W resistor | |
| R8 | 8.2 kΩ | 1/4 W resistor | |
| R9 | 15 kΩ | 1/4 W resistor | |
| R10 | 680 kΩ | 1/4 W resistor | |
| R11a | 120 kΩ | 1/4 W resistor | |
| R11b | 27 kΩ | 1/4 W resistor | |
| R12a | 15 kΩ | 1/4 W resistor | |
| R12b | 1.8 kΩ | 1/4 W resistor | |
| IC1 | Viper16L | PMW controller | ST |
| IC2 | TS431 | Voltage reference | ST |
| IC3 | PC817 | Optocoupler | |
| L1 | 1 mH | Filter inductor BC type | EPCOS |
| L2 | short circuit | | |
| L3 | 1 µH | Small signal inductor | |
| T1 | 1335.0062 | Flyback transformer | Magnetica |
| | 7508110342 Rev. 6A | | Wurth |
| J | Jumper | | |

# 3 Transformer

The transformer characteristics are listed in the table below.

**Table 3. Transformer characteristics**

| Parameter | Value | Test conditions |
|---|---|---|
| Manufacturer | Magnetica | |
| Part number | 1335.0062 | |
| Primary inductance | 1.2 mH ±15 | Measured at 1 kHz 0.1V |
| Leakage inductance | 2.9% | Measured at 10 kHz 0.1V |
| Primary to secondary turn radio (4 - 5)/(7 - 8) | 7.85 ±0.5 | Measured at 10 kHz 0.1V |
| Primary to auxiliary turn radio (4 - 5)/(1 - 2) | 7.33 ±0.5 | Measured at 10 kHz 0.1V |

The following figures show size and pins distances ([mm]) of the transformer.

**Figure 6. Transformer pins distances**

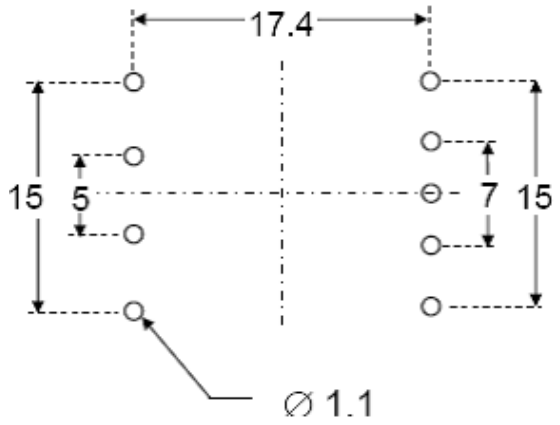



**Figure 7. Transformer electrical diagram**

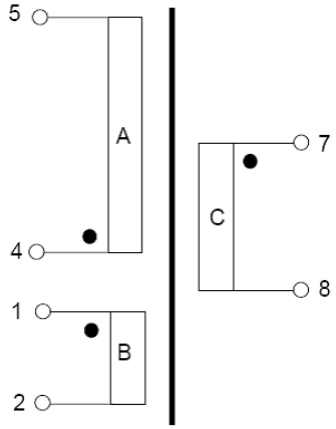



**Figure 8. Transformer side view**

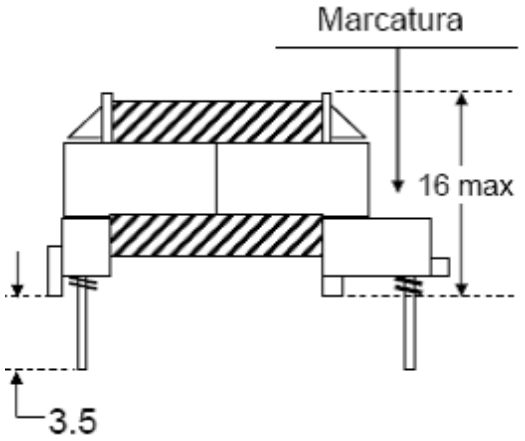
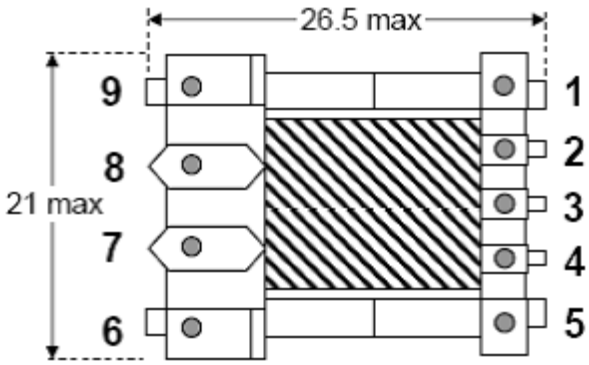



**Figure 9. Transformer terminal view**



# 4 Testing the board

## 4.1 Typical waveforms

Drain voltage and current waveforms in full load condition are reported for the two nominal input voltages in *Figure 10* and *Figure 11*, and for minimum and maximum input voltage in *Figure 12* and *Figure 13* respectively.

**Figure 10. Drain current and voltage at 115 $V_{AC}$, max load**

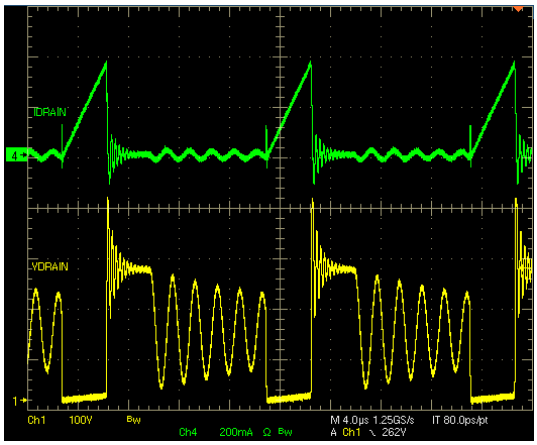



**Figure 11. Drain current and voltage at 230 $V_{AC}$, max load**

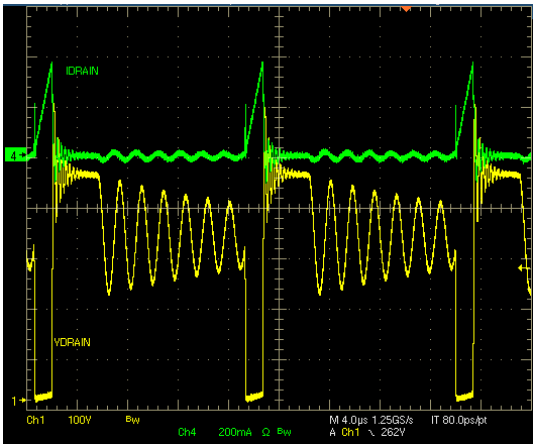



**Figure 12. Drain current and voltage at 90 $V_{AC}$, max load**

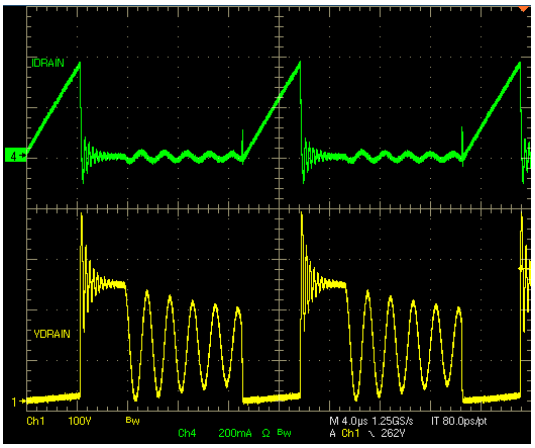
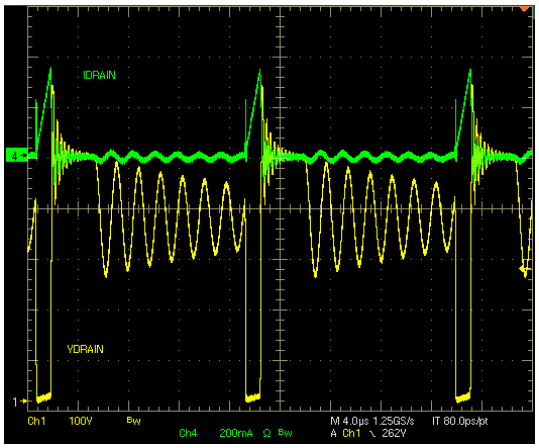



**Figure 13. Drain current and voltage at 265 $V_{AC}$, max load**




## 4.2 Precision of the regulation

The output voltage of the board has been measured in different line and load condition with the results shown in *Output voltage line-load regulation Table 4*. The output voltage practically is not affected by the line condition and by the IC biasing (self or external biasing).

**Table 4. Output voltage line-load regulation**

| $V_{IN}$ ($V_{AC}$) | $V_{OUT}$ (V) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | No load | | 50% Load | | 75% Load | | 100% Load | |
| | Self biasing | External biasing | Self biasing | External biasing | Self biasing | External biasing | Self biasing | External biasing |
| 90 | 12.12 | 12.12 | 12.06 | 12.06 | 12.05 | 12.05 | 12.05 | 12.04 |
| 115 | 12.12 | 12.12 | 12.08 | 12.06 | 12.05 | 12.04 | 12.05 | 12.04 |
| 150 | 12.12 | 12.12 | 12.08 | 12.06 | 12.06 | 12.04 | 12.04 | 12.04 |
| 180 | 12.12 | 12.12 | 12.06 | 12.05 | 12.05 | 12.04 | 12.04 | 12.04 |
| 230 | 12.12 | 12.12 | 12.06 | 12.05 | 12.05 | 12.04 | 12.04 | 12.03 |
| 265 | 12.12 | 12.12 | 12.06 | 12.05 | 12.05 | 12.04 | 12.04 | 12.03 |

**Figure 14. Line regulation**

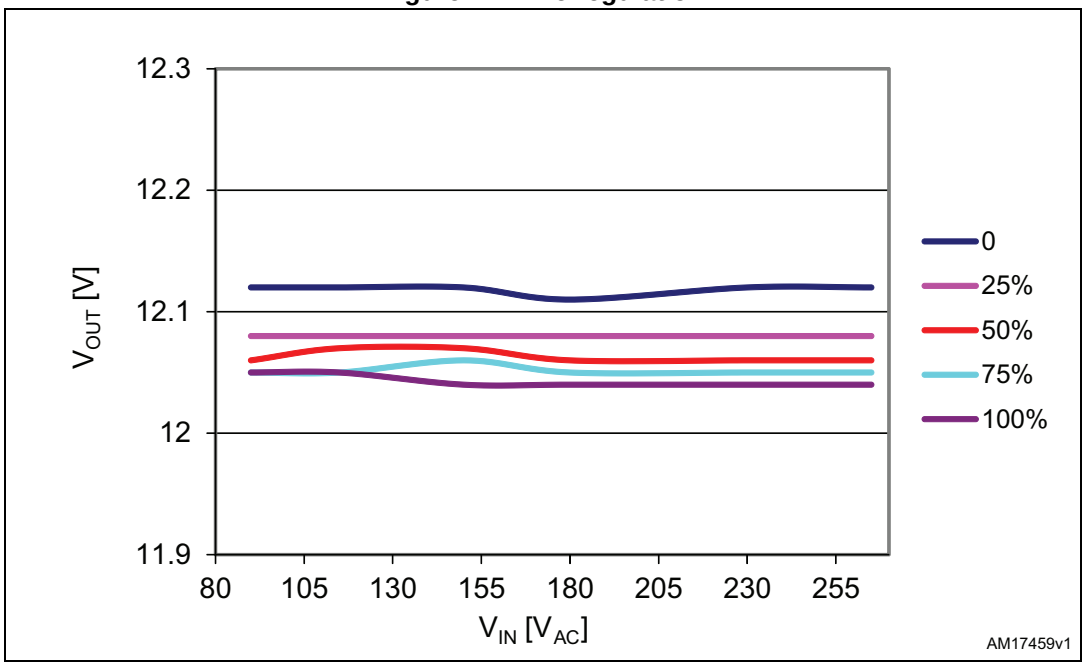


Figure 15. Load regulation

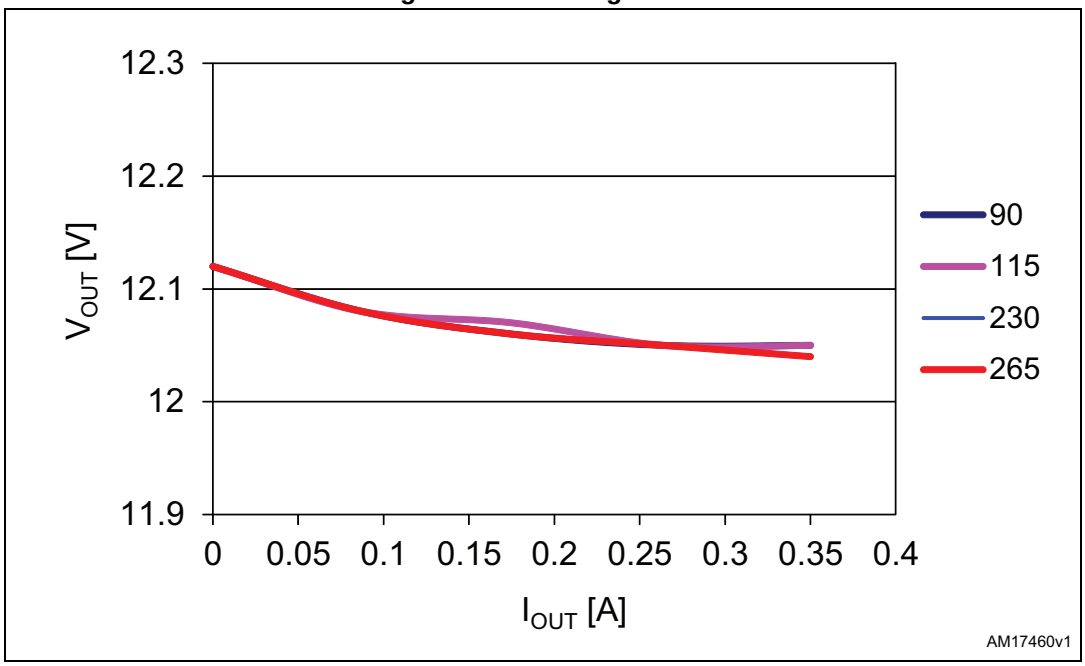



Figure 16. Output voltage ripple at 115 $V_{AC}$ full load

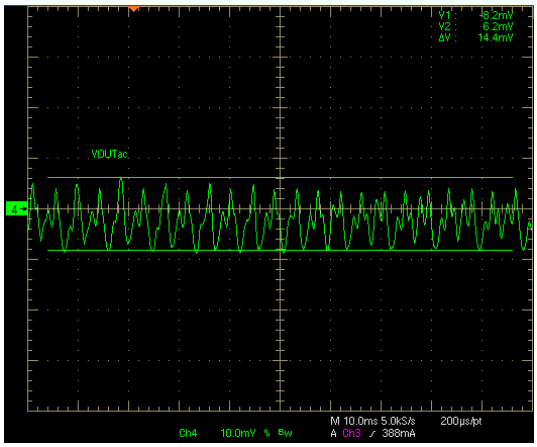
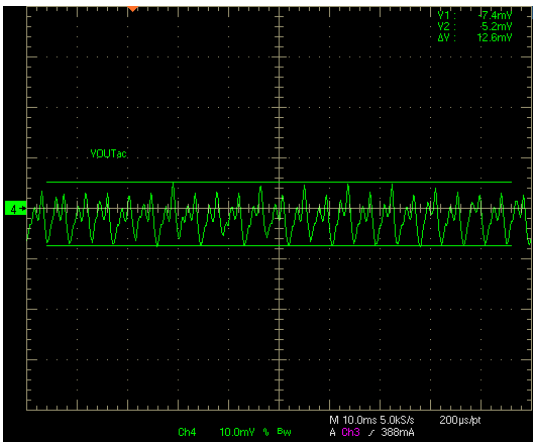



Figure 17. Output voltage ripple at 230 $V_{AC}$, full load



## 4.3 Burst mode and output voltage ripple

When the converter is lightly loaded, the COMP pin voltage decreases. As it reaches the shutdown threshold, $V_{COMPL}$ (1.1 V, typical), the switching is disabled and no more energy is transferred to the secondary side. So, the output voltage decreases and the regulation loop makes the COMP pin voltage increase again. As it rises 40 mV above the $V_{COMPL}$ threshold, the normal switching operation is resumed. This results in a controlled on/off operation which is referred to as “burst mode”. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected, making it easier to comply with energy saving regulations. The figures below show the output voltage ripple when the converter is no/lightly loaded and supplied with 115 $V_{AC}$ and 230 $V_{AC}$ respectively.

**Figure 18. Output voltage ripple at 115 $V_{AC}$, no load**

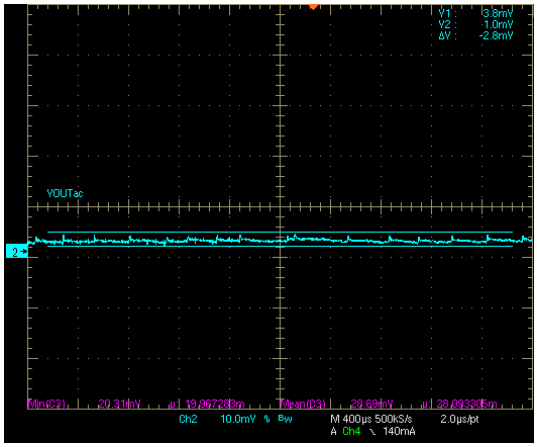



**Figure 19. Output voltage ripple at 230 $V_{AC}$, no load**

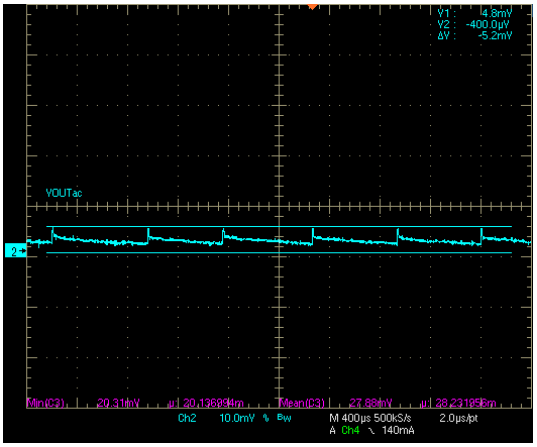



**Figure 20. Output voltage ripple at 115 $V_{AC}$, $I_{OUT}$ = 25 mA**

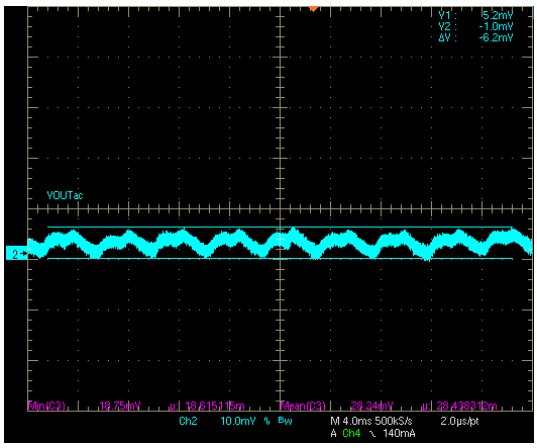
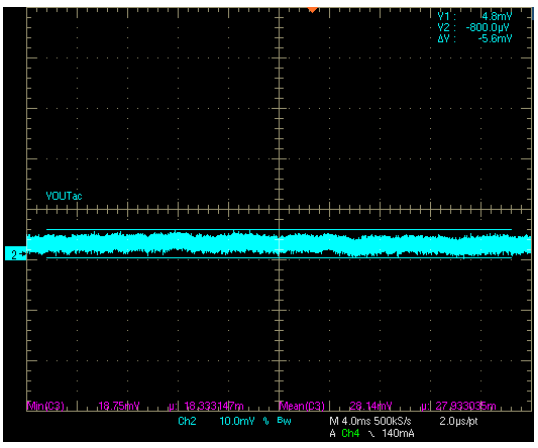



**Figure 21. Output voltage ripple at 230 $V_{AC}$, $I_{OUT}$ = 25 mA**



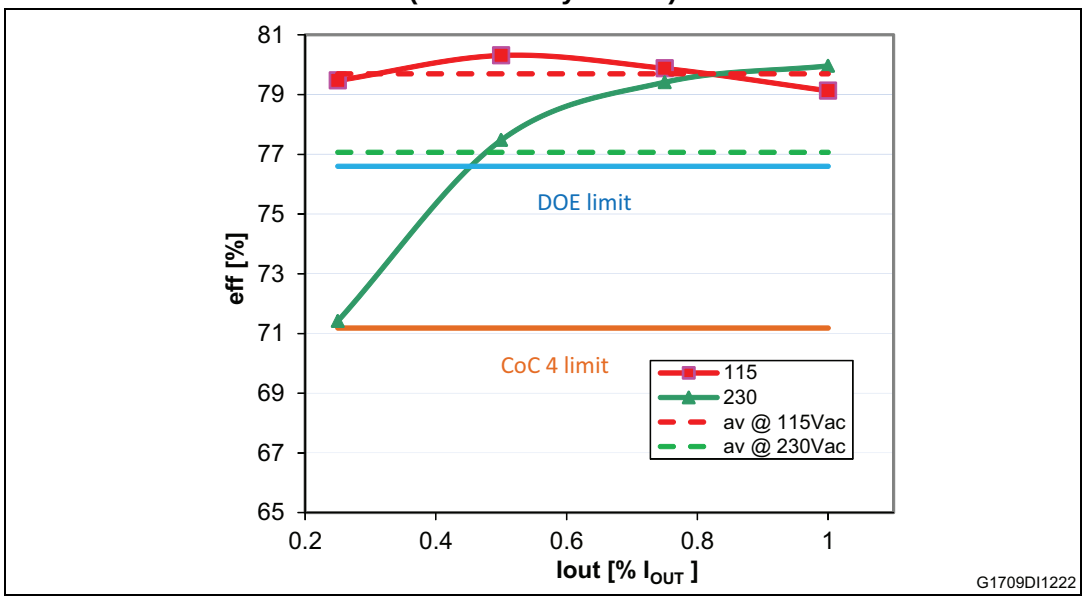
## 4.4 Efficiency

The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltage ($V_{IN}$ = 115 $V_{AC}$ and $V_{IN}$ = 230 $V_{AC}$). External power supplies (the power supplies which are contained in a separate housing from the end-use devices they are powering) need to comply with the code of conduct (version 4) “active mode efficiency” criterion, which states an active mode efficiency higher than 71.18% for a power throughput of 4.2 W.

Another standard to be applied to external power supplies in the coming years is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 76.6%.

If the IC is externally biased, the presented evaluation board is compliant with both standards, as can be seen from *Figure 22* where the average efficiencies of the board at 115 $V_{AC}$ (79.7%) and at 230 $V_{AC}$ (77.1%) are plotted with dotted lines, together with the above limits. In the same figure the efficiency at 25%, 50%, 75% and 100% of output load for both input voltages is also shown.

**Figure 22. Active mode efficiency and comparison with energy efficiency standards (IC externally biased)**




## 4.5 Light load performance

The input power of the converter has been measured in no load condition for different input voltages and the results are reported in *Table 5*.

**Table 5. No load input power**

| $V_{IN}$ ($V_{AC}$) | $P_{IN}$ (mW) | |
|---|---|---|
| | Self biasing | External biasing |
| 90 | 74.3 | 16.8 |
| 115 | 93 | 18.4 |
| 150 | 121 | 20.7 |
| 180 | 144 | 21.9 |
| 230 | 185 | 23 |
| 265 | 215 | 27 |

In version 4 of the code of conduct, also the power consumption of the power supply when it is no loaded is considered. The criteria to be compliant with are reported in *Table 6* below:

**Table 6. No load input power**

| Nameplate output power ($P_{no}$) | Maximum power in no load for AC-DC EPS |
|---|---|
| 0 to ≤ 50 W | < 0.3 W |
| > 50 W < 250 W | < 0.5 W |

Considering only the case of external biasing (by auxiliary winding), the power consumption of the presented board is more than ten times lower than the code of conduct, version 4 limit. Even if this performance seems to be disproportionately better than the requirements, it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirement about no load consumption and when the converter is used as an auxiliary power supply, the line filter is often the main line filter of the entire power supply that considerably increases standby consumption.

Even if the code of conduct, version 4 program does not have other requirements regarding light load performance, in order to give more information the consumption of the evaluation board in two other light load cases ($P_{OUT}$ = 25 mW and $P_{OUT}$ = 50 mW) has also been measured. The results versus line voltage are plotted in the figure below, together with the no load measurements reported in *Table 5*.

**Figure 23. $P_{IN}$ vs. $V_{IN}$ @ $P_{OUT}$ = 0; 25 mW; 50 mW, IC externally biased**

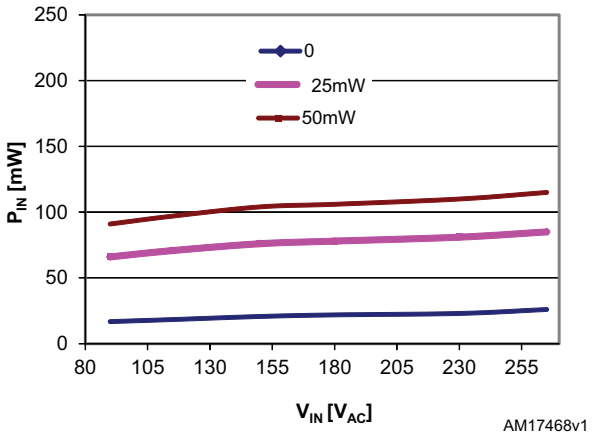
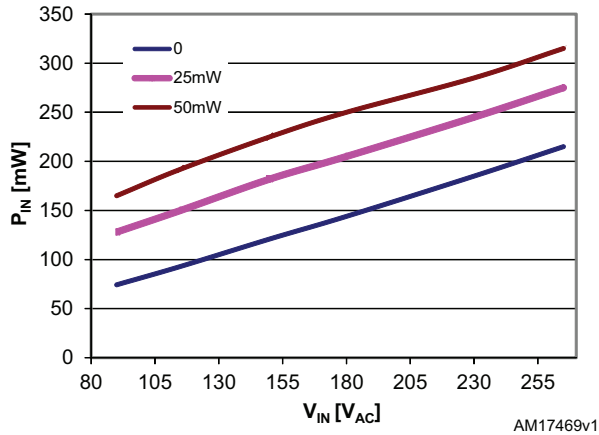



**Figure 24. $P_{IN}$ vs $V_{IN}$ @ $P_{OUT}$ = 0; 25 mW; 50 mW, IC self biased**




Depending on the equipment supplied, it is possible to have several criteria to measure the performance of a converter. One criterion is the measure of the output power (or the efficiency) when the input power is equal to one watt. This measurement is shown in *Figure 25* and *Figure 26* for different input voltage values.

**Figure 25. Efficiency @ $P_{IN}$ = 1 W, IC external biased**

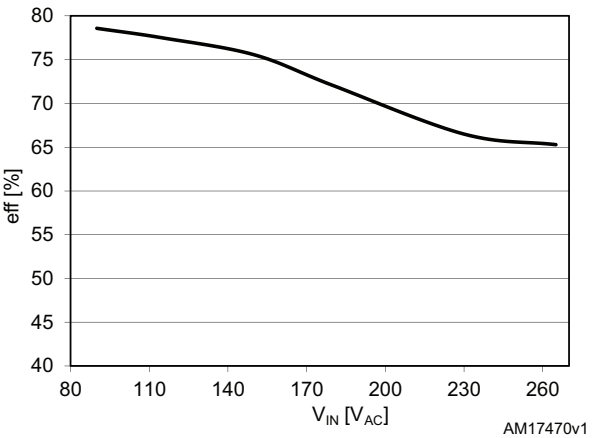
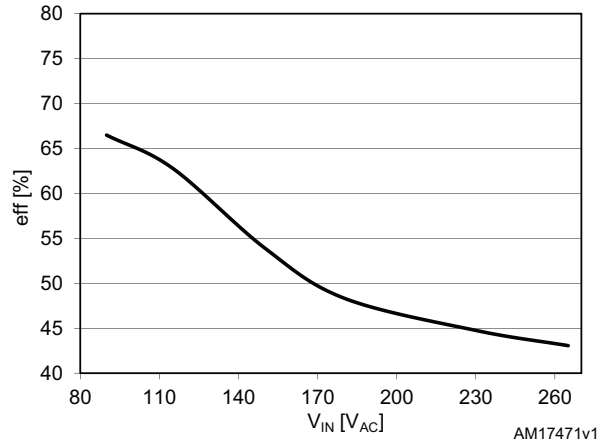



**Figure 26. Efficiency @ $P_{IN}$ = 1 W, IC self biased**




Another requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. When the IC is externally biased, the evaluation board can satisfy even this requirement, as shown in *Figure 27*. In *Figure 28* the performance with IC self supplied is shown.

**Figure 27. $P_{IN}$ @ $P_{OUT}$ = 0.25 W, IC externally biased**

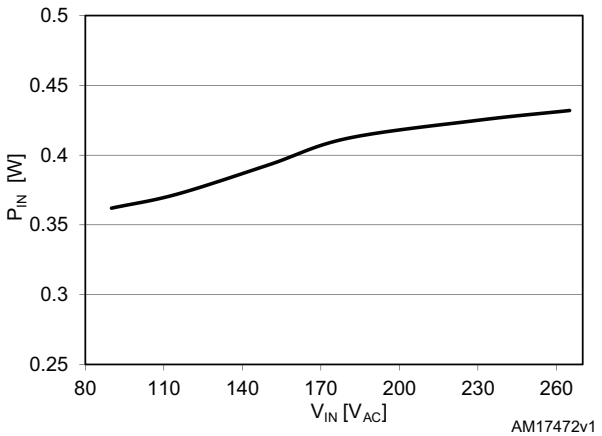
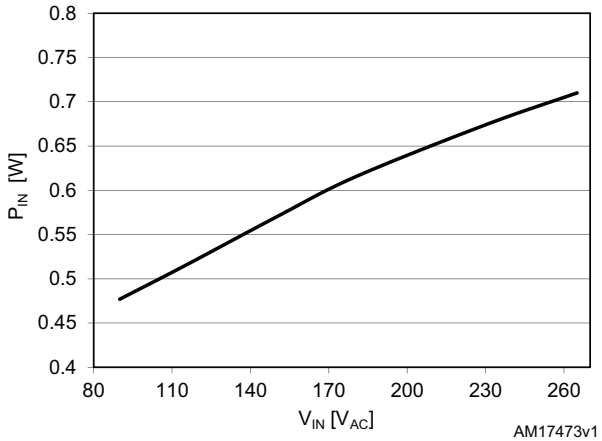



**Figure 28. $P_{IN}$ @ $P_{OUT}$ = 0.25 W, IC self biased**



# 5 Functional check

## 5.1 Soft start

At startup the current limitation value reaches $I_{DLIM}$ after an internally fixed time, $t_{SS}$, whose typical value is 8.5 msec. This time is divided into 16 time intervals, each corresponding to a current limitation step progressively increasing. In this way the drain current is limited during the output voltage increase, therefore reducing the stress on the secondary diode.

The soft start phase is shown in *Figure 29* and *Figure 30*.

**Figure 29. Soft start @ startup**

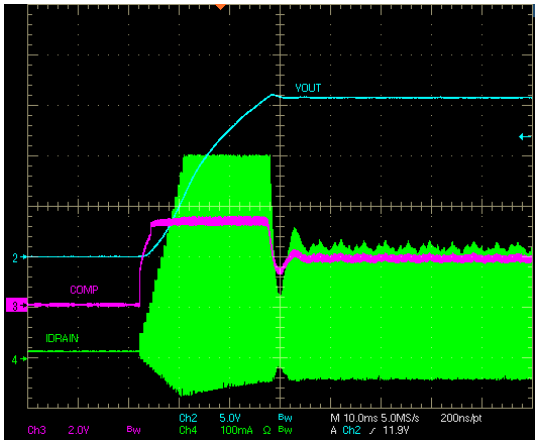
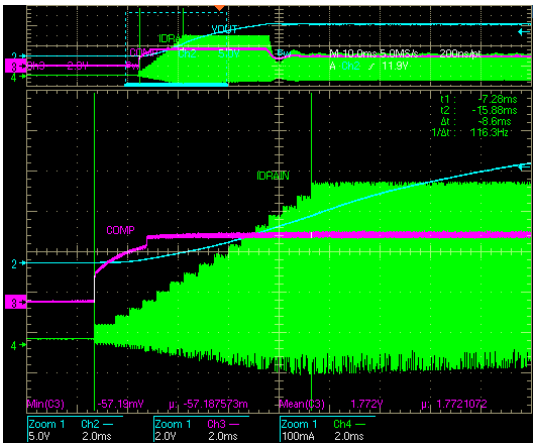



**Figure 30. Soft start @ startup (zoom)**




## 5.2 Overload protection

In case of over load or short circuit (see *Figure 31*), the drain current reaches the $I_{DLIM}$ value (or the one set by the user through the $R_{LIM}$ resistor). In every cycle where this condition is met, a counter is incremented; if it is maintained continuously for the time $t_{OVL}$ (50 msec typical, internally fixed), the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 sec typical). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (*Figure 32*). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events.

Furthermore, every time the protection is tripped, the internal soft startup function is invoked (*Figure 33*), in order to reduce the stress on the secondary diode.

After the short removal, the IC resumes normal working. If the short is removed during $t_{SS}$ or $t_{OVL}$, i.e. before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, the IC must wait for the $t_{RESTART}$ period to elapse before switching is resumed (*Figure 34*).

**Figure 31. Output short-circuit applied: OLP tripping**

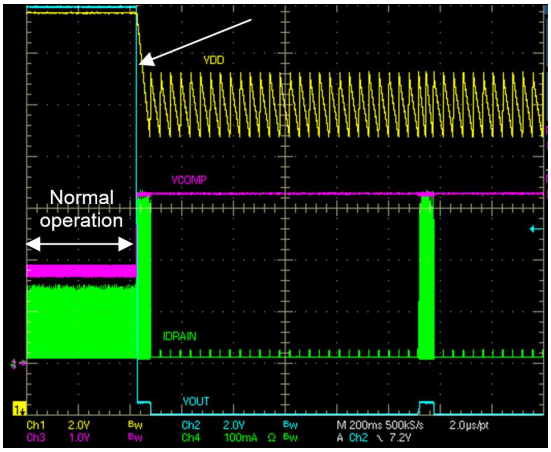



**Figure 32. Output short circuit maintained: OLP steady- state**

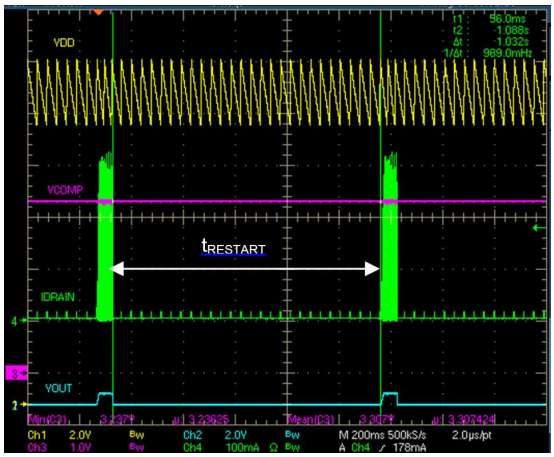



**Figure 33. Output short circuit maintained: OLP steady-state (zoom)**

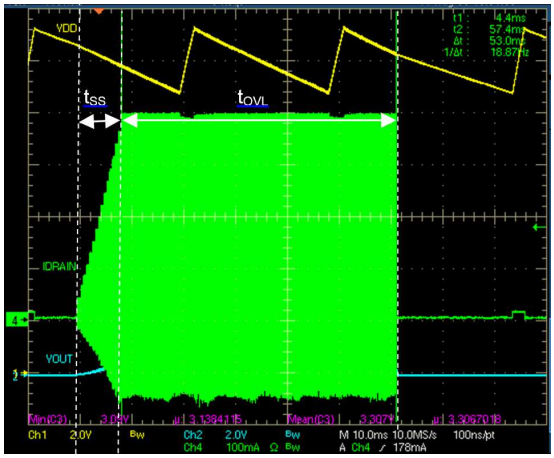
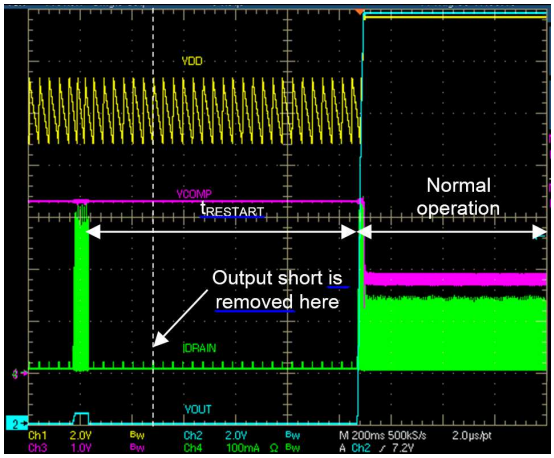



**Figure 34. Output short-circuit removal and converter restart**




## 5.3 Feedback loop failure protection

This protection is available only if the IC is not self-biased. As the loop is broken (R12 shorted or R11 open), the output voltage $V_{OUT}$ increases and the VIPER16 runs at its maximum current limitation. The $V_{DD}$ pin voltage increases as well, because it is linked to the $V_{OUT}$ through the auxiliary winding.

If the $V_{DD}$ voltage reaches the $V_{DD}$ clamp threshold (23.5 V min.) in less than 50 msec, the IC is shut down by open loop failure protection (see *Figure 35* and *Figure 36*), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low side resistor of the output voltage divider, R12 = R12a+R12b. The same behavior can be induced opening the high side resistor, R11 = R11a+R11b.

The protection acts in auto-restart mode with $t_{RESTART}$ = 1sec (*Figure 36*). As the fault is removed, normal operation is restored after the last $t_{RESTART}$ interval has been completed (*Figure 38*).

**Figure 35. Feedback loop failure protection: tripping**

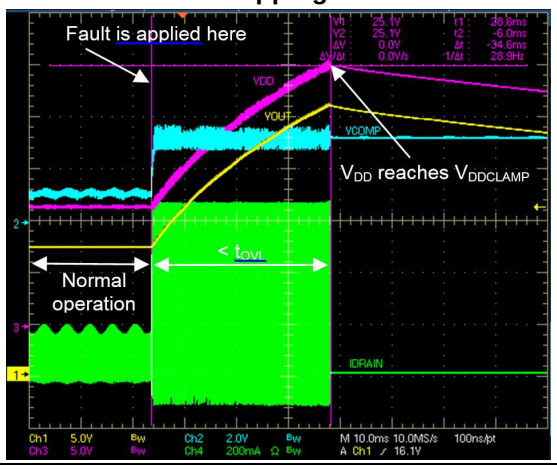



**Figure 36. Feedback loop failure protection: steady-state**

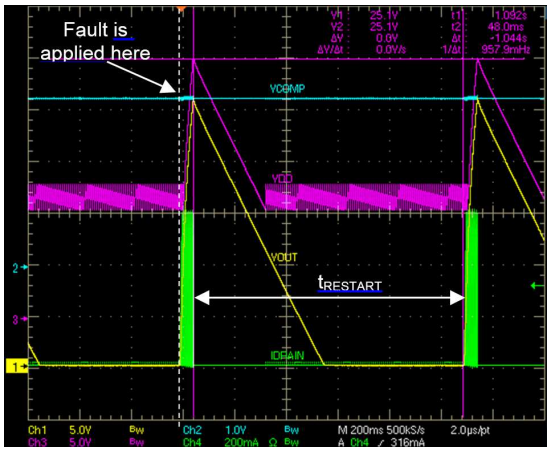



**Figure 37. Feedback loop failure protection: steady state (zoom)**

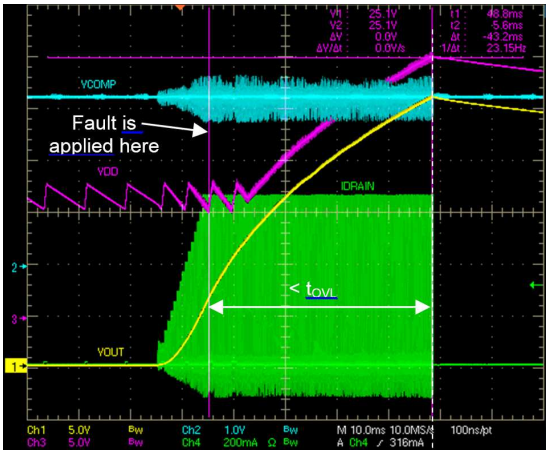
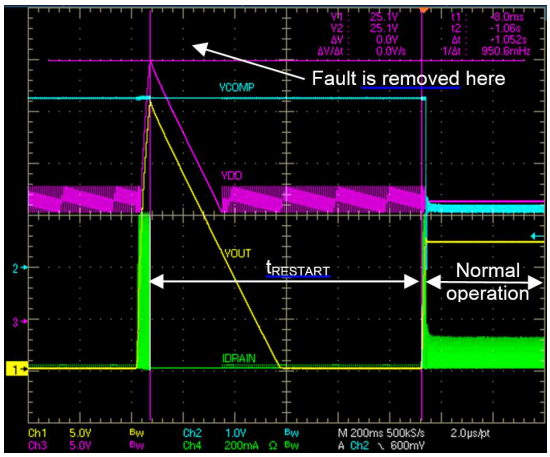



**Figure 38. Feedback loop failure protection: restore of normal operation after fault removal**

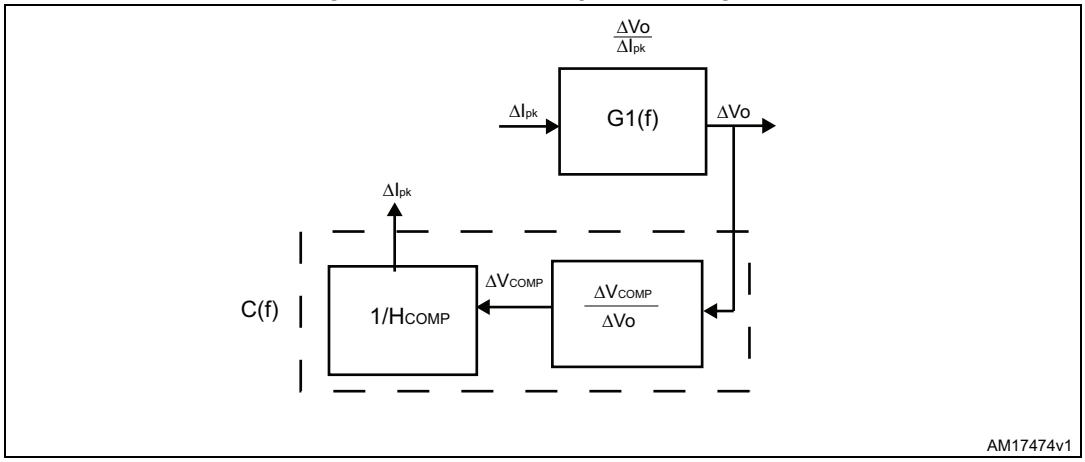


# 6 Feedback loop calculation guidelines

## 6.1 Transfer function

The set PWM modulator + power stage is indicated with G1(f), while C(f) is the “controller”, i.e. the network which is in charge to ensure the stability of the system.

**Figure 39. Control loop block diagram**




The mathematical expression of the power plant G1(f) is the following:

**Equation 1**

$$G_1(f) = \frac{\Delta V_{OUT}}{\Delta I_{pk}} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p})} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot f}{fz})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot f}{fp})}$$

where, considering the schematic of *Figure 5.*:

**Equation 2**

$$fp = \frac{1}{\pi \cdot C9 \cdot (R_{OUT} + 2ESR)}$$

is the pole due to the output load ($R_{OUT} = V_{OUT}/I_{OUT}$) and

**Equation 3**

$$fz = \frac{1}{2 \cdot \pi \cdot C9 \cdot ESR}$$

is the zero due to the ESR of the output capacitor C9. The mathematical expression of the compensator C(f) is:

**Equation 4**

$$C(f) = \frac{\Delta I_{pk}}{\Delta V_o} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{2 \cdot \pi \cdot f \cdot j \cdot \left(1 + \frac{f \cdot j}{fPc}\right)}$$

where:

**Equation 5**

$$C_0 = \frac{R_{COMP} \cdot CTR}{R11 \cdot R8 \cdot C11}$$

**Equation 6**

$$fZc = \frac{1}{2 \cdot \pi \cdot (R10 + R11) \cdot C11}$$

**Equation 7**

$$fPc = \frac{1}{2 \cdot \pi \cdot R_{COMP} \cdot C8}$$

will be chosen in order to censure the stability of the overall system.

In the formulas above, $H_{COMP}$ = 7Ω is the $\Delta V_{COMP}$ to $\Delta_{IDRAIN}$ ratio of VIPER16, $R_{COMP}$ = 15 kΩ is the dynamic resistance of the COMP pin, CTR is the current transfer ratio of the optocoupler.

## 6.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency, for instance:

fZc = fp/2

fPc = fz

fcross = 4kHz ≤ fsw/10

G1(cross) can be calculated from equation (1) and, since by definition it is | C(fcross)*G1(fcross) | = 1, $C_0$ can be calculated as follows:

**Equation 8**

$$C_0 = \frac{\left|2 \cdot \pi \cdot fcross \cdot j\right| \cdot \left|1 + \frac{fcross \cdot j}{fPc}\right|}{\left|1 + \frac{fcross \cdot j}{fZc}\right|} \cdot \frac{Hcomp}{\left|G1(fcross)\right|}$$

At this point the bode diagram of G1(f)*C(f) can be plotted, in order to check the phase margin for the stability.

If the margin is not high enough, another choice should be done for fZc, fPc and fcross, and the procedure repeated.

When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated, using the above formulas, as follows:

**Equation 9**

$$R12 = \frac{R11}{\frac{V_{OUT}}{V_{REF}} - 1}$$

**Equation 10**

$$C11 = \frac{R_{COMP} \cdot CTR}{R11 \cdot R8 \cdot C_0}$$

**Equation 11**

$$R10 = \frac{1}{2\pi \cdot C11 \cdot fZc} - R11$$

**Equation 12**

$$C8 = \frac{1}{2 \cdot \pi \cdot fPc \cdot R_{COMP}}$$

# 7 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for 115 VAC and 230 $V_{AC}$ mains input, full load condition, both with IC externally biased and self biased. The results are shown in *Figure 40*, *41*, *42* and *43*.

When the IC is self biased its temperature is higher, due to the power dissipated by the HV-startup generator.

**Figure 40. Thermal measurements at 90$V_{AC}$, full load, $I_C$ externally biased**

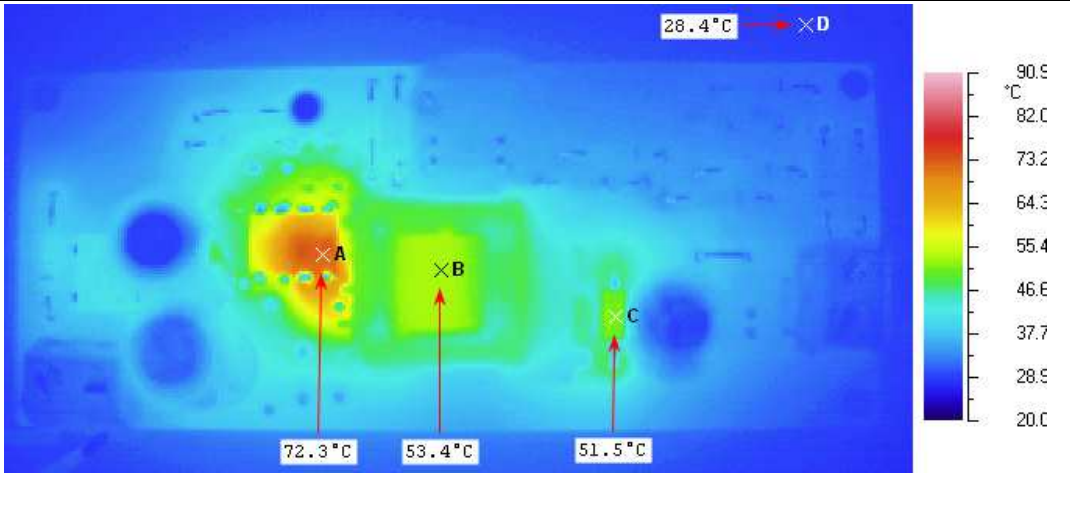



**Figure 41. Thermal measurements at 115$V_{AC}$, full load, $I_C$ externally biased**

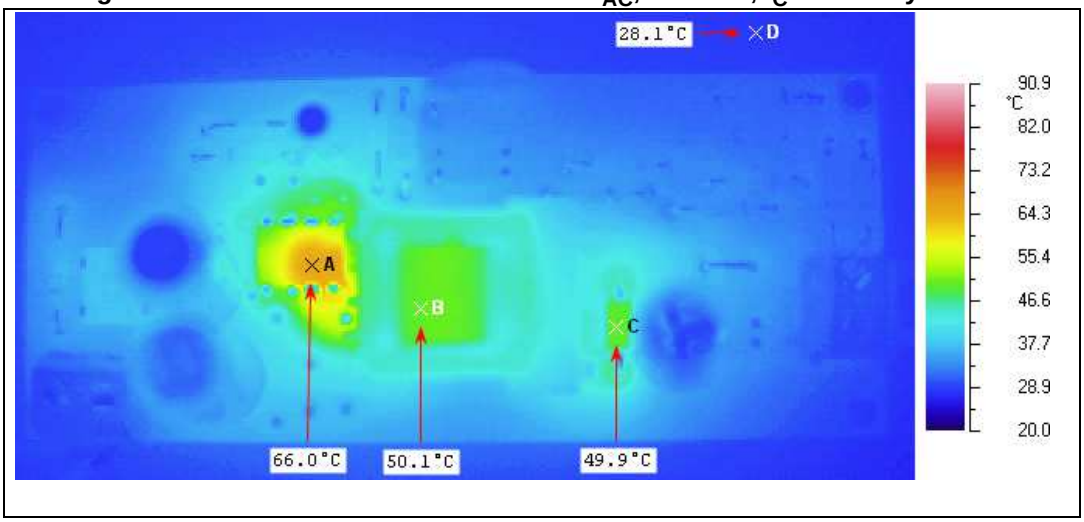


Figure 42. Thermal measurements at 230$V_{AC}$, full load, $I_C$ externally biased

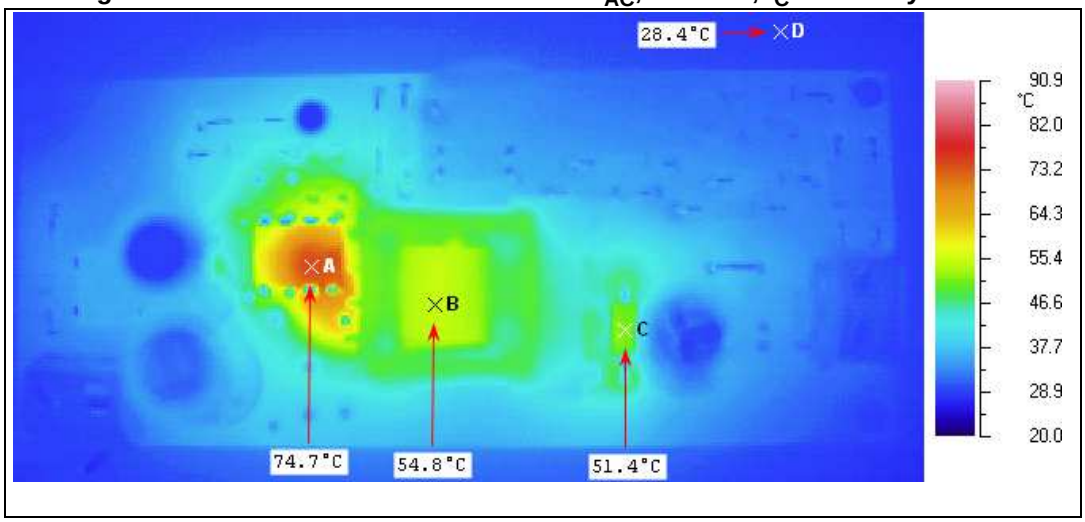
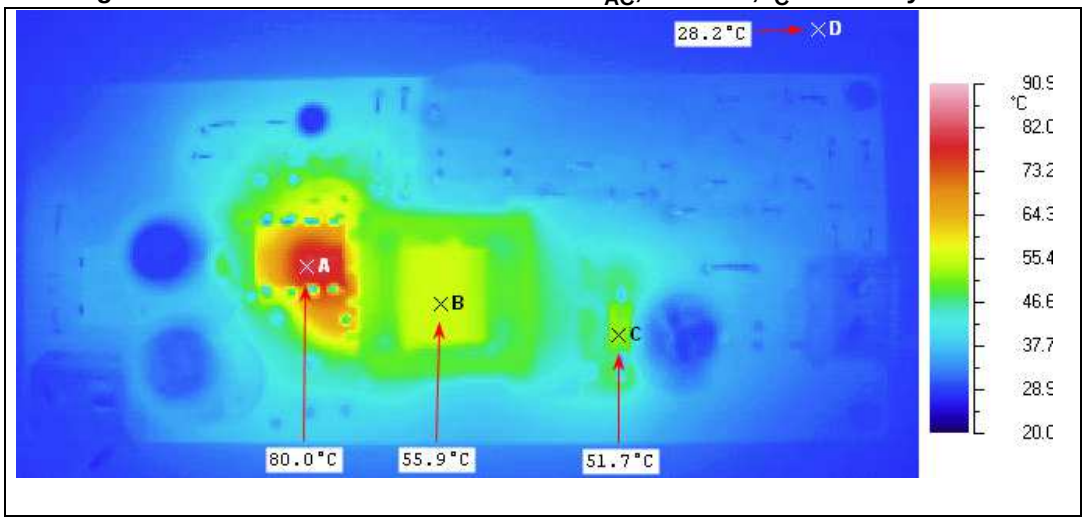



Figure 43. Thermal measurements at 265$V_{AC}$, full load, $I_C$ externally biased



# 8 EMI measurements

A pre-compliant tests to EN55022 (Class B) European normative has been performed using an EMC analyzer and a LISN.

The average EMC measurements at 115 $V_{AC}$/full load and 230 $V_{AC}$/full load have been performed and the results are shown in *Figure 44* and *Figure 45* respectively.

**Figure 44. Average measurement at $V_{IN}$ = 115 $V_{AC}$, full load**

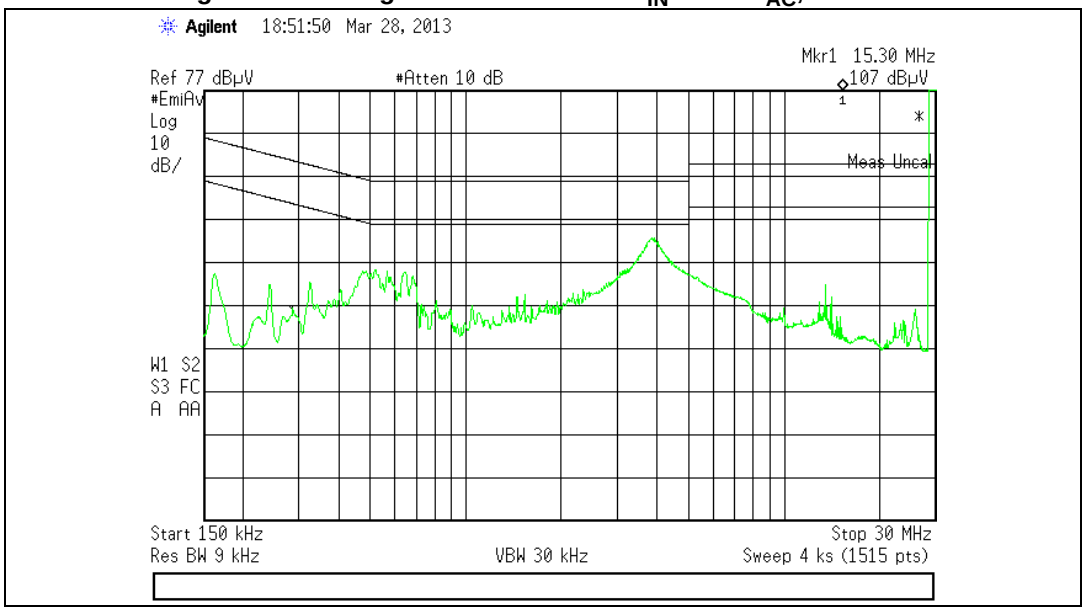
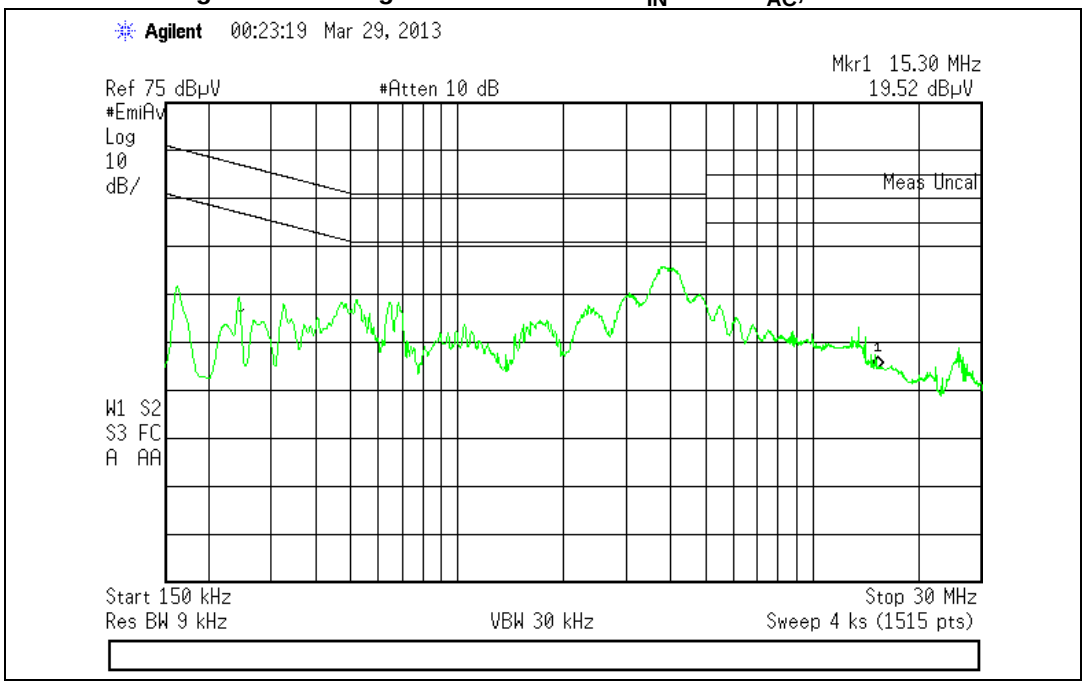
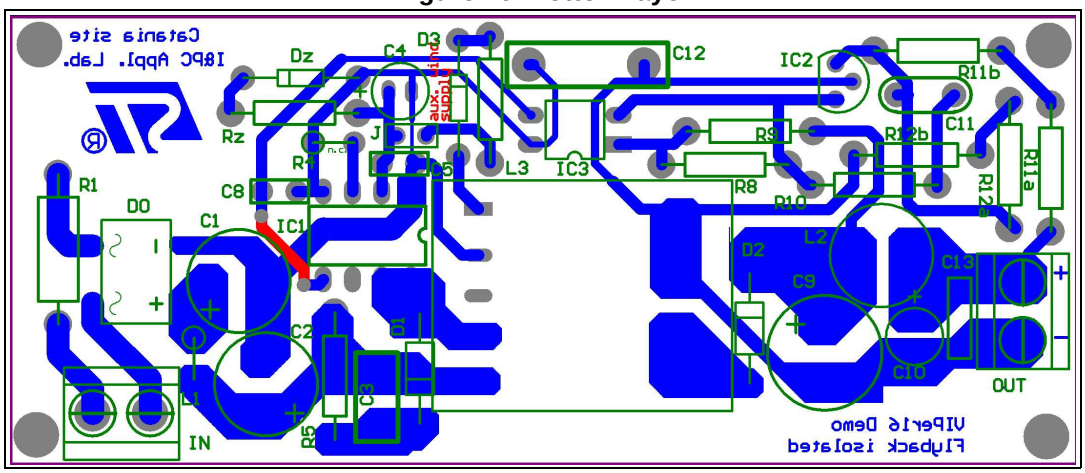



**Figure 45. Average measurement at $V_{IN}$ = 230 $V_{AC}$, full load**



# 9 Board layout

Figure 46. Bottom layer



# 10 Conclusion

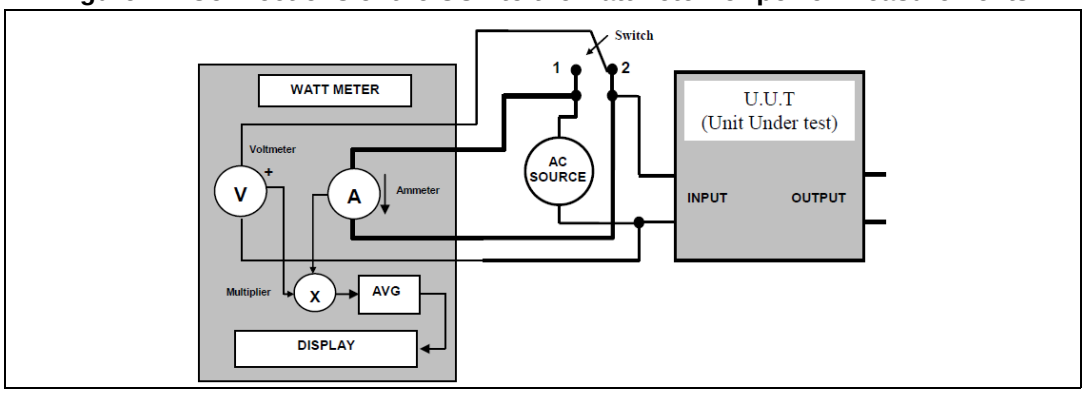
The VIPER16 allows a non-isolated converter to be designed in a simple way and with few external components. In this document a isolated flyback has been described and characterized. Special attention has been given to light load performance, confirmed as very good by bench analysis. The efficiency performance has been compared to the requirements of the Code of Conduct (version 4) for an external AC-DC adapter with very good results.

# Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

*Figure 47* shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

**Figure 47. Connections of the UUT to the wattmeter for power measurements**



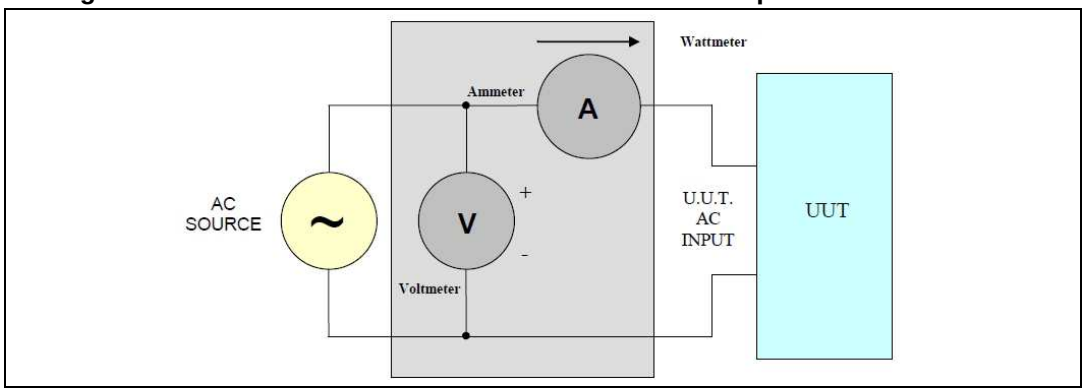

An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter's efficiency, which has been measured in different input/output conditions.

## A.1 Measuring input power

With reference to *Figure 47*, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

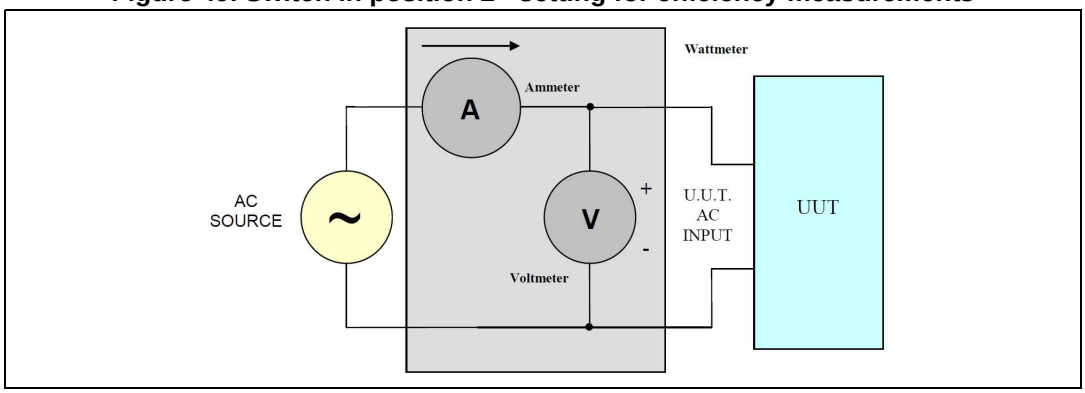
If the switch of *Figure 47* is in position 1 (see also the simplified scheme of *Figure 48*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we are measuring the input power of UUT in light load condition).

**Figure 48. Connections of the UUT to the wattmeter for power measurements**




In the case of high UUT input current (i.e. for measurements in heavy load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in *Figure 47* can be changed to position 2 (see simplified scheme of *Figure 49*) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

**Figure 49. Switch in position 2 - setting for efficiency measurements**




On the other hand, the position of *Figure 49* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is the reason why it is better to use the setting of *Figure 48* for light load measurements and *Figure 49* for heavy load measurements. If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value. As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current output for at least 30 minutes (warm up period) immediately prior to conducting efficiency measurements. After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured over time for both AC input and DC output. Some wattmeter models allow integration of the measured input power in a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is calculated dividing by the integration time itself.

# 11 References


- Code of Conduct on Energy Efficiency of External Power Supplies, Version 4
- VIPER16 datasheet

# 12 Revision history

Table 7. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 29-May-2015 | 1 | Initial release. |
| 19-May-2016 | 2 | Added: new T1 part 7508110342 Rev 6A in *Table 2*. |
| 10-Jan-2017 | 3 | Updated: *Table 5: No load input power*. |