AN4265
Application note

STEVAL-TDR031V1 and STEVAL-TDR034V1: LDMOS power module designs for two-way mobile radios

By Alfio Scuto

Introduction

Two-way radios are today present in almost every area of public life. They are an invaluable tool supporting professionals in a variety of industries ranging from transportation to energy, government and others. With two-way radios, there is no need to deploy supporting infrastructure in a field. In fact, two-way radios can offer an instant, private and cost-effective communication anywhere and anytime. Nevertheless, there is a vast and growing market among non-professional users who demand high-quality yet affordable equipment. The purpose of this application note is to provide both amateurs and professionals with the tools needed to create their own “two-way radio”, not linked to any specific standard product present in the market. This allows greater integration in radio systems currently in development and, in general, considerable savings in production costs.

Contents

List of figures

1 Design the final stage: preliminary trials using chip-on-board

This application note introduces two RF power amplifier modules working in the UHF band with the output power being the only main difference.

The name and target specifications of each amplifier are the following:

Table 1. Target specification

Symbol	Parameter	Min.	Typ.	Max.	Unit		P_{OUT}	Project name
V_{DD}	Supply voltage		12.5		V		45 W	STEVAL-TDR031V1
F	Frequency range	400		470	MHz			
P_{IN}	Input voltage		5		dBm	>>>		
ηT	Total efficiency	50			%		70 W	STEVAL-TDR034V1
2fo	2nd harmonic			-45	dBc			
ρin	Input return loss			-3	dB			

Both amplifiers use laterally diffused MOS (LDMOS) devices, respectively housed in three different packages: SOT-89, PowerFLAT™, PSO-10.

In order to meet the above targets, a line-up topology with three power stages has been used (*Figure 1*).

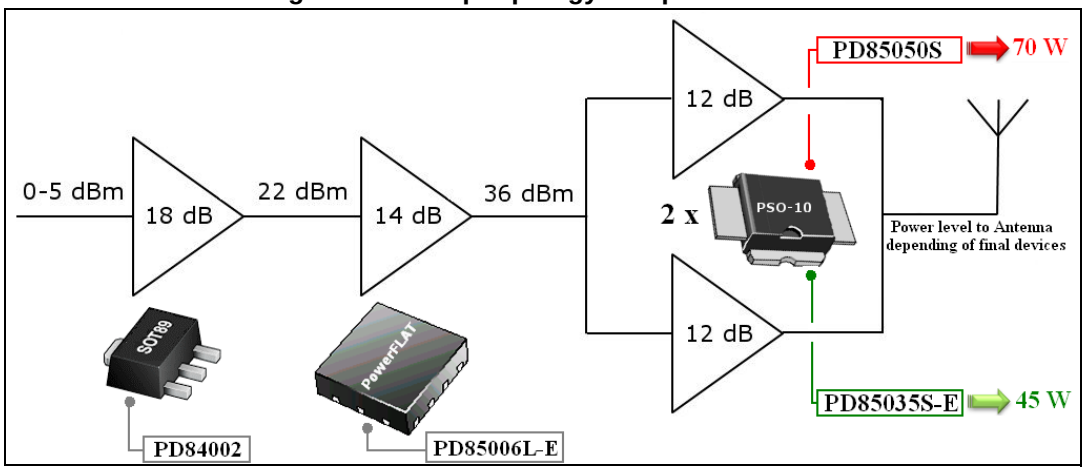
The basic idea was to consider the two projects as a single project (*Figure 1*), where the cascade 1st and 2nd stage should have enough power to drive the final stage of the two devices in parallel.

Depending on the output power (*Table 1*) the final stage has been designed with two devices in parallel, respectively: 2xPD85035S-E or 2xPD85050S.

Based on the two devices' datasheets (PD85035S-E and PD85050S) we calculated that a 36 dBm power level is required to achieve a 45 W or 70 W output power.

Similarly, for the drive stage (cascade 1st and 2nd stage), using the datasheets for PD84002 and PD85006L-E, we obtained the following power level chain.

Figure 1. Line-up topology and power levels



Each stage was simulated using the ADS software from Agilent. The intent was to get the right output impedance level to guarantee the desired power level all along the line-up.

Using library models available for each product employed (www.st.com/rf), several simulations were performed cascading the 1st and the 2nd stage in order to get a power level greater than 36 dBm.

Following the simulations at central frequency (435 MHz), the optimum load impedance for the final stage (2nd stage) is:

$$\begin{cases} Z_{lopt} = 50\,\Omega \\ Z_{lopt} = (3.818 - j * 1.189)\,\Omega \\ P_{delmax} = 38\ \text{dBm}\ (\approx 6.3\ \text{W}) \end{cases}$$

Using this impedance value at 435 MHz (Zlopt) performance was optimized along the required frequency band.

Figure 2. Power gain in the band

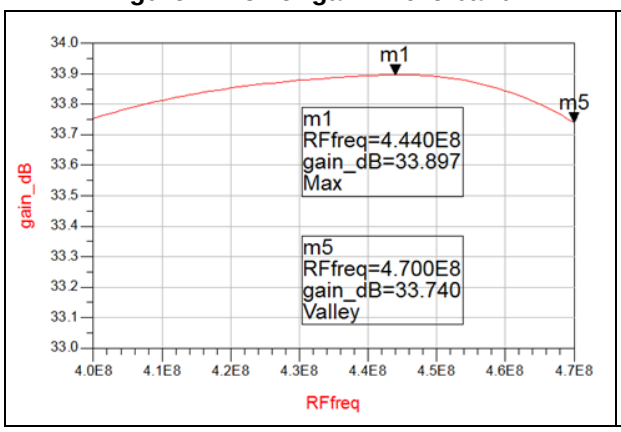
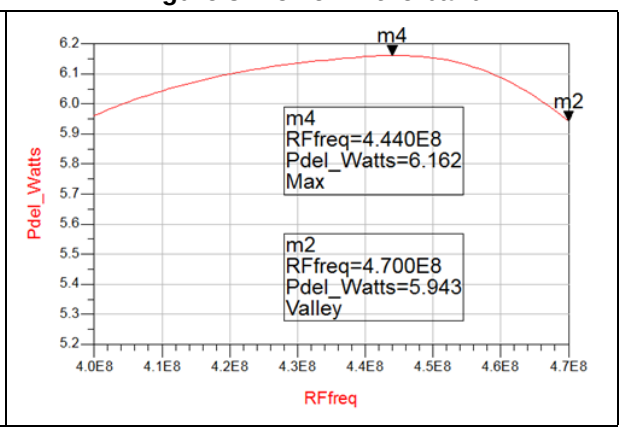


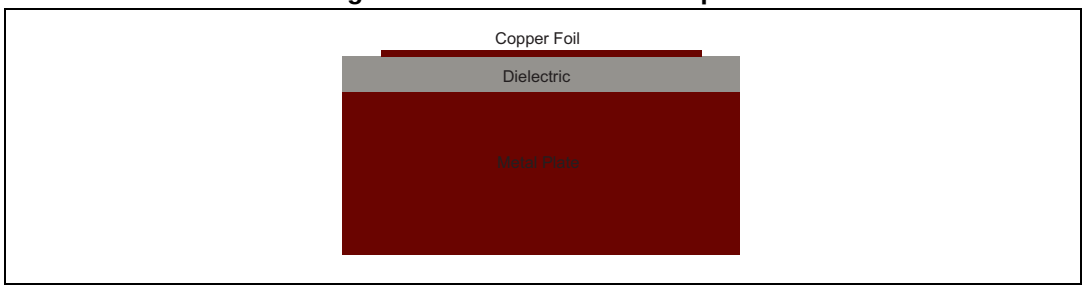
Figure 3. Power in the band



The two target projects (*Table 1*) were done using packaged LDMOS. Nevertheless it is valuable to explore all the potential capabilities offered by the technology directly using the dice (no package). In this section we analyze a hybrid combination between chip-on-board (COB) as final stage and two packaged products for 1st and 2nd stages.

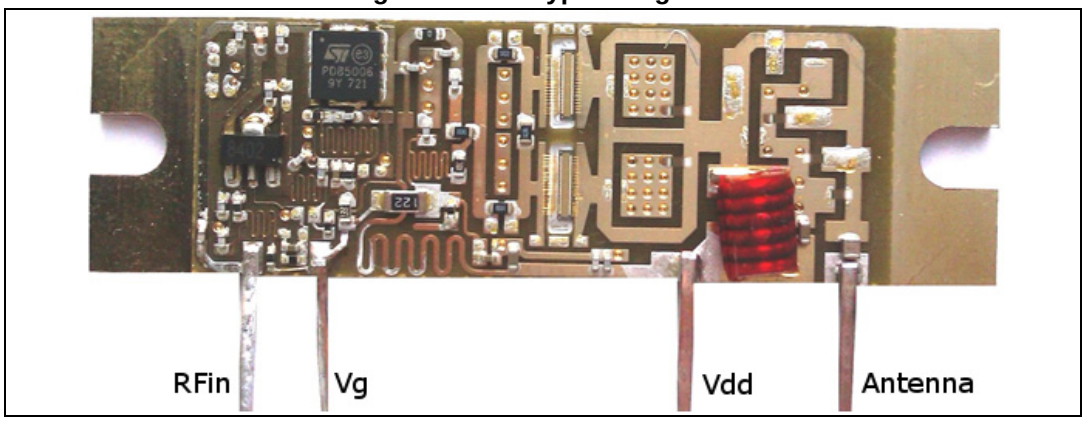
Thanks to the COB solution analysis we have better understood all the thermal aspects which are essential for this power stage.

Figure 4. Dielectric and metal plate



To realize the module, we have used the FR-4 substrate as dielectric (20 mils) bonded with a copper metal plate (1.6 mm), which ensures a very stable thermal condition for the power amplifier. On the top of the substrate FR-4 dielectric in *Figure 4*, there are two openings where the two dice have been directly bonded on copper metal gold finished layer and wired to the PCB (gate and drain side). The whole structure was simulated with HFSS (electromagnetic simulation) to extract all the parasitic parts and later using ADS (circuit simulation) we fixed the best RF performances into the required band. Finally, all the stages were assembled and the final circuit with chip-on-board (COB) is shown here:

Figure 5. Prototype using COB



The prototype (*Figure 5*) was then measured in order to verify all the RF performances (see test-bench *Figure 9*).

On the RF bench, the prototype was optimized and in some parts re-tuned.

The measurements are hereafter presented (*Figure 6* and *Figure 7*):

Figure 6. Power out vs. frequency for COB

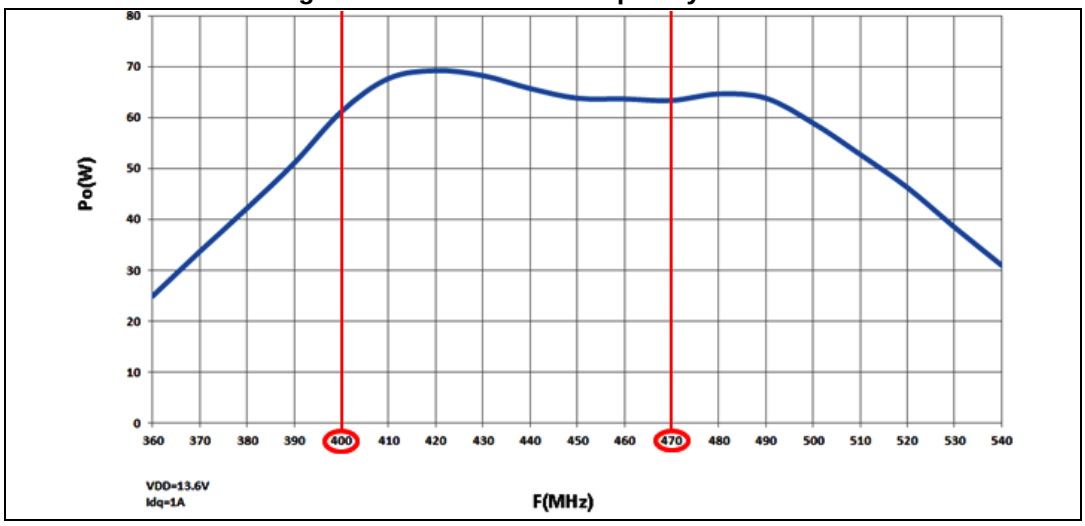
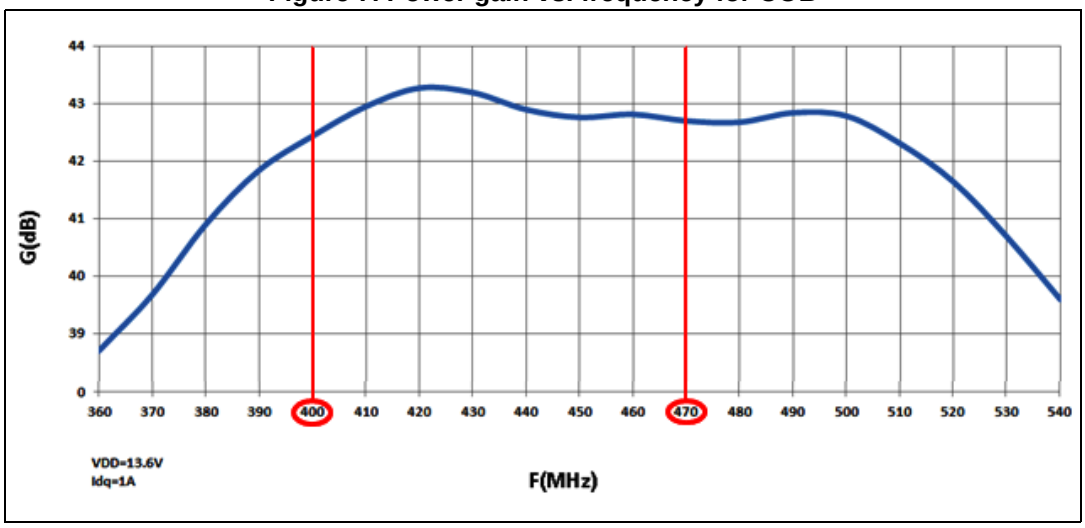


Figure 7. Power gain vs. frequency for COB



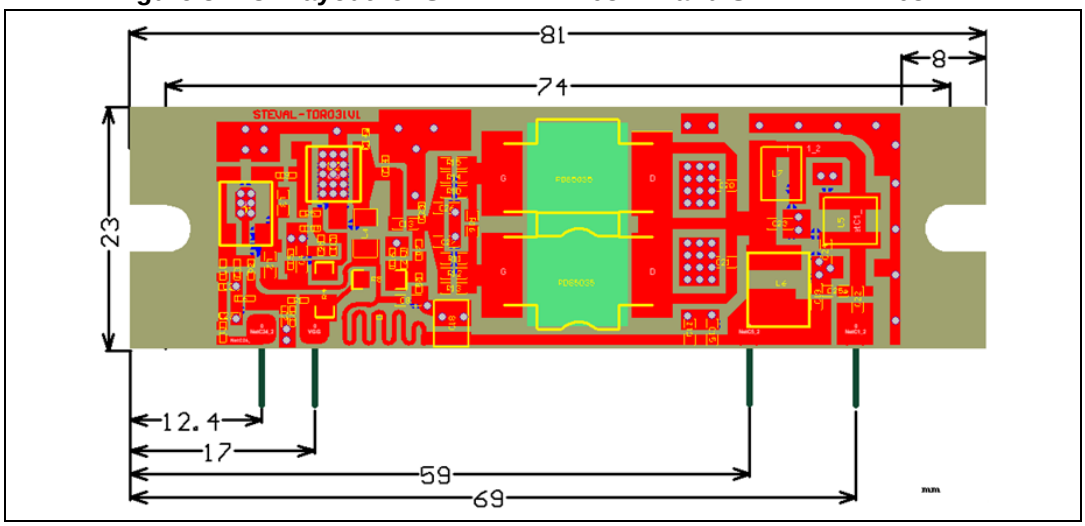
2 Design the discrete modules

Following the preliminary COB design, it is time to proceed to create the prototypes described in *Table 1*.

For both projects, we have used the same PCB topology shown in *Figure 8*.

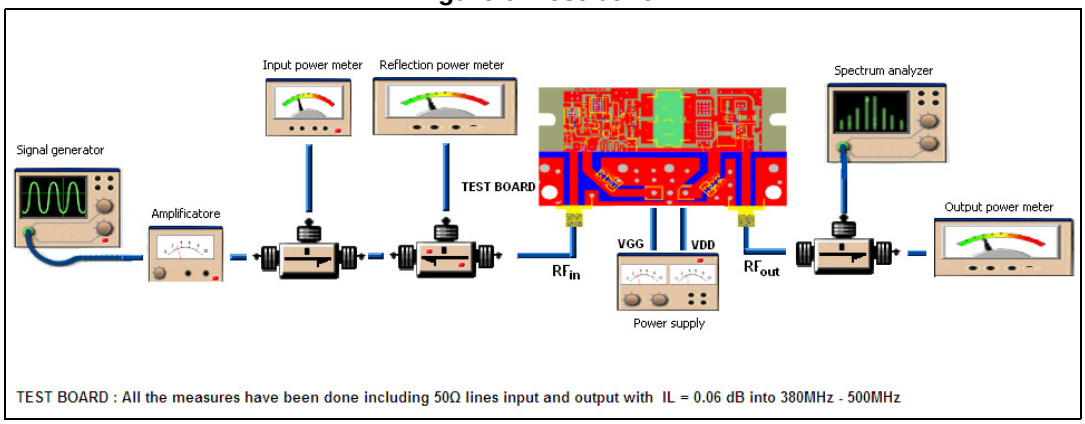
Moreover, to test the amplifiers, we have developed a special test board and heatsink (*Figure 9*). The BOM is presented in *Table 4*.

Figure 8. PCB layout for STEVAL-TDR031V1 and STEVAL-TDR034V1



All the measurements were done with test bench as shown in *Figure 9*.

Figure 9. Test bench



3 STEVAL-TDR031V1

This design moved along the same lines previously adopted for the COB version. No significant changes with regard to the 1st and the 2nd stage. All activity was focused on searching for the optimum load impedance at central frequency. The load was then used to optimize the RF behaviors along the frequency band. The result of this work is presented in the following graphs.

Figure 10. Power gain vs. frequency

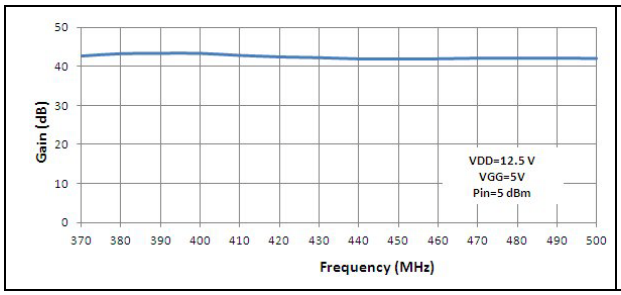


Figure 11. Input return loss vs. frequency

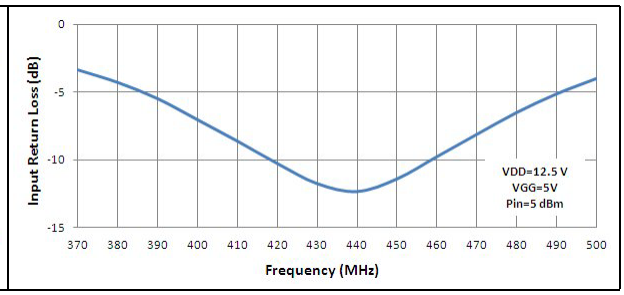


Figure 12. Output power, total efficiency vs. frequency

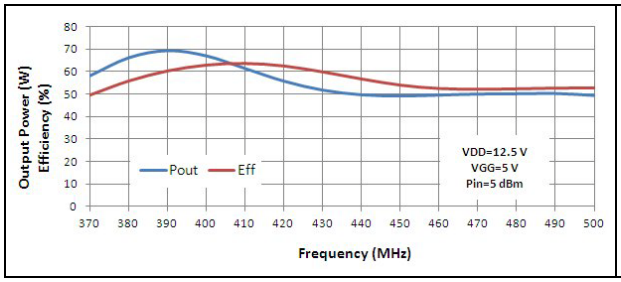


Figure 13. 2nd, 3rd harmonics vs. frequency

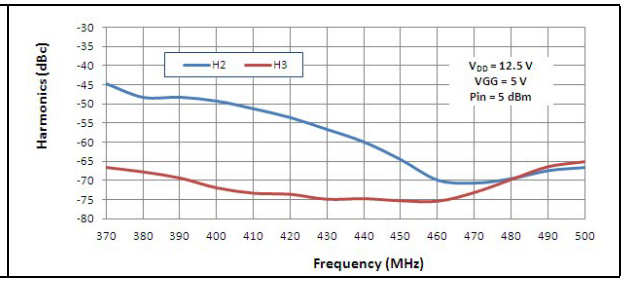
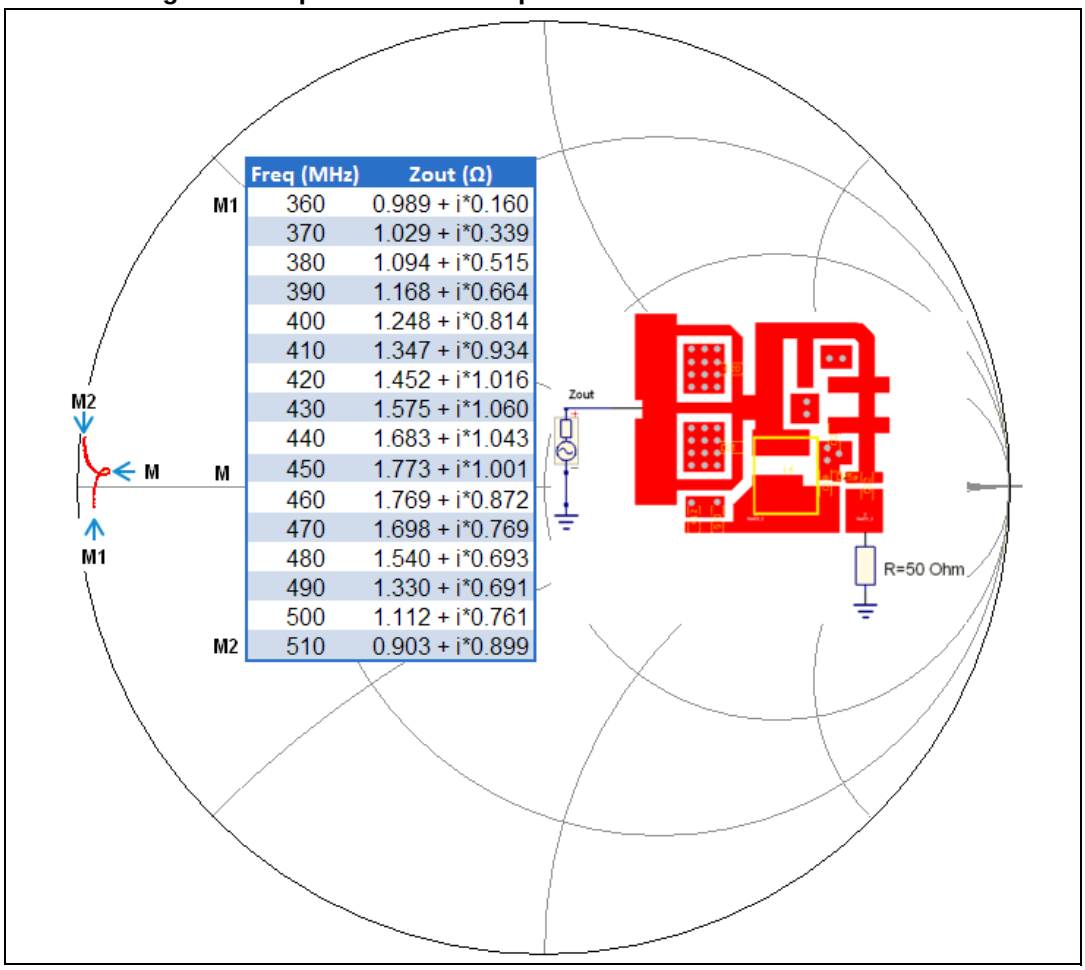


Figure 14. Equivalent drain impedances for the two PD85035S-E



In *Figure 14*, we observe the equivalent drain impedances for the two PD85035S-E, measured at the midpoint between the two drains.

The STEVAL-TDR031V1 is shown in *Figure 15*. For the schematic and BOM, refer to *Figure 16* and *Table 2*.

Figure 15. STEVAL-TDR031V1

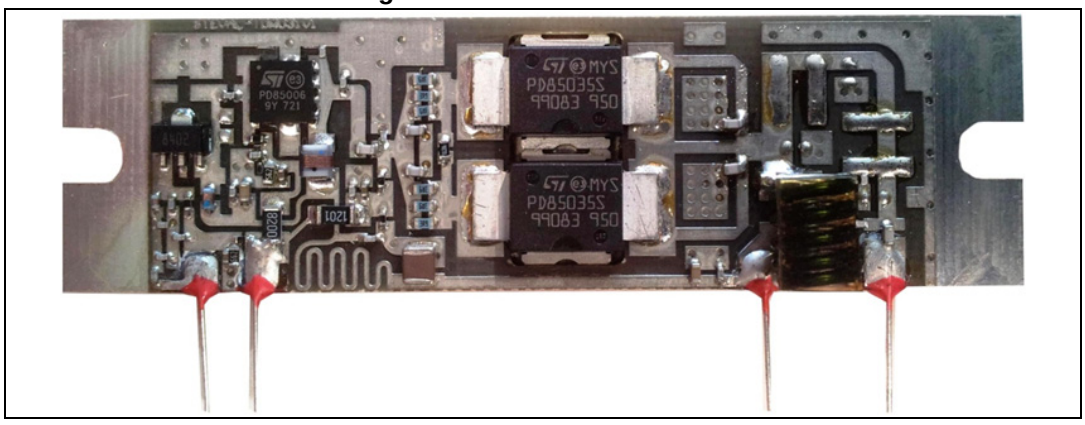


Figure 16. Circuit schematic for STEVAL-TDR031V1

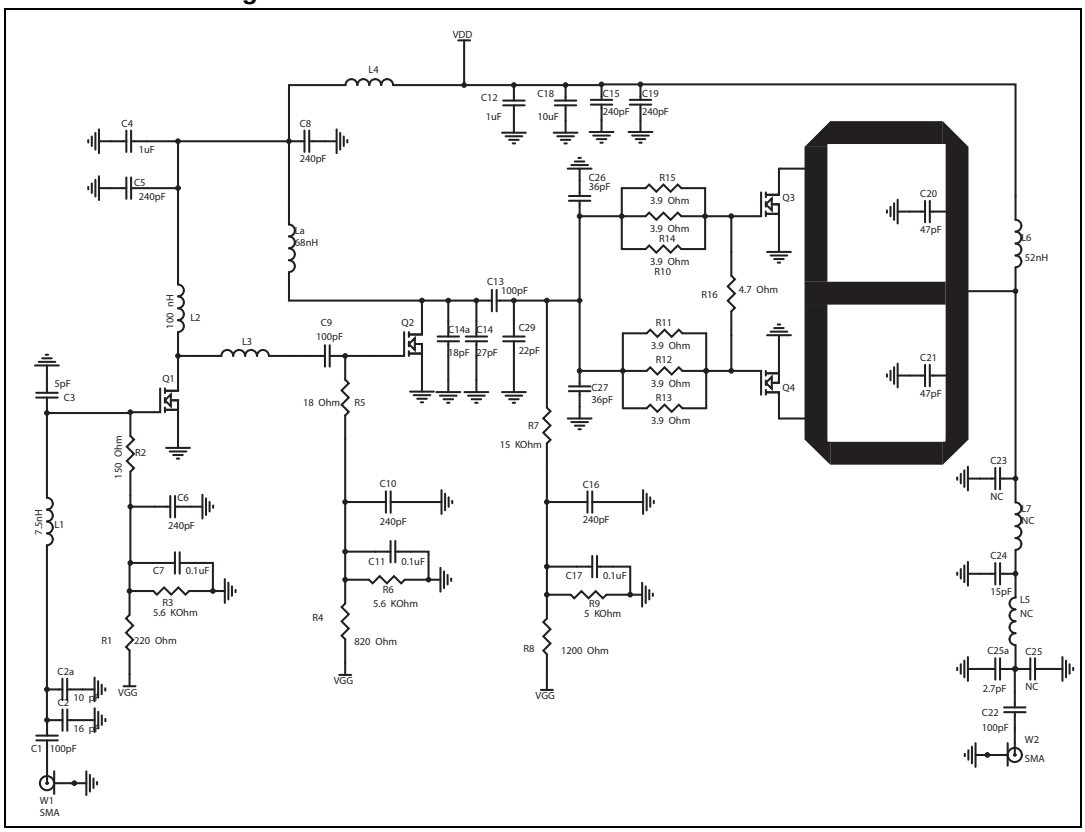


Table 2. BOM for STEVAL-TDR031V1

Designator	Manufacturer	Qty.	Value	Part number	Footprint
C1, C9	Murata	2	100 pF	GRM1555C1H101JA01	0402
C2	Murata	1	16 pF	GJM1555C1H160GB01#	0402
C2a	Murata	1	10 pF	GJM1555C1H100JZ01#	0402
C3	Murata	1	5 pF	GRM1555C1H5R0GA01#	0402
C4	Murata	1	1 µF	GRM188R61E105KA12#	0603
C5, C6, C8, C10, C15, C16, C19	Murata	7	240 pF	GRM1555C1H2241JA01#	0402
C7, C11, C17	Murata	3	0.1 µF	GRM155C81E104KA12#	0402
C12	Murata	1	1 µF	GRM188B31E105KA75#	0603
C13	Murata	2	100 pF	GQM1885C1H101GB01#	0603
C22	Murata	2	100 pF	GQM2195C1H101JB01#	0805
C14	Murata	1	27 pF	GRM1555C1H270FA01#	0402
C14a	Murata	1	18 pF	GRM1555C1H180JZ01#	0402
C18	Murata	1	10 µF	GRM32ER71H106KA12#	1210
C20, C21	Murata	2	47 pF	GQM1875C2E470GB12#	0603

Table 2. BOM for STEVAL-TDR031V1 (continued)

Designator	Manufacturer	Qty.	Value	Part number	Footprint
C24	Murata	1	15 pF	GQM1875C2E150GB12#	0603
C25a	Murata	1	2.7 pF	GCM1885C2A2R7CB01#	0603
C26, C27	Murata	2	36 pF	GRM1555C1H360GA01#	0603
C29	Murata	1	22 pF	GRM1555C1H220FA01#	0402
L1	Coilcraft	1	7.5 nH	0402CS-7N5XJLW	0402
L2	Coilcraft	1	100 nH	0603HP-R10X_LU	0603
L3, L4	NA	2	NA	NA	0402
L5	Coilcraft	1	10.2 nH	0807SQ-10N_LC	Mini A
L6	Coilcraft	1	52 nH	NA5778-AE	
L7	Coilcraft	1	3.7 nH	GA3092-ALC	Mini A
La	Coilcraft	1	68 nH	1008HQ-68NX_LC	0402
Q1	ST	1	SOT89	PD84002	SOT89
Q2	ST	1	PowerFLAT™	PD85006L	PowerFLAT™
Q3, Q4	ST	2	PSO-10	PD85035S	PSO-10
R1	Vishay	1	220 Ω	CRCW0402220RFKED	0402
R2	Vishay	1	150 Ω	CRCW0402150RFKED	0402
R3, R6	Vishay	2	5.6 KΩ	CRCW04025K60FKED	0402
R4	Vishay	1	820 Ω	CRCW1206820RFKEA	1206
R5	Vishay	1	18 Ω	CRCW040218R0FKED	0402
R7	Vishay	1	15 KΩ	CRCW040215K0FKED	0402
R8	Vishay	1	1200 Ω	CRCW12061K20FKEA	1206
R9	Vishay	1	4.99 KΩ	CRCW04024K99FKED	0402
R10, R11, R12, R13, R14, R15	KOA Speer	6	3.9 Ω	RK73H1JTTD3R90F	0603
R16	Vishay	1	4.7 Ω	CRCW06034R70FKEA	0603
Substrate			FR-4	20 mils 1oz copper	

4 STEVAL-TDR034V1

The final stage of this amplifier employs two PD85050S. Based on the latest low voltage LDMOS technology, these devices satisfy the increasing demand for power in the context of UHF mobile radios. In applications for digital communications, sometimes the linearity must be obtained with some dB of back-off from power saturation. Using the PD85050S device model, some load-pull simulations were performed in order to obtain the optimum load impedance that allowed the max output power. The value was then divided by 2 (parallel of two PD85050S) and considered as the starting point during the synthesis of the output network. The RF results and the impedance level measured at the drain level are shown in the graphs below.

Figure 17. Broadband performance

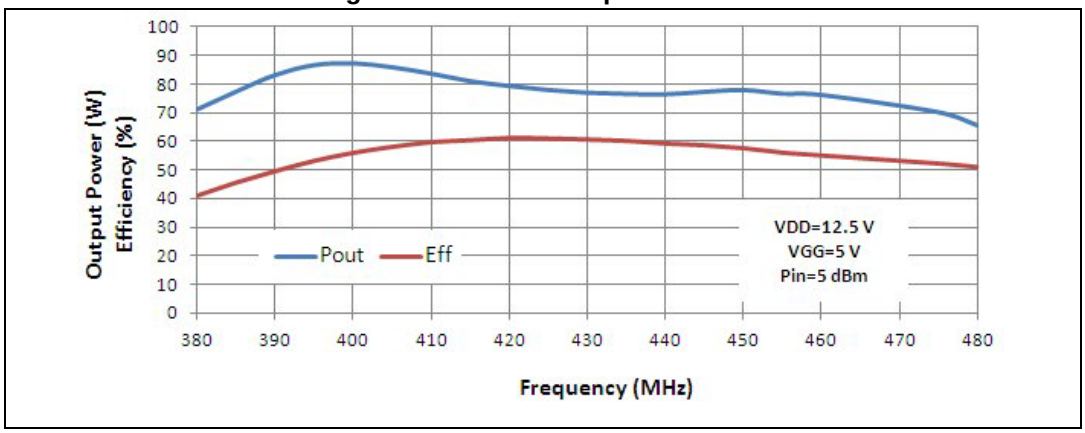


Figure 18. Output power and drain current vs. drain voltage

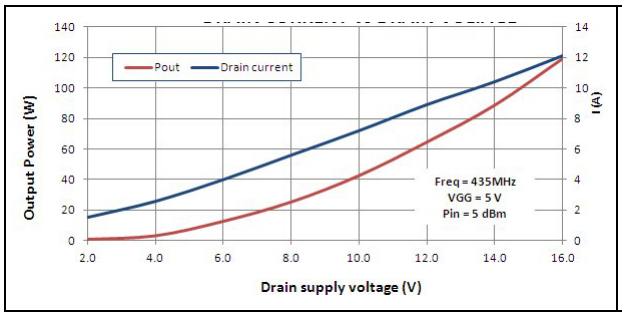


Figure 19. Output power and drain current vs. gate voltage

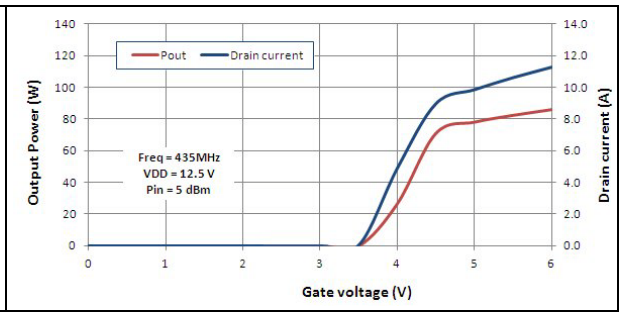
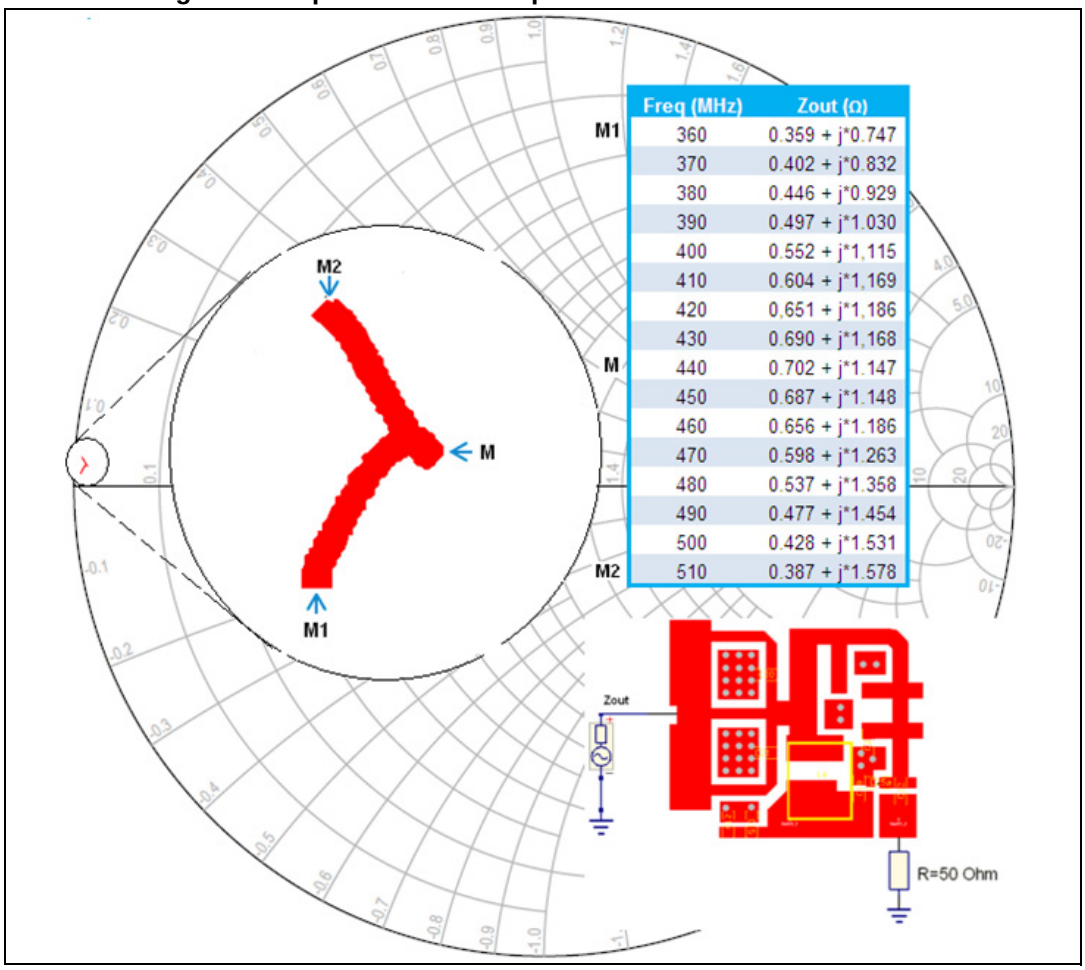


Figure 20. Equivalent drain impedances for the two PD85050S



The STEVAL-TDR034V1 is shown in *Figure 21*. For the schematic and BOM, refer to *Figure 22* and in *Table 3*.

Figure 21. STEVAL-TDR034V1

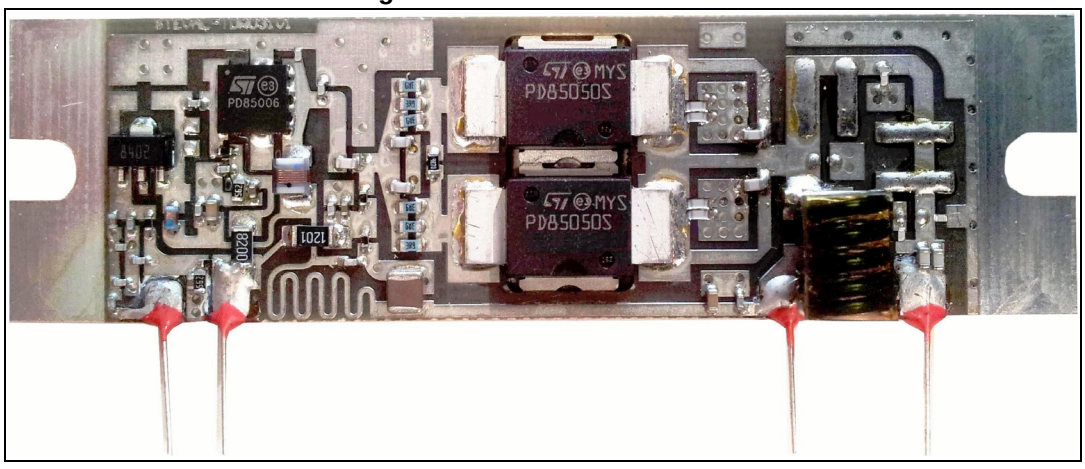


Figure 22. Circuit schematic for STEVAL-TDR034V1

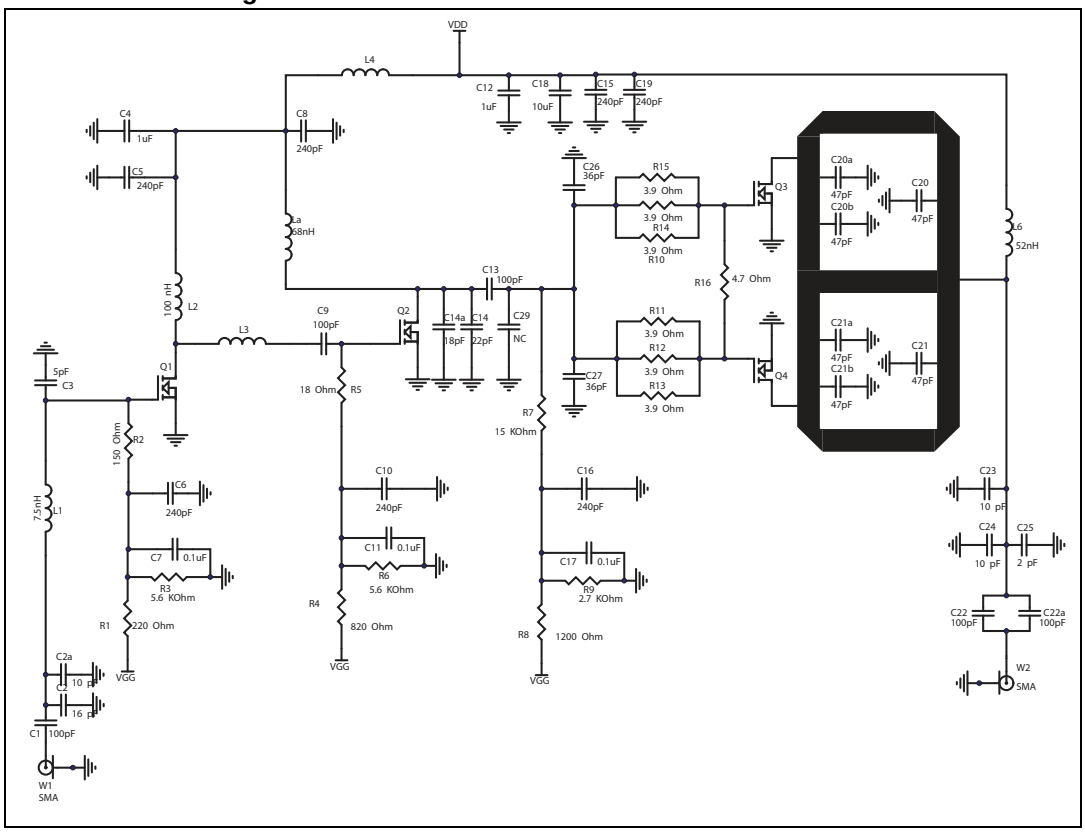


Table 3. BOM for STEVAL-TDR034V1

Designator	Manufacturer	Qty.	Value	Part number	Footprint
C1, C9	Murata	2	100 pF	GRM1555C1H101JA01	0402
C2	Murata	1	16 pF	GJM1555C1H160GB01#	0402
C2a	Murata	1	10 pF	GJM1555C1H100JZ01#	0402
C3	Murata	1	5 pF	GRM1555C1H5R0GA01#	0402
C4	Murata	1	1 µF	GRM188R61E105KA12#	0603
C5, C6, C8, C10, C15, C16, C19	Murata	7	240 pF	GRM1555C1H241JA01#	0402
C7, C11, C17	Murata	3	0.1 µF	GRM155C81E104KA12#	0402
C12	Murata	1	1 µF	GRM188B31E105KA75#	0603
C13	Murata	2	100 pF	GQM1885C1H101GB01#	0603
C22, C22a	Murata	2	100 pF	GQM2195C1H101JB01#	0805
C14	Murata	1	27 pF	GRM1555C1H270FA01#	0402
C14a	Murata	1	18 pF	GRM1555C1H180JZ01#	0402
C18	Murata	1	10 µF	GRM32ER71H106KA12#	1210
C20, C20a, C21, C21a, C21b	Murata	6	47 pF	GQM1875C2E470GB12#	0603

Table 3. BOM for STEVAL-TDR034V1 (continued)

Designator	Manufacturer	Qty.	Value	Part number	Footprint
C23, C24	Murata	2	10 pF	GQM1875C2E100GB12#	0603
C25	Murata	1	2 pF	GCM1885C2A2R0CB01#	0603
C26, C27	Murata	2	36 pF	GRM1555C1H360GA01#	0603
C29	Murata	1	NC		
L1	Coilcraft	1	7.5 nH	0402CS-7N5XJLW	0402
L2	Coilcraft	1	100 nH	0603HP-R10X_LU	0603
L6	Coilcraft	1	52 nH	NA5778-AE	
La	Coilcraft	1	68 nH	1008HQ-68NX_LC	0402
Q1	ST	1	SOT89	PD84002	SOT89
Q2	ST	1	PowerFLAT™	PD85006L	PowerFLAT™
Q3, Q4	ST	2	PSO-10	PD85050S	PSO-10
R1	Vishay	1	220 Ω	CRCW0402220RFKED	0402
R2	Vishay	1	150 Ω	CRCW0402150RFKED	0402
R3, R6	Vishay	2	5.6 KΩ	CRCW04025K60FKED	0402
R4	Vishay	1	820 Ω	CRCW1206820RFKEA	1206
R5	Vishay	1	18 Ω	CRCW040218R0FKED	0402
R7	Vishay	1	15 KΩ	CRCW040215K0FKED	0402
R8	Vishay	1	1200 Ω	CRCW12061K20FKEA	1206
R9	Vishay	1	2.7 KΩ	CRCW04022K7CEED	0402
R10, R11, R12, R13, R14, R15	KOA Speer	6	3.9 Ω	RK73H1JTTD3R90F	0603
R16	Vishay	1	4.7 Ω	CRCW06034R70FKEA	0603
Substrate			FR-4	20 mils 1oz copper	

Table 4. Test board

Designator	Manufacturer	Qty.	Value	Part number	Footprint
C1, C2		2	100 pF		Tantalum
C3, C4	Murata	2	10 µF	GRM42-6X7R225K25D52K	0402
C5, C6	Murata	2	2.2 µF	GRM42-6X5R106K25D539	0603
Substrate			FR-4	20 mils 1 oz copper	

5 Conclusion

In this application note, a design procedure and some practical solutions to build a multistage power amplifier were described.

The intent was to offer a low-cost and reliable way to design and produce customizable amplifiers.

The STEVAL-TDR031V1 and STEVAL-TDR034V1 were designed with plastic-packaged LDMOS devices, resulting in amplifiers with a high moisture sensitivity level typically not achievable with similar modules using chip-on-board technology.

STMicroelectronics can provide all the LDMOS devices presented in this application note, as well as any necessary technical support to revise the layout (gerber files) for system integration and/or components for cost reduction (BOM optimization).

Standard design support includes: device models, PCB gerbers, BOM and demonstration board. For further information, please visit www.st.com/rf.

6 References

1. Cripps, S. C., RF power amplifiers for wireless communications, Norwood, MA: Artech House, 1999.
2. Andrei Grebennikov, RF and microwave power amplifier design, McGraw Hill,2005.

7 Revision history

Table 5. Document revision history

Date	Revision	Changes
25-Jul-2013	1	Initial release.