AN4339
Application note

BLDC motor based ceiling fan solution proposal

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Introduction

Due to recent directives by the “Bureau of Energy Efficiency” (BEE) to reduce power consumption of consumer loads, it is necessary to analyze energy consumption by each of the house hold loads and implement how the energy can be saved in running such equipment. Some of the major loads that fall under this category are like lighting loads, refrigerators, air-conditioners, fans, televisions, audio equipment and so on. There are developments going on in different segments meet the desired energy saving norms. The fan is one of the major contribution in house hold as well as industrial usages. Currently fans build up with an AC induction motor which is approximately 60 - 70 W power rated. These motors are heavier and less efficient, not more than 50% of overall efficiency.

In the near future these motors will be phased out and instead a BLDC (brushless DC motor) is going to be introduced in fan application. In a practical scenario it is seen that a 40 - 50% lesser power rated motor can provide the same amount of air flow output. That means that the approximately 30 W BLDC based fan system will replace existing 60 - 70 W power consumption with the AC induction motor. This is a huge power saving. Moreover the BLDC motor are much lighter as compared to the heavy AC induction motor.

In this application note the proposed scheme to drive a BLDC fan motor is described. Usually the low voltage DC motor is well suited for this application, mainly a 24 V BLDC motor. The system requires mainly 2 sections: a front-end AC/DC power supply for the universal range followed by a 3-phase bridge inverter to drive a motor. The power supply has to be galvanic isolated having high efficiency, high PF and low THD. For the same the design of single stage high power factor flyback topology using the STMicroelectronics® innovative PFC L6564 controller is considered. The L6564 device is a current mode PFC controller operating in transition mode (TM). The highly linear multiplier, along with a special correction circuit that reduces crossover distortion of the mains current, allows wide range mains operation with an extremely low THD even over a large load range. This topology gives high power factor but on the other hand when operated in high PF configuration significant magnitude of twice of mains frequency ripple at output DC voltage because of no electrolytic capacitor after bridge rectification. But in our application, this will not impact the performance of the second stage driving motor.

Coming to the BLDC driver section i. e. second stage of this scheme (see *Figure 1*), we propose the ST's 3-phase brushless DC motor driver - L6235. The L6235 device is a highly integrated, mixed-signal power IC that allows to easily design a complete motor control system for a BLDC motor, specially for low power small motors. The IC integrates six power DMOS, a centralized logic circuit to decode Hall effect sensors and a constant t_{OFF} PWM current control technique (synchronous mode) plus other added features for safe operation and flexibility.

The typical BLDC motor power requirement is 24 V/1 A maximum including losses inside the driver stage and motor. This requires 24 W power supply to run the motor driving stage. Assuming efficiency of power supply as 85% over an universal voltage range, the power supply requires maximum input power somewhere around 28 W.

Contents

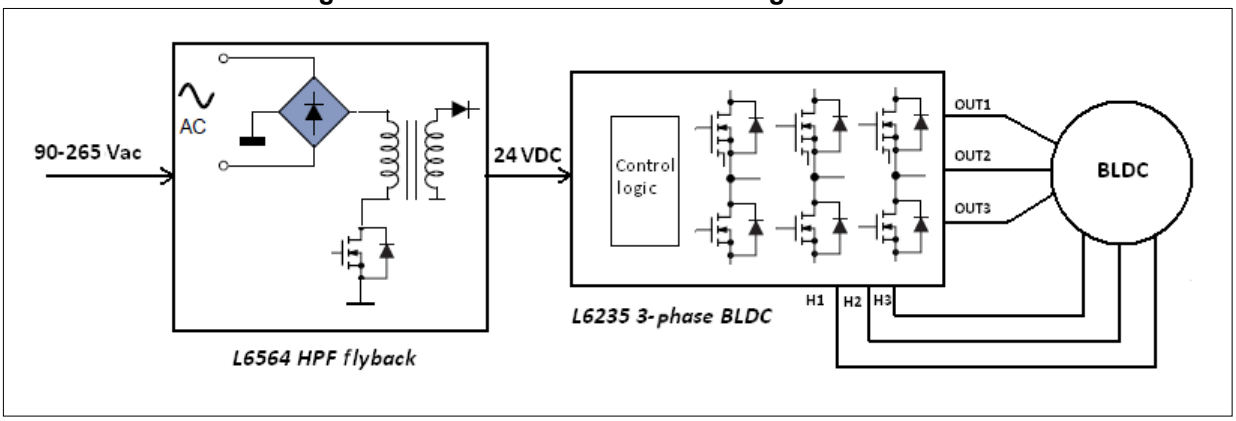
1 Description

1.1 BLDC fan solution block diagram

The solution comprises of 2 stages:

- 30 W power supply operating on universal mains range using the L6564 device
- BLDC driver stage using the L6235 device

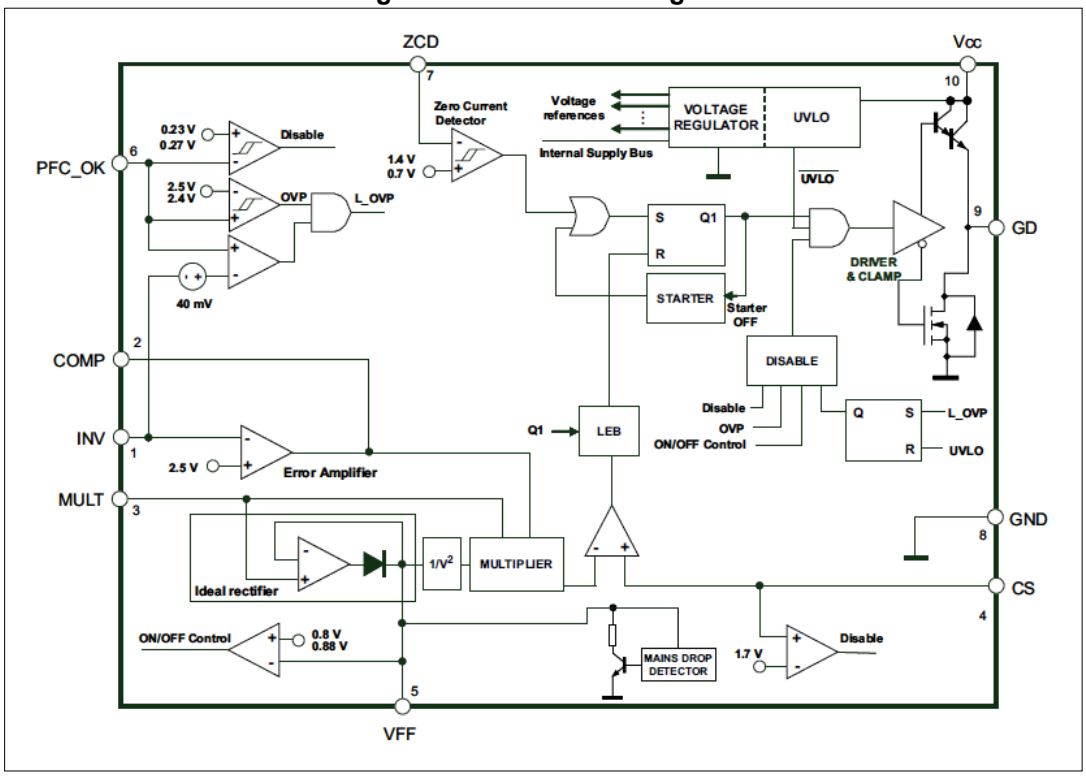
Figure 1. BLDC fan solution block diagram scheme



1.2 Power supply section - L6564 block

The power supply is designed using the PFC controller L6564 which works in transition mode of control in flyback isolated topology.

Figure 2. L6564 block diagram



Some of the important features of the L6564 device are shown below.

L6564 features

- Fast “bidirectional” input voltage feed-forward (1/V2 correction)
- Accurate adjustable output overvoltage protection
- Protection against feedback loop disconnection (latched shutdown)
- Inductor saturation protection
- AC brownout detection
- Low (≤ 100 µA) start-up current
- 6 mA max. operating bias current
- 1% (at T_J = 25 °C) internal reference voltage
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SSOP10 package

1.3 Description of power supply

The main feature of this converter is that the input current is almost in phase with the mains voltage, therefore the power factor is close to unity and hence low current harmonics. This is achieved by the L6564 TM PFC controller, which shapes the input current as a sine wave in phase with the mains voltage. The power supply utilizes a typical flyback converter topology, using a transformer to provide the required insulation between the primary and secondary side. The converter is connected after the mains rectifier and the capacitor filter, which in this case is quite small to avoid damage to the shape of the input current. The flyback switch is represented by the Power MOSFET M1, and driven by the L6564 device.

At startup, the L6564 device is powered by the V_{CC} capacitor (C_{14}), which is charged via resistors R_3 and R_9. As the capacitor C_{14} charges to turn on threshold of the L6564 device (typically at 12 V), the transformer T1 auxiliary winding (pins 5 - 6) generates the V_{CC} voltage, rectified by the D_7 and R_{12}, that powers the L6564 during normal operation. The R_{11} is also connected to the auxiliary winding to provide the transformer demagnetization signal to the L6564 ZCD pin, turning on the MOSFET at any switching cycle. The MOSFET used is the STP4N80K5, a standard, low cost 800 V device housed in a TO-220 package, and needing only a small heatsink. The transformer is layer type, using a standard ferrite size EF25. The flyback reflected voltage is close to 170 V, providing enough room for the leakage inductance voltage spike still within the reliability margin of the MOSFET even at 300 VAC input.

The RCD snubber circuit using the R_4, C_5 and D_6 clamps the peak of the leakage inductance voltage spike at the MOSFET turn-off. The resistor R_2 is usually inserted in series with a subbing capacitor C_5 to kill the spike and reduces further the EMI generated due to leakage spikes. The resistors R_{31} and R_{32} sense the current flowing into the transformer primary side. Once the signal at the current sense pin has reached the level programmed by the internal multiplier of the L6564, the MOSFET turns off. The divider R_7, R_{10}, R_{13} and R_{21} provides to the L6564 multiplier pin with instantaneous voltage information which is used to modulate the current flowing into the transformer primary side. The C_{16} is a small noise suppression capacitor, of course the purpose of this capacitor is not to disturb the actual sinusoidal mains information.

The output regulation is done by means of an isolated voltage loop by the optocoupler U2, and using an inexpensive TL431 device to drive the optocoupler. The opto-transistor modulates the input voltage of the L6564 internal amplifier, thus closing the voltage loop. The output rectifier is a Schottky rectifier, selected according to its maximum reverse voltage, forward voltage drop and power dissipation. A small LC filter is added on the output, filtering the high frequency ripple.

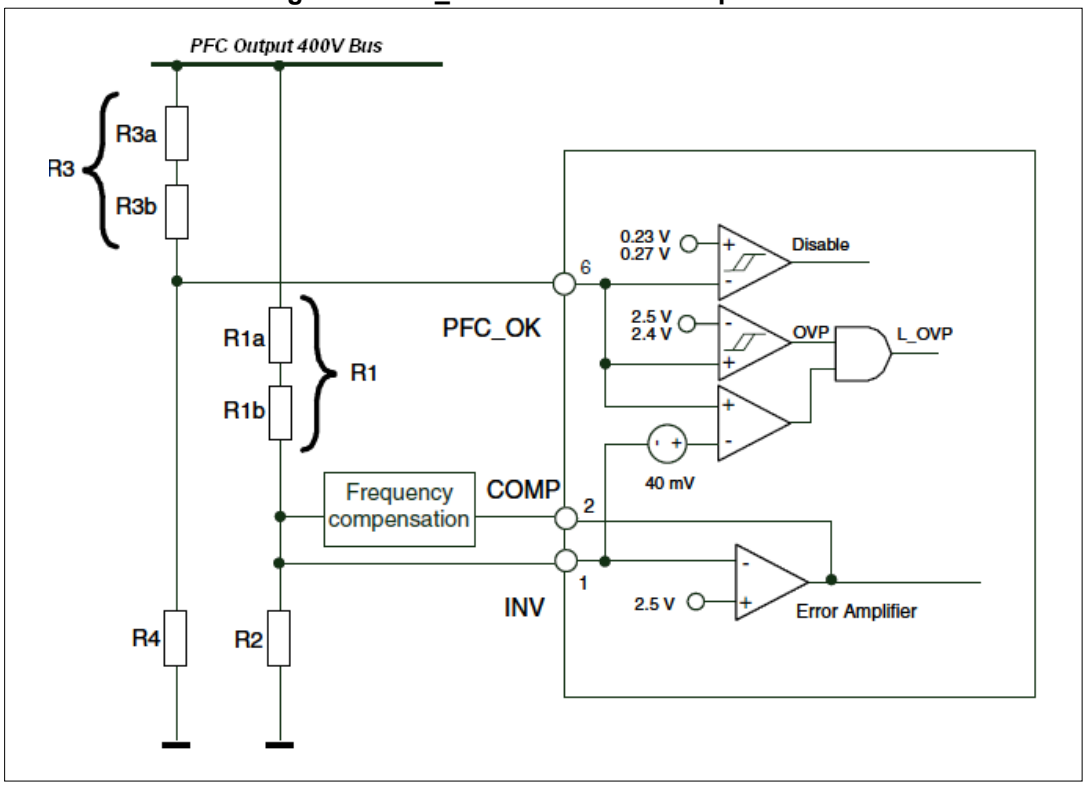
1.3.1 PFC_OK

PFC_OK function in PFC operation

PFC pre-regulator output voltage monitoring/disable function

This pin senses the output voltage of the PFC pre-regulator through a resistor divider and is used for protection purposes. If the voltage on the pin exceeds 2.5 V the IC stops switching and restarts as the voltage on the pin falls below 2.4 V. However, if the voltage of the INV pin falls 40 mV below that of the pin PFC_OK, a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling V_{CC}, bringing its value lower than 6 V before to move up to turn on threshold. If the voltage on this pin is brought below 0.23 V the IC is shut down. To restart the IC the voltage on the pin must go above 0.27 V. This can also be used as a remote on/off control input. Refer to *Figure 3: PFC_OK function in PFC operation*, the R_3 and R_4 composes the network to activate PFC output overvoltage shutdown.

Figure 3. PFC_OK function in PFC operation

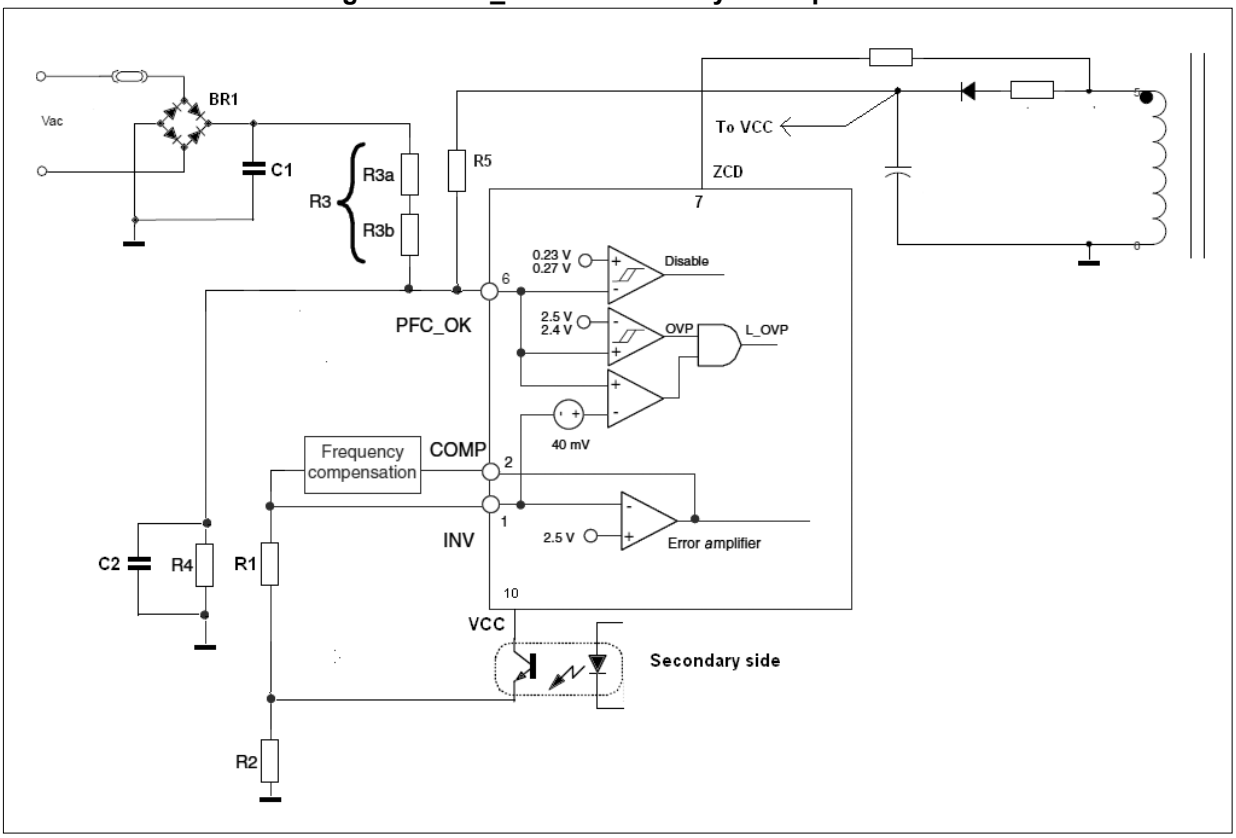


PFC_OK function in flyback operation

The same pin can also be used in case of flyback converter to shutdown the converter either in case of input overvoltage or output overvoltage. For input overvoltage protection, the pin one can be biased using the resistor divider network at rectified DC voltage to activate input overvoltage protection at the required mains OVP level. Referring to the circuit portion below, R_3, R_4 composes the network to activate mains overvoltage shutdown, where small capacitor C_2 is used to average the DC value of sensing voltage at the PFC_OK pin. In the schematic in *Figure 10 on page 18* the biasing components R_1, R_6, R_8 and R_{19} comprises the input OVP detection circuit. The divider ratio is selected to provide 2.5 V at required mains OVP level.

If output overvoltage protection is preferred instead of mains OVP, we can utilize the auxiliary winding output, which is used to provide the operating voltage to the controller as well as demagnetization input to ZCD. Since we get the reflection of output voltage at auxiliary output supply so we can simply tap the signal for PFC_OK which is programmed to 2.5 V using resistor divider network at desired output OVP. This is achieved using the resistor divider network R_4 and R_5 at auxiliary output supply in *Figure 4*. In our circuit we have implemented input OVP protection network to bias PFC_OK. So the R_{14} in the schematic is kept open.

Figure 4. PFC_OK function in flyback operation

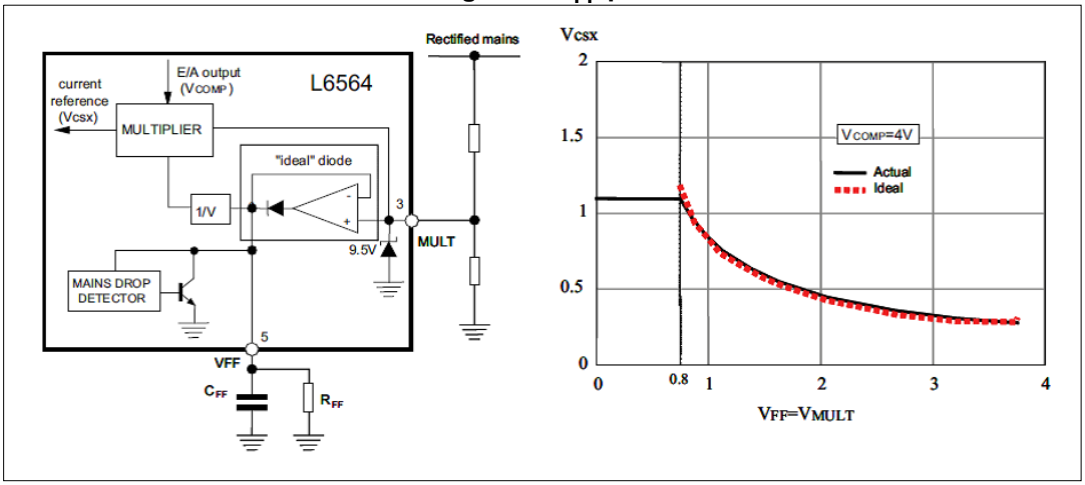


1.3.2 V_{FF} (feed-forward function) and brownout protection

This is second input to the multiplier block for $1/V^2$ function. A capacitor and a parallel resistor must be connected from this pin to GND. They complete the internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage at this pin, a DC level equal to the peak voltage on the pin MULT (pin 3), compensates the control loop gain dependence on the mains voltage. The variation of internal current reference signal V_{CSX} versus the mains voltage level detected at MULT input ($V_{FF} = V_{MULT}$) is shown in the graph in *Figure 5*. This is the ultimate signal which is compared with the error signal to output the required gate signal ON time. Never connect the pin directly to GND but with a resistor ranging from 100 KΩ (minimum) to 2 MΩ (maximum). This pin is internally connected to a comparator in order to provide brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The IC restarts as the voltage at this pin goes above 0.88 V.

This is one of the important features of the L6564 device where we can manage the overload condition and it prevents excessive current to flow through the input section at worst low mains operating condition. So as the mains voltage drops below a programmed level, the IC stops as V_{FF} pin detects the brownout level.

Figure 5. V_{FF} pin



1.3.3 Power supply basic specifications

Table 1. SMPS basic specifications

Parameters	Limits
Rated input voltage range	90 - 265 VAC
Operating input voltage range	90 - 280 VAC
Input overvoltage shutdown	> 280 VAC
Input supply frequency (f_L)	47 - 63 Hz
Input / output isolation	Yes, > 2.7 KV
Power factor correction	Yes, > 0.9
THD	As per IEC61000-3-2
Nominal output voltage	24 V+/-1 V
Load current	1 A
Total output power	24 W
Efficiency (full load for wide mains variations)	> 85%
Output voltage pk-pk ripple (2.fL)	< 20%
Topology	Single stage HPF flyback
Maximum ambient temperature	45 °C

1.3.4 Calculations

Min. AC input, Vacmin = 90 VAC
Max. AC input, Vacmax = 265 VAC
Output DC voltage, V_{OUT} = 24 VDC
Load current, I_{OUT} = 1 A
Overall efficiency, η = 0.87
Output voltage 2fL ripple = 2 Vpk-pk
Reflected voltage, V_{OR} = 170 V
Minimum switching frequency, fswmin = 40 KHz

Min. DC voltage:

Equation 1

$$Vpkmin = \sqrt{2}.Vacmin - Vdson$$

$$Vpkmin = 123\ V \text{ (taking } Vdson = 4\ V)$$

Max. DC voltage:

Equation 2

$$Vpkmax = \sqrt{2}.Vacmax - Vdson$$

$$Vpkmax = 370\ V$$

Input power:

Equation 3

$$P_{IN} = P_{OUT}/\eta$$

$$P_{IN} = 27.6\ W$$

Peak to reflected voltage:

Equation 4

$$Kv = Vpkmin/VR$$

$$Kv = 0.723$$

Flyback characteristic functions are:

Equation 5

$$F1(Kv) = \frac{0.637 + 4.6 \bullet 10^{-3} \bullet Kv}{1 + 0.729 \bullet Kv}$$

$$F1(Kv) = 0.42$$

Equation 6

$$F2(Kv) = \frac{0.5 + 1.4 \bullet 10^{-3} \bullet Kv}{1 + 0.815 \bullet Kv}$$

$$F2(Kv) = 0.315$$

Equation 7

$$F3(Kv) = \frac{0.424 + 5.7 \bullet 10^{-4} \bullet Kv}{1 + 0.862 \bullet Kv}$$

$$F3\ (Kv) = 0.26$$

Peak primary current:

Equation 8

$$Ipkp = \frac{2 \bullet pin}{Vpkmin \bullet F2(Kv)}$$

$$Ipkp = 1.42\ A$$

RMS primary current:

Equation 9

$$Irmsp = Ipkp \bullet \sqrt{\frac{F2(Kv)}{3}}$$

$$Irmsp = 0.46\ A$$

Peak secondary current:

Equation 10

$$Ipks = \frac{2 \bullet Iout}{Kv \bullet F2(Kv)}$$

$$Ipks = 8.8\ A$$

RMS secondary current:

Equation 11

$$Irmss = Ipks \bullet \sqrt{\frac{Kv \bullet F3(Kv)}{3}}$$

$$Irsms = 2.2\ A$$

1.3.5 Multiplier setting

Equation 12

$$\text{Select} \quad V_{multpkmax} = 2.65\ V$$

$$V_{multpkmin} = V_{multpkmiax} \bullet \frac{V_{pkmin}}{V_{pkmax}}$$

$$V_{multpkmin} = 0.88\ V$$

Resistor divider ratio:

Equation 13

$$K_p = \frac{V_{multpkmax}}{V_{pkmax}}$$

$$K_p = 7.17\ E - 03$$

$$\text{Let} \quad R_{multL} = 47\ K\Omega$$

Equation 14

$$\text{So} \quad R_{multH} = R_{multL}/K_p$$

$$R_{multH} = 6555\ K\Omega$$

$$\text{Select} \quad R_{multH} = 6600\ K\Omega$$

Actual divider ratio:

Equation 15

$$K_p = 7.12\ E - 03$$

Rsense calculation:

Equation 16

$$V_{cxpk} = 1.33 \bullet V_{multpkmin}$$

(As per the L6564 datasheet, MULT setting).

Equation 17

$$V_{cxpk} = 1.17\ V$$

Considering the saturation current of primary = 20% higher of maximum peak current at 90 VAC.

Equation 18

$$I_{pkp\_s} = 1.7\ A$$

$$R = \frac{V_{cxpk}}{I_{pkp\_s}}$$

$$R_{cs} = 0.68\ E$$

1.3.6 Transformer design

Primary inductance value is calculated by *Equation 19*:

Equation 19

$$L_p = \frac{V_{pkmin} \bullet 10^3}{(1 + Kv) \bullet f_{swmin} \bullet I_{pkp}}$$

$$Lp = 1.25\ mH$$

Select $Lp = 1\ mH$

Primary to secondary turn ratio:

Equation 20

$$n = \frac{V_{or}}{V_{OUT} + VF}$$

$$n = 6.911$$

Primary number of turns:

Equation 21

$$N_p = \frac{L_p \bullet 10^{-3} \bullet I_{pkp}}{B_{max} \bullet A_e \bullet 10^{-4}}$$

Considering max flux density:

$$Bmax = 0.3\ T$$

Select core EE25 (After calculating the minimum area product required, not described in this section).

Cross sectional area:

Equation 22

$$Ae = 0.52\ cm^2$$

Primary number of turns:

Equation 23

$$Np = 91$$

Select $Np = 90\ T$

Secondary number of turns:

Equation 24

$$Ns = Np/n$$

$$Ns = 13\ T$$

Aux. voltage required: $V_{aux} = 15\ V$

Number of turns required for auxiliary winding:

Equation 25

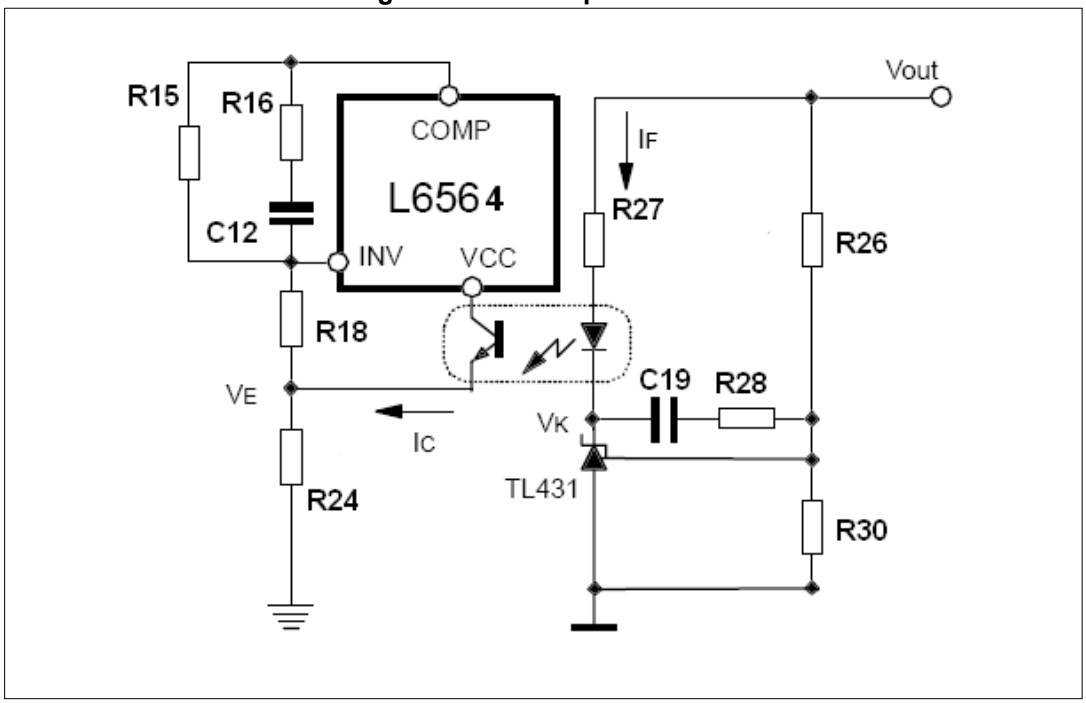
$$N_{aux} = \frac{V_{aux} \bullet N_s}{V_{out}}$$

Naux = 8 T

1.3.7 Control loop design

The error amplifier block is shown in *Figure 6*:

Figure 6. Error amplifier block



Error amplifier transfer function is:

Equation 26

$$G1(s) = \frac{-R15}{R18} \bullet \frac{\left(1 + \frac{\frac{s}{1}}{C12 \bullet R16}\right)}{\left[1 + \frac{\frac{s}{1}}{C12 \bullet (R15 + R16)}\right]}$$

Poles and zero from error amplifier transfer function are:

Equation 27

$$fz1 = \frac{1}{2 \bullet \pi \bullet C12 \bullet R16}$$

$$fp1 = \frac{1}{2 \bullet \pi \bullet C12 \bullet (R15 + R16)}$$

Transfer function of feedback loop is:

Equation 28

$$H(s) = \frac{1}{R27} \bullet \frac{R18 \bullet R24}{R18 + R24} CTR_{min} \bullet \frac{\left[1 + \frac{\frac{s}{1}}{C19 \bullet (R28 + R26)}\right]}{\left(\frac{\frac{s}{1}}{R26 \bullet C19}\right)}$$

Where CTRmin = 0.5 - minimum current transfer ratio of optocoupler in feedback loop.

Poles and zero of above transfer function are:

Equation 29

$$fp2 = \frac{1}{2 \bullet \pi \bullet R26 \bullet C19}$$

$$fz2 = \frac{1}{2 \bullet \pi \bullet C19 \bullet (R28 + R26)}$$

Selecting R_{15} = 47 KΩ, R_{26} = 47 KΩ, R_{28} = 4.7 KΩ, C_{19} = 1 µF, C_{12} = 22 nF; the open loop cross over frequency is 13 Hz and desired phase margin is 40°.

Figure 7. Open loop overall transfer function

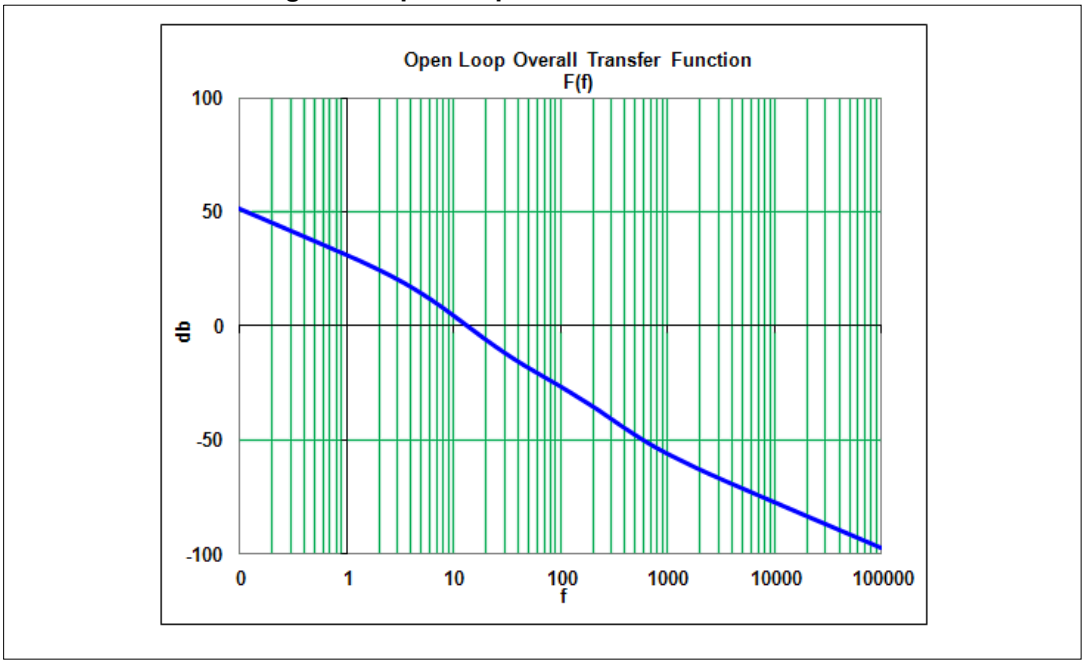
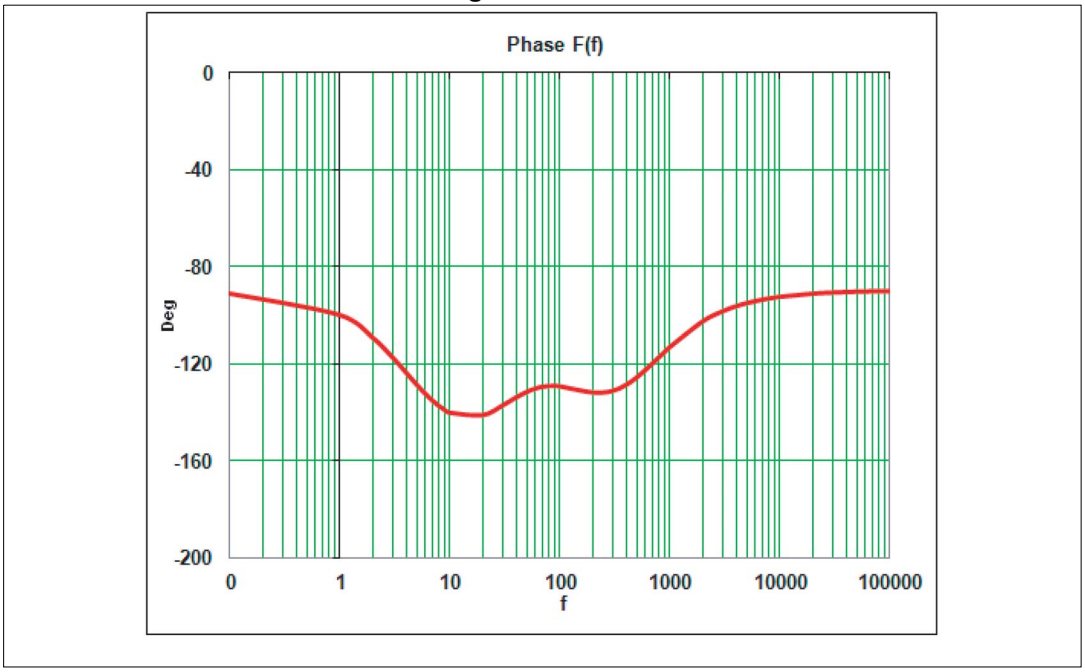


Figure 8. Phase



1.3.8 Transformer specification

Table 2. Transformer specification

Max. output power	Max. 28 W (typ. operating power is 24 W)
Input voltage range	90 - 280 VAC
Primary inductance	1.0 ± 0.1 mH at 50 KHz
Primary side leakage inductance	< 3 μH at 50 KHz
Peak primary current	1.42 A
Saturation current	1.8 A
RMS primary current	0.46 A
Peak secondary current	8.8 A
RMS secondary current	2.2 A
Minimum switching frequency	40 KHz
Core size	E25/13/7
Ferrite material	N87, EPCOS
Bobbin	12 pins horizontal
Dielectric strength	> 2.7 KV

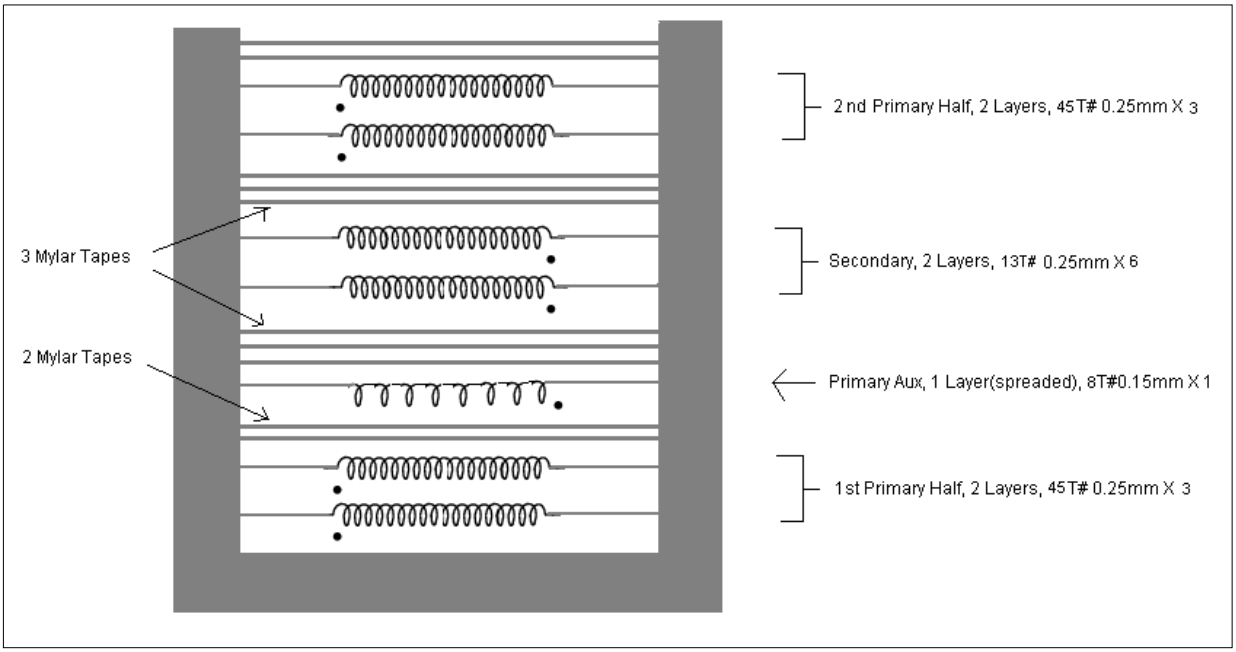
1.3.9 Winding details

Table 3. Winding details

Winding name	Start	Stop	No. of turns	Wire gauge	Order of windings
Np1	3	2	45	3 x 0.25 mm	Bottom
Naux	5	6	8	1 x 0.15 mm	Above Np1
Nsec	12, 11	10, 9	13	6 x 0.25 mm	Above Naux
Np2	2	1	45	3 x 0.25 mm	Topmost

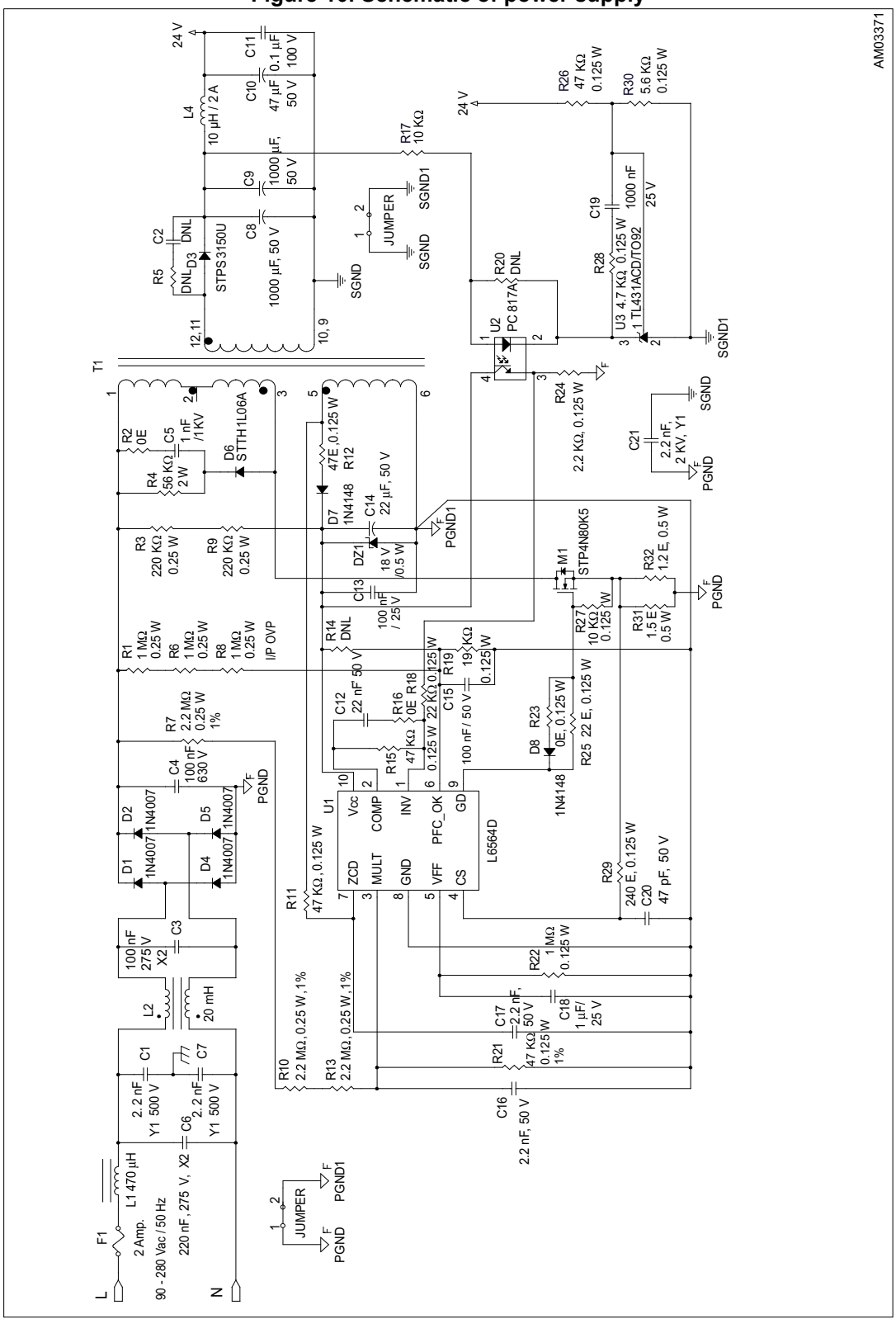
1.3.10 Transformer construction

Figure 9. Transformer construction



1.3.11 Schematic of power supply

Figure 10. Schematic of power supply



1.4 BLDC motor driver - L6235 details

Motor specifications are

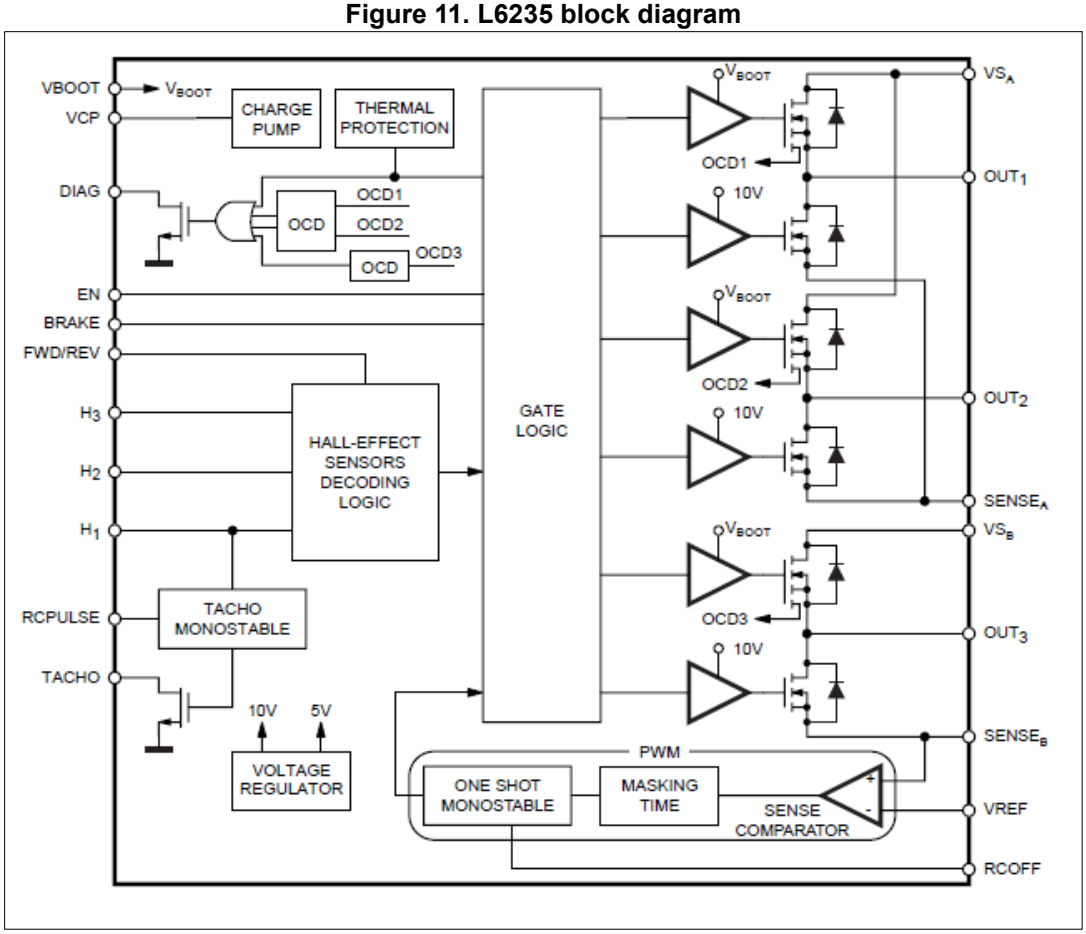
- 3-phase BLDC motor
- DC input voltage: 24 V
- Typical operating current: 1 A
- 3 Hall sensor detection method

To drive the BLDC motor with Hall effect sensors incorporated, the L6235 device is used. The L6235 device is a DMOS fully integrated 3-phase motor driver with overcurrent protection. The device combines isolated DMOS power transistors with CMOS and bipolar circuits on the same chip. The device includes all the circuitry needed to drive a 3-phase BLDC motor including: a 3-phase DMOS bridge, a constant off time PWM current controller and the decoding logic for single ended Hall sensors that generates the required sequence for the power stage. The L6235 device features a non-dissipative overcurrent protection on the high side Power MOSFETs and thermal shutdown. Some of the important features of the driver are listed below:

- Operating supply voltage from 8 to 52 V
- 5.6 A output peak current (2.8 ADC)
- $R_{ds(on)}$ 0.3 W typ. value at T_J = 25 °C
- Operating frequency up to 100 KHz
- Non dissipative overcurrent, detection and protection
- Diagnostic output
- Constant T_{OFF} PWM current controller
- Slow decay synchronous. rectification
- 60° and 120° Hall effect decoding logic
- Brake function
- TACHO output for speed loop
- Cross conduction protection
- Thermal shutdown
- Undervoltage lockout
- Integrated fast freewheeling diodes

1.4.1 L6235 block diagram

Figure 11. L6235 block diagram



The detail description of some of the pins of driver is given in *Section 1.4.2* to *Section 1.4.10*.

1.4.2 $SENSE_A$ and $SENSE_B$

These are half bridge sections source pins. $SENSE_A$ and $SENSE_B$ pins have to be connected together and to power ground through a sensing power resistor. At the pin $SENSE_B$, the inverted pin of an internal sense comparator is connected.

1.4.3 Hall sensors inputs (H_1, H_2, and H_3)

These are Hall sensor inputs to controller to detect the position of motor. We need pull-up resistors connected at these pins to connect the Hall sensors inputs.

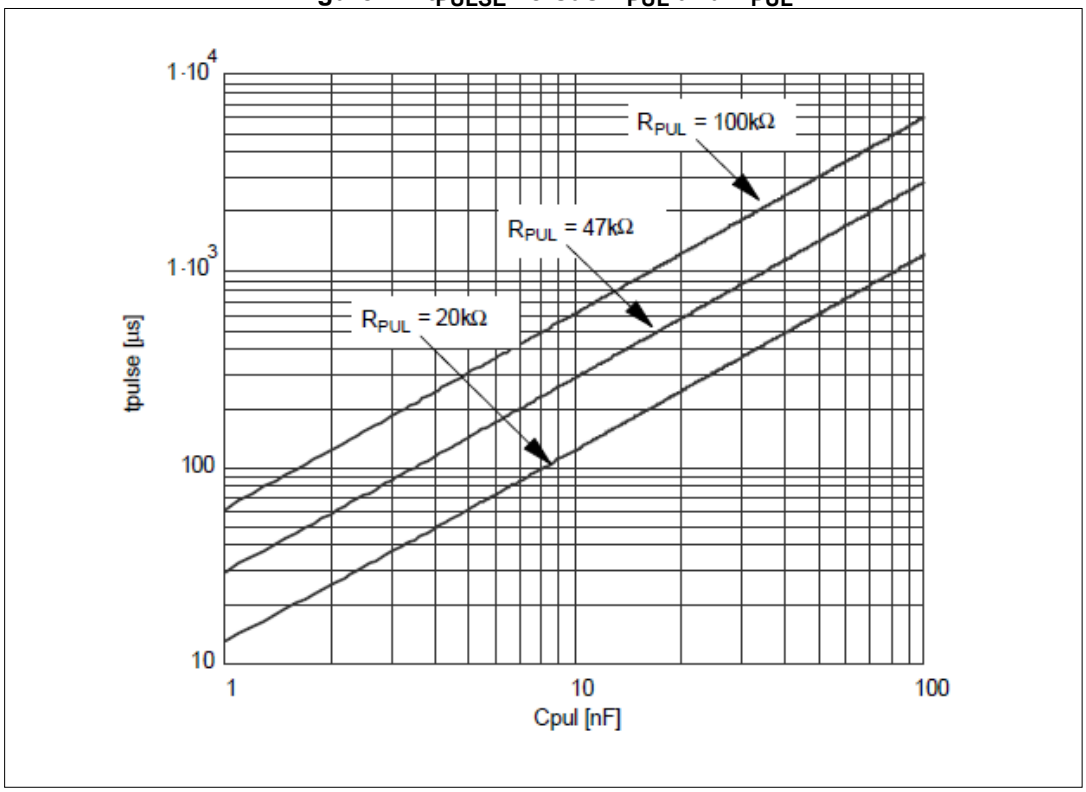
1.4.4 TACHO

It allows developing an easy speed control loop by using an external op-amp. This is an open drain output. At each rising edge of the Hall effect sensors H_1, the monostable is triggered and the MOSFET connected to the pin TACHO is turned off for a constant time t_{PULSE} (as shown in *Figure 12*). The off time t_{PULSE} can be set using the external RC network (R_{PUL}, C_{PUL}) connected to the pin RCPULSE. *Figure 12* gives the relation between t_{PULSE} and C_{PUL}, R_{PUL}. We have approximately:

Equation 30

$$t_{PULSE} = 0.6 \cdot R_{PUL} \cdot C_{PUL}$$

Figure 12. t_{PULSE} versus C_{PUL} and R_{PUL}



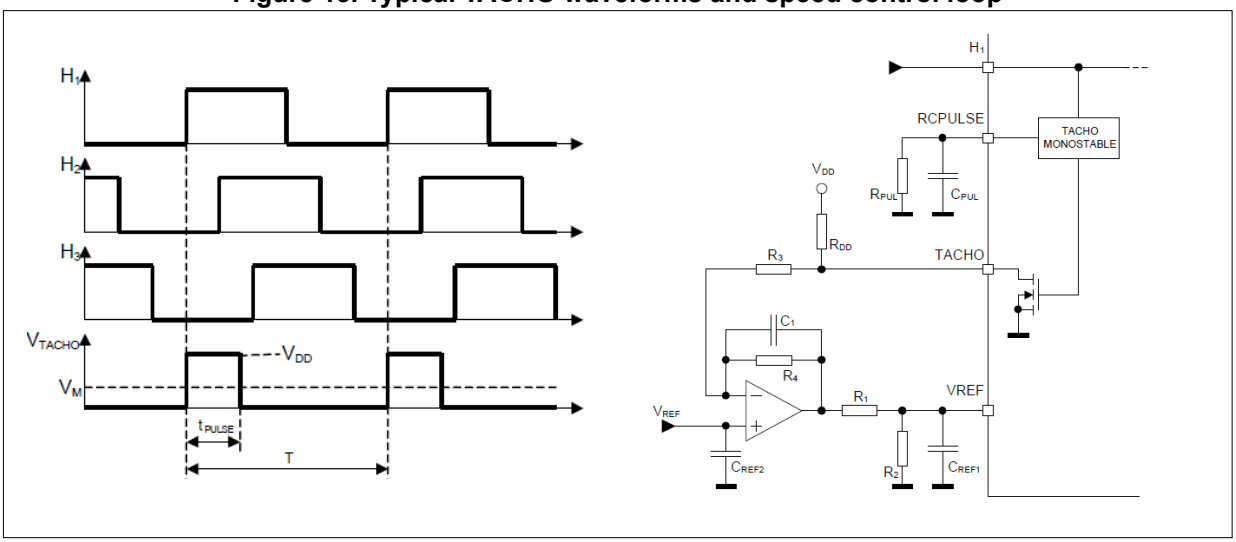
Where C_{PUL} should be chosen in the range of 1 nF to 100 nF and R_{PUL} in the range of 20 KΩ to 100 KΩ. By connecting the tachometer pin to an external pull-up resistor, the output signal average value V_M is proportional to the frequency of the Hall effect signal and, therefore, to the motor speed. This realizes a simple frequency-to-voltage converter. An op-amp, configured as an integrator, filters the signal and compares it with a reference voltage V_{REF}, which sets the speed of the motor. So we can also connect the non-inverting pin of op-amp by using a potentiometer at V_{REF} pin to vary the speed of motor.

Equation 31

$$V_M = \frac{t_{PULSE}}{T} \bullet V_{DD}$$

1.4.5 Typical TACHO waveforms and speed control loop

Figure 13. Typical TACHO waveforms and speed control loop



1.4.6 BRAKE function

Brake input pin. Low logic level switches on all high side Power MOSFETs, implementing the brake function. If not used, it has to be connected to +5 V.

1.4.7 FWD/REV functions

Input to forward and reverse function for the motor i.e to select the direction of the rotation. HIGH logic level sets forward operation, whereas LOW logic level sets reverse operation. If not used, it has to be connected to GND or +5 V.

1.4.8 Enable input (EN)

Chip enable input. LOW logic level switches OFF all Power MOSFETs. If not used, it has to be connected to +5 V.

1.4.9 RC_{PULSE}

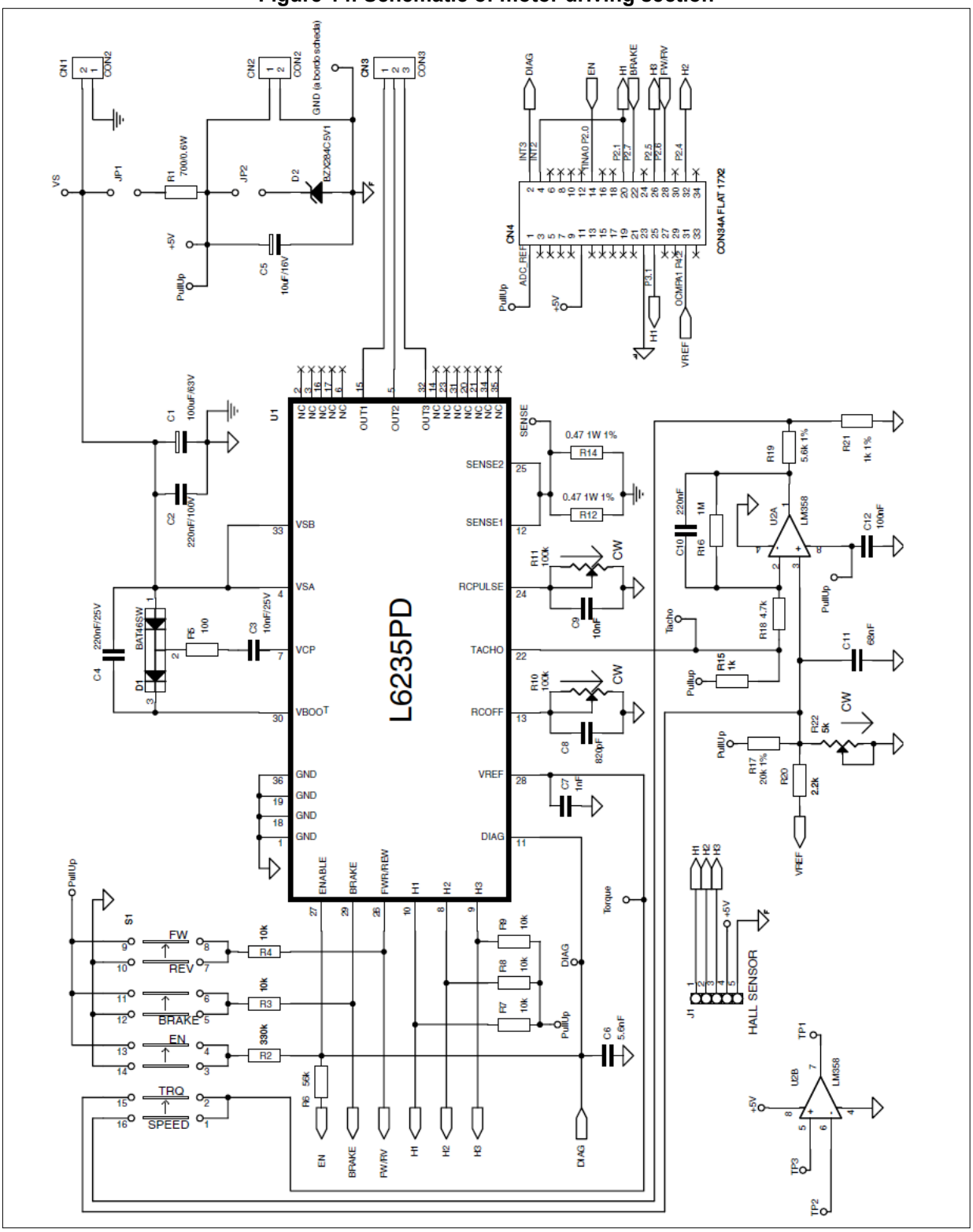
RC network pin. A parallel RC network connected between this pin and ground sets the duration of the monostable pulse used for the frequency-to-voltage converter.

1.4.10 RC_{OFF}

An external parallel RC network is connected to the RC_{OFF} to set the current controller off time.

1.4.11 Schematic of motor driving section

Figure 14. Schematic of motor driving section



1.4.12 Hall sensors

Following bipolar type Hall sensors can be used for this application:

- Part no: US2881
- Manufacturer: Melexis

Figure 15. Typical application schematic

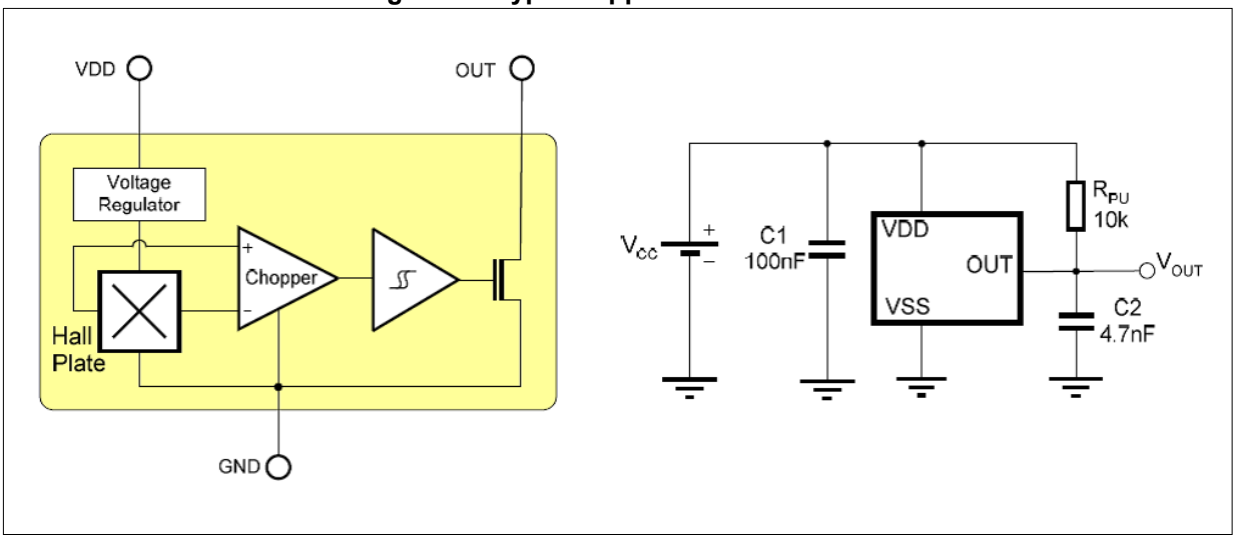


Table 4. Pin descriptions

SE pin no.	UA pin no.	Name	Type	Function
1	1	VDD	Supply	Supply voltage pin
2	3	OUT	Output	Open drain output pin
3	2	GND	Ground	Ground pin

Figure 16. SE and UA package

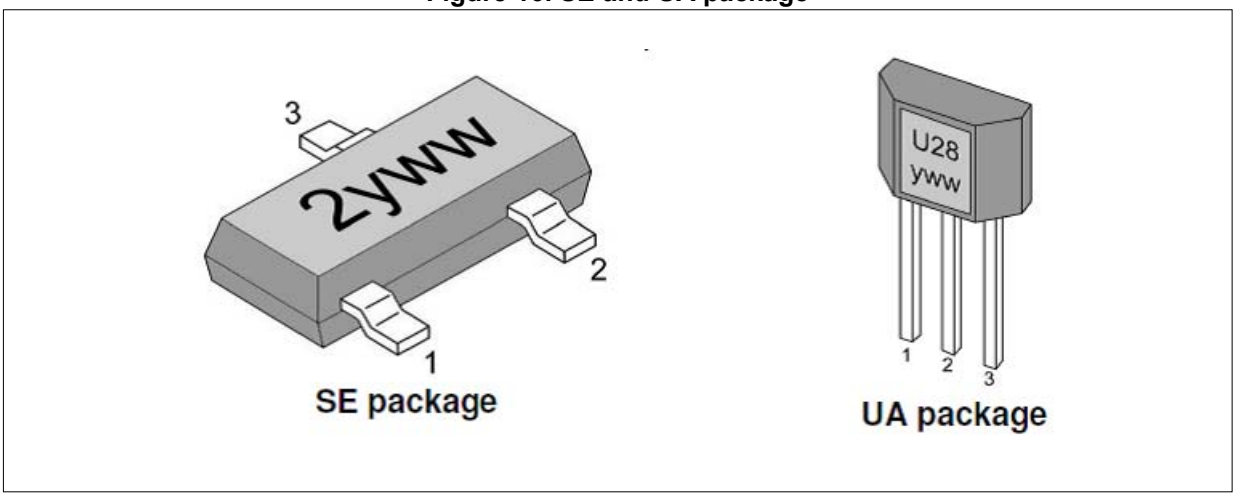


Table 5. Bill of material (ST parts only)

Part description	Quantity
PFC controller, L6564D	1
MOSFET, STP4N80K5	1
Rectifier STPS3150U	1
Rectifier STTH1L06A	1
3-phase BLDC driver, L6235PD	1
Operational amplifier, LM358	1

2 References

1. AN1059: Design equations of high-power-factor flyback converters based on the L6561.
2. L6564 datasheet: 10 pin transition-mode PFC controller.
3. L6235 datasheet: DMOS driver for three-phase brushless DC motor.
4. EVAL6235PD databrief.

3 Revision history

Table 6. Document revision history

Date	Revision	Changes
29-Nov-2013	1	Initial release.