AN4374
Application note

The LED1642GW and ALED1642GW start-up guide

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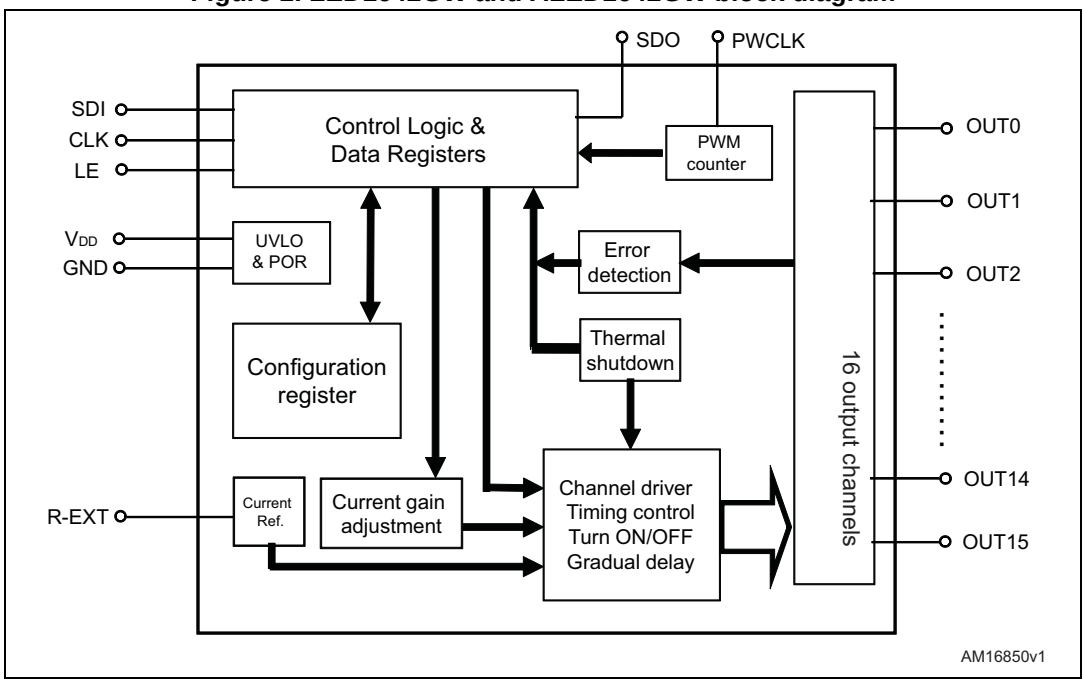
Introduction

The use of LEDs in applications like displays, information and advertising panels, signs, traffic signals, automotive lighting and architectural lighting is becoming more and more popular. The LED array drivers, with accurate constant current regulation and embedded serial interface, are the solution suitable for the above mentioned applications. This document provides an overview about the LED1642GW LED array driver and the ALED1642GW (automotive grade version). The first part of this document is focused on the device startup, as well as the main communication key explanation for an easy use of this product. The last part of this document gives some general guidelines relative to the application dimensioning and the PCB design.

Figure 1. LED1642GW and ALED1642GW block diagram



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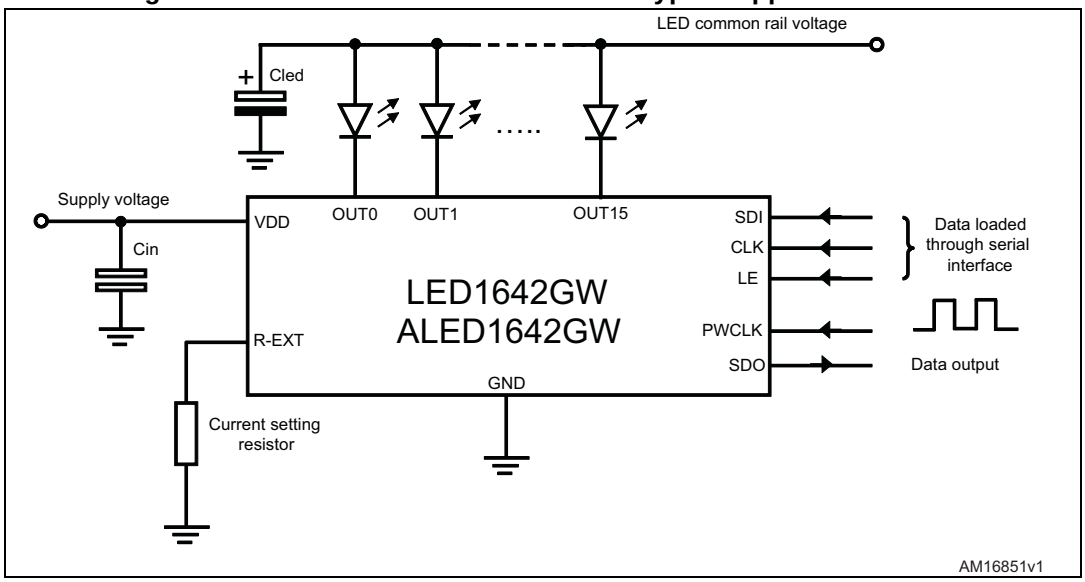
1 The LED1642GW and ALED1642GW basic circuit

The below figure shows the LED1642GW and ALED1642GW basic application schematic:

Figure 2. LED1642GW and ALED1642GW typical application circuit



we can use C_{in} =1 uF, C_{LED} = 47 uF, V_{LED}= 5V, V_{DD} = 3.3V, R_{EXT} =11 K and on PWCLK pin a continuous square wave (0 to 3.3 V) with 50% duty cycle and a frequency of about 8 MHz have to be applied. Starting from these conditions, a correct pattern sequence on SDI, CLK and LE pins (0 to 3.3 V with a CLK frequency for example of about 1 MHz) have to be provided so to obtain the LED power-on. The following examples refer to this circuit unless otherwise specified.

2 First LED power-on

There are, at least, three different registers to be managed:

- The configuration
- The brightness
- The switch

As first set-up, by using the default values, the configuration register can be neglected, while the brightness register and the switch register have to be managed in order to have the LED power-on.Therefore:

- The configuration register = default, no pattern needed for configuration register set-up.
- As far as the brightness register is concerned, a 16-bit value has to be sent for each of 16 outputs, 16x16 bit patterns (256 bits totally) are necessary; the first 15 have a data latch (LE high for 3 CLK rising edges), last pattern has a global latch (LE high for 5 CLK rising edges). 16x16 times SDI=1 have to be sent to program the maximum brightness.The below images shown exactly the elements of this protocol with a

brightness pattern (see*Table 1* and *Figure 3* and *Figure 4*).

Table 1. Digital key summary-data latch

Number	#CLK rising edge when the LE is 1	Command description
1	1-2	Write switch (to turn on/off output channels)
2	3-4	Brightness data latch
3	5-6	Brightness global latch
4	7	Write configuration register
5	8	Read configuration register
6	9	Start open error detection mode
7	10	Start short error detection mode
8	11	Start combined error detection mode
9	12	End error detection mode
10	13	Thermal error reading
11	14	Reserved
12	15	Reserved

Figure 3. Digital key summary chart-data latch

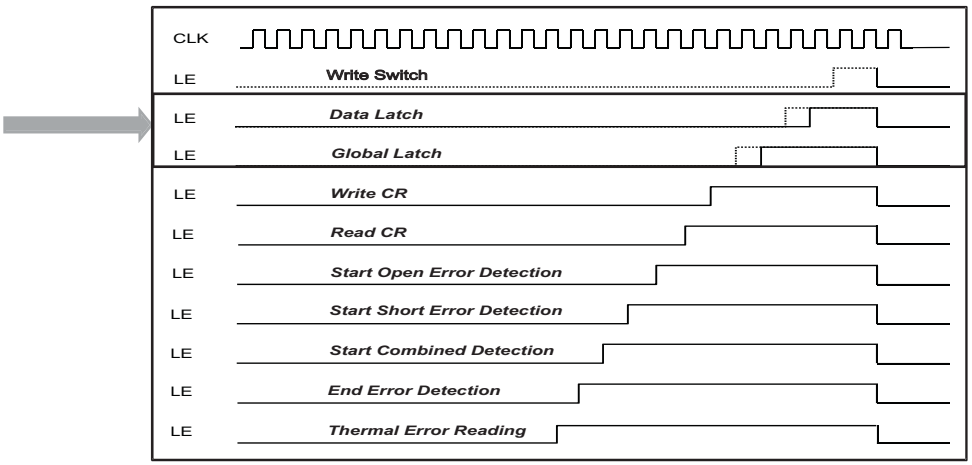
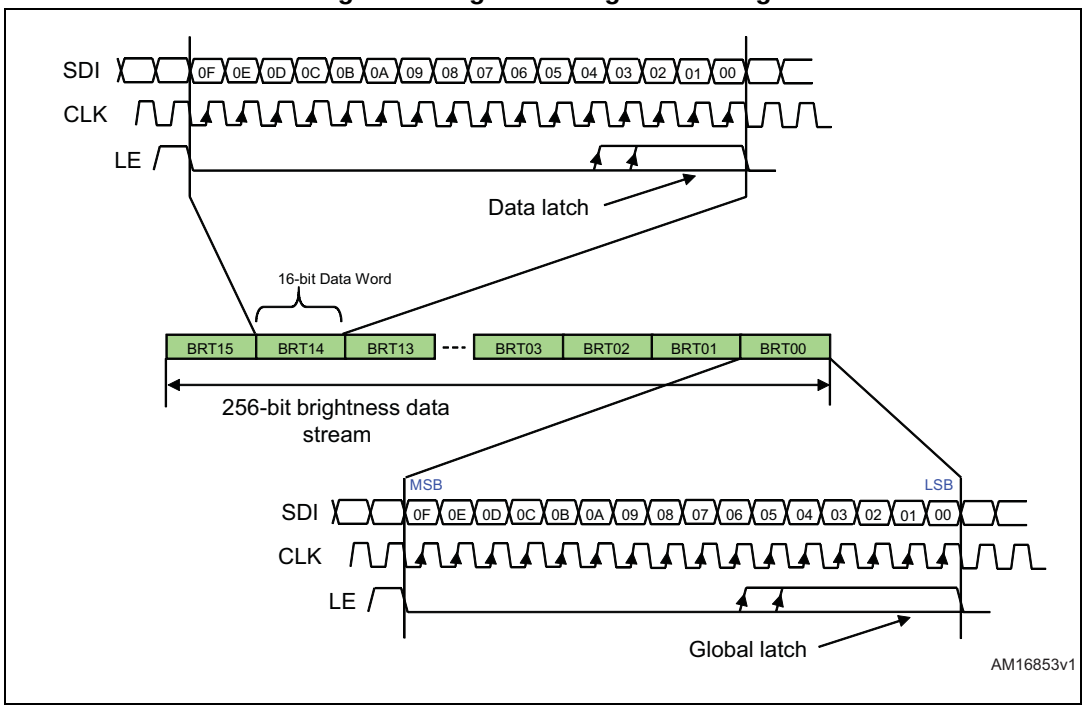
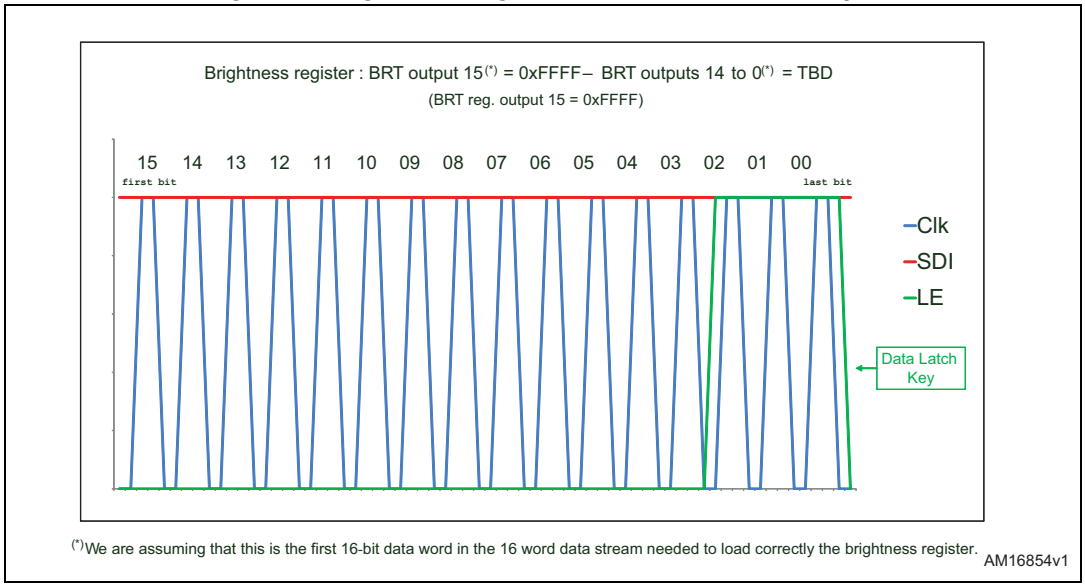


Figure 4. Brightness register setting



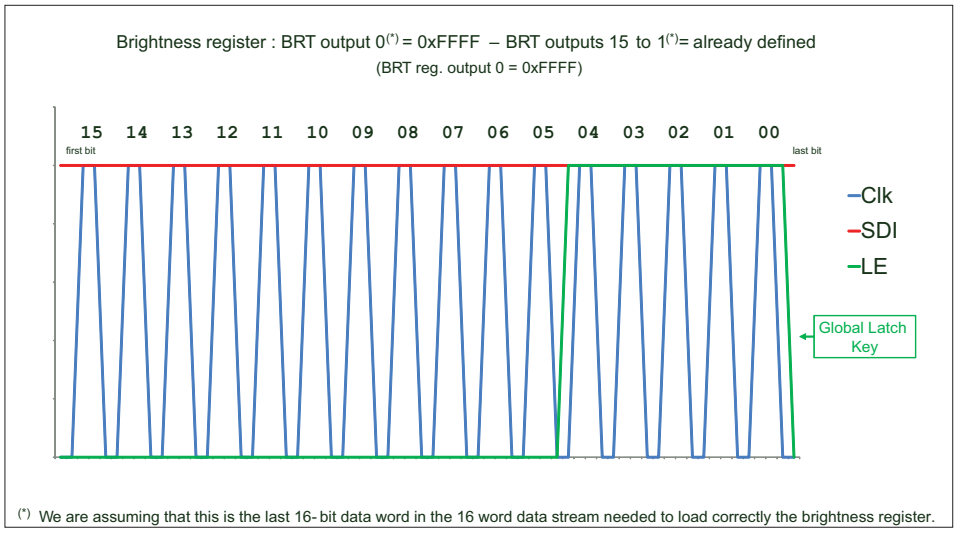
As mentioned, a 16-bit word with data latch has to be sent 15 times (see *Figure 5*).

Figure 5. Brightness register: first BRT word example



At the end of the above sequence a 16-bit word with global latch must be sent, see *Figure 6*.

Figure 6. Brightness register: last BRT word example



- The output switch enable has to be sent. 16 bits with SDI=1 on switch register have to be sent to have all 16 outputs ON (see *Table 2* and *Figure 7* and *Figure 8*).

Table 2. Digital key summary-write switch

Number	#CLK rising edge when the LE is 1	Command description
1	1-2	Write switch (to turn on/off output channels)
2	3-4	Brightness data latch
3	5-6	Brightness global latch
4	7	Write configuration register
5	8	Read configuration register
6	9	Start open error detection mode
7	10	Start short error detection mode
8	11	Start combined error detection mode
9	12	End error detection mode
10	13	Thermal error reading
11	14	Reserved
12	15	Reserved

Figure 7. Digital key summary chart-write switch

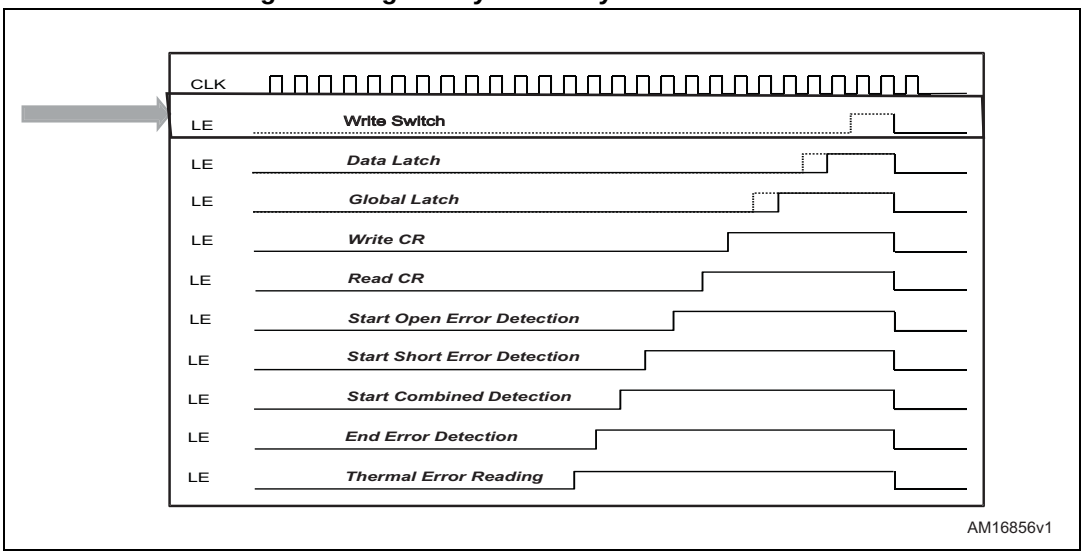
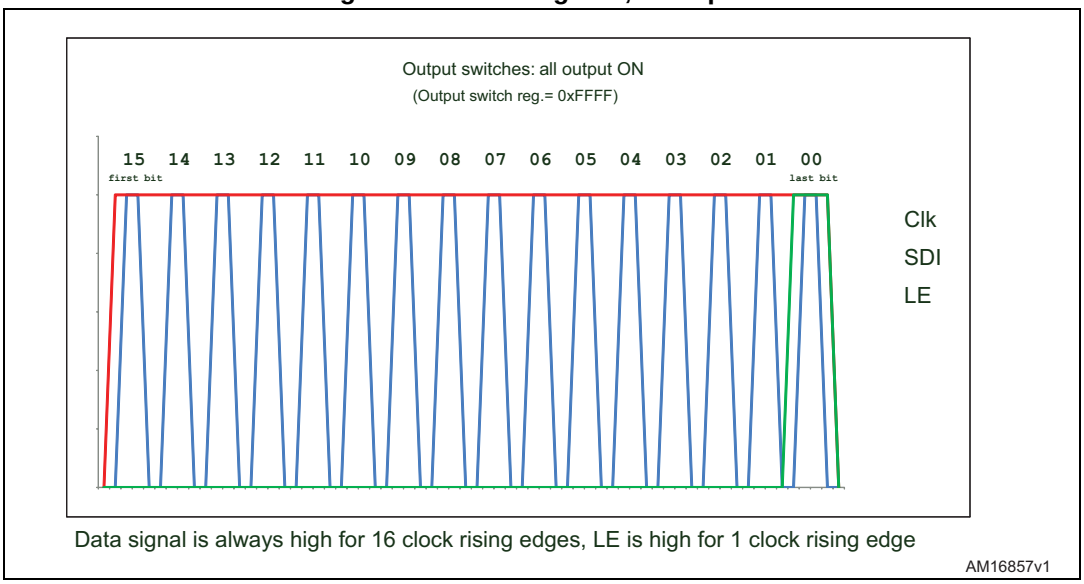


Figure 8. Switch register, example 1



The result of above seventeen 16-bit words is the LED power-on at ILED = 3 mA and 100% duty cycle.

3 LED power-on at maximum current and 50% duty cycle

This example is similar to the previous one but, the configuration register value has been changed so to have the brightness counter at 12 bits and the current gain to the maximum. Besides, the brightness register set-up has been changed to have a PWM duty cycle of about 50%.

- In order to get the maximum LED current, configuration register bits from CFG-0 to CFG-6 need to be changed from 0 to 1. At the same time, to change the brightness counter from16 to 12 bits, CFG-15 has to be changed.

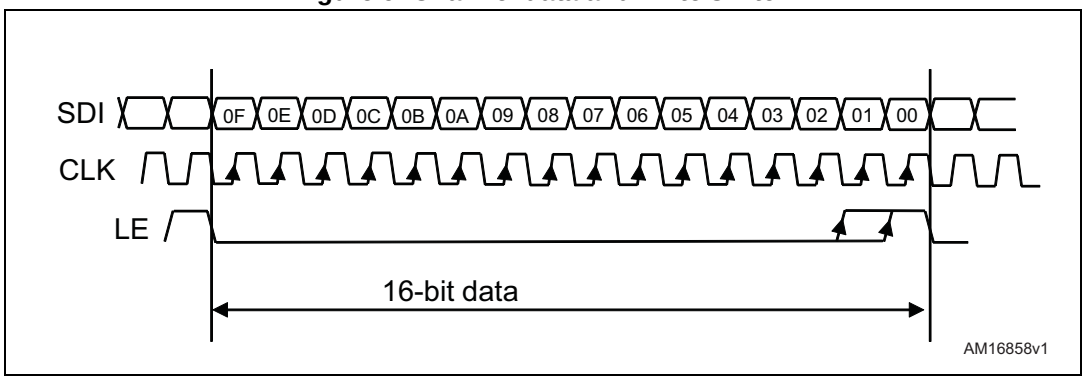
Table 3. Configuration register

Bit	Definition	R/W	Description					Default
CFG-0	Current gain adjustment	R/W	6-bit DAC allows adjusting the device output current in 64 steps for each range (defined by CFG-6)					0
CFG-1								0
CFG-2								0
CFG-3								0
CFG-4								0
CFG-5								0
CFG-6	Current range	R/W	”0” low current range “1” high current range					0
CFG-7	Error detection mode	R/W	“0” normal mode “1” reserved mode					0
CFG-8	Shorted-LED detection thresholds	R/W	Programmable output shorted-LED detection thresholds	CFG-9	CFG-8	Th. volt		0
				0	0	1.8 V		
				0	1	2.5 V		
CFG-9		R/W		1	0	3 V		0
				1	1	3.5 V		
CFG-10	Auto OFF shutdown	R/W	“0” device always ON ”1” auto power shutdown active (auto OFF)					0
CFG-11	Output turn-on/off time	R/W	Programmable output rise and fall time (20% to 80%)	CFG-12	CFG-11	Turn-on	Turn-off	0
				0	0	30 ns	20 ns	
				0	1	100 ns	40 ns	
CFG-12		R/W		1	0	140 ns	80 ns	0
				1	1	180 ns	150 ns	
CFG-13	SDO delay	R/W	If “0” no delay is present on SDO If “1” the data is shifted out and synchronized with the falling edge of the CLK signal					0

Table 3. Configuration register (continued)

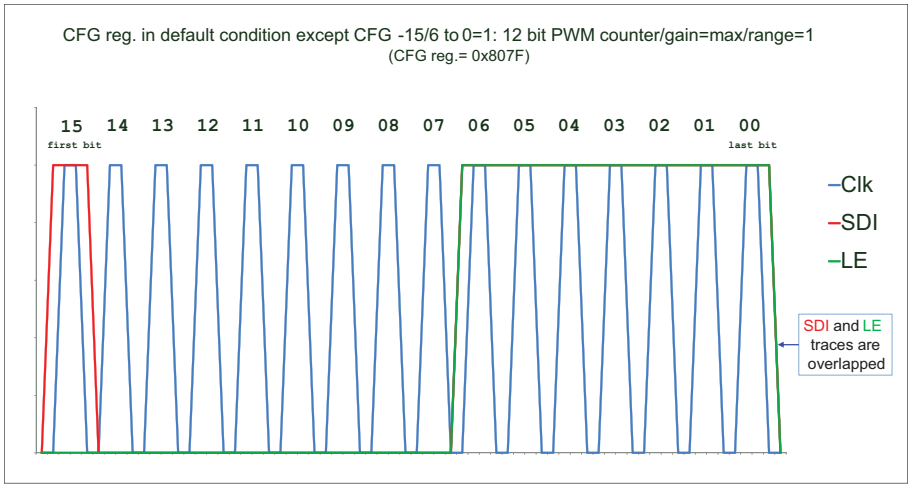
Bit	Definition	R/W	Description	Default
CFG-14	Gradual output delay	R/W	“0” a progressive delay is applied to output (10 ns per channel) ”1” no delay is applied to output	0
CFG-15	12/16 PWM counter	R/W	“0” to select 16-bit brightness register (65536 grayscale rightness steps). “1” to select 12-bit brightness register (4096 grayscale brightness steps)	0

Figure 9. Channel data and write switch



To carry on the changes both on the configuration register and on brightness register, the patterns are shown in *Figure 10*, *Figure 11* and *Figure 12*.

Figure 10. LED1642GW and ALED1642GW configuration register



Data signal is high for clock rising edges 15, 06 to 00; LE is high for 7 clock rising edges

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- In *Figure 11* and *Figure 12*, as in the previous example, a 16-bit value has to be sent for each of 16 outputs, in particular, the first 15 patterns have a data latch (LE high for 3 CLK rising edges), last pattern has a global latch (LE high for 5 CLK rising edges). Unlike the first example, this time, the value to be programmed is 0x0800 to get 50% PWM duty cycle (12-bit counter) for all driver outputs:

Figure 11. LED1642GW and ALED1642GW brightness register: first word example

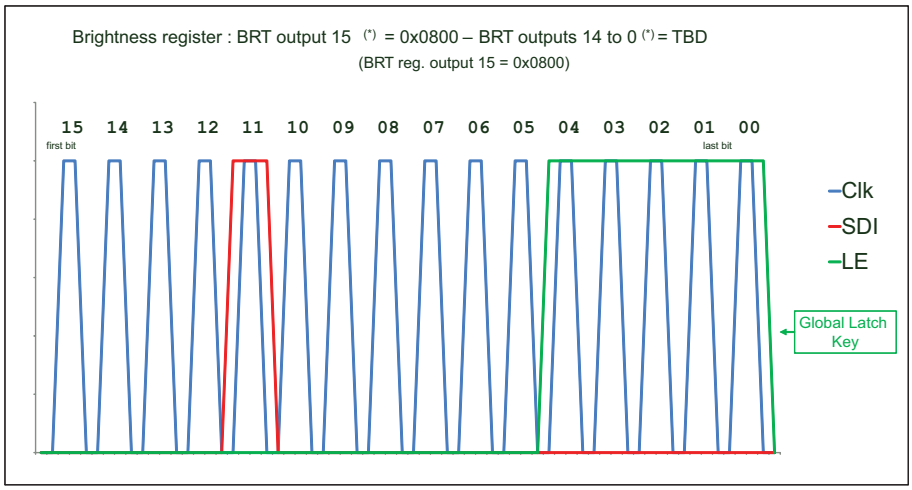
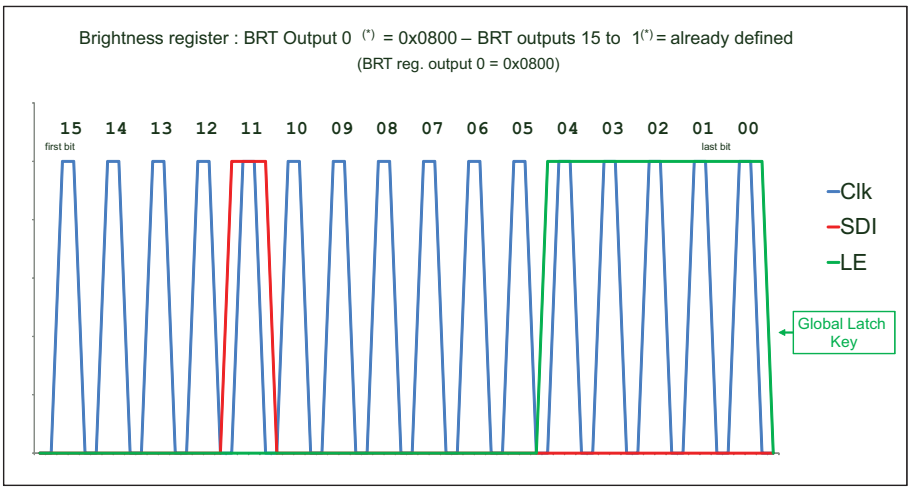


Figure 12. LED1642GW and ALED1642GW brightness register: last word example



- As last pattern, the output switch power-on has to be sent. SDI=1 on switch register has to be sent 16 times (see previous example) to have all 16 outputs ON.

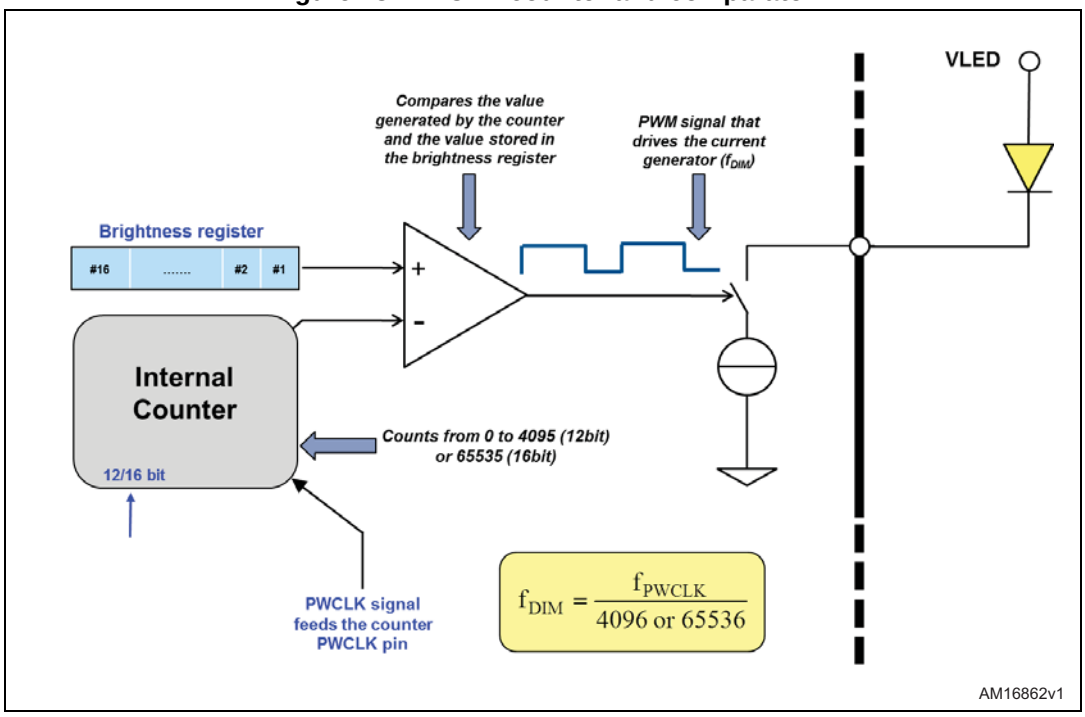
The result of the above eighteen 16-bit words is the LED power-on at ILED=36 mA and 50% duty cycle.

4 The PWCLK frequency choice

The PWCLK frequency must be selected to avoid visible flicker on the dimmed LEDs. The LED PWM frequency is linked to PWCLK frequency and in particular, the PWM frequency is the PWCLK frequency dived by 65536 (16-bit counter) or 4096 (12-bit counter) related to the configuration register set-up. To avoid LED flicker, usually, the PWM frequency must be higher than 100 Hz; to get this set-up, the PWCLK frequency has to be higher than 100x4096 = 410 kHz with CFG-15=1 (12-bit counter), we can round at 500 kHz.

In case of 16-bit counter, the minimum PWCLK frequency must be higher than 100x65536 = 6.5 MHz with CFG-15=0 (16-bit counter), we can round at 7 MHz. *Figure 13* shows the internal PWM signal generation.

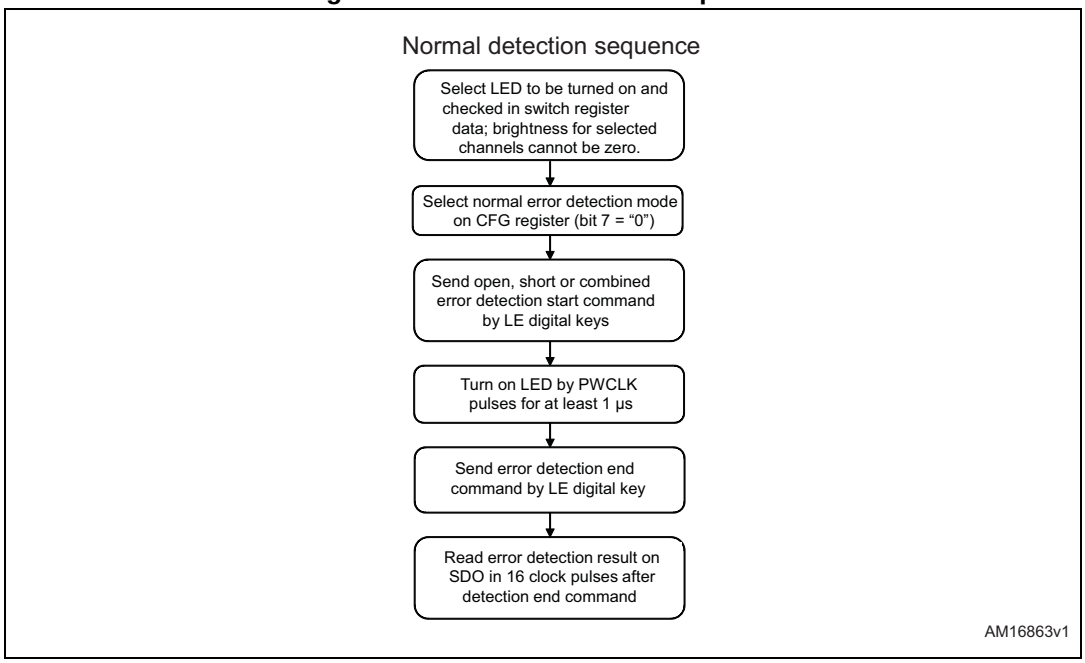
Figure 13. PWCLK counter and comparator



5 Output error detection

Stopping the normal activity of the display and turning on all driver channels allows the error detection to be performed and failed LED or display defects to be checked. The error detection is active when the CFG -7 bit in the configuration register is "0". The diagnostics is performed as shown in *Figure 14*:

Figure 14. Normal detection sequence



- The LED has to be selected turning on the relative channel on the switch register (powering on or off the output channels); the brightness register value for this channel cannot be zero.
- The appropriate digital key must be sent (see*Table 4* and *Figure 15*) to choose the type of detection (open, short or combined):

Table 4. Digital key summary-detection

Number	#CLK rising edge when the LE is 1	Command description
1	1-2	Write switch (to turn on/off output channels)
2	3-4	Brightness data latch
3	5-6	Brightness global latch
4	7	Write configuration register
5	8	Read configuration register
6	9	Start open error detection mode
7	10	Start short error detection mode
8	11	Start combined error detection mode
9	12	End error detection mode
10	13	Thermal error reading
11	14	Reserved
12	15	Reserved

Figure 15. Digital key summary chart-detection

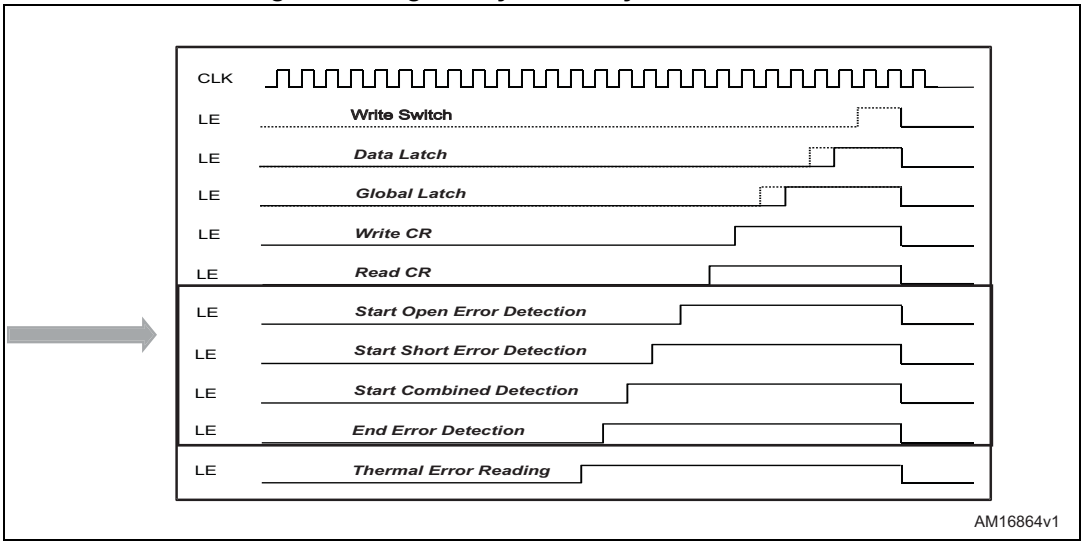
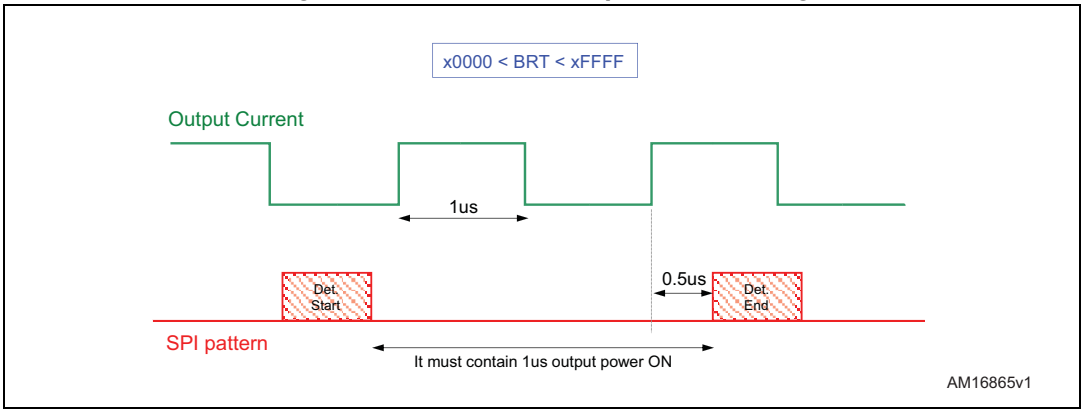


Figure 16. Error detection power-on timing



- After the error detection starts, the channel under test has to be turned on at least 1 µs (the LED is at the nominal current). Please note that, the output power-on depends on the PWCLK signal and in several applications this signal is not synchronized with the serial interface clock (CLK pin). Therefore, to be sure that, between the detection start and the detection end, the output power-on is 1 µs and moreover, that last power-on, in the interval, starts at least 0.5 µs before than detection end, it is suggested that the error detection should be performed just after the device startup (brightness counter reset) with all channels ON, before applying the PWCLK signal (see *Figure 16*).
- The result of the detection ("0" indicates a fault condition) is shifted out SDO in 16 clock pulses after the "detection end command" is provided, first output bit represents channel 15. Please note that (with SDO delay off) output 15 detection result is available just after the 1st clock pulse rising edge, so it can be sampled on the rising edge of the second clock pulse. In the same way, the output 0 detection result is available just after the 16th clock pulse rising edge, so it can be sampled on the rising edge of the 17th CLK pulse.

Pattern examples for error detection:

Figure 17. LED1642GW and ALED1642GW error detection: open detection start

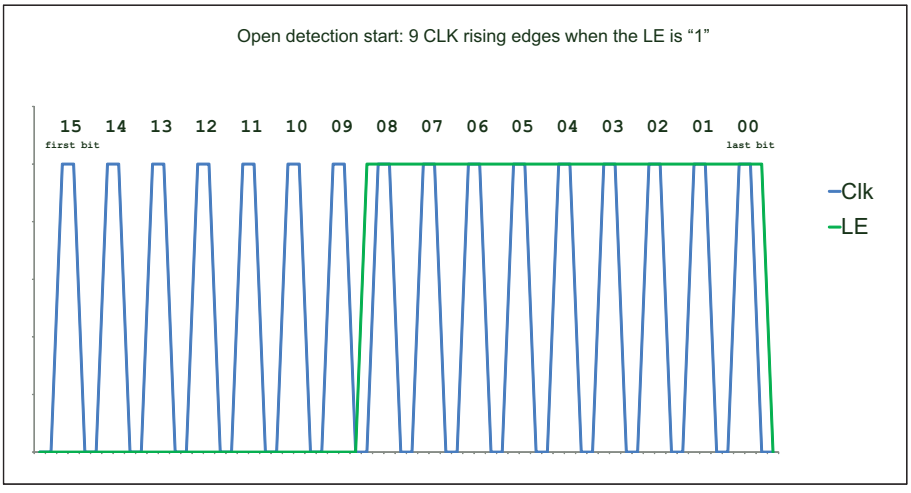


Figure 18. LED1642GW and ALED1642GW error detection: short detection start

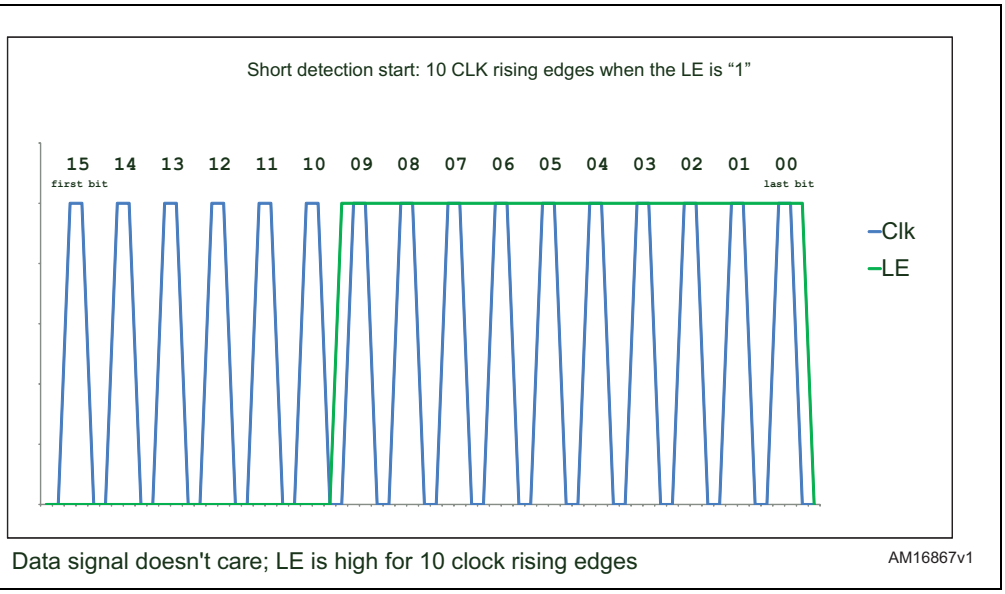


Figure 19. LED1642GW and ALED1642GW error detection: combined detection start

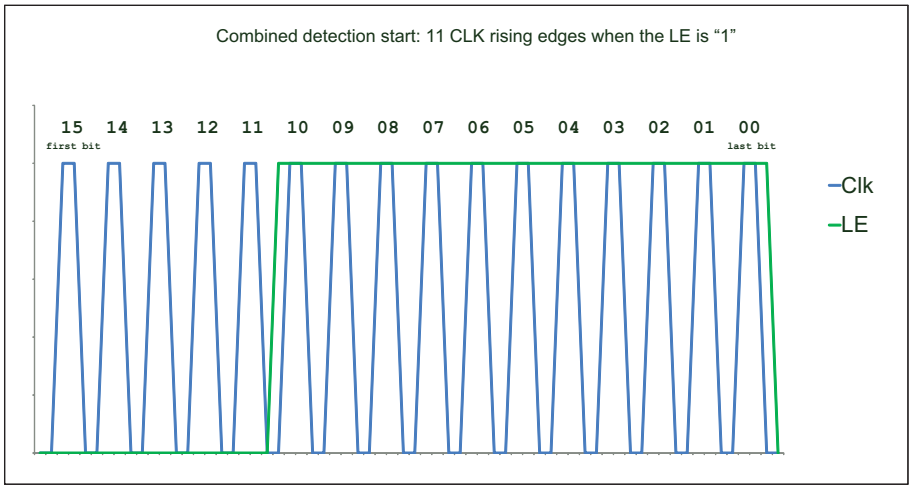
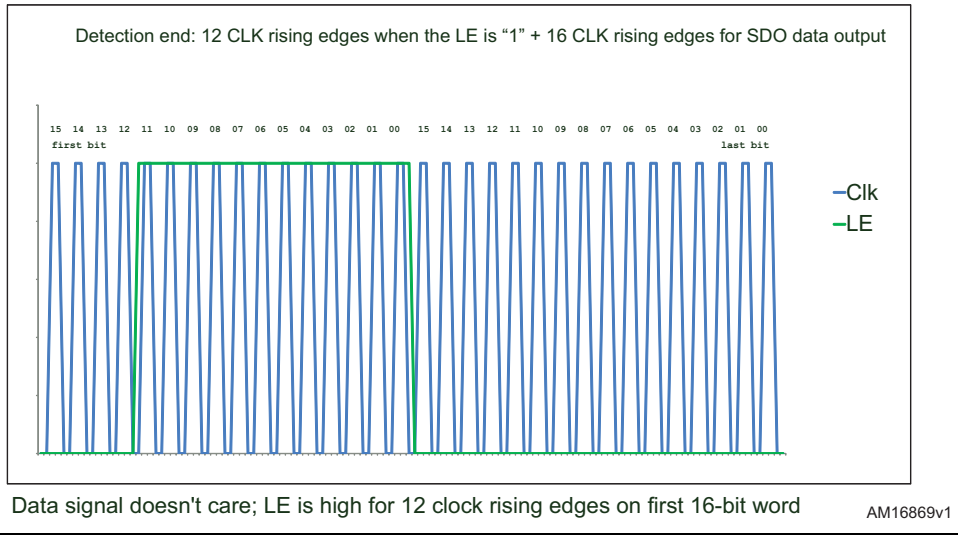


Figure 20. LED1642GW and ALED1642GW error detection: detection end



Error detection conditions:

During the error detection phases for each channel, the following parameters are checked:

- The output current in open detection mode (digital key: 9 CLK rising edges when LE is "1").
- The output voltage in short detection (digital key: 10 CLK rising edges when LE is "1").
- Both parameters (output voltage and current) in combined error detection mode (digital key: 11 CLK rising edges when LE is "1").

The thresholds for the error diagnostics are listed in *Table 5*:

Table 5. Diagnostics thresholds

Error detection modes		Checked malfunction	CFG-9	CFG-8	Thresholds (V)		
					Min.	Typ.	Max.
Open detection	Combined mode	Open line or output short to GND	x	x		$I_O \leq 0.5 \times I_{O\_programmed}$	
Short detection		Short on LED or short to V_{LED}	0	0	1.15	$V_O \geq 1.8$	2.05
			0	1	2.25	$V_O \geq 2.5$	2.75
			1	0	2.75	$V_O \geq 3.0$	3.25
			1	1	3.25	$V_O \geq 3.5$	3.80

6 LED supply voltage

The choice of the LED supply voltage (V_{LED}) must be carried out considering several parameters:

- The voltage drop across current generators (V_O) must guarantee the desired current (see dedicated section in the datasheet).
- The maximum LED forward voltage ($V_{F,max}$).
- The maximum power can be dissipated by the package under the application ambient conditions.
- The accuracy of the supply voltage itself (V_{LED} can vary in a range and the minimum value should be considered).

Therefore the minimum LED supply voltage can be calculated as:

Equation 1

$$V_{LED,min} = V_{o,typ} + V_{F,max}$$

The LED supply voltage should be higher than $V_{LED,min}$ (to consider any fluctuation of the involved parameters) but not too high in order to keep low the power dissipation:

Equation 2

$$P_D = V_{DD} \cdot I_{DD} + \sum_{i=I}^{16} V_{0,i} \cdot I_{CHi}$$

where V_{DD} is the device voltage supply, I_{DD} the device supply current, $V_{O,i}$ and I_{CHi} are respectively the voltage drop across, the current generator *i* and the channel current *i* (the worst case is to consider all channels connected to LEDs at minimum V_F and maximum V_{LED}). In particular the power dissipation should be kept below the maximum power dissipation, defined as:

Equation 3

$$P_{D,max} = \frac{(T_j - T_a)}{\theta_{ja}}$$

where T_j and T_a are respectively the junction and the ambient temperature, whereas Θ_{ja} is the junction-to-ambient thermal resistance. Junction temperature should be maintained below 125 °C for industrial devices and below 150 °C for automotive grade devices. To summarize, the choice of the proper power supply must be a trade-off between the correct value assuring the desired LED current and the low power dissipation. In RGB applications, there can be a significant variability of the LED forward voltage (e.g. red LEDs have a lower forward voltage compared to green and blue ones).

In this case, the supply voltage must be chosen high enough to correctly switch on the LEDs with the highest forward voltage (green or blue). However this supply voltage is higher than the voltage required by red LEDs. Thus, the excess of voltage in the lines with red LEDs drops on the current generators, brings an increase of the power dissipation and loss of efficiency.

Moreover, the extra-voltage across the red LED driving generators could cause an erroneous shorted-LED condition detection.

To avoid these drawbacks, two different approaches are possible:

- A resistor in series can be added to each red LED. In this manner, the voltage excess drops across the resistor instead of dropping across the current generators. This solution reduces significantly the power dissipated by the chip (lower T_j). However, the total power dissipation does not change and a remarkable part of the power wastes on the series resistor. This affects the efficiency and also raises the cost of the system due to the need to dissipate the generated heat.
- Another solution is to split the LED voltage rail: one for blue and green LEDs (V_{LED}) and one for red LEDs (V_{LED_RED}), which can be derived using a switching regulator. This solution is the most advantageous in terms of power dissipation. Voltage rails are tailored to LEDs they drive and the wasted power is significantly reduced as well as the heat produced.

7 Higher current requests (outputs in parallel)

When the application requires to drive high power LEDs, the current demand could be higher than the current provided by a single channel. In this case, a higher current capability can be achieved by connecting together two or more channels (in accordance with the current value to be regulated). Generally, no stability issues are shown using this output connection but in any case a bypass capacitor on driver power supply (of about 1 uF) and in particular a bypass capacitor near LED anodes on V_{LED} power supply rail (of about 47 uF) are strongly recommended.

8 PCB layout guidelines

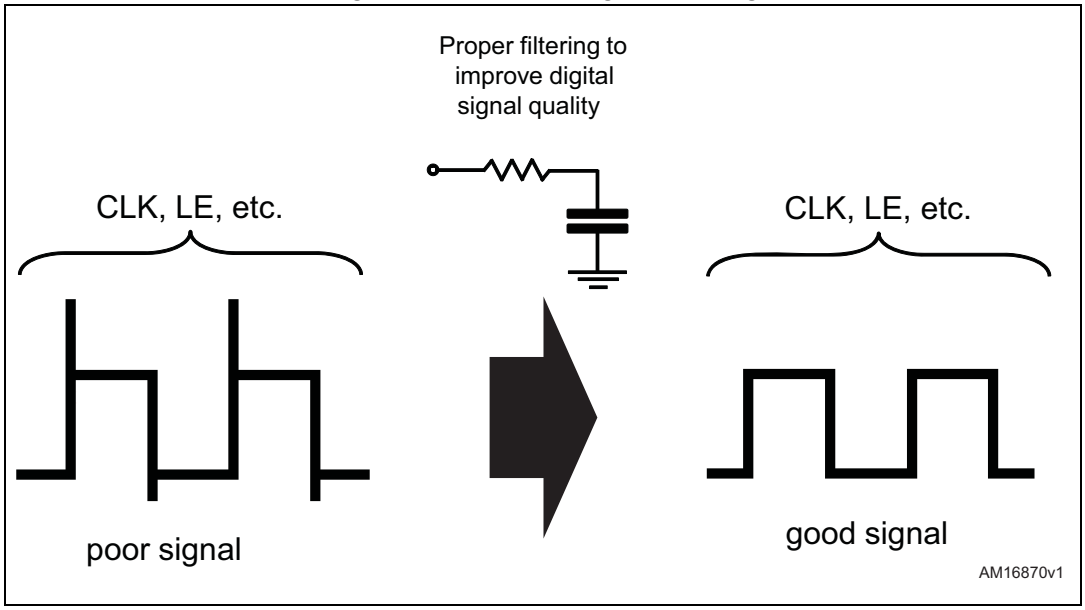
The aim of this section is to provide some useful advice to design the application PCB. General suggestions for PCB design are always valid. Beyond general recommendations, there are some other important considerations, tailored for this device family especially to reduce as minimum as possible EMI effects and maintain good signal integrity.

Signal integrity and radiated/conducted immunity

- The external programming resistor between R_{EXT} and GND should be connected as closer as possible to the device.
- The serial bus should be routed on the board and shielded.
- Try to widen spaces among signal lines till routing restrictions allow.
- Do not draw traces closer than three times the dielectric height and moreover, the distance between the centers of two adjacent traces should be at least four times the trace width.
- Design the transmission line so that the conductor is as closer to the ground plane as possible. This technique couples the transmission line tightly to the ground plane and helps to decouple it from adjacent signals.
- All SPI signals should proceed to the same direction on the board by a bus (same electrical length) to avoid CLK/LE skew (CLK and SDI are re-synchronized device-by-device).
- As far as the serial bus is concerned, whenever it is possible, vias should be avoided, tracing all strips on a single layer. Provide a ground plane close to this layer. In case of an inner layer, insert the strips sandwiched between two GND surfaces. Reduce the length of connections from the main bus to the device chain (traces derived: stubs), especially for the CLK and PWCLK. Keep CLK and PWCLK traces as straight as possible (corners should be rounded).
- In the chain configuration, last device’s SDO signal has the maximum delay compared to CLK source signal (strip propagation delay), the controller compares a "delayed" SDO signal with a local "not delayed CLK" (check the set-up time and clock distribution).
- In case of poor digital signals or noise pick-up on SPI lines some low pass-filters represent a suitable solution to be implemented. The RC time constant must be chosen case-by-case considering CLK frequency and noise characteristics. For

example, with 1 MHz CLK frequency, an adequate value could be 15 ns (e.g. 100 Ohm + 150 pF).

Figure 21. Interface signal filtering



Radiated emission reduction (EMI)

- In order to decrease the electromagnetic noise during LED power-on/off, the driver output lines should follow the shortest path "power rail/LED/driver". Besides, in order to keep the system stability, a good electrolytic capacitor should be connected to the power supply rail as near as possible the LED anodes (the inductive LED power supply rail component should be compensated by added capacitance; in case of wide PCB, place more distributed capacitors). Another filter capacitor must be added to each driver power supply pin (V_{DD}).
- Shorten as minimum as possible the SPI connection strips (from controller to LED driver).

Device thermal management

- In order to improve the power dissipation (to decrease the device working temperature), solder the package exposed pad (if available) to the board.
- In order to improve the thermal performance at least a 4-layer (e.g. 2S2P) PCB should be used.
- The copper area below the package thermal pad should be as large as possible, outside the package perimeter (using the package sides without pins).
- A reasonable number of vias must connect the copper area below the package to all available PCB layers especially just below the device package (e.g. 3x3 or 4x3 vias array) but also outside the package perimeter. Smaller and closely spaced

vias could be a good solution.The best implementation is represented by copper filled vias.

– On each inner layer, a copper area must be provided for dissipation (if possible, at least 4 times wider than the package dimensions). A good condition is to have at least a power layer as an entire copper area (e.g. GND layer).
– Traces for pin connection must be enlarged till layout constrains allow.
– Several devices in power dissipation on the same board must be adequately spaced.

9 Revision history

Table 6. Document revision history

Date	Revision	Changes
11-Oct-2013	1	Initial release.
14-Nov-2014	2	Updated title and introduction in cover page. Updated *Figure 1: LED1642GW and ALED1642GW block diagram*, *Section 1: The LED1642GW and ALED1642GW basic circuit*, *Section 3: LED power-on at maximum current and 50% duty cycle* and *Section 5: Output error detection*. Minor text changes.