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Application note

New P-channel trench technology from ST for low power DC-DC conversions and load switching applications

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Introduction

P-channel and N-channel MOSFETs show a different electrical performance. Due to lower hole mobility (three times smaller than electrons), the magnitude of specific on-resistance is greater in the P-channel structure. A larger die-size is needed to reach the same $R_{DS(on)}$ performance. However, an important advantage of P-channel devices is the simplicity and the driving circuitry optimization. In this document, new STripFET VI DeepGATE trench P-channel technology is deeply analyzed, from a technological point of view and in some of most popular applications for P-channel FETs, such as: low power DC-DC conversions (buck, boost) and load switches.

Contents

1 Description

P-channel MOSFETs don't play a relevant role in high-current applications, where a low $R_{DS(on)}$ is required to minimize the system conduction losses. In fact, with the same die-size, the P-channel device's $R_{DS(on)}$ is around 2.5/3 times higher than N-channel one, in other words, a bigger die-size for P-channel structures is needed to achieve the same on-state performance. This is a serious drawback in terms of overall system cost, efficiency and thermal management when the system works at a high switching frequency. If the die-size is bigger, device's intrinsic capacitances and switching losses are higher. However, there are several application segments where P-channel FETs can be used with a good performance, thanks to their electrical features. First of all, in low power DC-DC converters (buck converter, with maximum load current in the range of 2 - 3 A), a P-channel device can be used as high-side switch, without any additional external gate driving circuitry (i.e. charge pump), simplifying the overall circuit complexity. Secondly, in boost converters with low input voltages, a P-channel device can be used as an output synchronous rectifier, replacing a low-VF diode and improving the converter efficiency thanks to its figure-of-merit (FOM = $R_{DS(on)} * Q_G$). Finally, one of the most common P-channel MOSFET applications is the load switch, a pass element connecting a power source (battery, adapter) to a given load (display, ASIC…); by shutting off the load switch, the loads can be temporarily disconnected improving battery autonomy. Load switches are gaining ever-increasing importance because battery life is becoming one of the most important requirements for modern handheld devices.

2 P-channel technology overview

The main target of silicon technology for P-channel structure has always been the $R_{DS(on)}$ improvement. Old planar devices (*Figure 1*) show specific $R_{DS(on)}$ (also known as $R_{DS(on)}$ x area) values, measured in $m\Omega * mm^2$, not competitive, with bigger die-sizes to achieve the desired specifications. But, in this way, costs increase and the dynamic performance of the FET worses, due to higher intrinsic capacitances. To center the electrical specifications required by modern applications, the fixed course is to choose trench technology for new low voltage P-channel MOSFETs. New STripFET VI DeepGATE trench technology develops in order to produce a P-channel Power MOSFET with low $R_{DS(on)}$ and high robustness during reliability stress. The cross section of new trench MOSFET, highlighting both body and source contacts, is reported in *Figure 2*.

Figure 1. P-channel planar device structure

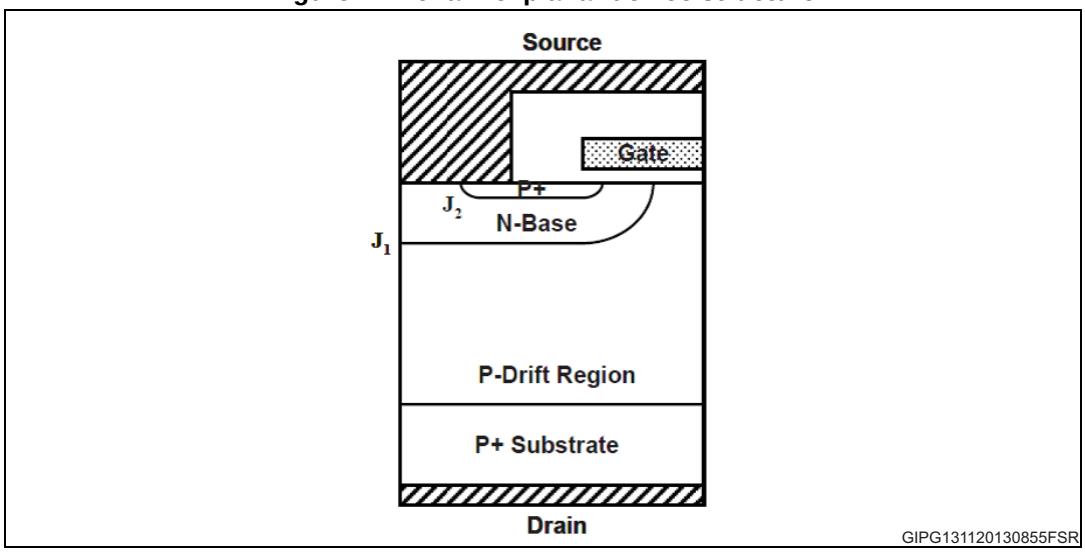
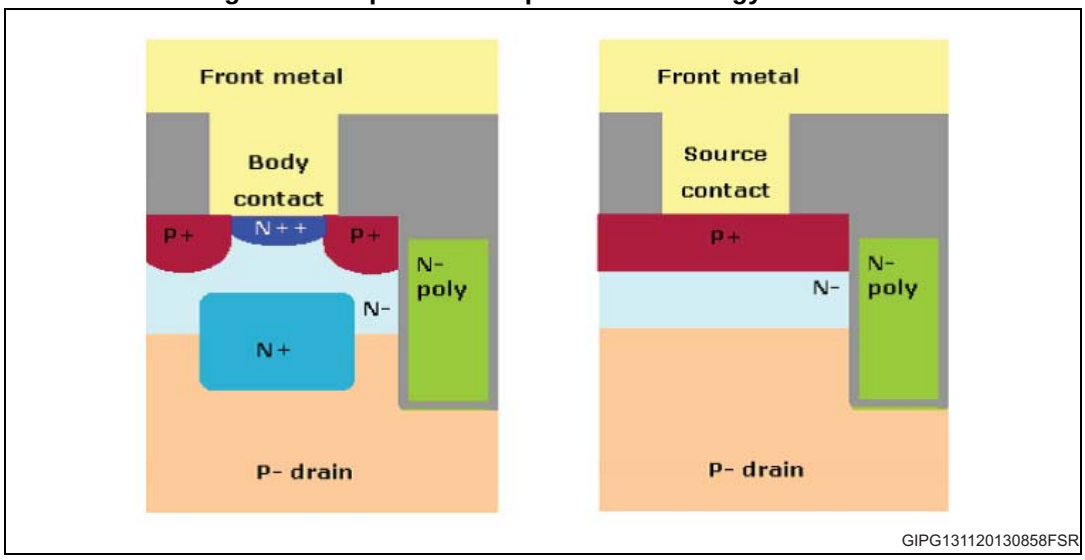


Figure 2. STripFET VI DeepGATE technology structure



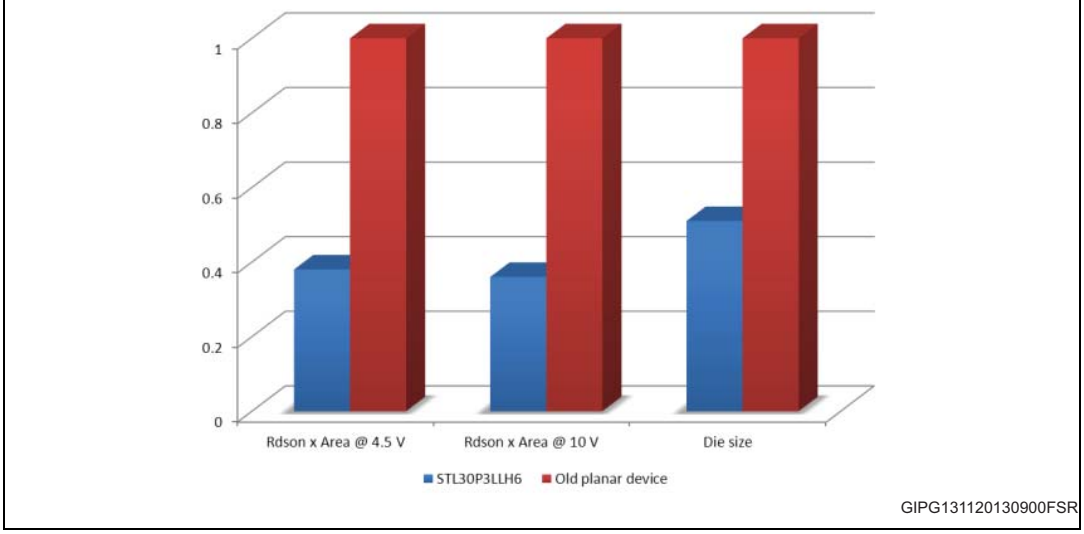
In a trench structure, the gate electrode is made up of a deep dug polysilicon electrode, isolated by a gate oxide layer. So, the trench extends beyond the bottom of N- body region to form a channel connecting P+ source region to P- drift region. The elimination of JFET region, which affects negatively the $R_{DS(on)}$ planar structures, allows very competitive $R_{DS(on)}$ values to be achieved and the cell pitch to be reduced, with additional benefits in other $R_{DS(on)}$ components.The main electrical parameters of two MOSFETs are reported in *Table 1*: the STL30P3LLH6 is realized with the new STripFET VI DeepGATE technology and is compared with an old planar device.

Table 1. MOSFET electrical parameters

Type	BV_{DSS} @ 250 µA	$R_{DS(on)}$ typ. @ 5 V	$R_{DS(on)}$ typ. @ 10 V	V_{TH} @ 250 µA	C_{iss} @ 25 V	C_{rss} @ 25 V	C_{oss} @ 25 V	R_G
STL30P3LLH6	> 30 V	39 mΩ	28 mΩ	1.8 V	1300 pF	125 pF	175 pF	2.3 Ω
Old planar device	> 30 V	65 mΩ	45 mΩ	1.6 V	1350 pF	130 pF	490 pF	3 Ω

In *Figure 3* there is a comparison between the $R_{DS(on)}$ x area and die-size of two above mentioned devices:

Figure 3. STripFET VI DeepGATE technology vs. planar one



As shown in the previous chart, the STL30P3LLH6 $R_{DS(on)}$ x area improvement is around 60% (both at 4.5 V and 10 V), while its die-size is halved.

3 P-channel FETs in low power DC-DC converters

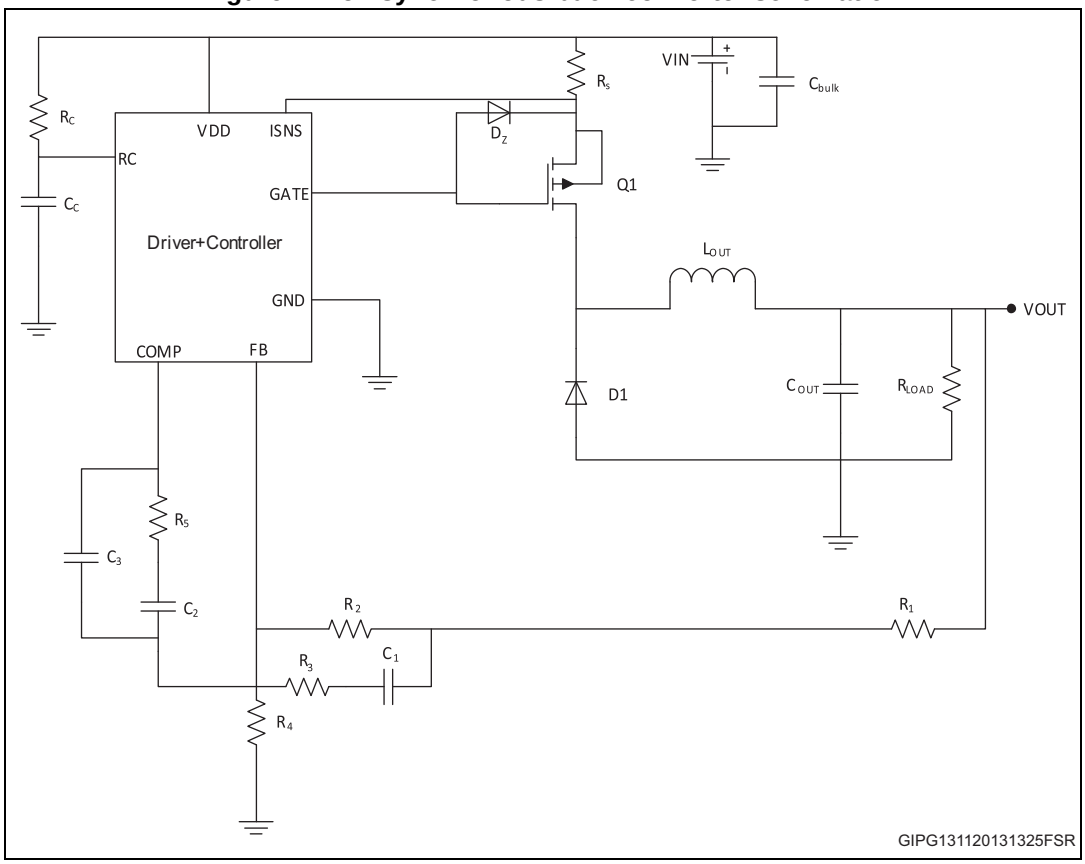
For low power DC-DC converters, the above described MOSFETs are tested in the following topologies:

1. Non synchronous buck converter, where the P-channel device is used as main switch.
2. Synchronous boost converter, where the P-channel FET works as synchronous device, replacing a low-V_F diode.

3.1 12 V - 5 V, 2.5 A, 450 kHz non synchronous buck converter

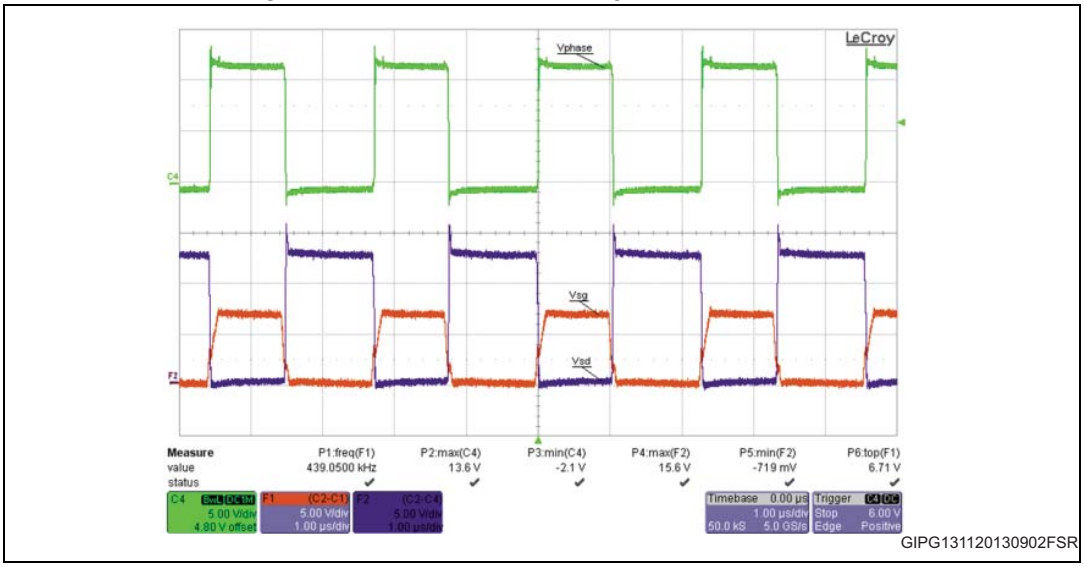
The simplified schematic of the buck converter, highlighting its main sections, is shown in *Figure 4*. Q1 is the P-channel FET, mounted as main switch; the synchronous element is the Schottky diode D1. L_{OUT} and C_{OUT} form the converter output filter, while RC networks, connected to FB and COMP controller pins, are the feedback circuit and compensation network.

Figure 4. Non synchronous buck converter schematic



The switching behavior is evaluated by capturing full load waveforms ($I_{OUT,MAX}$ = 2.5 A), at steady-state and during turn-on and off transients. *Figure 5* and *Figure 6* refer to the STL30P3LLH6 while *Figure 7* and *Figure 8* show old planar device waveforms.

Figure 5. STL30P3LLH6 steady-state waveforms



Turn-on waveforms are not reported because of V_{DS} and V_{GS} signals, which are regular without relevant stresses.

Figure 6. STL30P3LLH6 turn-off waveforms

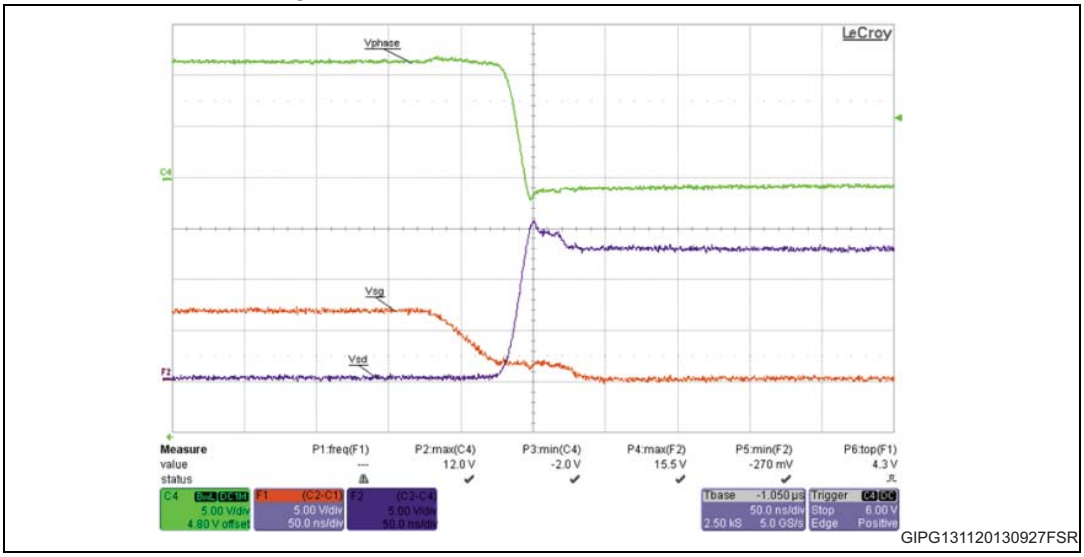


Figure 7. Old planar device steady-state waveforms

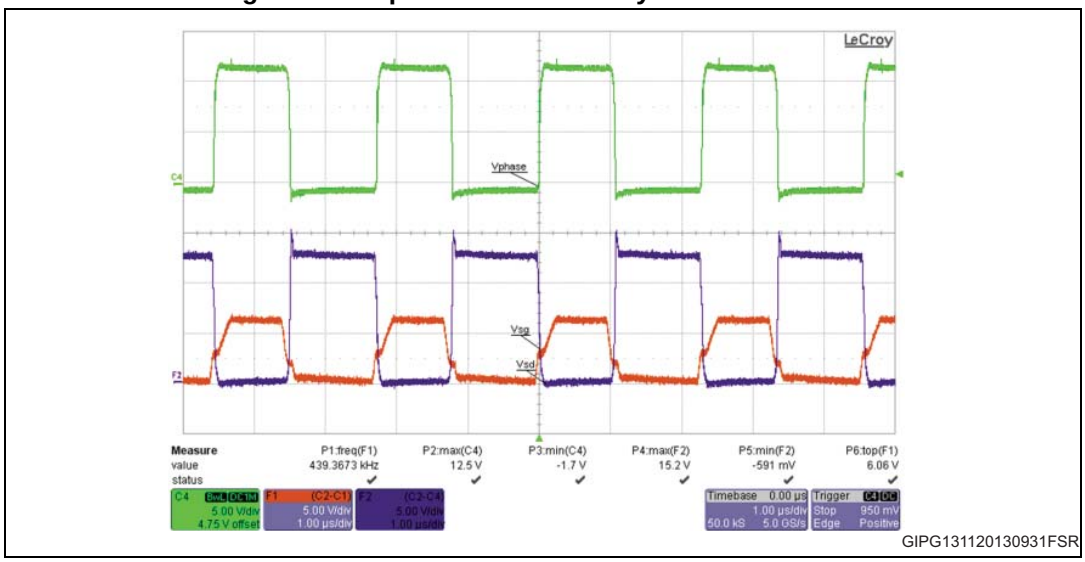
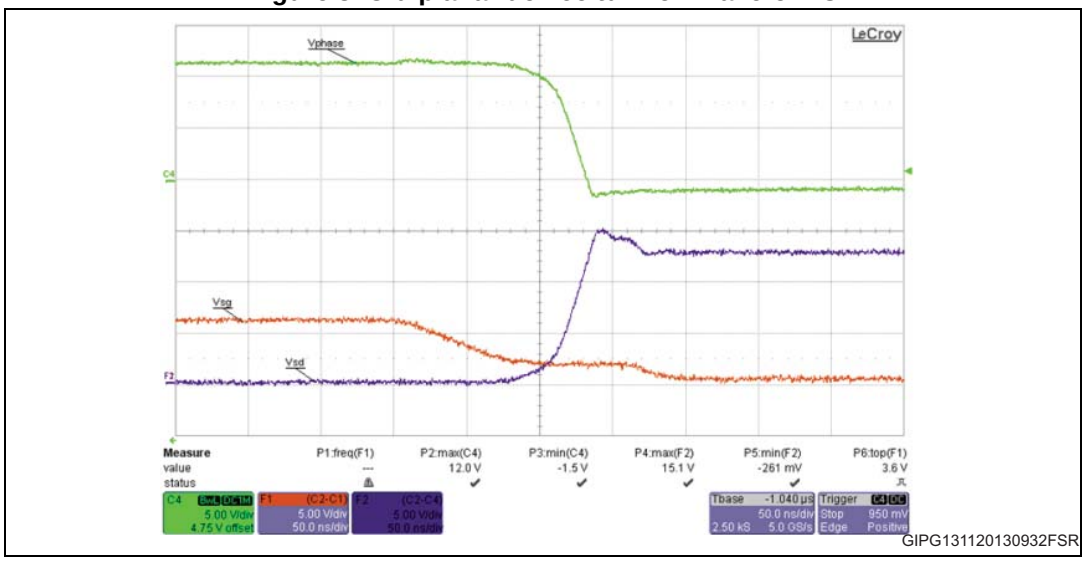


Figure 8. Old planar device turn-off waveforms



Comparing *Figure 6* and *Figure 8*, two FETs are perfectly aligned, maximum V_{DS} spike is much lower than BV_{DSS} rating. In a buck converter, high-side (or main switch) switching losses are given by:

Equation 1

$$P_{sw} = \frac{1}{2} \cdot V_{IN} \cdot \left(I_{OUT} \cdot f_{sw} \cdot Q_{GD} + \frac{Q_{GS}}{2} \right) \cdot (t_{s(L-H)} + t_{s(H-L)})$$

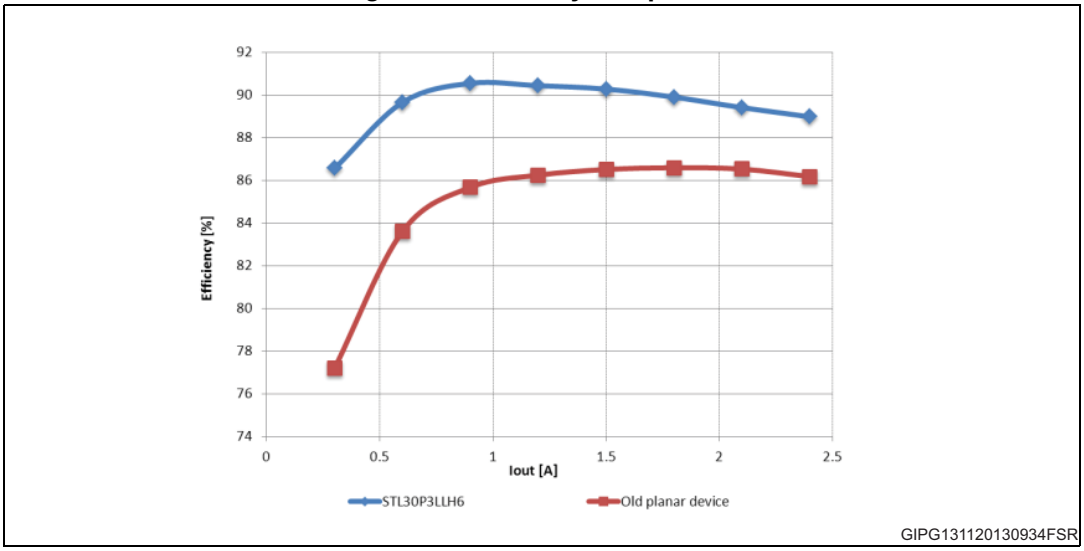
where $t_{s(L-H)}$ and $t_{s(H-L)}$ are the switching times (linked to driver supply voltage, pull-up/down and gate resistances), Q_{GD} and Q_{GS} the gate-drain and gate-source MOSFET charge. If the switching frequency is higher, device switching losses increase. The conduction losses are:

Equation 2

$$P_{COND} = D \cdot R_{DS(on)} \cdot I^2$$

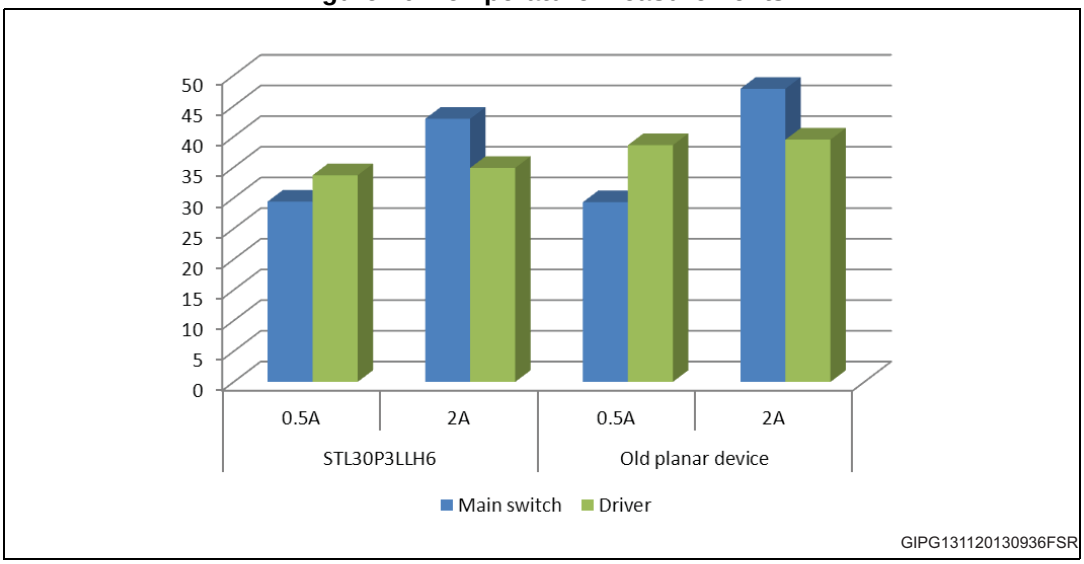
D is the converter duty-cycle ($D=V_{OUT}/V_{IN}$) and I the drain current. Increasing D, conduction losses become more significant. Converter losses can be minimized only if MOSFET dynamic (Q_G, gate charge) and static ($R_{DS(on)}$, drain-source resistance) parameters are as low as possible. In *Figure 9* efficiency curves are shown:

Figure 9. Efficiency comparison



The efficiency gain is high both at light and full load, due to simultaneous switching and conduction loss minimization. Finally, *Figure 10* shows thermal measurements at light (I_{OUT} = 0.5 A) and full load (I_{OUT} = 2 A):

Figure 10. Temperature measurements



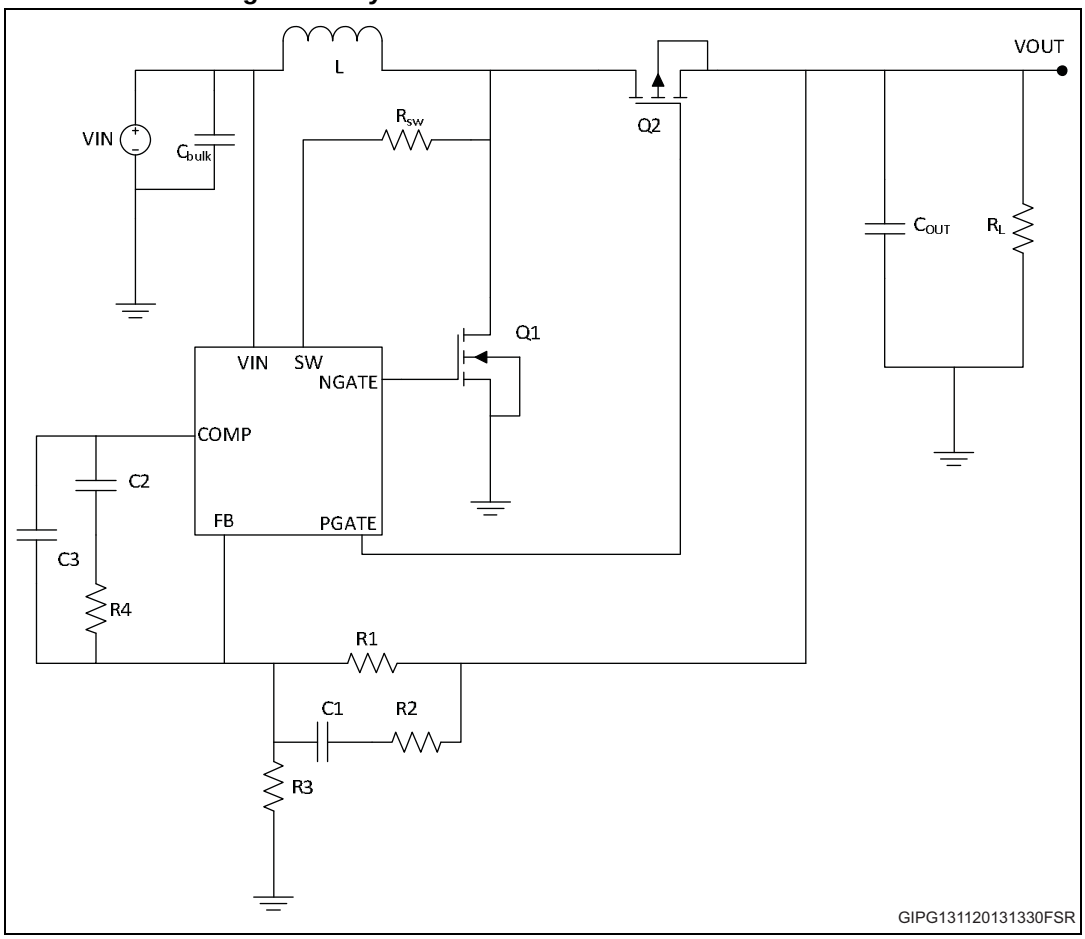
At low currents, thanks to lower intrinsic capacitances, the STL30P3LLH6 has lower switching losses and gate drive losses (they are needed to switch on and off the device):

hence, the driver is also cooler. At high-currents, a better $R_{DS(on)}$ allows higher efficiency and lower temperature.

3.2 2.5 V - 5 V, 1 A, 600 kHz synchronous boost converter

Low power synchronous boost converters are widely used: in fact, their input voltage range (typically, from 2.5 V to 4.2 V) allows operation from a 3.3 V source or directly from a Li-ion battery. In this converter (*Figure 11*), P-channel FET (Q2) can be used as synchronous element, replacing a low-V_F diode with lower voltage drop increasing the efficiency of the entire system.

Figure 11. Synchronous boost converter schematic



The STL30P3LLH6 and planar device's switching and efficiency behavior (see *Table 1*) are compared. Due to low input voltage level, there are not D-S voltage stress issues, with maximum values well lower than the device breakdown rating (*Figure 12* and *Figure 13*). So, waveforms are quite regular for both devices.

Figure 12. STL30P3LLH6 turn-off waveforms

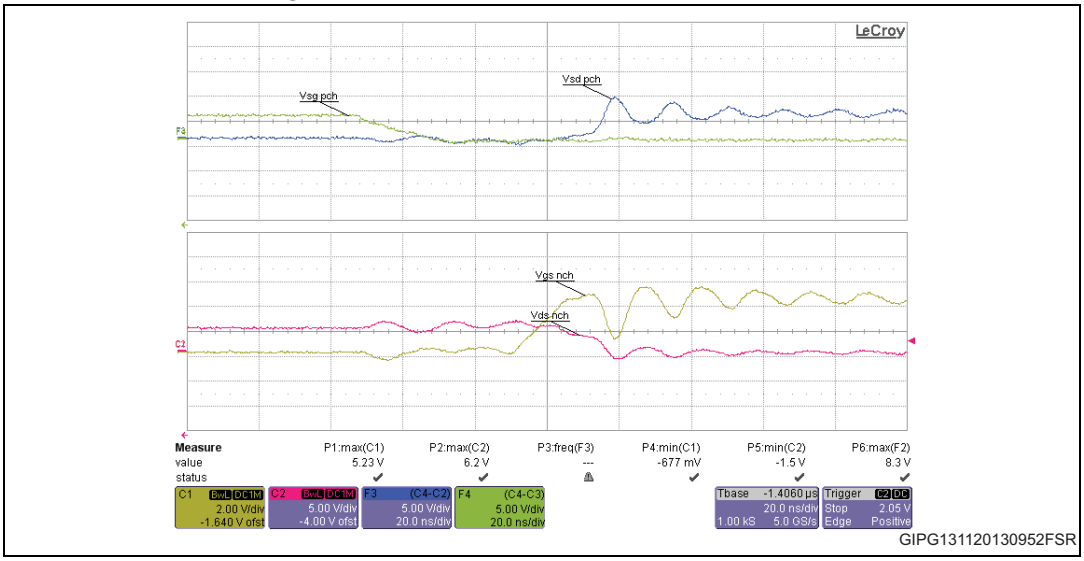
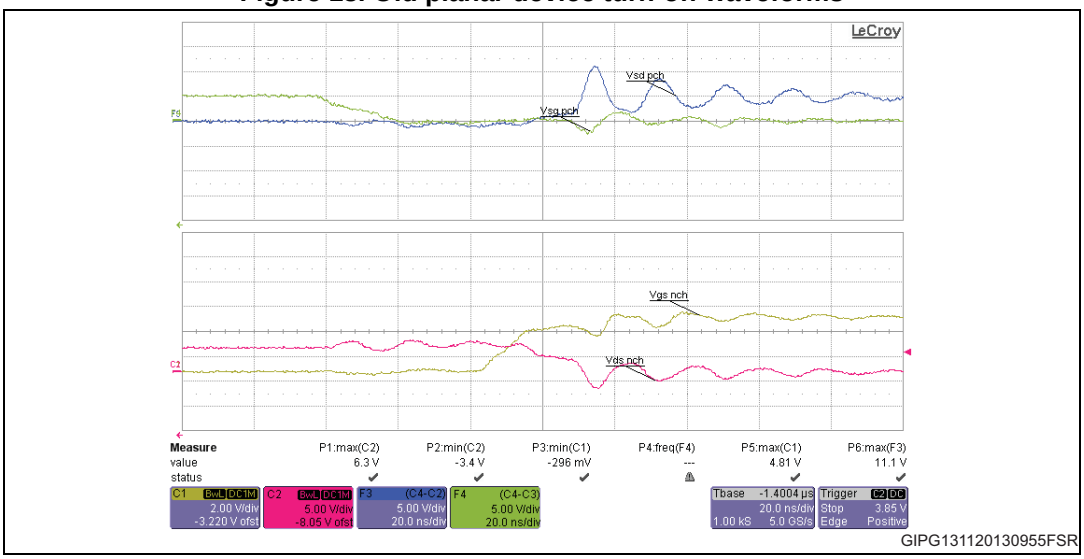


Figure 13. Old planar device turn-off waveforms



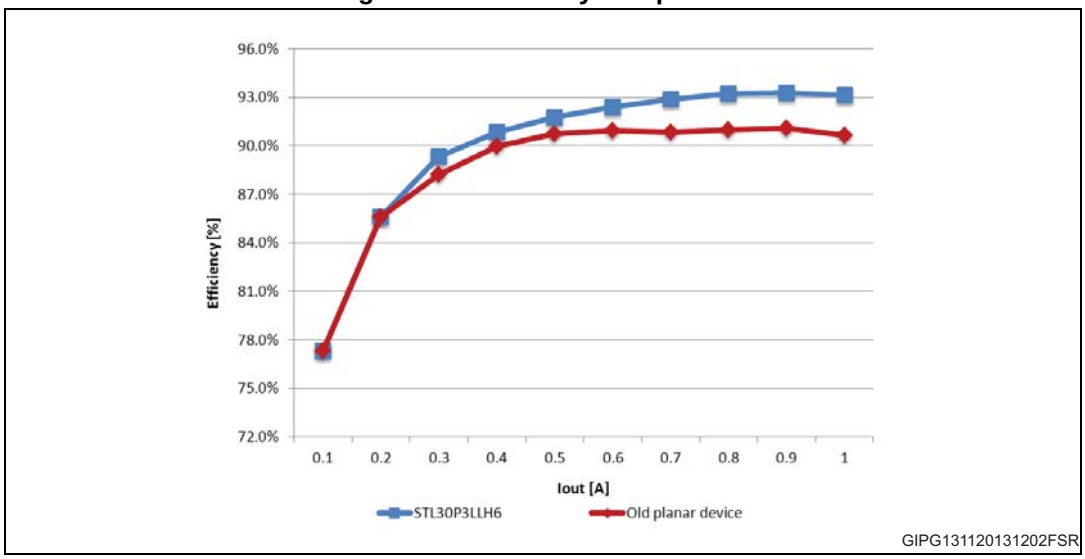
Due to converter duty cycle, δ (Q2 is ON for most of time), the major loss factor for synchronous device is the conduction loss, strictly related to FET $R_{DS(on)}$:

Equation 3

$$P_{cond} = R_{DS(on)} \cdot \frac{I_{OUT}^2}{1-\delta}$$

The $R_{DS(on)}$ improvement achieved thanks to P-channel trench technology allows the STL30P3LLH6's conduction loss minimization, exalting the overall efficiency at medium and full load (*Figure 14*).

Figure 14. Efficiency comparison



Finally, together with the efficiency improvement, Q2 (synchronous device) and driver temperatures are cooler when the STL30P3LLH6 is mounted.

Table 2. Thermal measurements @ 4 W (°C)

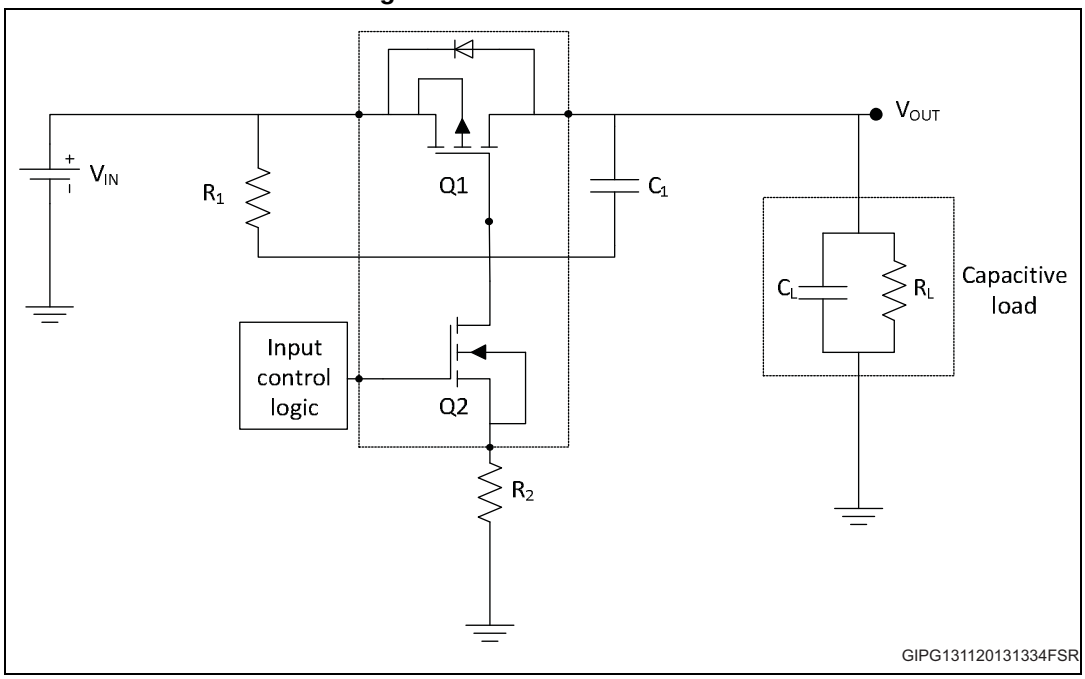
Device	T(Q1)	T(Q2)	T(DRV)
STL30P3LLH6	34.4	35.1	34.4
Old planar device	35	38.1	35.6

Thanks to $R_{DS(ON)}$ optimization, STripFET VI DeepGATE technology allows a good converter performance, especially in efficiency and thermal management, together with die-size shrinking and micro-package assembly availability.

3.3 P-channel FETs as load switches

Load switches are gaining ever-increasing importance (widely used in mobile phones, notebooks, tablets, handheld gaming system, etc…) playing a crucial role in the modern mobile system performance maximization. In fact, they provide a simple way to connect a voltage rail to a specific load, depending on the particular system operating mode. Disconnecting the unused load, the entire system can work more efficiently. *Figure 15* shows a P-channel device used as load switch:

Figure 15. Load switch circuit



Q1 is the load switch, while Q2 is the control FET (N-channel): when Q2 is ON (by a high logic signal), Q1 gate is at GND level, turning on Q1 ($V_{OUT} = V_{IN}$) level. The main advantage of a P-channel FET as load switch is the driving circuit, because no additional circuit (i.e. charge pump) is needed to turn on and off the switch. Moreover, it is the best choice for low power and high V_{OUT} load switch applications. In *Table 3*, the main application requirements are reported:

Table 3. Load switch application requirements

Parameter	Value
V_{IN}	12 V
I_{LOAD}	1 A
R_L	12 Ω
C_L	47 pF

In *Table 1*, the main electrical parameters of the tested devices are reported.

The load switch can be characterized by a series of switching parameters, which are briefly shown below:

1. Enable time, time between 50% of logic signal (applied to Q2 gate), in the rising edge, and 10% of V_{OUT}
2. Disable time, time between 50% of logic signal, in falling edge, and 90% of V_{OUT}
3. V_{OUT} rise time, time between 10% and 90% of output voltage, during rising edge
4. V_{OUT} fall time, time between 90% and 10% of output voltage, in the falling edge

As shown in *Figure 16* and *Figure 17*, the STL30P3LLH6's turn-on time is shorter than planar device, allowing faster V_{OUT} rising phase and therefore lower rise time (23 μs vs. 34

µs, *Figure 16* and *Figure 17*). Vice versa, the output voltage fall time is less sensitive to Q1 switching speed variations, because it is strictly linked to load capacitance and R1 values.

Figure 16. STL30P3LLH6 turn-on waveforms

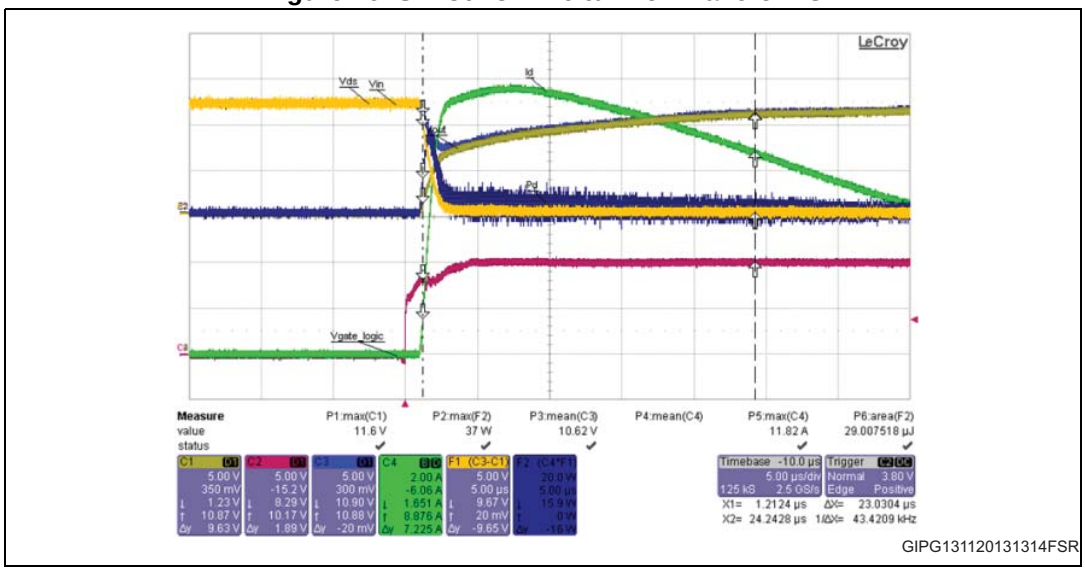
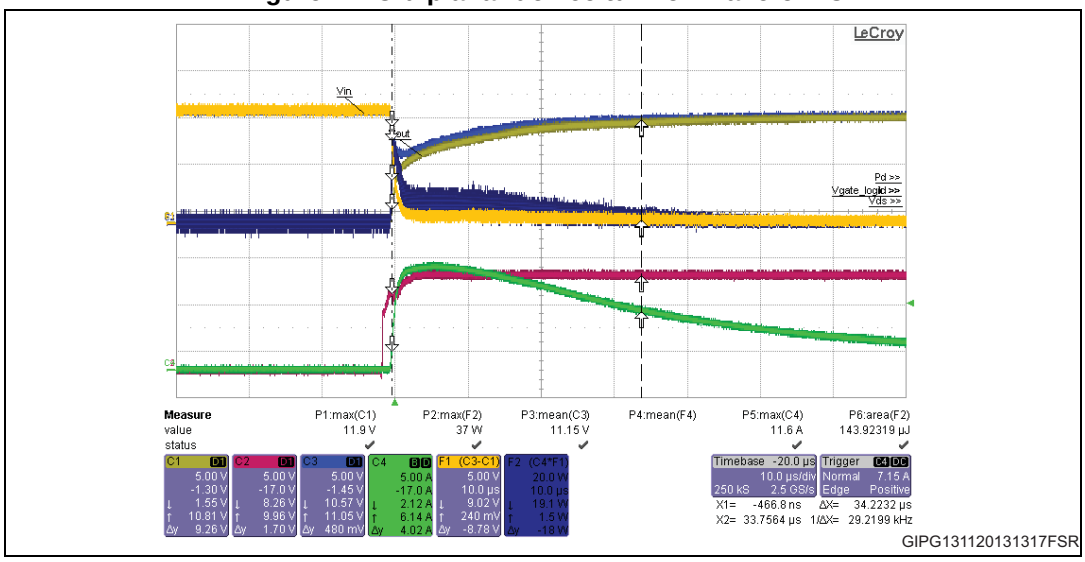


Figure 17. Old planar device turn-on waveforms



The shorter turn-on process also implies lower turn-on power losses (41 µJ vs. 54 µJ), as shown in *Figure 18* and *Figure 19*. During ON state (output load enabled), the STL30P3LLH6 has lower conduction losses thanks to its better $R_{DS(on)}$; so, combining a better performance both during switching transients and in ON state, the STL30P3LLH6 has lower power losses during one entire cycle ($E_{CYCLE} = E_{SW} + E_{ON}$). These results are summarized in *Figure 20*.

Figure 18. P-channel FET1 turn-on losses

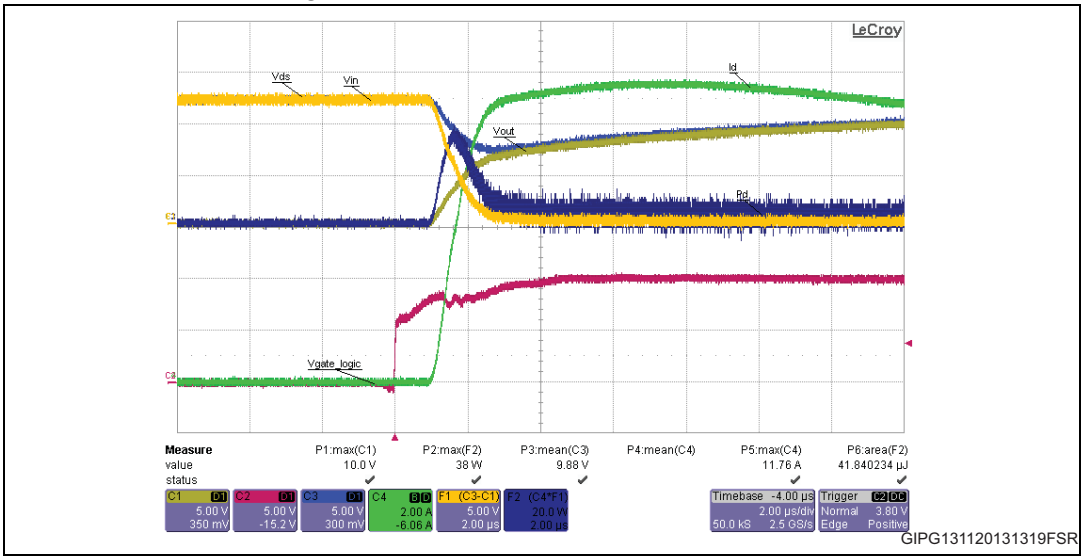


Figure 19. P-channel FET2 turn-on losses

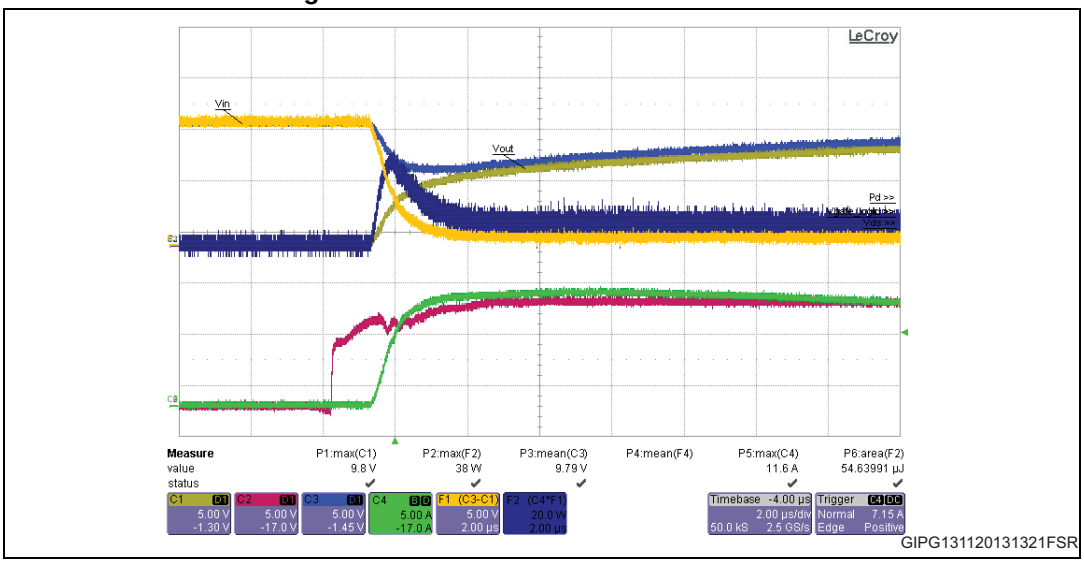
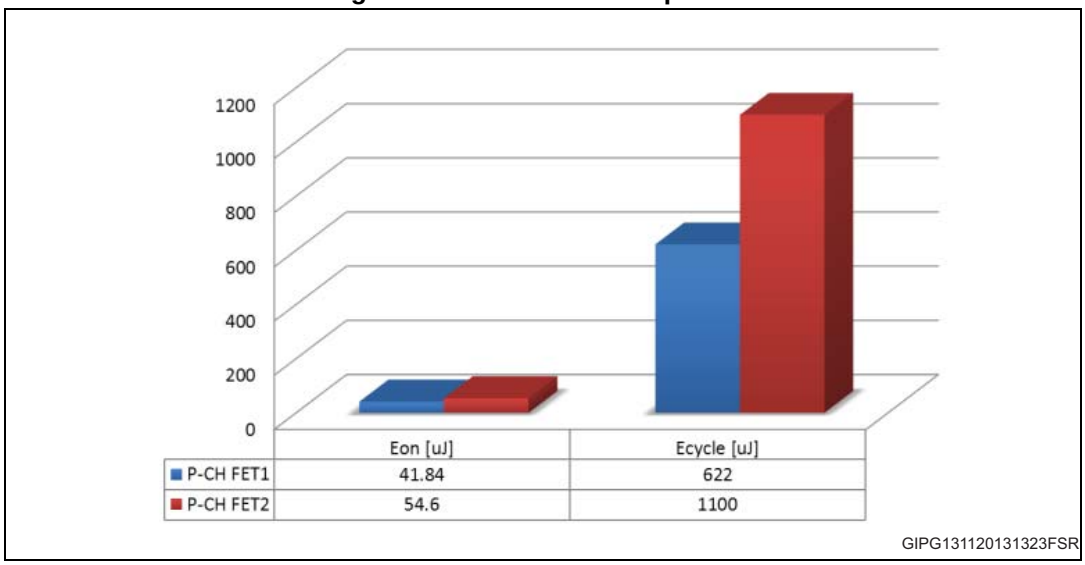


Figure 20. Power loss comparison



In load switch applications, STripFET VI DeepGATE technology, with its optimized figure-of-merit, allows the switching time optimization (enable, disable, rise and fall times) and power loss minimization. So, the specific load can be connected and used in more efficient way.

4 Conclusions

Thanks to some of its electrical features, P-channel MOSFETs are very often used in low power DC-DC converters (as main switch or synchronous device) and in load switching applications. FOM (FOM= $R_{DS(on)} \cdot Q_G$) minimization is mandatory for both applications to optimize the overall system performance. STripFET VI DeepGATE technology allows a strong $R_{DS(on)}$ x area minimization (-60% than old planar technology), maintaining a good switching performance: this implies an excellent thermal and efficiency performance, both at light and at full load, in low power DC-DC converters, but also fast switching times and low overall system losses in load switch applications.

5 References

B. Jayant Baliga, Fundamentals of Power Semiconductor Devices, Springer Science, 2008

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
21-Nov-2013	1	Initial release.