AN4444
Application note

ST7590 PRIME compliant power line networking SoC design guide

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Introduction

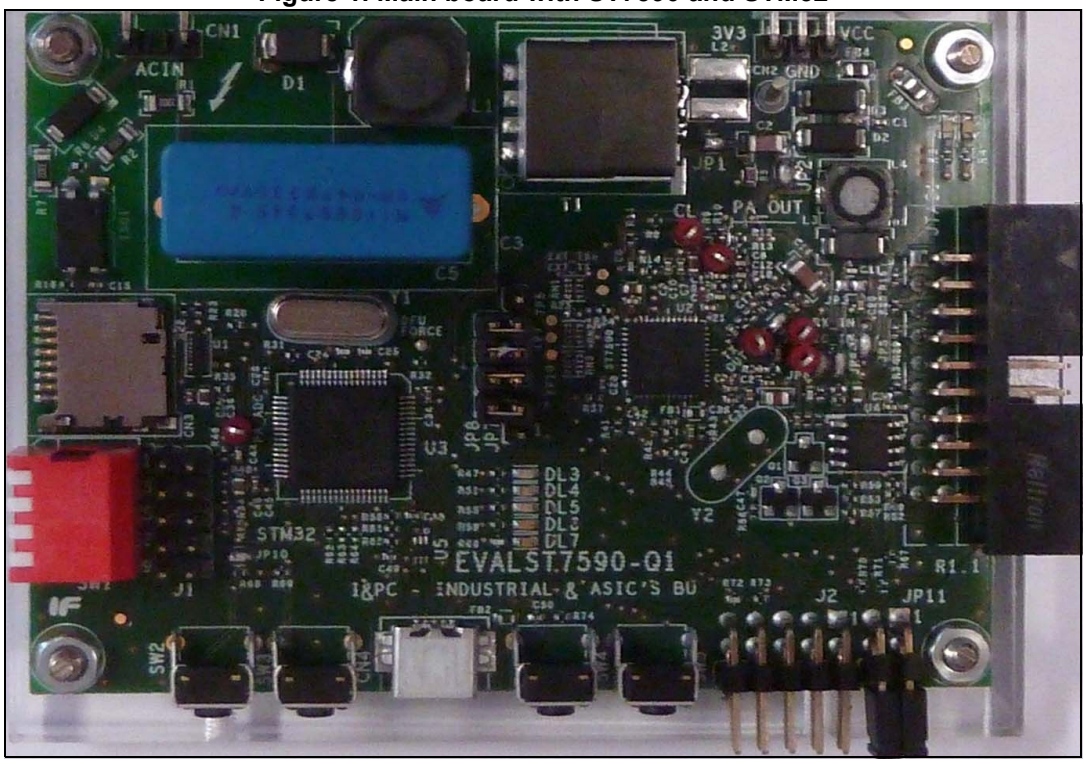
The ST7590 reference design has been realized as a useful tool that exploits the performance capability of the ST7590 power line networking system-on-chip.

With this reference design, it is possible to evaluate, directly on the power line, the transmitting and receiving performance of a power line communication node based on the ST7590 device.

The line coupling interface is designed to allow the ST7590 device to transmit and receive on the AC mains line using the PRIME OFDM signal within the European CENELEC EN50065-1 standard A band, specified for “Automatic Meter Reading” (AMR) applications (see Part 1 of *Section 14: Normative references on page 63*).

An STM32™ microcontroller has been included in the reference design to make it very flexible and suitable for use as a standalone smart PLC node.

Figure 1. Main board with ST7590 and STM32



As it can be seen from *Figure 1*, a special effort has been done to make the reference design compact and optimized, while including all the features enabling the ST7590 device to perform at its best.

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1 Abbreviations used in this document

Table 1. List of abbreviations

Abbreviation	Description
AC	Alternate current
AFE	Analog front-end
AMN	Artificial mains network
AMR	Automatic meter reading
AWGN	Additive white Gaussian noise
BER	Bit error rate
BoM	Bill of material
CE	Conducted emissions
DC	Direct current
DL	Data link layer
DSP	Digital signal processor
EMC	Electromagnetic compliance
EMI	Electromagnetic interference
FSK	Frequency shift keying
GUI	Graphical user interface
NBI	Narrowband interferer
LISN	Line impedance stabilization network
OFDM	Orthogonal frequency division multiplexing
PA	Power amplifier
PCB	Printed circuit board
PHY	Physical layer
PLC	Power line communication
PSK	Phase shift keying
PSU	Power supply unit
RBW	Resolution bandwidth
SBW	Signal bandwidth
SNR	Signal-to-noise ratio
SoC	System-on-chip

2 Electrical characteristics

Table 2. Electrical and thermal characteristics of the ST7590 reference design

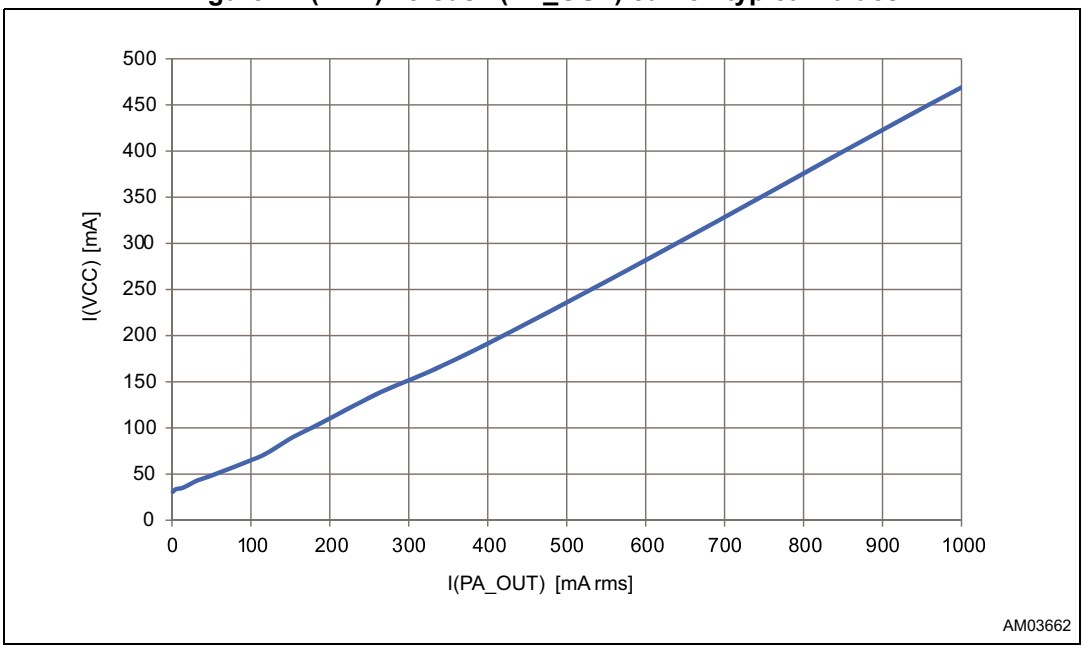
Parameter	Value				Notes
	Min.	Typ.	Max.	Unit	
Thermal data					
Ambient operating temperature	-40		85	°C	
ST7590 thermal resistance			50(1)	°C/W	Measured on the ST7590 reference design 2-side PCB with thermal pad and 4 x 4 thermal via array
Transceiver section					
Transmitting specifications (Tx mode)					
Transmitted signal -20 dB bandwidth		50		kHz	
Transmitted output current limit		1		A rms	
Receiving specifications (Rx mode)					
Minimum detectable received signal for the EVALKITST7590-Q1 board with AC supply		58		dBµV rms	B-PSK coded BER ≤ 10^{-3}
Passive Rx filter -3 dB bandwidth		100		kHz	
Power supply requirements					
V_{CC} power supply voltage	8	13	18	V	
V_{CC} power supply current absorption - Rx mode		8		mA	
V_{CC} power supply current absorption - Tx mode		30		mA	Tx with no load
		65		mA	Tx over EN50065 AMN
		355		mA	Tx over PRIME AMN
		460		mA	Tx over short-circuit
V_{DDIO} digital supply voltage	-10%	3.3	+10%	V	
V_{DDIO} digital supply current absorption		9		mA	STM32 under reset, ST7590 under reset
		55		mA	STM32 operative, ST7590 under reset (3 mA from DL5)
		90		mA	STM32 operative, ST7590 operative

1. Measured over a continuous transmission period of 3000 seconds (steady state thermal dissipation). See *Figure 45: Measured ST7590 thermal impedance curve (typical) on page 54* for the thermal impedance typical curve.

Table 3. TX_OUT level vs. TX_GAIN - typical values for BPSK modulation

Tx level	TX_OUT	
	[V p-p]	[dBµV rms]
7	0.315	101
6	0.425	104
5	0.630	107
4	0.865	110
3	1.205	113
2	1.690	116
1	2.380	119
0	3.330	121

Figure 2. I(VCC) versus. I(PA_OUT) curve - typical values



3 Safety recommendations

The board must be used by expert technicians only. Due to the high voltage (85 - 265 V ac) present on the non-isolated parts, special care must be taken in order to avoid electric risks for people safety.

There are no protections against high voltage accidental human contact.

After disconnection of the board from the mains all the live part must not be touched immediately because of the energized capacitors.

It is mandatory to use a mains insulation transformer to perform any tests on the high voltage sections, using test instruments like, for instance, spectrum analyzers or oscilloscopes.

Do not connect any probe to high voltage sections if the board is not isolated from the mains supply, in order to avoid damaging instruments and demonstration tools.

STMicroelectronics® assumes no responsibility for the consequences of any improper use of this development tool.

4 ST7590 power line networking system-on-chip description

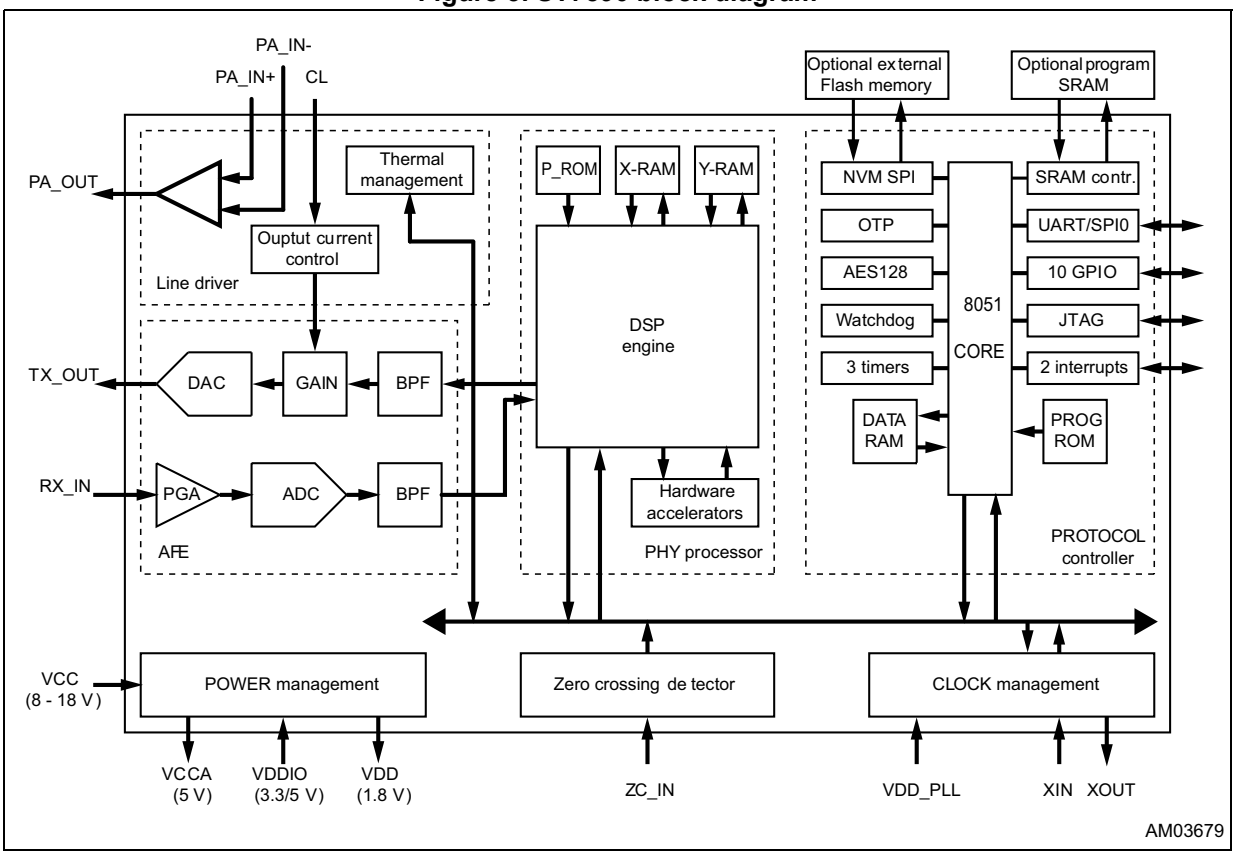
The ST7590 device is the first complete narrowband OFDM power line communication system-on-chip made using a multipower technology with state of the art VLSI CMOS lithography. The ST7590 device is based on dual core architecture to assure outstanding communication performance with a very high level of flexibility and programmability for either open standard or fully customized implementations.

The ST7590 device operates with a dedicated Cortex™-M3 FW library plus an embedded FW code to implement the full PRIME protocol stack (PHY, MAC and “Convergence Layer”), developed mainly for smart metering applications using the CENELEC A band (PRIME Alliance).

The embedded PHY layer (PRIME PHY), hosted in a DSP engine, is PRIME compliant (OFDM with 96 subcarriers in the 41.992 kHz to 88.867 kHz range) and implements different n-PSK modulations: the BPSK, QPSK and 8PSK modulation with a channel quality estimation, convolutional coding and Viterbi decoding, delivering a throughput from 21.4 kbps up to 128.6 kbps.

For further details, please refer to *1.* and *2.* in *Section 13: References on page 63*.

Figure 3. ST7590 block diagram



5 EVALKITST7590-Q1 description

The ST7590 reference design is available as a board set comprising:

- One main board with the ST7590 and the STM32
- One EVLALTAIR900-M1 as a power supply unit.

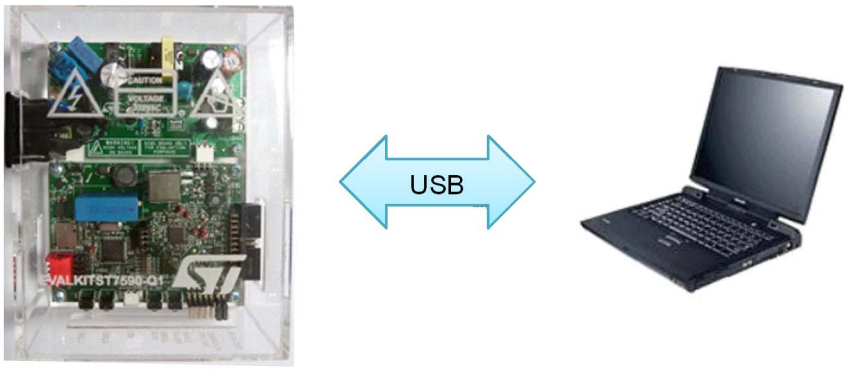
6 Evaluating with PRIME GUI

In addition to use as a developing platform for the PRIME compliant application, the EVALKITST7590-Q1 can be used in a complete PRIME evaluation environment.

A typical evaluation environment is composed by two or more EVALKITST7590-Q1 devices with a proper STM32 FW for a USB connection to the PC. The user can manage the PRIME communication services connecting the PRIME GUI to the nodes.

The PRIME GUI software tool running on a PC can be used to evaluate the ST7590 power line communication features of both the PRIME base node and PRIME service node.

Figure 4. Typical evaluation environment



6.1 VCP driver installation

In order to connect an EVALKITST7590-Q1 to the PRIME GUI running on a PC, the user has to install the USB/UART adapter driver (if not installed yet) following the steps below:

1. Download the latest available “Virtual COM Port” (VCP) drivers from the ST website (see *5.* in *Section 13: References on page 63*.) and unzip them to a location on the host PC.
2. Launch the setup file “VCP_V1.3.1_Setup.exe” to install the “Virtual COM Port” driver on the PC.

6.2 Loading the STM32 FW

Our EVALKITST7590-Q1 + PRIME GUI environment allow the evaluation of both PRIME base node and PRIME service node. The STM32 on-board has to be loaded with a proper FW based on the PRIME node type to be evaluated:

- PRIME service node: “PC BRIDGE SN” FW
- PRIME base node: “UART bypass” BN FW

STM32 programming can be done using the ST-LINK or ST-LINK/V2 in-circuit debuggers/programmers and the STM32 ST-LINK Utility software. For further details visit www.st.com.

6.3 Connection procedure

The following procedure is required for every node to be connected:

1. Verify that the JP7 and JP8 strips are connected as reported in *Figure 6*
2. Connect the EVALKITST7590-Q1 to the PC using a mini-USB cable
3. Plug a power cable into the board AC power connector
4. Plug the power cable into the power socket
5. The “STMicroelectronics Virtual COM Port” is recognized by the PC “Device Manager”.

7 Test and measurement tools

- Spectrum/network/impedance analyzer
  - Agilent 4395A:
    - 10 Hz - 500 MHz
  - Agilent 43961A Impedance Test Kit
- Differential active probe
  - Agilent 1141A Differential Probe:
    - 1 MΩ, 7 pF
  - Agilent 1142A Probe Control and Power Module:
    - DC reject 0.05 Hz
- EMC analyzer
  - Rohde & Schwarz ESL
    - 9 kHz - 3 GHz
    - Suitable for pre-compliance tests
- Two-line V-network (LISN)
  - Rohde & Schwarz ENV216
- Isolation transformer
  - 1000 VA, 0 - 250 V variable output
- Oscilloscope
  - Tektronix DPO 7104C
    - 1 GHz, 20 GS/s
- Surge/burst generator
  - Volta UCS 500-M

8 ST7590 reference design description

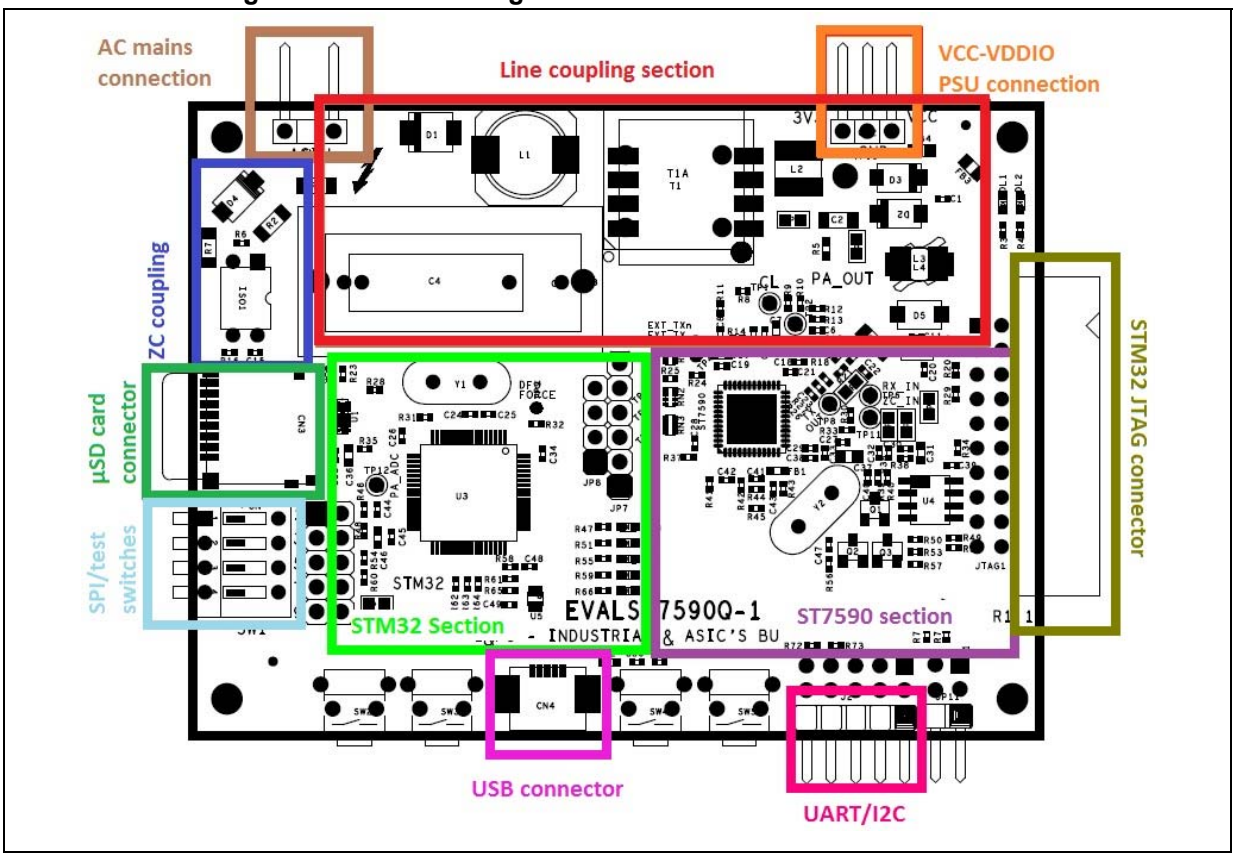
The ST7590 reference design is composed of the following sections:

- ST7590 device section
- Line coupling section, including four subsections:
  - Line driver
  - Reception filter (with optional amplifier)
  - Power line coupling
  - Zero crossing coupling
- STM32 microcontroller section

The board has also the following external connections:

- AC mains (line and neutral) on CN1 connector
- VCC (8 to 18 V), VDDIO (3.3 V) supply voltages on CN2 connector
- STM32 USB interface to PC on CN4 mini USB connector
- STM32 UART1 and I2C1 on J2 (5 x 2 connector)
- STM32 JTAG interface on JTAG1 connector (10 x 2 connector)
- STM32 SPI2 on DIP switches and J1 strip connector, also for STPMxx optional connectivity
- SD storage card on CN3 MicroSD connector.

Figure 5. Board drawing with indication of the various sections



The schematics of the reference design are reported below, divided by subsection.

Table 4: Bill of materials on page 22 lists the components chosen to realize the reference design board. All the parts have been selected to get good performance in a real case application.

The layout of the printed circuit board is reported in *Appendix A: on page 64* - *Figure 50*, *51*, *52*.

Figure 6. ST7590 reference design - ST7590 section

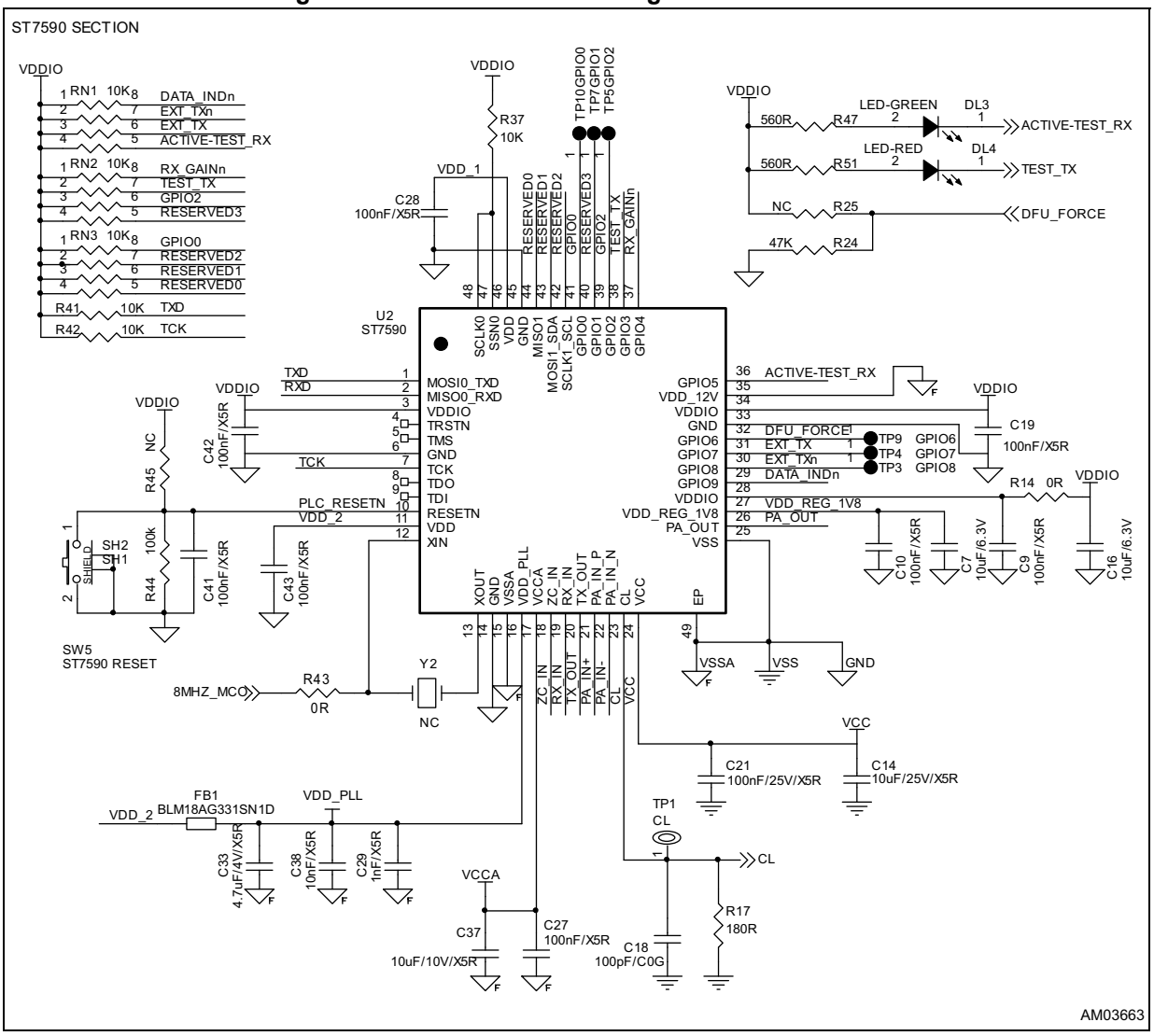


Figure 7. ST7590 reference design - power supply connections and ST7590 control lines

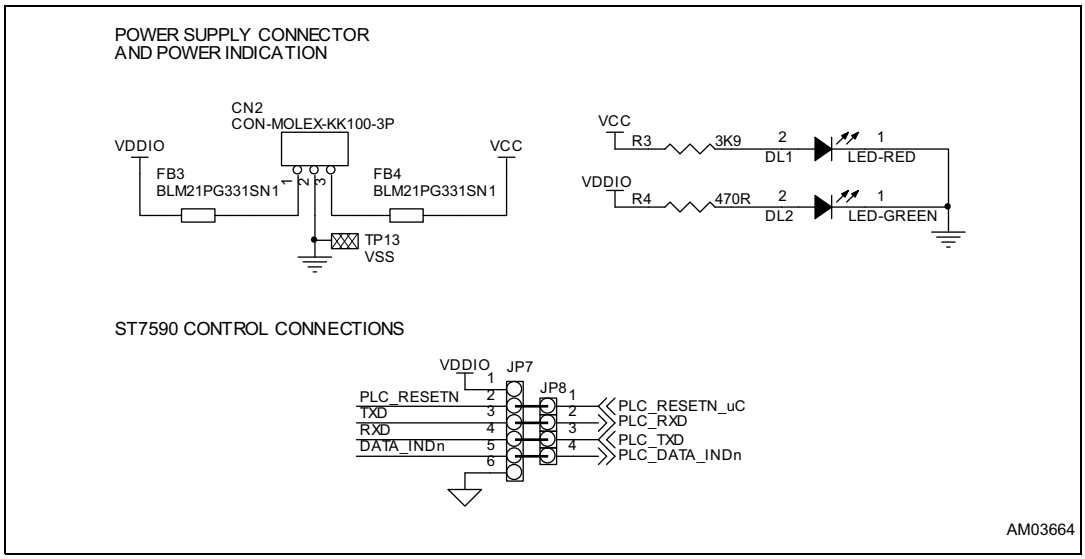


Figure 8. ST7590 reference design - PLC coupling section

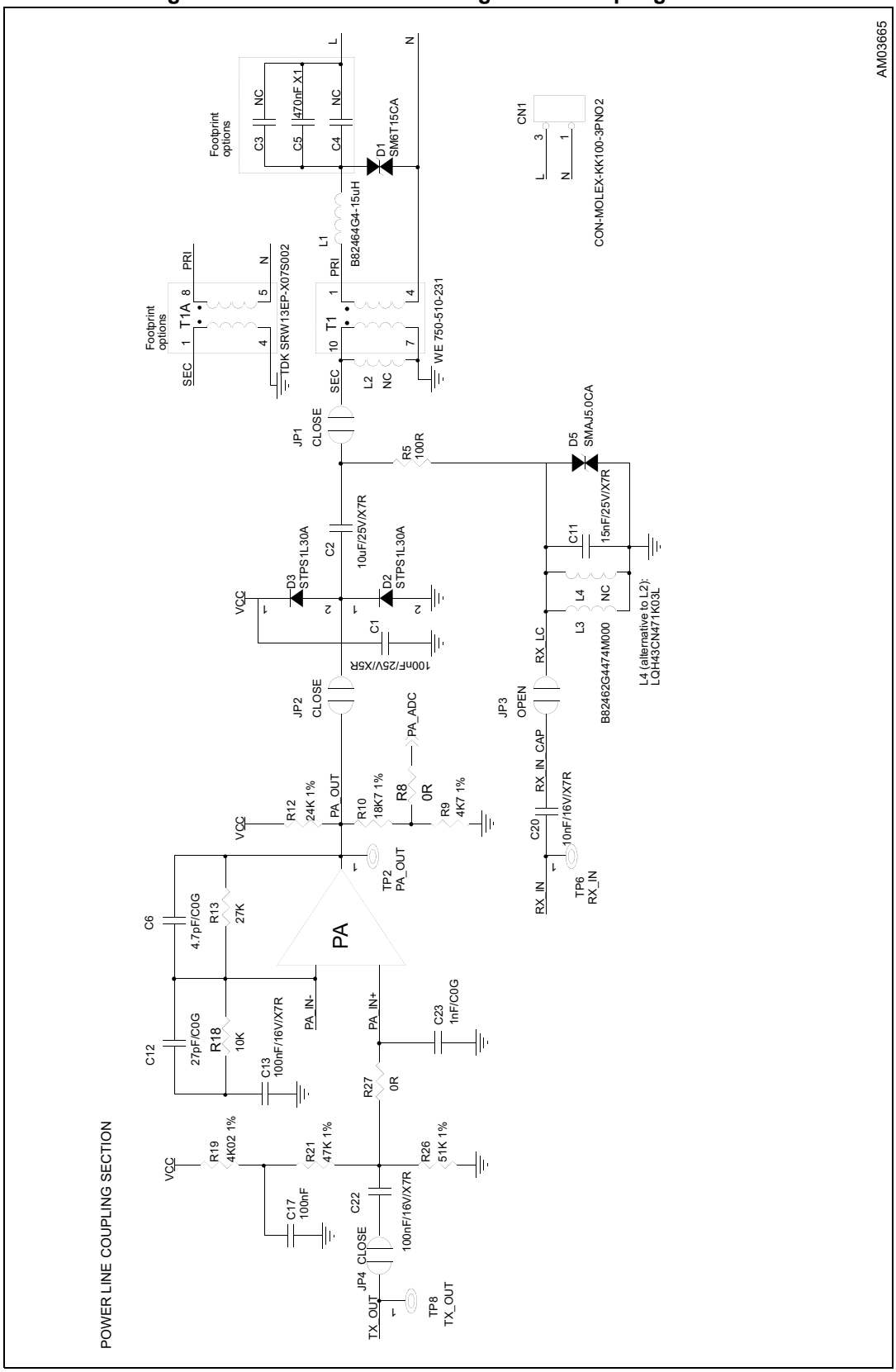


Figure 9. ST7590 reference design - optional zero crossing detection and Rx amplifier circuits

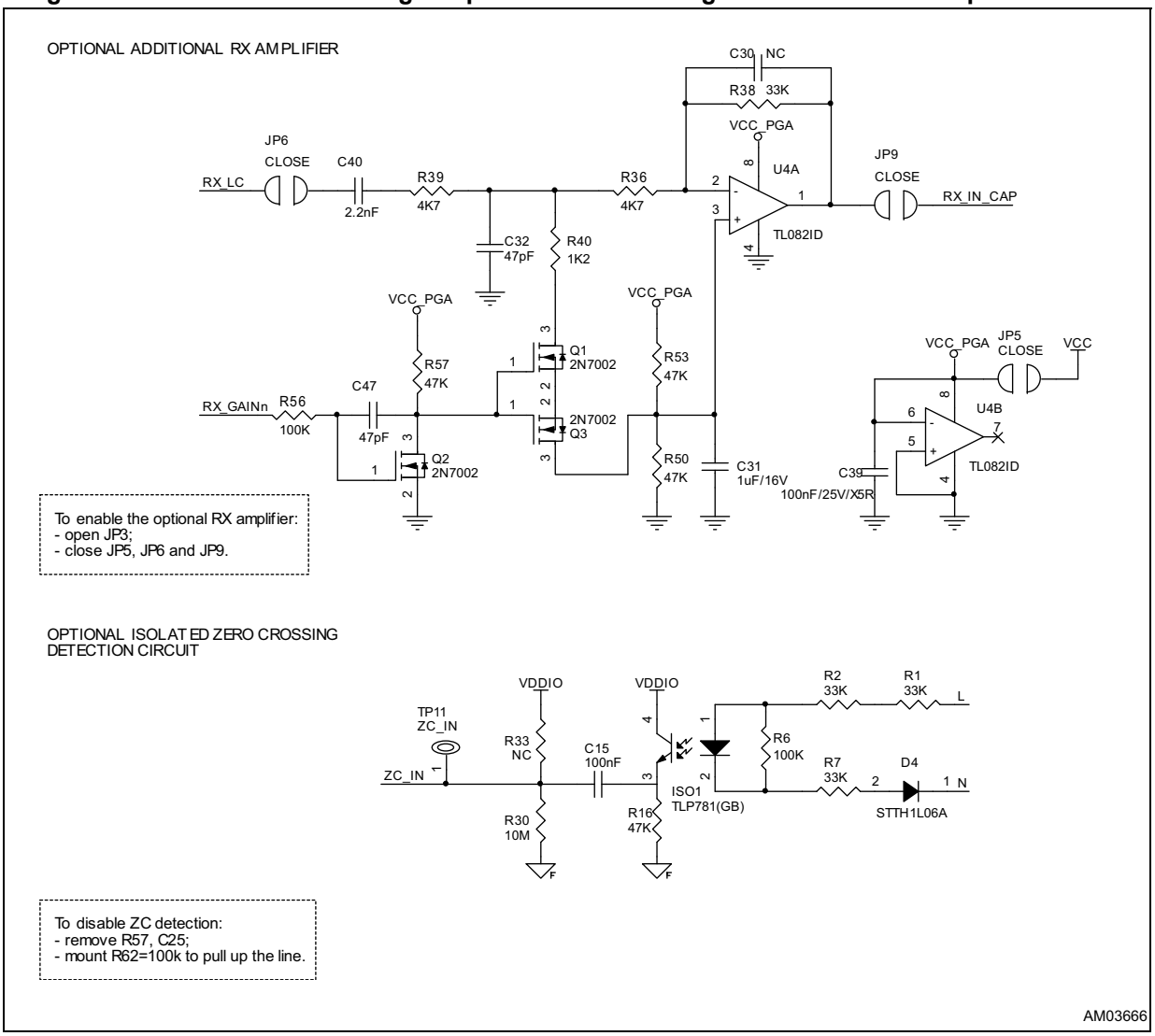


Figure 10. ST7590 reference design - MCU section

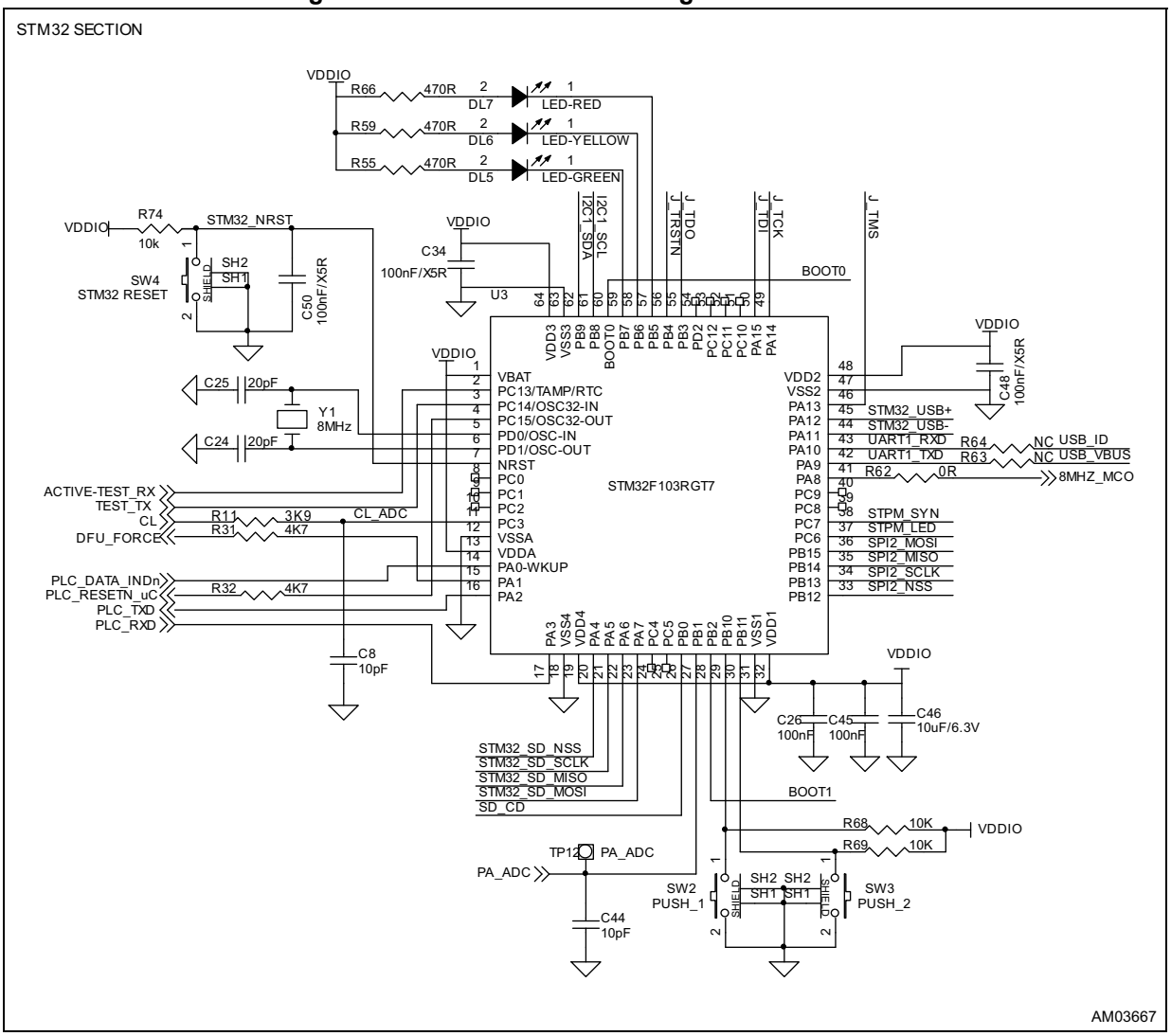


Figure 11. ST7590 reference design - MCU connectivity (part 1)

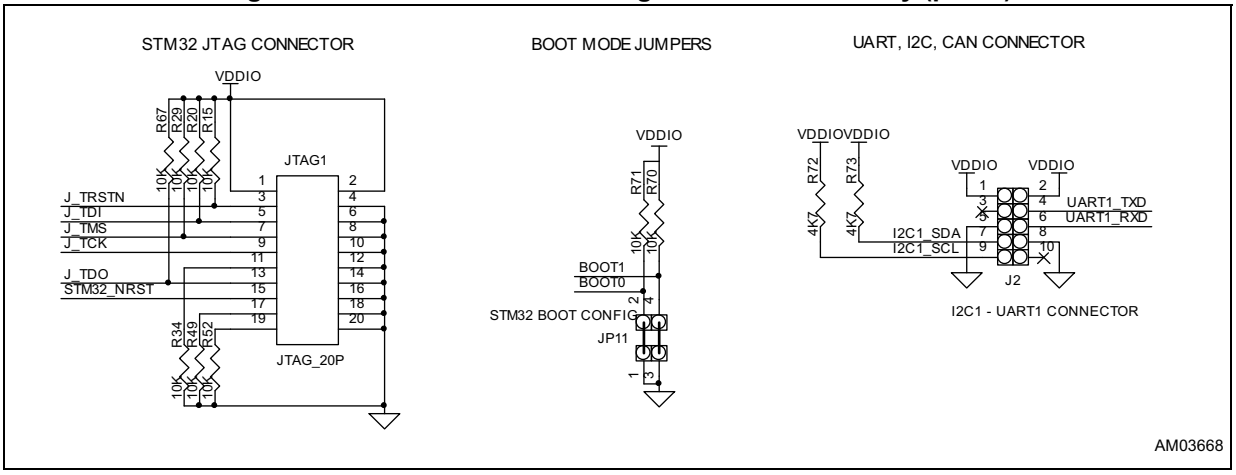


Figure 12. ST7590 reference design - MCU connectivity (part 2)

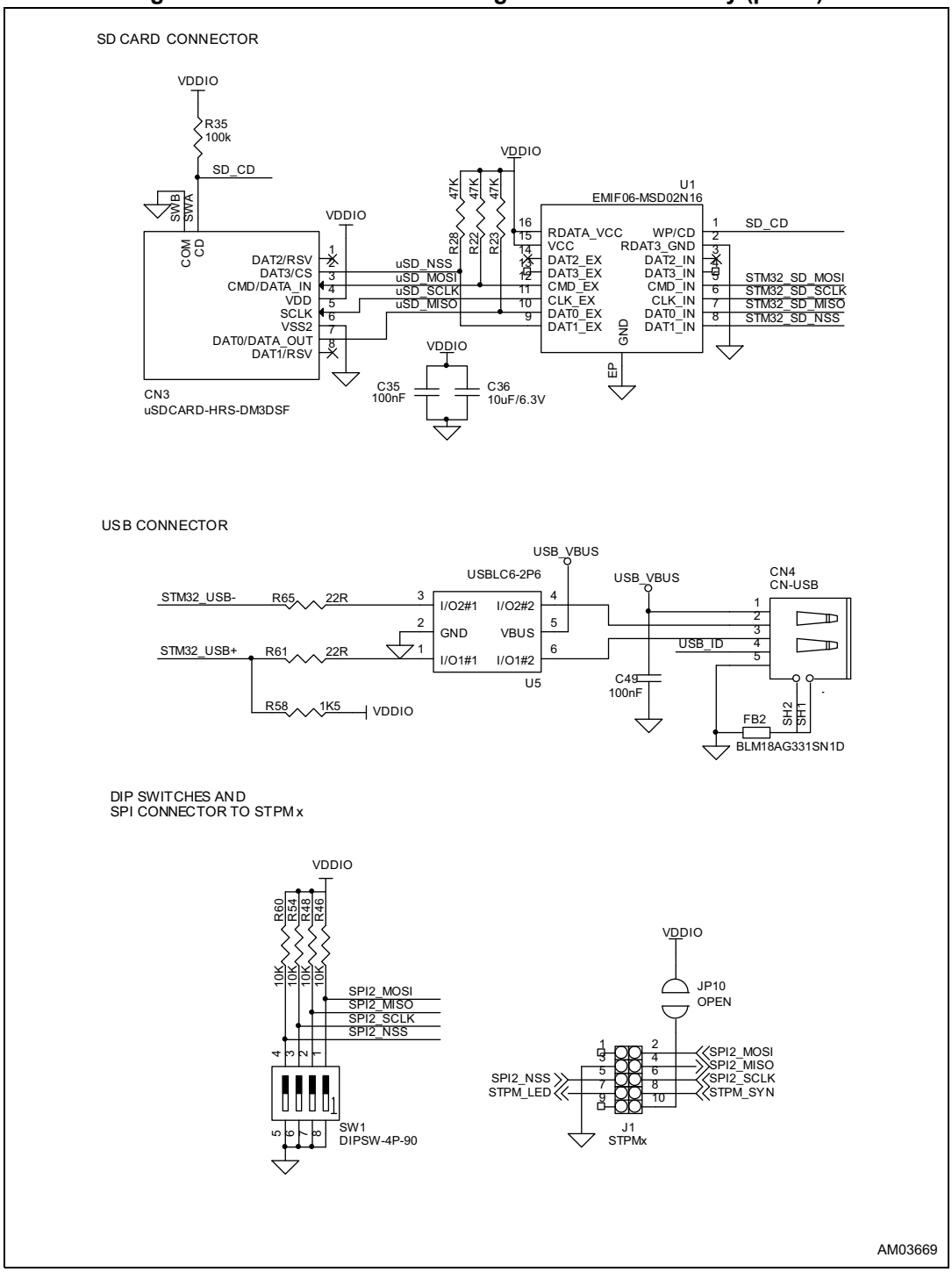


Table 4. Bill of materials

Item	Qty.	Reference	Value	Description
1	1	CN1	CON-MOLEX-KK100-3P	CON-MOLEX-42376-3P-90° (pin 2 removed)
2	1	CN2	CON-MOLEX-KK100-3P	CON-MOLEX-42376-3P-90°
3	1	CN3	µSDCARD-HRS-DM3DSF	µSDCARD-HRS-DM3DSF
4	1	CN4	CN-USB	USBMB-HRS-UX60SC
5	3	C1, C21, C39	100 nF/25 V/X5R	SMD-0402
6	1	C2	10 µF/25 V/X7R	SMD-1206
7	1	C3	NC	
8	1	C4	NC	
9	1	C5	470 nF X1	
10	1	C6	4.7 pF/C0G	SMD-0402
11	4	C7, C16, C36, C46	10 µF/6.3 V	SMD-0603
12	2	C8, C44	10 pF	SMD-0402
13	11	C9, C10, C19, C27, C28, C34, C41, C42, C43, C48, C50	100 nF/X5R	SMD-0402
14	1	C11	15 nF/25 V/X7R	SMD-0402
15	1	C12	27 pF/C0G	SMD-0402
16	2	C13, C22	100 nF/16 V/X7R	SMD-0402
17	1	C14	10 µF/25 V/X5R	SMD-1206
18	6	C15, C17, C26, C35, C45, C49	100 nF	SMD-0402
19	1	C18	100 pF/C0G	SMD-0402
20	1	C20	10 nF/16 V/X7R	SMD-0402
21	1	C23	1 nF/C0G	SMD-0402
22	2	C24, C25	20 pF	SMD-0402
23	1	C29	1 nF/X5R	SMD-0402
24	1	C30	NC	SMD-0402
25	1	C31	1 µF/16 V	SMD-0603
26	2	C32, C47	47 pF	SMD-0402
27	1	C33	4.7 µF/4 V/X5R	SMD-0402
28	1	C37	10 µF/10 V/X5R	SMD-0805
29	1	C38	10 nF/X5R	SMD-0402
30	1	C40	2.2 nF	SMD-0402
31	3	DL1, DL4, DL7	LED - red	SMD-0603
32	3	DL2, DL3, DL5	LED - green	SMD-0603
33	1	DL6	LED - yellow	SMD-0603

Table 4. Bill of materials (continued)

Item	Qty.	Reference	Value	Description
34	1	D1	SM6T15CA(1)	SMB
35	2	D2, D3	STPS1L30A(1)	DO214AC
36	1	D4	STTH1L06A(1)	DIODO-SMA
37	1	D5	SMAJ5.0CA(1)	DIODO-SMA-BIDIR
38	2	FB1, FB2	BLM18AG331SN1D	SMD-0603
39	2	FB3, FB4	BLM21PG331SN1	SMD-0805
40	1	ISO1	TLP781(GB)	Optocoupler
41	4	JP1, JP2, JP4, JP5, JP6, JP9, JP10	CLOSE	2-way solder jumper
42	4	JP3	OPEN	2-way solder jumper
43	1	JP7	6-pin strip connector	
44	1	JP8	4-pin strip connector	
45	1	JP11	CLOSE 1 - 2, 3 - 4	Jumper 2 x 2 - 90°
46	1	JTAG1	JTAG_20P	Flat connector - 10 x 2 - 90°
47	1	J1	STPMx connector	Strip connector - 5 x 2
48	1	J2	I2C1 - UART1 connector	Strip connector - 5 x 2 - 90°
49	1	L1	EPCOS B82464A4153M WE 744776115	SMD power inductor
50	1	L2	NC	
51	1	L3	EPCOS B82462G4474 WE 74477824	SMD power inductor
52	1	L4	NC	
53	3	Q1, Q2, Q3	2N7002	SOT23
54	3	RN1, RN2, RN3	10 KΩ	RESN-CAY10
55	3	R1, R2, R7	33 KΩ	SMD-1206
56	2	R3, R11	3.9 KΩ	SMD-0402
57	4	R4, R55, R59, R66	470 Ω	SMD-0402
58	1	R5	100 Ω	SMD-0603
59	2	R13	27 KΩ	SMD-0402
60	5	R8, R14, R27, R43, R62	0 Ω	SMD-0402
61	1	R9	4.7 KΩ 1%	SMD-0402
62	1	R10	18.7 KΩ 1%	SMD-0402
63	1	R12	24 KΩ 1%	SMD-0402
64	20	R15, R18, R20, R29, R34, R37, R41, R42, R46, R48, R49, R52, R54, R60, R67, R68, R69, R70, R71, R74	10 KΩ	SMD-0402

Table 4. Bill of materials (continued)

Item	Qty.	Reference	Value	Description
65	8	R16, R22, R23, R24, R28, R50, R53, R57	47 KΩ	SMD-0402
66	1	R17	180 Ω	SMD-0402
67	1	R19	4.02 KΩ 1%	SMD-0402
68	1	R21	47 KΩ1%	SMD-0402
69	4	R25, R33, R63, R64	NC	SMD-0402
70	1	R26	51 KΩ 1%	SMD-0402
71	1	R30	10 MΩ	SMD-0402
72	6	R31, R32, R36, R39, R72, R73	4.7 KΩ	SMD-0402
73	3	R6, R35, R56	100 KΩ	SMD-0402
74	1	R38	33 KΩ	SMD-0402
75	1	R40	1.2 KΩ	SMD-0402
76	2	R47, R51	560 Ω	SMD-0402
77	1	R58	1.5 KΩ	SMD-0402
78	2	R61, R65	22 Ω	SMD-0402
79	1	SW1	DIPSW-4P-90	4-line DIP switch
80	1	SW2	PUSH_1	Button - 6 x 6-PTH-90
81	1	SW3	PUSH_2	Button - 6 x 6-PTH-90
82	1	SW4	STM32 RESET	Button - 6 x 6-PTH-90
83	1	SW5	ST7590 RESET	Button - 6 x 6PTH-90
84	1	TP1	CL	
85	1	TP2	PA_OUT	
86	1	TP3	GPIO8	
87	1	TP4	GPIO7	
88	1	TP5	GPIO2	
89	1	TP6	RX_IN	
90	1	TP7	GPIO1	
91	1	TP8	TX_OUT	
92	1	TP9	GPIO6	
93	1	TP10	GPIO0	
94	1	TP11	ZC_IN	
95	1	TP12	PA_ADC	
96	1	TP13	VSS	
97	1	T1	WE 750510231	PLC transformer
		T1A	TDK SRW13EP-X07S002	

Table 4. Bill of materials (continued)

Item	Qty.	Reference	Value	Description
98	1	U1	EMIF06-MSD02N16(1)	EMI / ESD protection - MicroQFN 16L
99	1	U2	ST7590(1)	QFN48 with exposed pad
100	1	U3	STM32F103RGT7(1)	LQFP64
101	1	U4	TL082ID(1)	General purpose dual op amp - SO8
102	1	U5	USBLC6-2P6(1)	SOT-666
103	1	Y1	8 MHz	XTAL-HC49U
104	1	Y2	NC	XTAL-HC49U

1. ST parts on board.

8.1 Line coupling section

The line coupling section is composed of five different subsections: the line driver, the power line coupling, the reception filter, the optional reception amplifier and the zero crossing coupling.

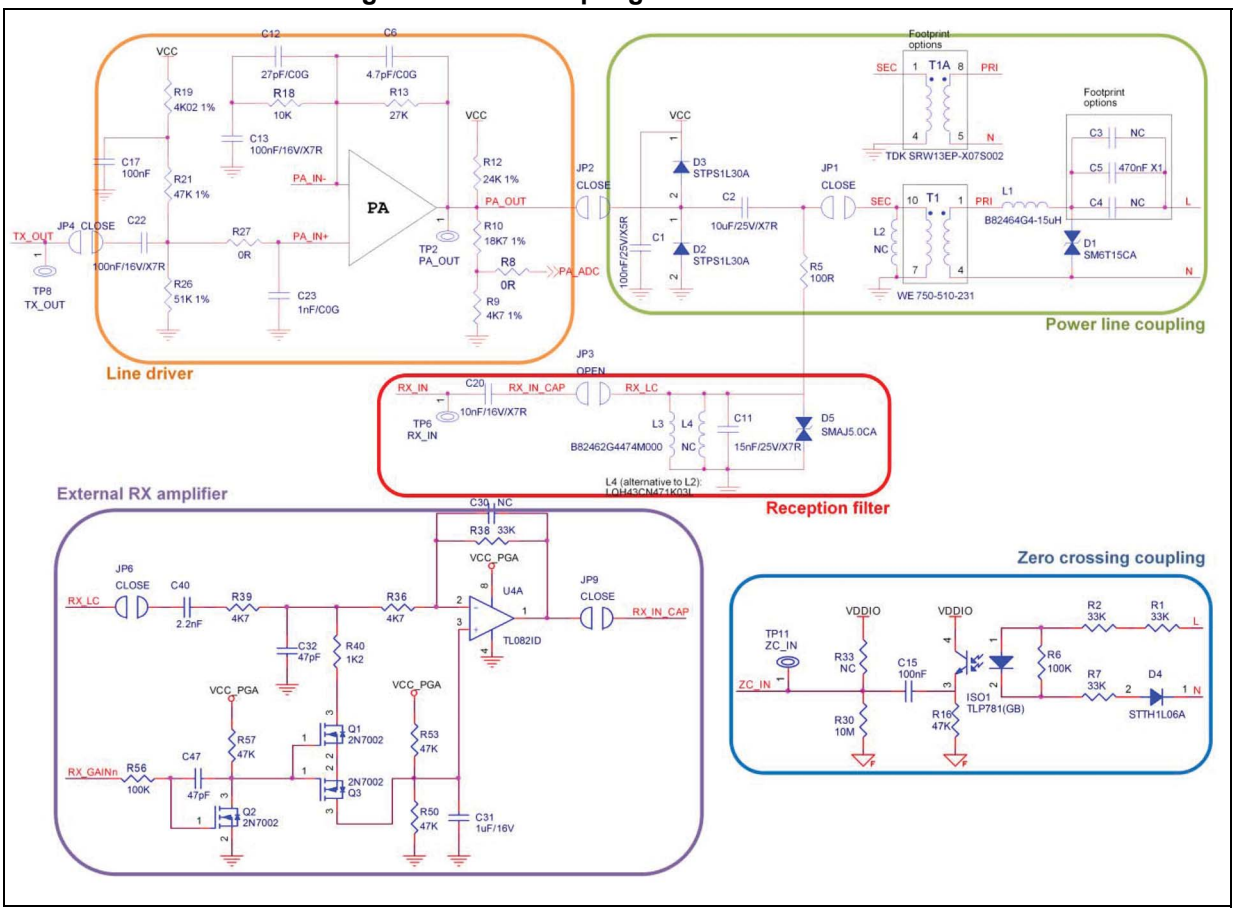
All subsections are described from *Section 8.1.1: Line driver* to *Section 8.1.4: Zero crossing coupling on page 35*. For each subsection, calculations and measured behavior are reported.

The frequency response of the filters is usually sensitive to tolerance of component values. Actual components used in the ST7590 reference design have the following tolerances: ± 20% for the X1 capacitor and the coils, ± 5% for SMD ceramic capacitors, ± 1% for SMD resistors.

To evaluate the sensitivity to these possible variations, simulated responses are also included, with Montecarlo statistical analysis of response variation vs. the spread of component values.

For the line driver, C0G/NPO type capacitors are required to guarantee linearity and stability against signal amplitude and frequency.

Figure 13. Line coupling section schematics



8.1.1 Line driver

The line driver subsection is based on the ST7590 internal “Power Amplifier” (PA), whose input and output pins are externally available to allow configurability of the circuit.

The ST7590 PA has very high linearity, so in this reference design it has been used in all-pass configuration. A simple R-C low-pass network, for minimum out-of-band filtering, is built using the 1 kΩ output resistance of the TX_OUT and capacitor C23, obtaining a corner frequency of 159 kHz.

In the frequencies of interest (PRIME signal band) the capacitors C13, C6 and C12 impedances are negligible with respect to the R18 and R13, so the in-band amplifier gain can be calculated as:

Equation 1

$$\left|G_{TX}\right| = 1 + \frac{R_{13}}{R_{18}} = 3.7 = 11.4\ \text{dB}$$

C13 is used to set the DC gain of the filter to 0 dB (input bias and output bias voltage must be both VCC/2), while *C6* and *C12* provide gain compensation by reducing the gain at high frequencies.

Figure 14 shows the frequency response of the line driver circuit, while *Figure 15* reports the Montecarlo simulation.

Figure 14. Measured frequency response of the line driver (typical)

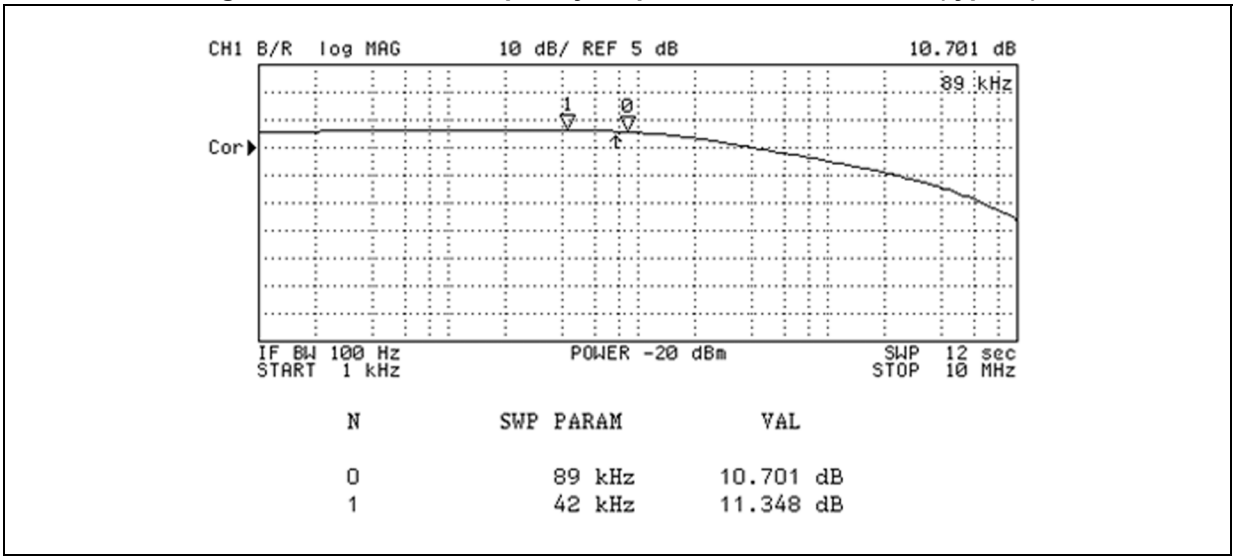
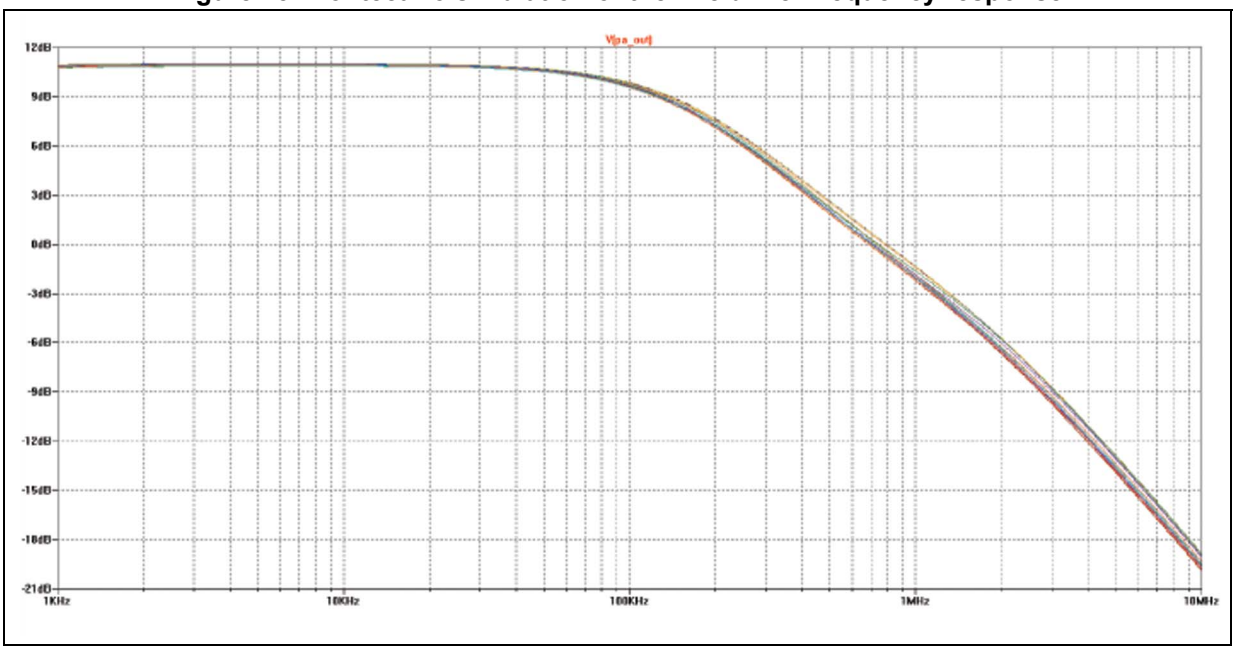


Figure 15. Montecarlo simulation of the line driver frequency response



8.1.2 Power line coupling

The coupling to the power line requires some passive components in addition to the active filtering stage. In particular, it includes the DC decoupling capacitor C2, the line transformer T1, the power inductor L1 and the X1 safety capacitor C5.

L1 has been accurately chosen to have high saturation current (> 2 A) and very low equivalents series resistance (< 0.1 Ω), to limit distortion and insertion losses even with heavy line load.

Center frequency for the series resonance can be calculated at first approximation as:

Equation 2

$$fc = \frac{1}{2\pi\sqrt{L_1' \cdot C_5}} = 58\,\text{kHz}$$

provided that the C2 capacitance is much greater than the C5 capacitance. L_1 is the series of L1 and the leakage inductance of the coupling transformer T1, adding about 1 µH to L1.

The Q factor of this coupling circuit is driven by the mains line impedance: the choice of the L1 and C5 values, anyway, leads to a limited attenuation due to either a parasitic impedance or a resonance selectivity.

If loaded with a 2 Ω line impedance, the coupling circuit shows a Q factor equal to 1.2 and a -3 dB bandwidth of 56 kHz (typical values).

Particular attention has been paid in choosing the line transformer. The required characteristics are listed in *Table 5*. In order to have a good signal transfer and minimize the insertion losses, it is recommended to choose a transformer with a primary (shunt) inductance of 0.5 mH or greater, a leakage inductance much smaller than L1 and a total DC resistance lower than 0.5 Ω.

Table 5. Line coupling transformer specifications

Parameter	Value
Turn ratio	1:1
Shunt inductance	≥ 0.5 mH
Leakage inductance	≤ 1.5 µH
DC total resistance	≤ 0.5 Ω
DC saturation current	≥ 15 mA
Inter-winding capacitance	< 30 pF
Withstanding voltage	≥ 4 kV for double insulation ≥ 1.5 kV for functional insulation

In *Figure 16* the measured response of the whole transmission coupling, loaded with the LISN impedance as set by the EN50065-1 document, is reported. *Figure 16* highlights a slight filtering effect added by the passive L-C series resonant combined with the LISN reactive load.

Figure 17 shows the Montecarlo simulation in the same configuration.

Figure 16. Measured frequency response of the transmission line coupling loaded with the EN50065-1 LISN impedance (typical)

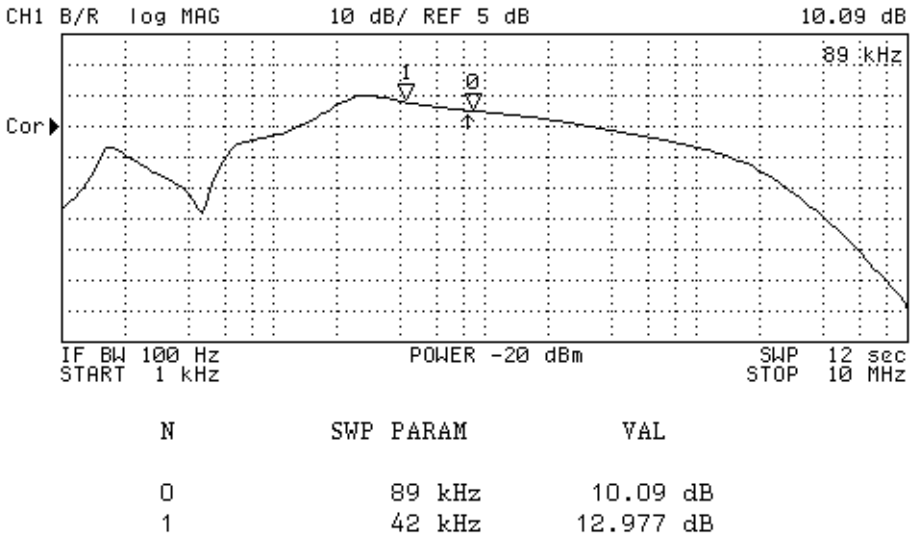


Figure 17. Montecarlo simulation of the transmission line coupling response loaded with the EN50065-1 LISN impedance

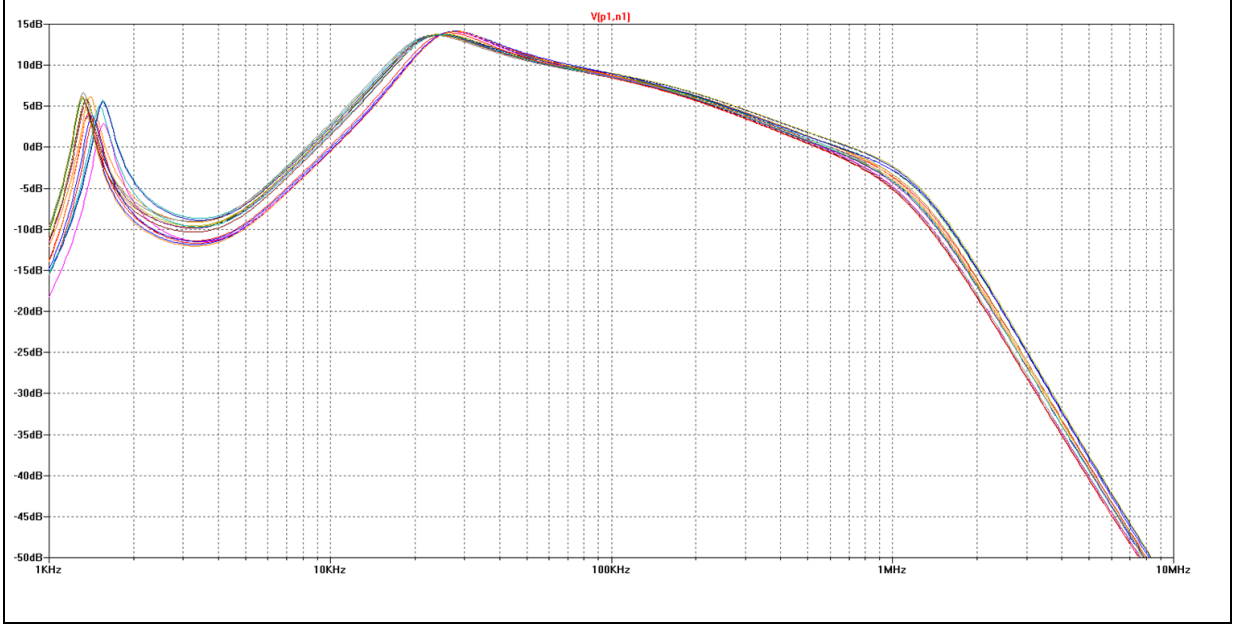


Figure 18 shows the coupling response with a PRIME LISN impedance for PRIME compliance, while *Figure 19* reports the Montecarlo simulation in the same conditions.

Figure 18. Measured frequency response of the transmission line coupling loaded with the PRIME LISN impedance (typical)

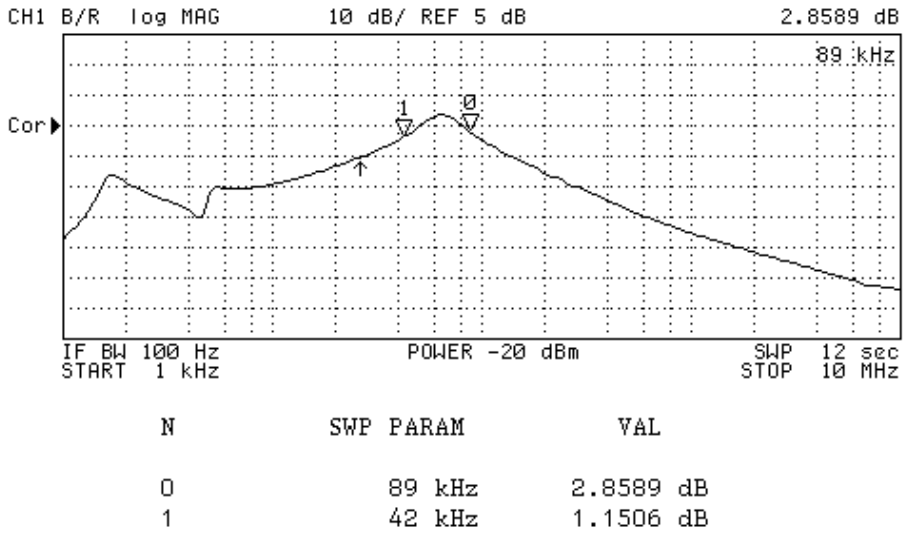
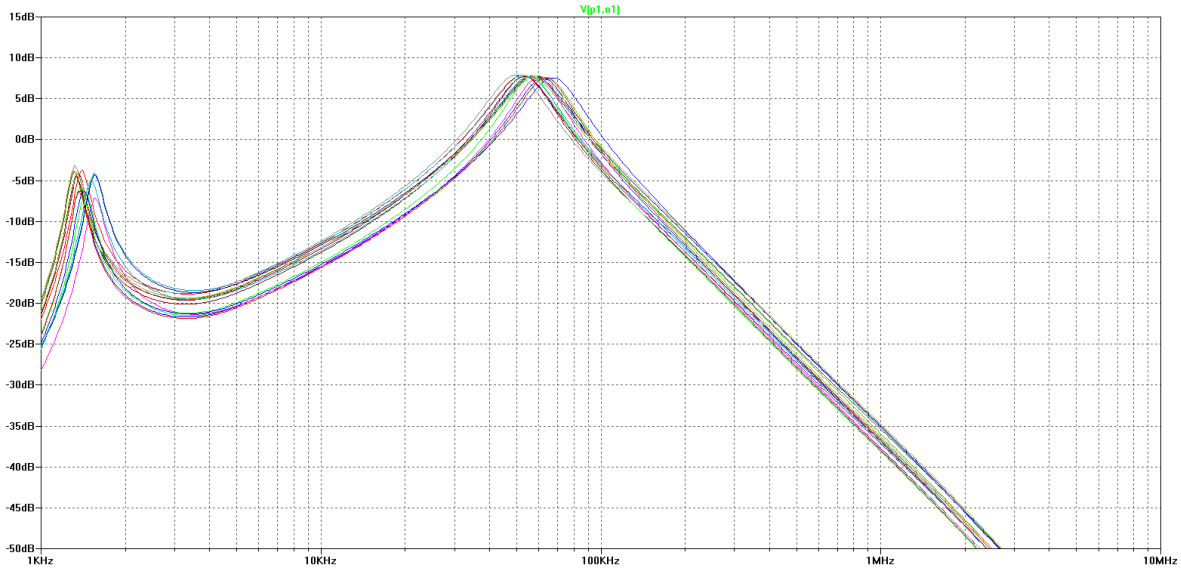


Figure 19. Montecarlo simulation of the transmission line coupling response loaded with the PRIME LISN impedance



8.1.3 Reception filter

Reception passive filter

The reception filter is made of a resistor in series with a parallel L-C resonant. The transfer function of the filter can be written as:

Equation 3

$$R(s) = \frac{\frac{s \cdot L_3 + R_L}{R_5 L_3 C_{11}}}{s^2 + \frac{R_5 R_L C_{11} + L_3}{R_5 L_3 C_{11}} \cdot s + \frac{R_5 + R_L}{R_5 L_3 C_{11}}}$$

where R_L is the DC series resistance of the inductor (with L11 = B82462G4474M000, R_L = 2.7 Ω max).

The center frequency and the quality factor of the filter can be expressed as:

Equation 4

$$fc = \frac{1}{2\pi} \cdot \omega_C = \frac{1}{2\pi} \sqrt{\frac{R_5 + R_L}{R_5 L_3 C_{11}}} \cong \frac{1}{2\pi\sqrt{L_3 C_{11}}} = 60\ \text{kHz}$$

$$Q = \frac{R_5 L_3 C_{11}}{R_5 R_L C_{11} + L_3} \cdot \omega_C = 0.56$$

The quality factor and the filter selectivity depend mainly on R5 value. Lower R5 leads to the lower steepness of the resonance, while higher R5 gives higher selectivity.

R_L value may impact insertion losses. To evaluate the relationship between the R_L and the received signal loss, the following simplified expression can be used:

Equation 5

$$\left|R(j \cdot 2\pi f_C)\right| \cong Q \cdot \frac{\omega_C \cdot L_3}{R_5} = \frac{1}{1 + R_L \cdot R_5 \cdot \frac{C_{11}}{L_3}}$$

With actual values of the components, we get almost unitary transfer at center frequency.

By looking the transfer function formula:

Equation 6

$$Q \cdot \frac{\omega_C \cdot L_3}{R_5}$$

It can be noticed that a higher Q can help keeping the losses small. But a high Q would also bring to a higher sensitivity of the filter to components tolerance.

Figure 20 represents the Rx passive filter frequency response. The filter shows quite flat response in the PRIME signal band (41 - 90 kHz) and null attenuation at f_C. *Figure 21* reports the Montecarlo simulated response.

Figure 20. Measured frequency response of the reception passive filter (typical)

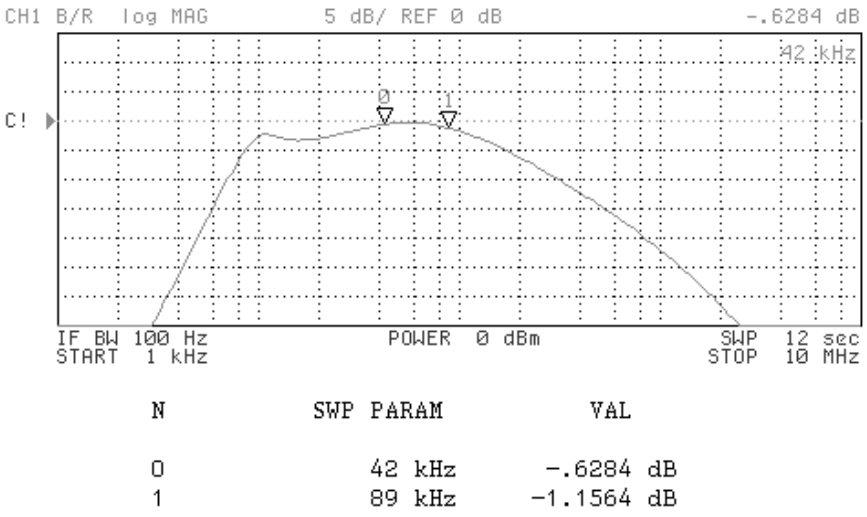
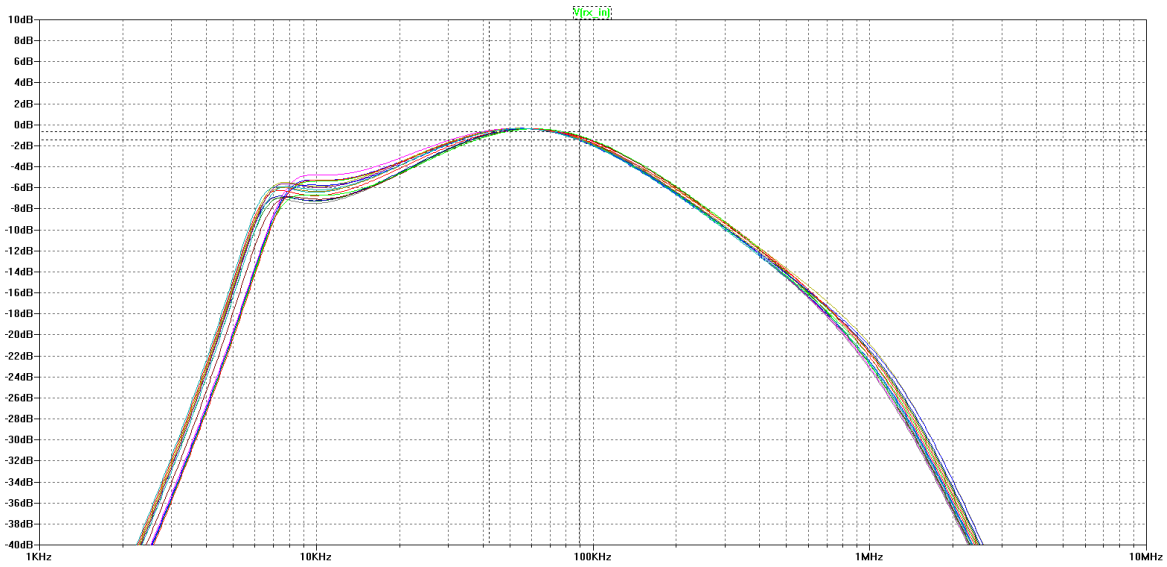


Figure 21. Montecarlo simulation of the reception passive filter response



Reception optional amplifier

An additional all-pass amplifier has been included as an option to extend the dynamic range of the communication.

The gain of the external amplifier only (to be combined with the reception passive filter response) can be calculated as:

Equation 7

$$|G_{RX}| = \frac{R_{38}}{R_{36} + R_{39}} = 3.5 = 10.9 \text{ dB}$$

This extra gain could lead to ST7590 Rx input stage saturation if the input signal is very strong. In that case, an automatic algorithm has been implemented to attenuate the input signal. This attenuation can be calculated as:

Equation 8

$$|G_{RX}| = \frac{R_{36} // R_{40}}{R_{39} + R_{36} // R_{40}} \cdot \frac{R_{38}}{R_{39} + R_{36} // R_{40}} = 0.99 \approx 0 \text{ dB}$$

Figure 22 and *Figure 23* report the measured frequency response in amplification and attenuation cases, compared with the passive filter response. *Figure 24* and *Figure 25* show the result of Montecarlo simulation for the same cases.

Figure 22. Measured frequency response of the reception external amplifier + passive filter (higher curve) vs. reception passive filter only (lower curve)

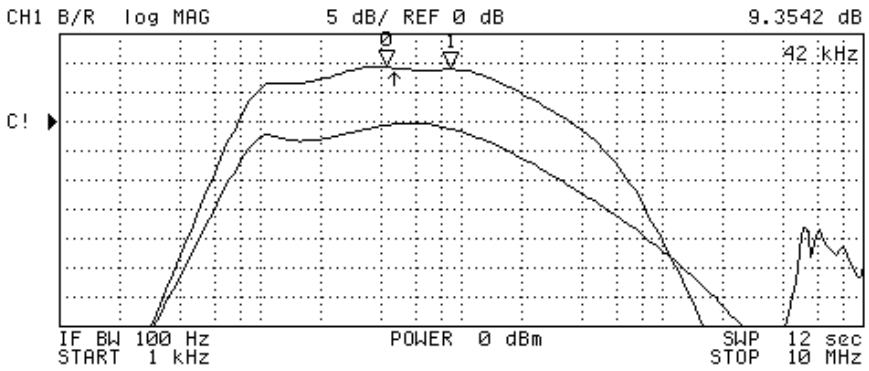


Figure 23. Measured frequency response of the reception external amplifier with automatic attenuation (dark curve) vs. reception passive filter (light curve)

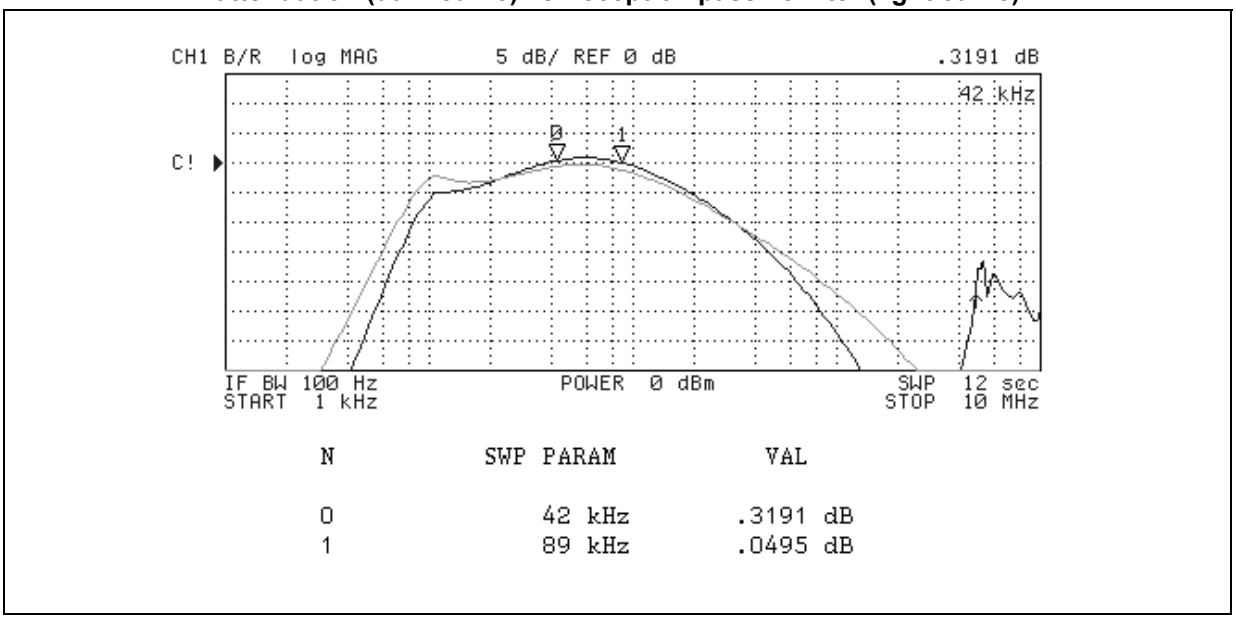


Figure 24. Montecarlo simulation of the reception external amplifier

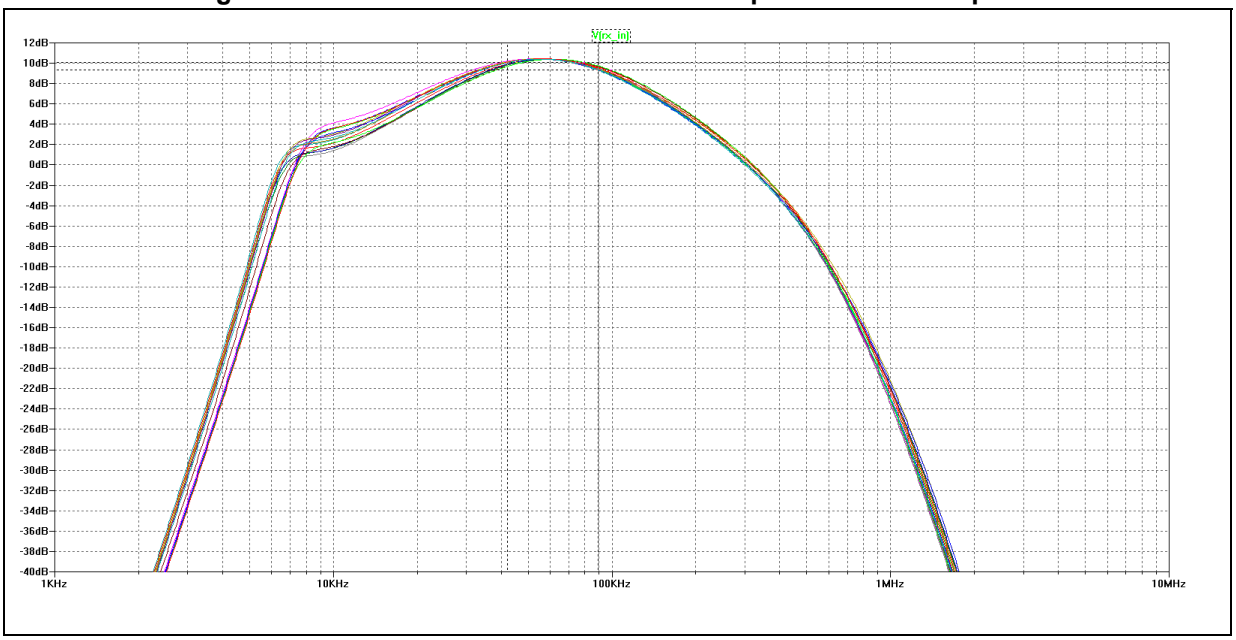
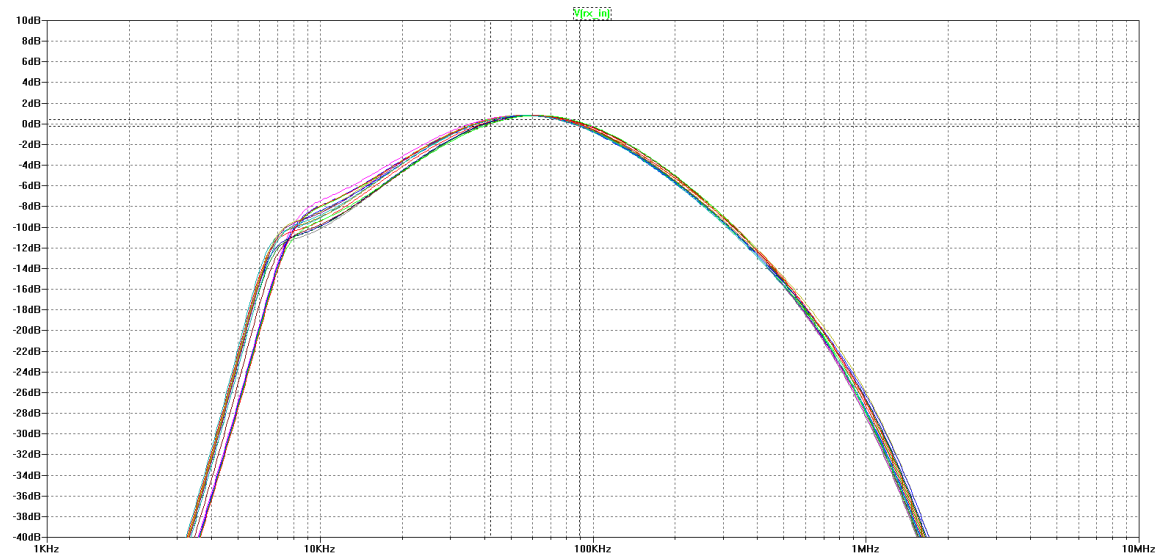


Figure 25. Montecarlo simulation of the reception external amplifier with automatic attenuation

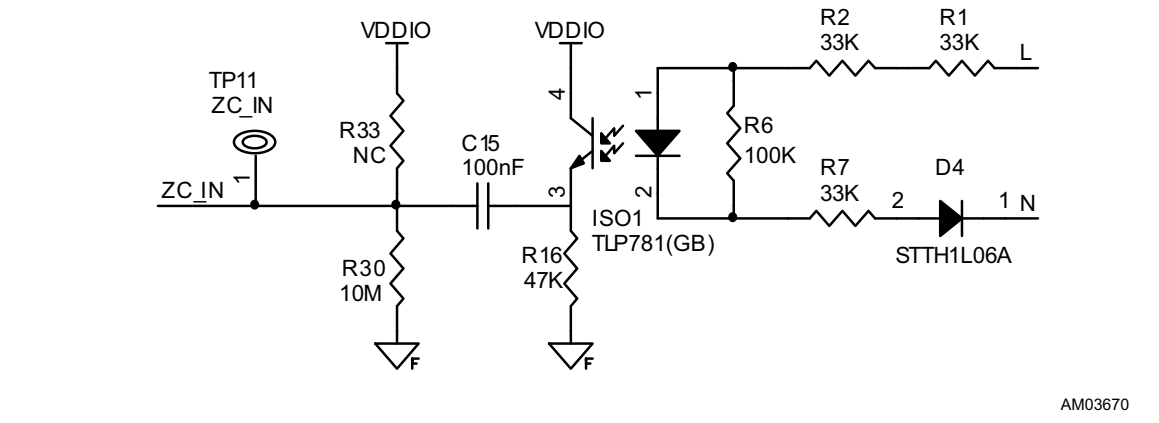


8.1.4 Zero crossing coupling

The zero crossing coupling circuit is aimed at providing a bipolar (AC) signal synchronous with the mains network voltage to the ZC_IN pin. This signal must be centered on VSS and limited to ± 5 V peak (see Part 1 of *Section 13: References on page 63*).

The isolated zero crossing circuit is realized through an optocoupler in non-inverting configuration. Neutral and phase lines are brought to the optocoupler through 33 kΩ resistors in series, as represented in *Figure 26*. The STTH1L06A diode protects photodiode during negative half-wave. The three 33 kΩ series resistors limit the photodiode input current to nearly 2 mA rms at 230 V AC. Having two resistors on the L line helps preventing short-circuits in case of resistor degradation.

Figure 26. Isolated zero crossing coupling circuit



The timing characteristics of this circuit, according to the oscilloscope screenshots reported below, are listed in *Table 6*.

Table 6. Zero crossing coupling - measured timing characteristics

Edge	ZC delay	ZC jitter
Positive	478 µs	50 µs
Negative	210 µs	48 µs

Figure 27. Zero crossing coupling - positive edge delay

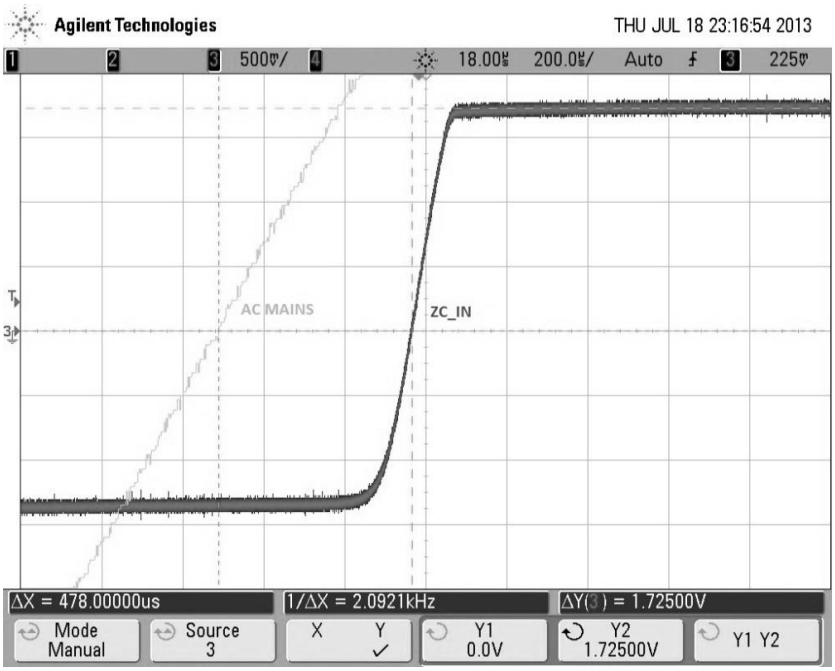
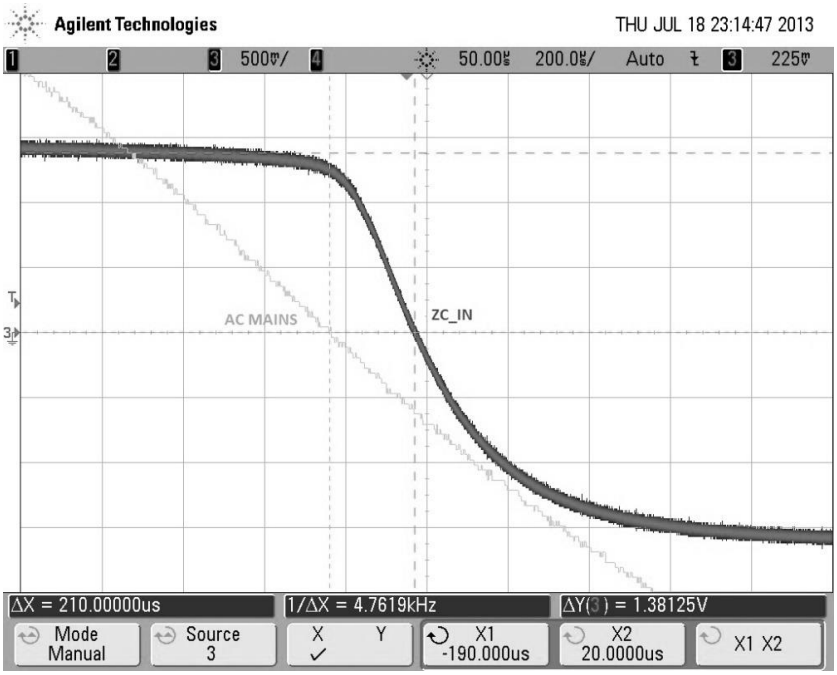


Figure 28. Zero crossing coupling - negative edge delay



8.2 STM32 section

The EVALKITST7590-Q1 is equipped with an STM32F103RGT7 device, a medium-density ARM® based 32-bit microcontroller.

For complete information on device characteristics, please refer to Part 3 of *Section 13: References on page 63*.

On the EVALKITST7590-Q1 board, the STM32F103RGT7 microcontroller can be used for following purposes:

- Handle the ST7590 device through direct connections
- External access through several interface types: USB, SPI, I^2C, USART, JTAG
- Store and read data to/from an external µSD card
- Develop test functions

On the EVALKITST7590-Q1, the STM32 microcontroller shares its VDD supply voltage with the VDDIO digital supply of the ST7590 device.

A dedicated 8 MHz crystal has been provided with two suitable load capacitors according to recommendations in Part 4 of *Section 13: References on page 63*.

8.2.1 Connections between STM32 microcontroller and ST7590

The STM32F103 microcontroller provides connections to the ST7590 device for both digital and analog parts. These connections involve several pins and features of the ST7590 modem, as listed in *Table 7*.

Table 7. Connections between STM32F103RGT7 and ST7590 devices on EVALKITST7590-Q1 board

Connection	Connection type	ST7590 pins	STM32F103 pins	Notes
Host interface	Digital	MISO0_RXD	PA2	See Part 2 of *Section 13: References on page 63*.
		MOSI0_TXD	PA3	
		GPIO9	PA0/WKUP	
Reset	Digital	RESETN	PC15	This direct connection allows the STM32 microcontroller driving the RESETN pin of the ST7590 device.
Clock	Digital	XIN	PA8	The connection must provide an 8 MHz clock signal to the ST7590 modem in accordance with specifications in Part 1 of *Section 13: References on page 63*.
Power line communication activity	Digital	GPIO5	PC13	As the two lines give information about power line communication activity of the ST7590, the connections can be used as input data for the STM32.
		GPIO3	PC14	
Transmitted power line signal levels	Analog	PA_OUT	PB1	The connection allows the STM32 monitoring the ST7590's PA_OUT voltage level. The connection is realized through a suitable partition (between two high values 1% tolerance resistors) to properly limit the signal level within the STM32 input range.
CL voltage level	Analog	CL	PC3	The connection allows the STM32 to monitor the ST7590's CL pin voltage level and to extract information about the ST7590 output current during power line transmission.

8.2.2 Digital interfaces to STM32

The EVALKITST7590-Q1 allows accessing the STM32F103RGT7 microcontroller via its available interfaces:

- Serial wire/JTAG debug , that enables either a serial wire debug or a JTAG compliant debug through a JTAG1 connector
- USB 2.0 full speed through a mini-USB CN4 connector
- 2 SPI interfaces:
  - One is used to access an external µSD card with FAT32 support through a µSD CN3 connector
  - The second one works at 18 Mbit/s and presents the SPI signals at a J1 strip connector.
- I^2C
- A second UART (TXD and RXD signals), besides the one used for ST7590 connections

I^2C and UART signals are accessible through the same double strip connector J2.

The NRST signal is externally accessible through a push-button.

8.2.3 Metrology interface to STM32

The EVALKITST7590-Q1 provides a free STM32 SPI interface at a J1 strip connector. This SPI is available for connection to STPMxx metrology boards. Note that DIP switches must be opened when a metrology board is connected.

8.2.4 General purpose push-buttons and LEDs

The EVALKITST7590-Q1 provides configurable input and output connections to the STM32F103 microcontroller for both externally generated events and signaling purposes. In fact, the board presents:

- 3 signaling LEDs, connected to PB5, PB6, PB7 outputs
- 2 push-buttons connected to PB10, PB11, to generate manually events triggering programmable functions.

9 Reference design standard tests

9.1 Input impedance

The input impedance of a power line communication node is another critical point. According to the network impedance measurements carried out in some European distribution networks (Italy, Germany and France) the following characteristics can be associated to the impedance of a typical low voltage (LV) power line:

- Typical impedance magnitude is around 5 Ω
- Nearly 90% of measured values range between 0.5 and 10 Ω
- The impedance value depends on the measurement point
- The measured value changes over time.

The reasons for these characteristics can be described as follows:

- The LV distribution network has a “tree” structure, with many branches and sub-branches acting as parallel impedances
- Several electronic devices connected to the LV network offer a very low impedance, mostly because of the EMI input filters installed at their mains connection
- The type and number of electronic loads connected to the mains network varies over time.

For all these reasons, particular attention must be paid to the impedance of the ST7590 line coupling circuit. Specifically:

- In receiving (idle) mode, the coupling impedance must be high enough to make the power line source impedance negligible and to minimize the mutual interference between different PLC nodes connected to the same network
- In transmitting mode, the coupling impedance must be very low inside the signal bandwidth but high enough for out-of-band frequencies.

According to such requirements, the EN50065-7 standard document fixes the following constraints for the PLC node operating in the A band (see Part 7 of *Section 14: Normative references on page 63*):

In Rx mode, minimum impedance is:

- 10 Ω from 3 to 9 kHz
- 50 Ω between 9 and 95 kHz only inside the signal bandwidth (free for frequencies outside the signal bandwidth), which means 50 Ω minimum from 42 KHz to 89 kHz for the ST7590 device
- 5 Ω from 95 to 148.5 kHz.

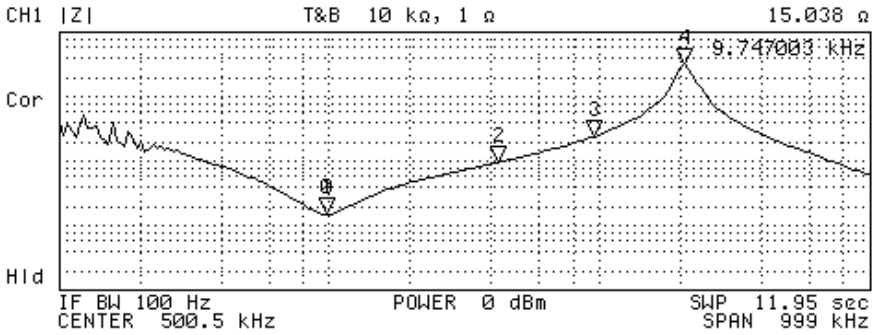
In Tx mode, minimum impedance is:

- Free in the range 3 to 95 kHz
- 3 Ω from 95 to 148.5 kHz.

Figure 29, *Figure 30* and *Figure 31* show the input impedance magnitude vs. frequency measured in the transmission and reception mode.

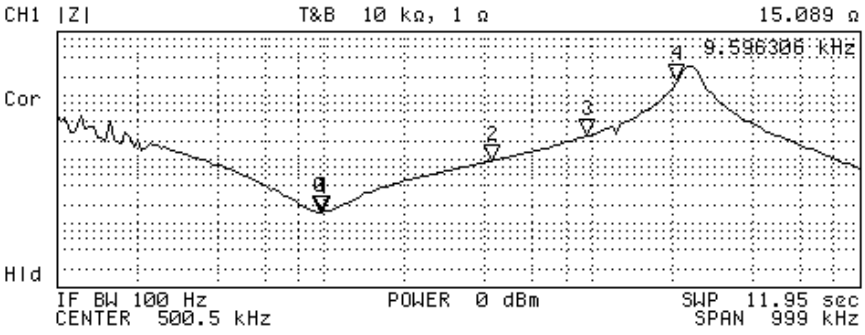
The impedance magnitude values prove that the ST7590 reference design is compliant with the EN50065-7 requirements. At the same time, the line interface gives an efficient signal coupling both in transmission and reception.

Figure 29. Measured input impedance of the line coupling - reception mode



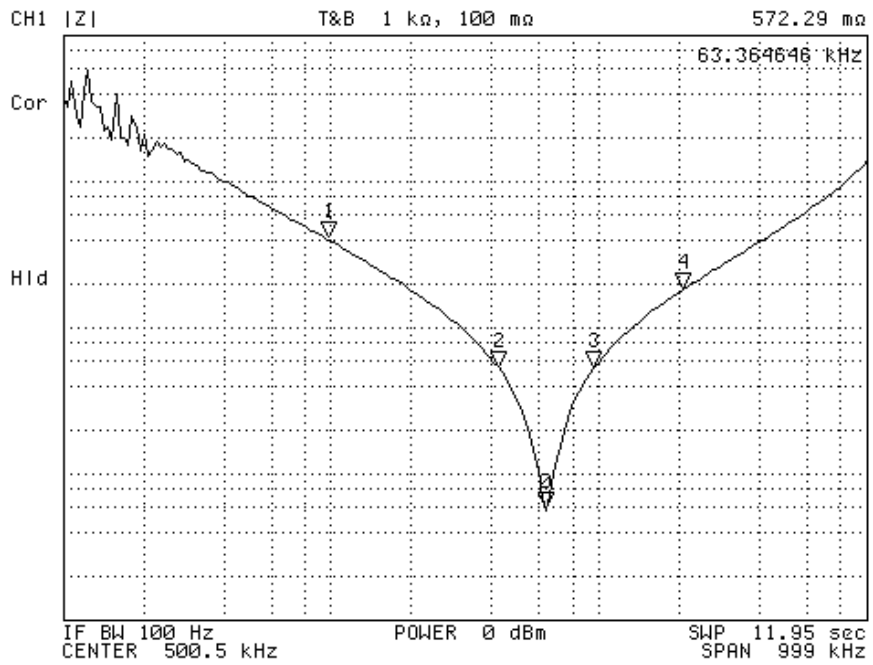
N	SWP PARAM	VAL
0	9.747003 kHz	15.038 Ω
1	9.696539 kHz	15.064 Ω
2	42 kHz	94.622 Ω
3	95.017077 kHz	238.32 Ω
4	207.637627 kHz	3.0891 kΩ

Figure 30. Measured input impedance of the line coupling - reception mode (with optional Rx amplifier)



N	SWP PARAM	VAL
0	9.596306 kHz	15.089 Ω
1	9.696539 kHz	15.061 Ω
2	42 kHz	94.817 Ω
3	95.017077 kHz	229.71 Ω
4	207.637627 kHz	1.7038 kΩ

Figure 31. Measured input impedance of the line coupling - transmission mode



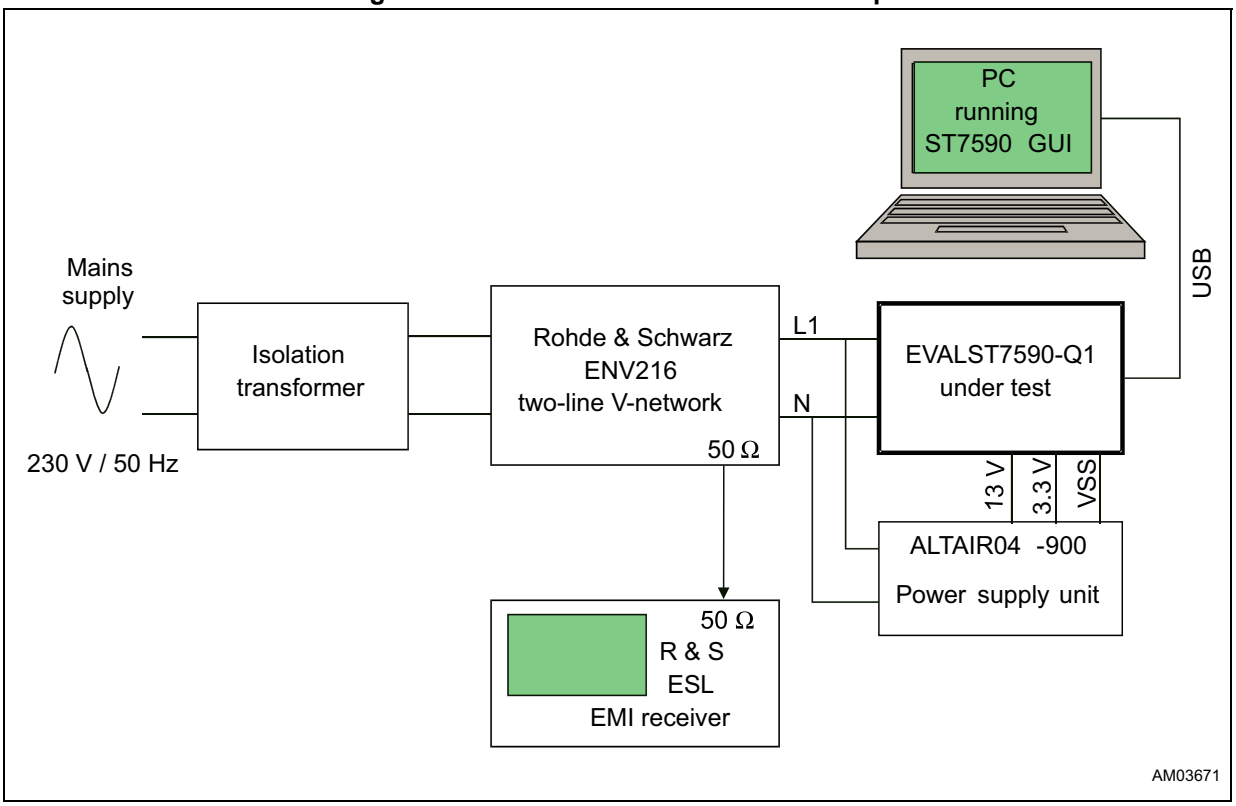
9.2 Conducted emission (CE) measurements

The EN50065-1 standard describes the test setup and procedures for this kind of tests (see Part 1 of *Section 14: Normative references on page 63*).

The compliance tests have been performed in the following conditions:

- Mains voltage = 230 V AC (isolated supply)
- Output signal level = 12 V peak-to-peak (maximum output level for the ST7590 GUI) corresponding to 1.5 V rms
- Mode = BPSK uncoded
- PHY payload length = 256 bytes
- Duty cycle = 55 / 180 ms = 30 %.

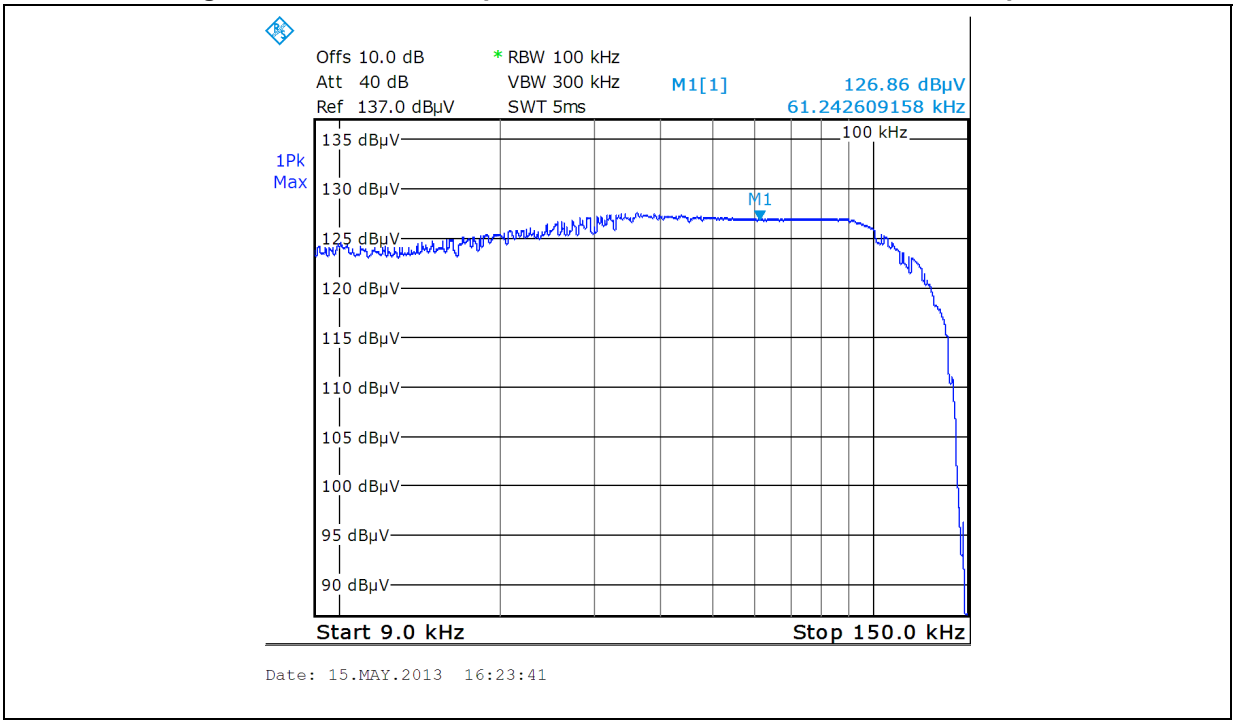
Figure 32. Conducted emissions test setup



The conducted emissions measurement results are reported from *Figure 34* to *Figure 37*. Quasi-peak and average measurements have been performed, as required by the EN50065-1 standard document. The measured spectrum is always compared to the EN50065-1 compliance limit mask.

9.2.1 Maximum output level

Figure 33. Maximum output level on EN50065 AMN measurement port



9.2.2 Conducted emissions

Figure 34. 3 - 150 kHz conducted emissions on EN50065 AMN line measurement port

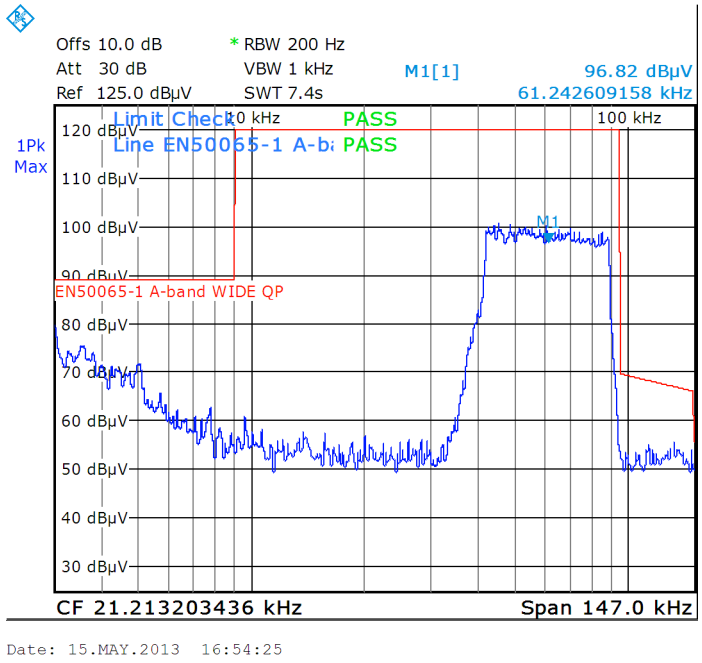


Figure 35. 3 - 150 kHz conducted emissions on EN50065 AMN neutral measurement port

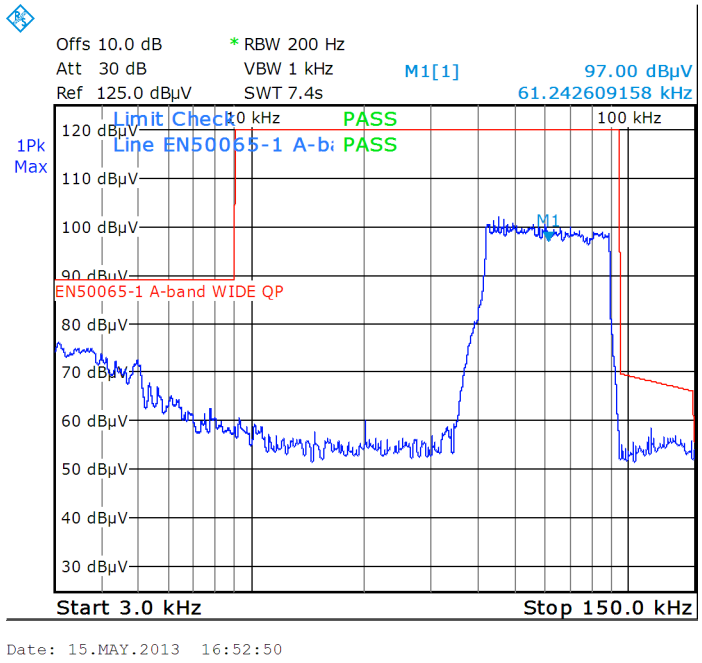


Figure 36. 150 kHz - 30 MHz conducted emissions on EN50065 AMN line measurement port

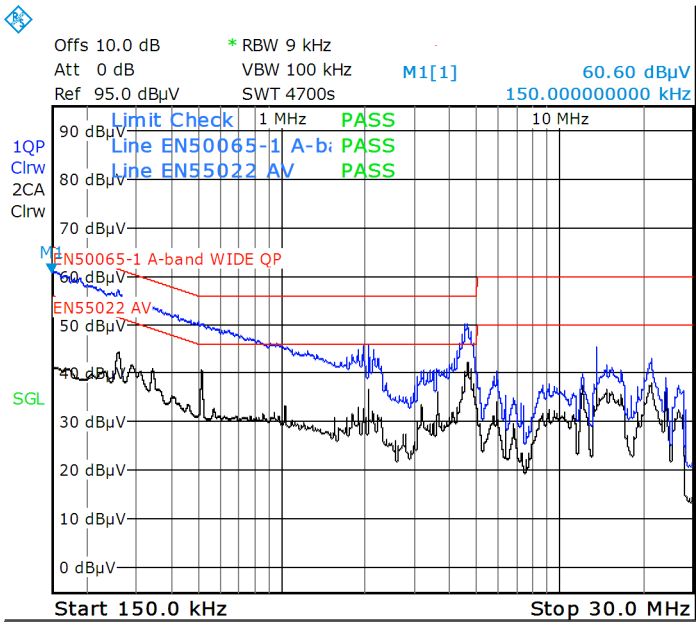
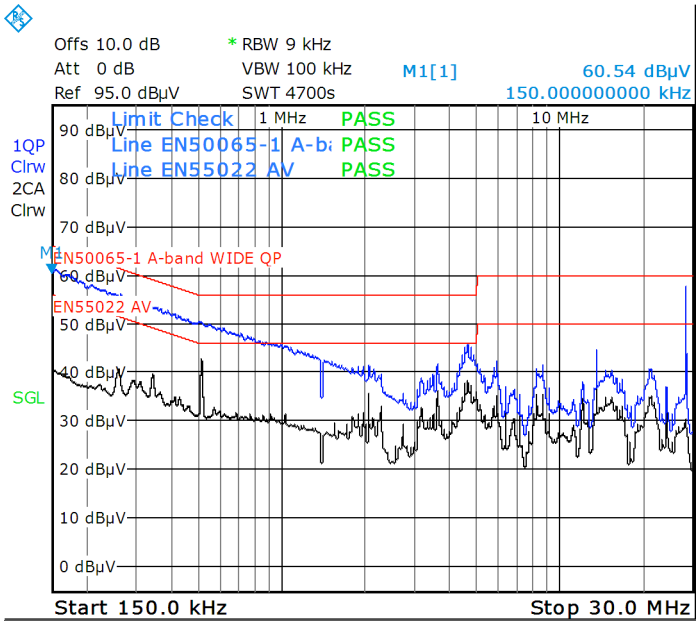


Figure 37. 150 kHz - 30 MHz conducted emissions on EN50065 AMN neutral measurement port



9.3 EMI immunity tests

The specific structure of the coupling interface circuit of the application is a weak point against high voltage disturbances that can come from the external environment. In fact an efficient coupling circuit with low insertion losses realizes consequently a low impedance path from the mains to the power line interface of the device.

For this reason it is recommended to add some specific protections on the mains coupling path, to prevent high energy disturbances coming from the mains from damaging the internal power circuitry of the ST7590.

Possible environments for this kind of application can be both indoor and outdoor: residential, commercial and light industrial locations. To verify the immunity of the system to environmental electrical phenomena, a series of immunity specification standard and tests must be applied to the power line application.

The immunity requirements for any PLC metering application, communicating in the European A band (9 - 95 kHz), are listed in the EN50065-2-3 document, which refers to the EN61000 and ENV50204 for tests to be applied (see Part 2 - 3 of *Section 14: Normative references on page 63*).

These standards include surge tests, both common mode and differential mode (± 4 kV peak, t_R = 1.2 µs, t_N = 50 µs) and fast transient (burst) tests (± 2 kV peak, t_R = 5 ns, t_H = 50 ns, repetition frequency 5 kHz).

For the application to be able to withstand such a severe electrical overstress, the line coupling capacitor C5 must be an X1 or Y2 type part, rated for 4 kV or higher pulses.

In case of non-metering applications, communicating outside the A band, the requirements are listed in the EN50065-2-1 document, which sets lower pulse levels.

Beside the line coupling capacitor, safety and robustness of the application are guaranteed by protection devices included in the board design, such as an input varistor (MOV) and protection diodes. The effect of the protection diodes is described below.

Figure 38 and *Figure 39* show the protection against common mode disturbances. The low-drop Schottky diodes D2 and D3 are able to absorb quickly fast transient disturbances exceeding the supply rails.

Figure 38. Common mode disturbance protection - positive disturbance

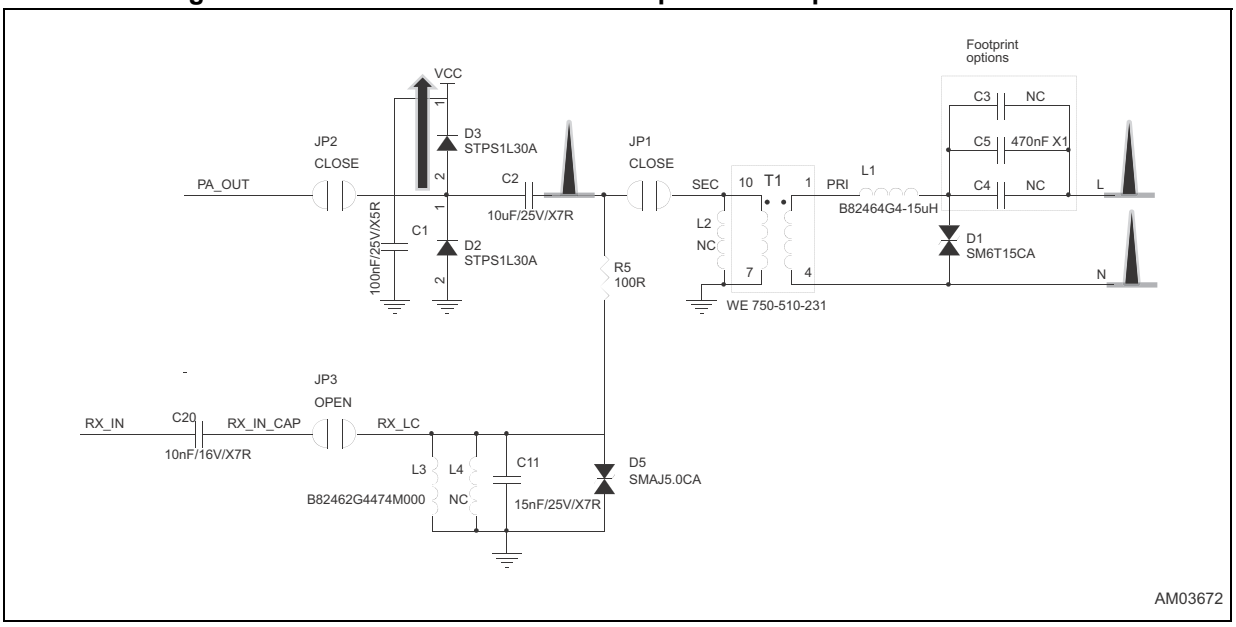


Figure 39. Common mode disturbance protection - negative disturbance

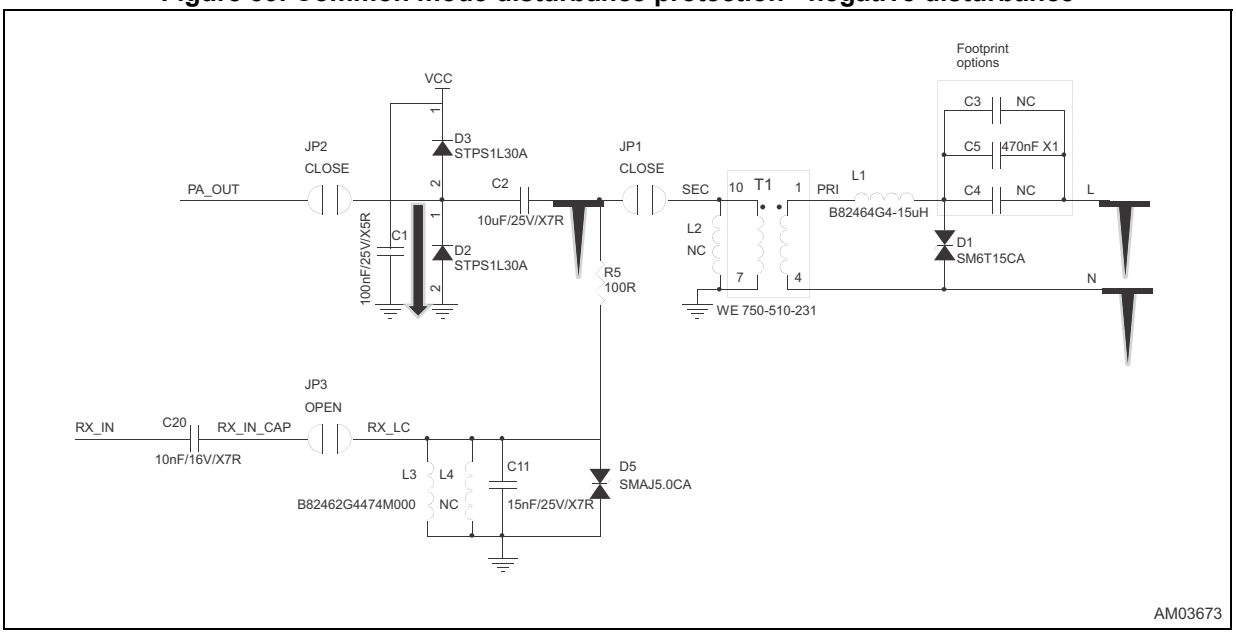
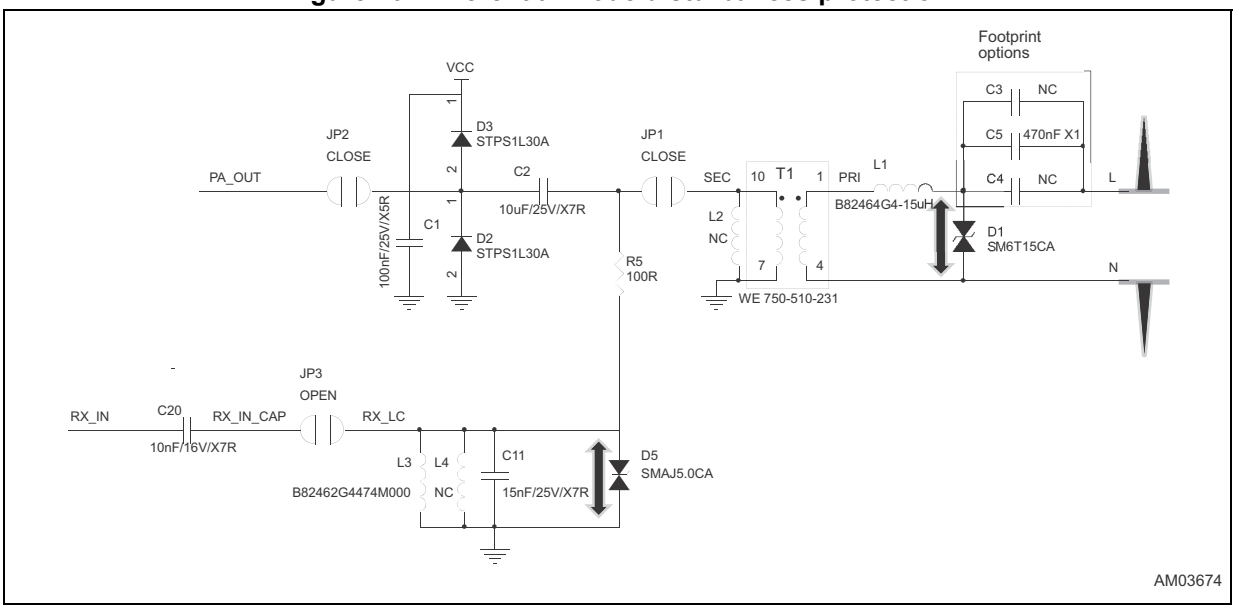


Figure 40 describes the protection intervention in case of differential mode disturbances. A differential voltage higher than 15 V p-p is clamped by the D1 bidirectional Transil™ diode. The D1 is the most robust protection and also the one that is able to absorb most of the energy of any incoming disturbance.

Figure 40. Differential mode disturbances protection



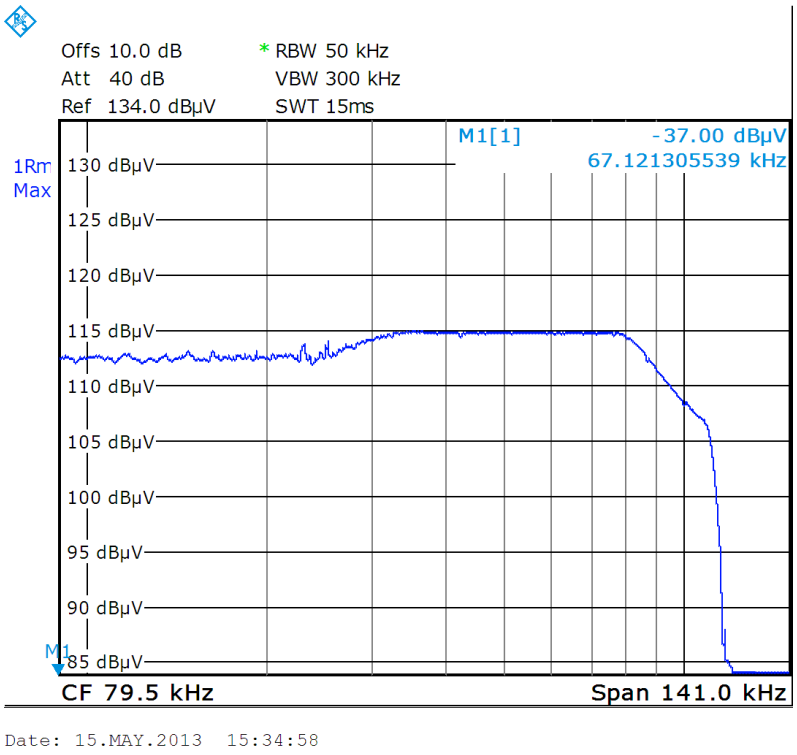
9.4 PRIME pre-compliance tests

Minimum output level over PRIME LISN

The ST7590 reference design is capable to provide a 121 dBµV over PRIME LISN, thus complying with the 120 dBµV minimum level set by PRIME specifications.

Note that, as indicated by PRIME specifications, the measurement result is 6 dB lower than the actual value, being it measured between the line and ground (half signal power).

Figure 41. Output level on PRIME LISN measurement port with EVALKITST7590-Q1



10 Design guidelines

10.1 PCB layout guidelines

10.1.1 Thermal performance

The ST7590 device can operate within the standard industrial temperature range, from -40 to 85 °C ambient temperature. Especially in high ambient temperature conditions, the effect of the power dissipation of the device must be considered to keep it operating in safe conditions.

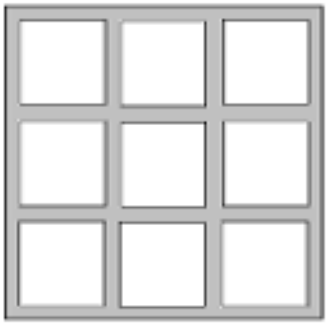
Even if the ST7590 features a built-in thermal shutdown circuitry which turns off the power amplifier (P_A) when the die temperature (T_J) exceeds 150 °C, it is recommended not to exceed 125 °C during normal operation to ensure the functionality of the IC.

A QFN48 package with an exposed pad has been chosen for the ST7590 device to have a very good thermal performance. However, in order to take full advantage from this, the PCB must be designed to effectively conduct heat away from the package.

To get a low impedance thermal path to the PCB, a 5 x 5 mm thermal pad has been realized on the top layer under the device. In order to effectively remove the heat, the exposed pad must be well soldered to the PCB thermal pad. Therefore, the out-gassing phenomenon due to the soldering process must be controlled to reduce solder voids between the QFN48 exposed pad and the PCB thermal pad. To achieve this, smaller multiple openings in the solder paste stencil should be used instead of one big opening on the thermal pad region. This has also the advantage to reduce the amount of solder paste used, thus avoiding bridges with perimeter pads.

A suitable example for the QFN48 package is shown in *Figure 42*.

Figure 42. Example of stencil openings for the QFN48 package



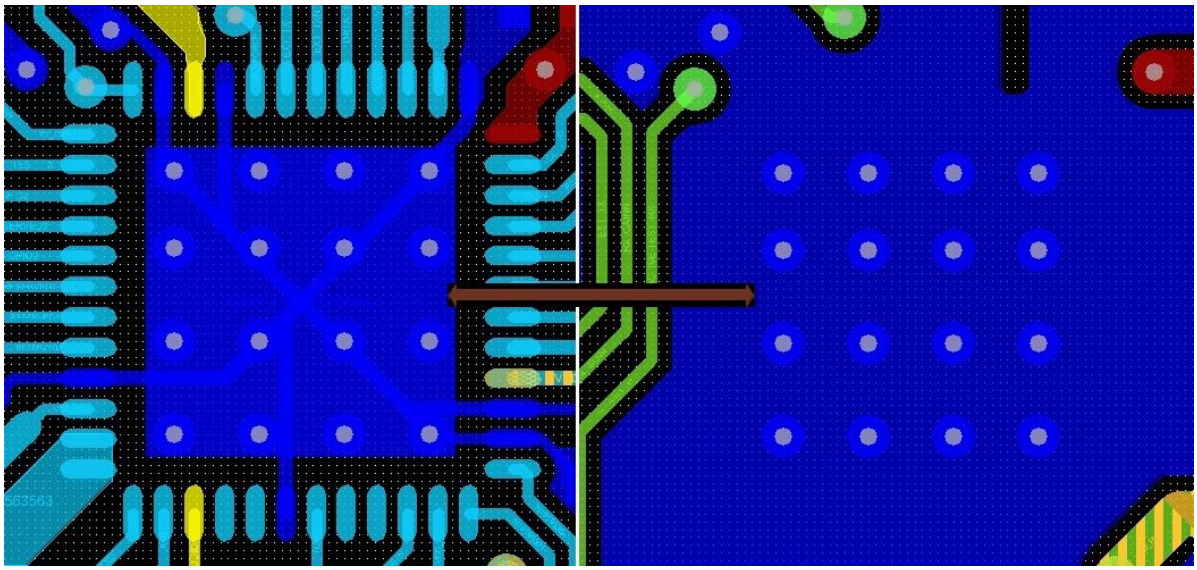
Another technique to improve heat conduction on the top layer is to fill all unused areas with copper tied to the dissipating ground plane.

In order to have an effective heat transfer from the top layer of the PCB to the bottom layer, thermal vias need to be included within the thermal pad area. If properly designed, thermal vias are the most efficient paths for removing heat from the device.

An array of 4 x 4 thermal vias at 1.0 mm pitch, with a via diameter of 0.3 mm, has been incorporated in the thermal pad, as shown in *Figure 43*.

To minimize solder wicking effect due to open vias, possibly leading to poor soldering of the QFN48 exposed pad, the via encroaching technique has been adopted (see the bottom side of *Figure 43*). The bottom side solder resist has only small openings (nearly 0.2 mm larger than the via drill diameter) around the vias; the reduced area of exposed copper on the bottom reduces the amount of solder paste flowing down the vias.

Figure 43. PCB copper dissipating area on top layer (left) and bottom layer (right) for the ST7590 reference design board



Another important parameter for effective heat dissipation is the copper thickness for both top and bottom layers. 1 oz copper is considered as the minimum value to ensure good dissipation.

The bottom side routing plays an important role too. The solid ground area of copper under the device must be as large as possible to minimize the thermal impedance. Therefore, traces on the bottom side must run as far as possible from the device area.

10.1.2 Ground connections

Good soldering of the ST7590 exposed pad is required also to minimize ground noise. Being the exposed pad connected to VSSA, its cleanness is directly related to the noise level detected by the receiving circuitry (i.e.: to the actual sensitivity level) and to the PLL behavior.

It is very important to filter each supply pin to its respective ground: VCC to VSS, VCCA and VDD_PLL to VSSA, VDDIO and VDD to GND.

10.2 Thermal impedance and power dissipation calculation

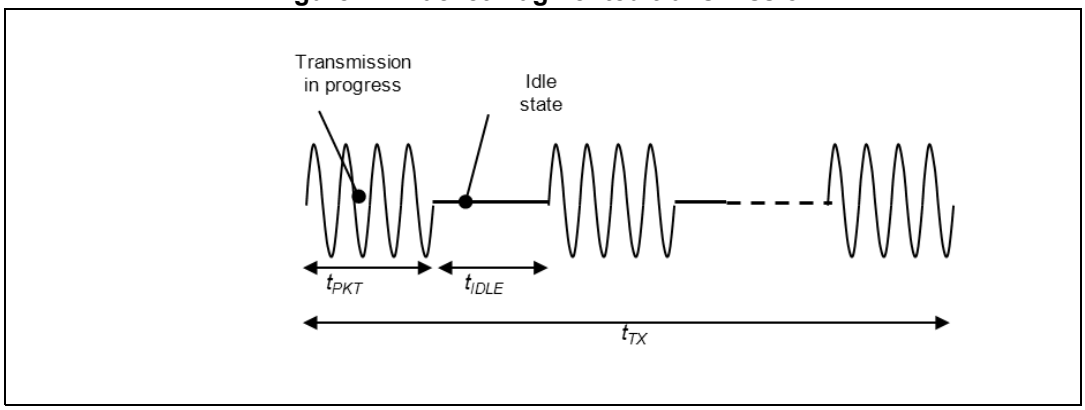
The relationship between junction temperature (T_J) and power dissipation during transmission (P_D) is described by the following formula:

Equation 9

$$T_J(t_{TX}, d) = T_A + P_D \cdot Zth_{JA}(t_{TX}, d)$$

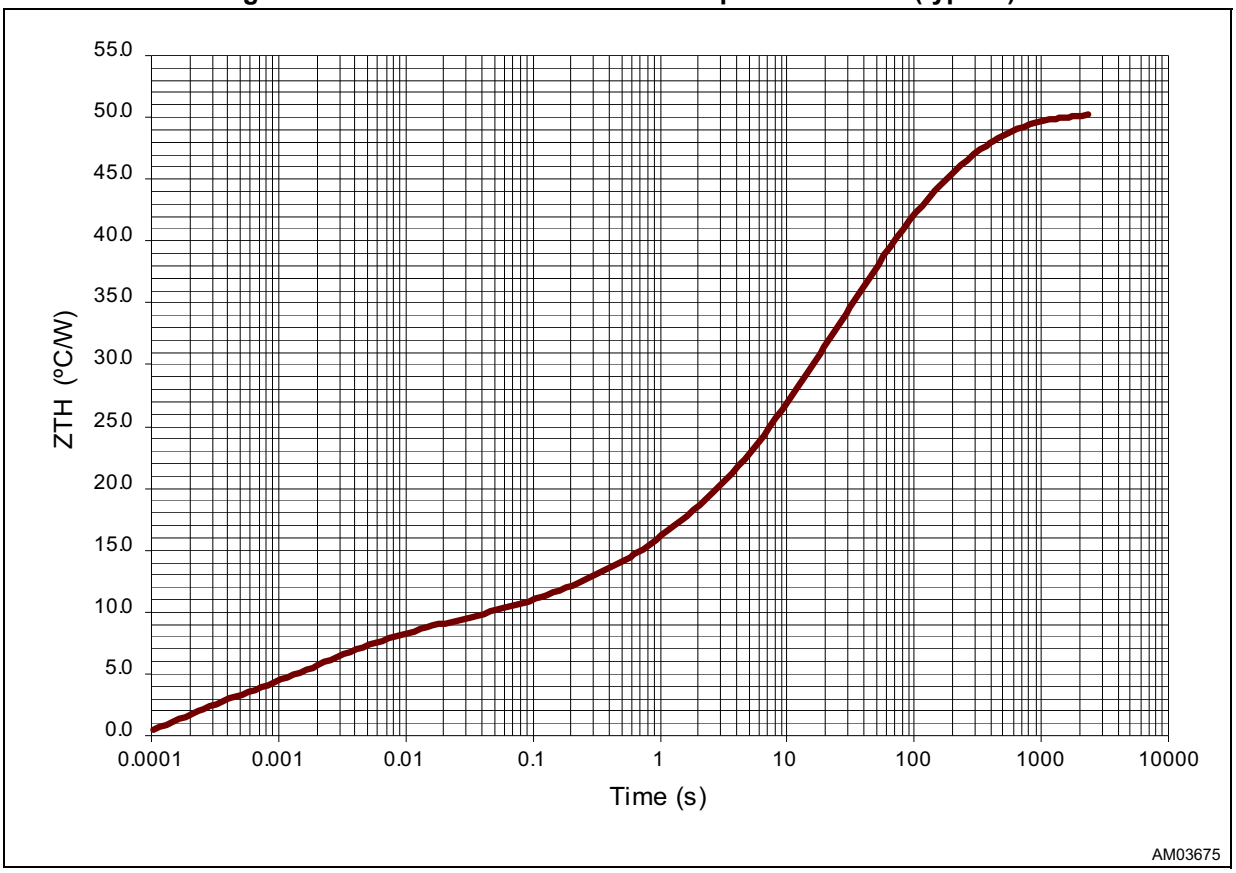
where T_A is the ambient temperature (from -40 to +85 °C) and Zth_{JA} is the junction to ambient thermal impedance of the ST7590 IC, which is related to the length of the transmission (t_{TX}) and to the duty cycle $d = t_{PKT} / (t_{PKT} + t_{IDLE})$, assuming a packet-fragmented transmission as illustrated by *Figure 44*.

Figure 44. Packet-fragmented transmission



When soldered to a proper dissipating area on the PCB as explained above, the ST7590 IC is characterized by a steady state thermal resistance Rth_{JA} of about 50 °C/W. The thermal impedance curve obtained as power dissipation step response is reported in *Figure 45*.

Figure 45. Measured ST7590 thermal impedance curve (typical)

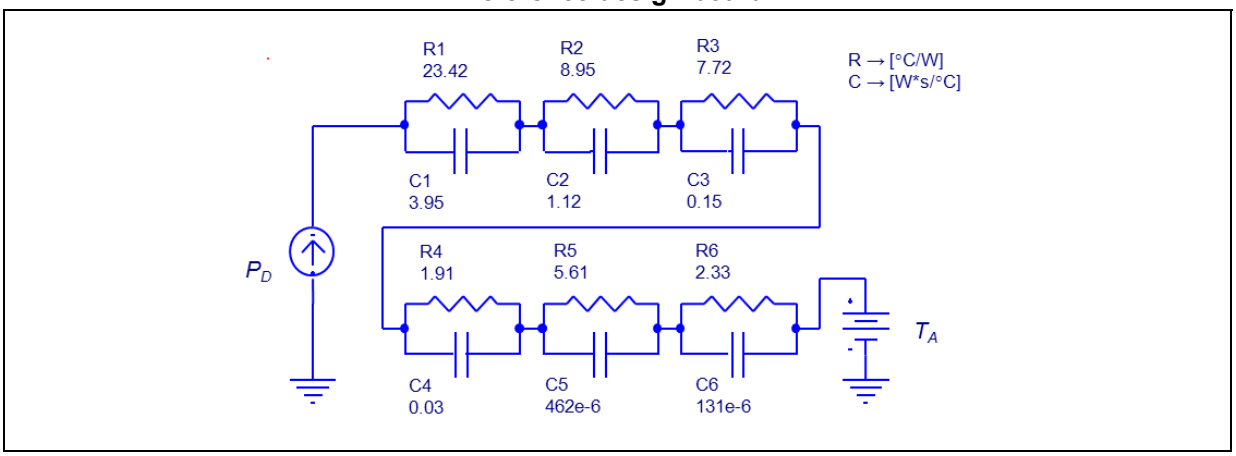


It can be noticed that the transient of Zth_{JA} takes some thousand seconds, after which the static value of 50 °C/W is reached. This means that during the transient phase (i.e.: if the transmission time t_{TX} is some seconds or even less) the IC is able to dissipate a power that is well higher than the one sustainable at steady state.

For this reason, a complete thermal analysis requires to take into account the characteristics of the transmission, i.e.: duty cycle and duration, determining the value reached by the thermal impedance and then the allowed power dissipation.

The thermal impedance as a response to dissipation at different duty cycle and duration values can be estimated by simulating a 6-cells equivalent model obtained through curve fitting from *Figure 45*, as shown in *Figure 46*.

Figure 46. Simulation model of the thermal impedance Zth_{JA} of the ST7590 mounted on the reference design board



The actual dissipated power P_D can be calculated as:

Equation 10

$$P_D = P_{IN} - P_{OUT}$$

where

Equation 11

$$P_{IN} = V_{CC} \cdot I_{CC}$$

and

Equation 12

$$P_{OUT} = V_{OUT\ rms} \cdot I_{OUT\ rms}$$

Note that power consumption by receiving circuitry and linear regulators is considered negligible for thermal analysis purpose. The relationship between current absorption from the power supply (I_{CC}) and PA output current to the load (I_{OUT}) is shown in *Figure 2 on page 9*.

A transmission output level $V_{OUT\ rms}$ of 1.5 V, together with the current limit $I_{OUT\ rms(LIMIT)}$ of 1 A, correspond to a maximum output power P_{OUT} of 1.5 W. In these conditions, the required dissipation results as follows:

Equation 13

$$P_{D(MAX)} = P_{IN(LIMIT)} - P_{OUT(LIMIT)} \cong (13V \cdot 0.47A) - (1.5V \cdot 1A) = 4.6\,W$$

Referring to the relationship between dissipated power and temperature, it can be proved that in a continuous transmission, i.e.: with Zth_{JA} at its steady state value of 50 °C/W, with an ambient temperature of 25 °C the maximum dissipation can be 2 W. However, controlling the transmission duty cycle and total duration it becomes possible to get higher dissipation.

An example of communication with realistic values can be used to understand the point. Let's consider the following conditions:

- Modulation: B-PSK uncoded
- PHY payload: 256 bytes
- Packet transmit time = 55 ms
- Duty cycle = 30%

With these parameters, sending 100 messages will take less than 20 seconds. According to the model of *Figure 46*, in these conditions the Zth_{JA} will reach 15 °C/W, allowing maximum dissipation $P_{D(MAX)}$ with an ambient temperature up to 50 °C.

If the ambient temperature is 70 °C, $P_{D(MAX)}$ would be manageable for 6 consecutive transmissions.

10.3 Oscillator section

The ST7590 internal oscillator circuitry requires a crystal having a maximum load capacitance of 20 pF and a maximum ESR of 100 Ω. It is recommended to choose a quartz crystal with overall tolerance not greater than ± 50 ppm (including aging and temperature) to ensure stability of carrier frequency and digital timing.

It is very important to keep the crystal oscillator and the load capacitors as close as possible to the device.

The resonant circuit must be far away from noise sources such as:

- Power supply circuitry
- Burst and surge protections
- Mains coupling circuits
- Any PCB track or via carrying a RF switching signal

To properly shield and separate the oscillator section from the rest of the board, it is recommended to use a ground plane, on both sides of the PCB, filling all the area below the crystal oscillator. No tracks or vias, except for the crystal connections, should cross the ground plane.

Connecting the case to ground could be a good practice to reduce the effect of radiated signals on the oscillator.

10.4 Power supply

The power supply requirements for the ST7590 reference design are listed in *Table 2 on page 8*.

Anyway, the power supply circuit design is not only relevant in terms of available power. Two points are particularly sensitive for a power line communication application:

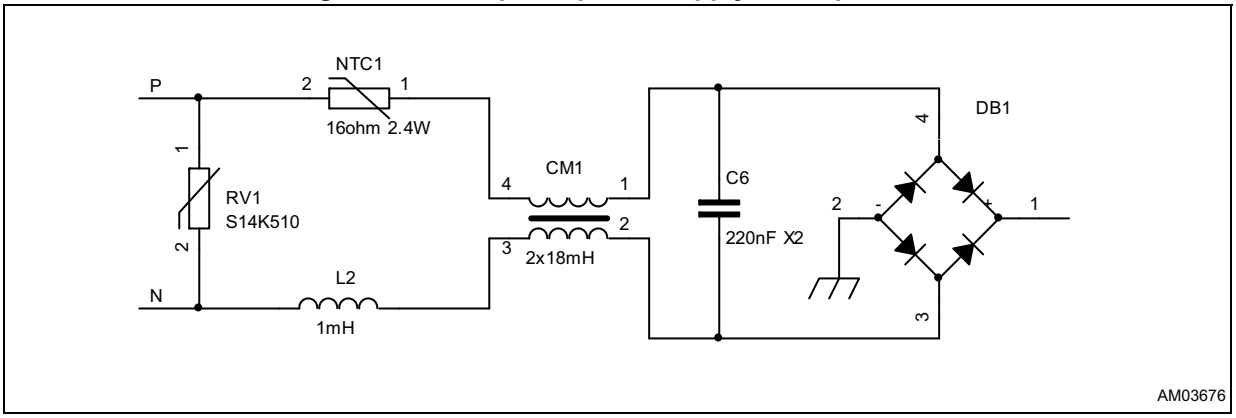
- The noise injected on the line
- The input impedance of the power supply unit

For the first point, a quasi-resonant switching mode power supply based on the ALTAIR04-900 device has been chosen. This kind of switching controller spreads the switching disturbances over a wide frequency range, thus minimizing the overall disturbance amplitude.

The second point involves the EMI input filter design. The suggested circuit of *Figure 47* has been designed to have minimum influence on the ST7590 line coupling circuit, in terms of a load impedance and linearity.

The 220 nF X2 capacitor has been put close to the bridge to avoid capacitive loading on the ST7590 transmitted signal.

Figure 47. Example of power supply EMI input filter



11 Application ideas

3-phase zero crossing coupling

For the zero crossing coupling, even if only one phase at a time can be used as reference, the possibility to switch to another phase is required in case of fault on the reference line. This can be achieved through one of the suggested circuits of *Figure 48* and *Figure 49*.

The external host has to control the LCA715 opto relays according to the phase status information provided by the measurement circuitry. The host controller is also responsible of ensuring that only one opto relay is turned on, thus guaranteeing isolation between the 3 phases.

Figure 48. 3-phase isolated zero crossing coupling circuit

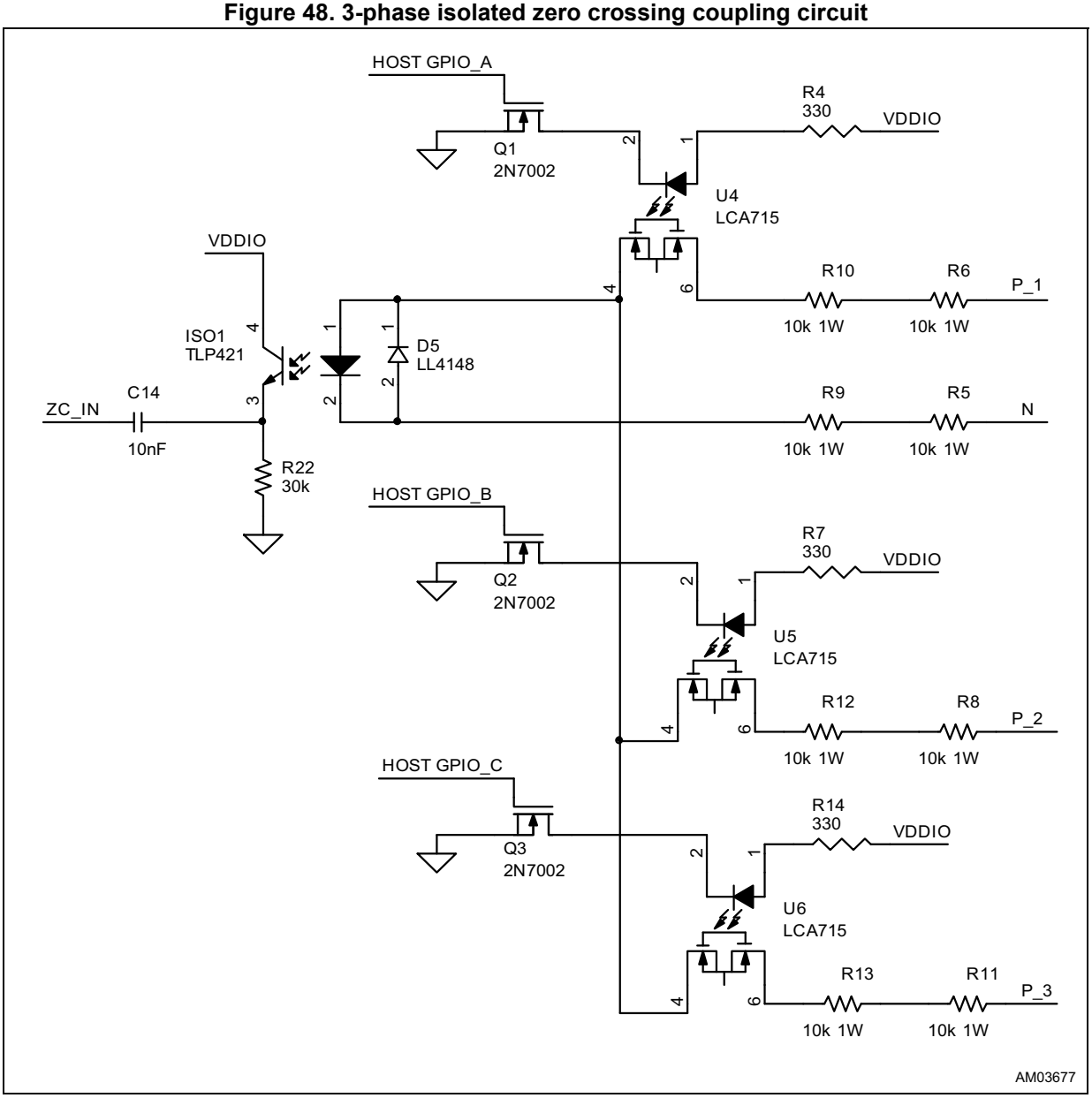
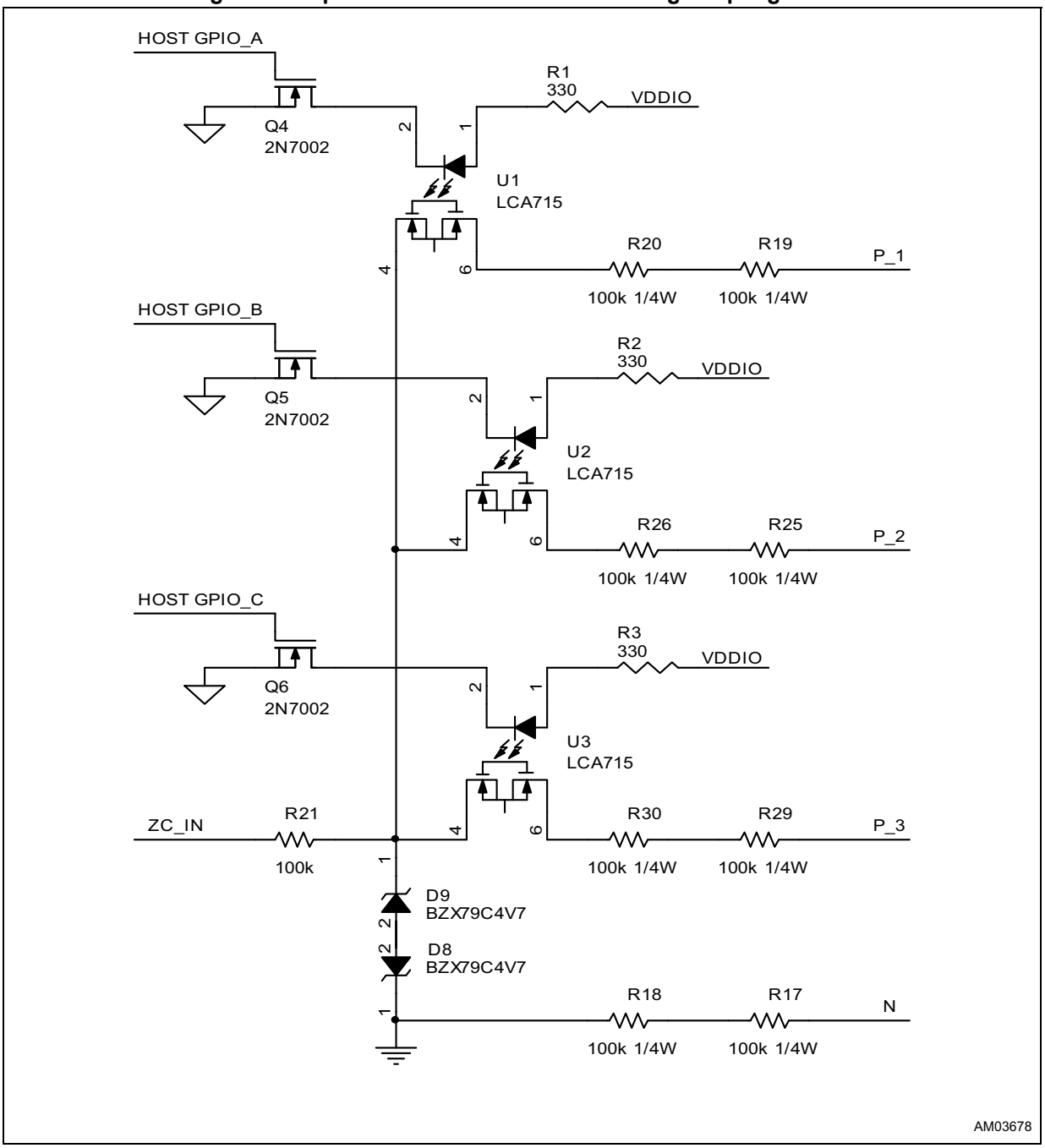


Figure 49. 3-phase non-isolated zero crossing coupling circuit



12 FAQ and troubleshooting

In this section the most frequently asked questions and the solutions to common ST7590 reference design usage problems are described.

12.1 FAQ

Q: *Is it possible to use ST power line transceivers on medium or high voltage AC line?*

A: Yes. The same circuit solution as for a low voltage AC line can be used, provided that a coupling interface (and particularly line transformer, power inductor and X1 capacitor) guarantees an adequate and safe isolation from the AC line.

Q: *Is it possible to use the ST7590 on a DC or de-energized line?*

A: Yes, the ST7590 can communicate over any wired connection, given that a suitable coupling circuit is used to connect the device to the line.

Q: *Which kind of protocols can be used with the ST7590?*

A: The ST7590 device has been conceived to support the PRIME protocol.

Q: *Does the ST7590 reference design meet FCC part 15 specifications?*

A: Yes. In fact, the EN normative compliance intrinsically guarantees the compliance with the FCC part 15 regulations as well.

Q: *Why with power line communication cannot I get 100% reachability even though the range is few meters?*

A: Probability lower than 100% to reach a PLC node within such a small distance can depend on two main factors:

- Attenuation or losses on the power line (for example because of some heavy capacitive load connected close to the transmitter)
- Noise coming from electric or electronic equipment connected on the power line (for example SMPS, ballasts, motors).

It can be useful to measure the signal level at the transmitter and receiver to understand if there are undesired losses. It is also important to measure the noise level and spectral distribution to find whether the PLC channel is somehow “jammed” by noise.

Q: *Will the power line communication work if a power distribution transformer is present between two nodes?*

A: The communication could work, but the transformer impedance at the signal frequency must be taken into account, since it could introduce strong attenuation in the signal level. A signal coupler (for example, a capacitive coupling) between the two sides of the distribution transformers could be required.

Q: *What method of coupling is preferred for “Medium Voltage” and “Low Voltage” mains line: capacitive or inductive?*

A: For MV line, a capacitive coupling is preferable for a narrowband PLC. In the case of a LV line, being the actual line impedance unpredictable because of the number of electrical devices connected on it, the solution should be an L-C series resonant circuit tuned at channel frequency, designed to have low Q even with a very low line impedance (5 Ω and below).

Q: *Is it possible to detect the channel quality by the ST7590 device?*

A: Yes. Using the ST7590 estimators, always available for the external host, it is possible to evaluate the channel quality over the physical link between the transmitter and receiver.

Q: *Why using zero crossing synchronization?*

A: The zero crossing synchronization is not mandatory for the power line communication, however it has several advantages.

For instance, it can improve the communication immunity against line noise, since most of the electric equipment generates noise on the power line in correspondence of the mains voltage peak. Zero crossing synchronization allows establishing the link between the transmitter and receiver during the time with the minimum time-dependent noise.

Zero crossing synchronization is also needed for 3-phase communication. In the case that one node must communicate with nodes that are connected on other phases of the mains network, zero crossing synchronization allows understanding which phase a certain message is coming from via delta-phase calculation.

Q: *What could be the main sources of harmonic distortion in the ST7590 transmitted signal?*

A: Generally, harmonics can rise up because of

- High output current, due to low line impedance;
- Saturation of magnetic components in the line coupling circuit, due to either poor dimensioning of the saturation current or to 50 Hz residual current;
- Capacitive load applied to the power amplifier output;
- Insufficient margin to the supply rails (low VCC or high output voltage).

12.2 Troubleshooting

1. **Problem:** the ST7590 reference design board doesn't work at all.

What to check:

a) Check that the AC mains supply cable is well connected.

b) Check the voltage on VCC, VDDIO, VCCA, VDD, VDD_PLL lines. All those voltages must be present to turn the ST7590 on.

c) Verify if an 8 MHz clock is present on the XOUT pin (13) of the ST7590 device.

2. **Problem:** the ST7590 reference design board is not responding.

What to check:

a) Check if some activity is there when trying to communicate via a USB with the board.

b) Try disconnecting and reconnecting the USB cable; sometimes the USB driver fails during the COM port opening.

c) Try to reinstall the USB VCP driver for the STM32 on the PC.

d) Try to reprogram the STM32 device with the VCP driver FW.

3. **Problem:** the ST7590 reference design board does not transmit.

What to check:

a) Check the bias voltage on the PA_OUT test point (TP2) with the oscilloscope probe referred to VSS power ground. A DC voltage of VCC/2 must be measured.

b) Set the ST7590 in transmission via the PRIME GUI. A modulated signal should be detected by the oscilloscope probe, with amplitude equal to the TX_OUT programmed level multiplied by the PA gain (see *Section 8.1.1: Line driver on page 26*). In this case, no problem is there about the transmitter section of the ST7590.

4. **Problem:** the ST7590 reference design board transmits only for a short while; the transmission is interrupted.

What to check:

a) Verify the external temperature of the ST7590 device.

b) Check if there is a short-circuit (i.e.: capacitive) impedance on the mains at the carrier frequency. It could lead to the device overheating and PA thermal shutdown.

5. **Problem:** the ST7590 reference design board does not receive.

What to check:

Check if the transmitted signal reaches the ST7590 device by measuring the RX_IN line voltage (TP6) with the oscilloscope probe referred to VSSA signal ground.

6. **Problem:** During a communication test, the PRIME GUI shows high “Bit Error Rate” (BER).

Note: (This point refers to a half-duplex communication involving two ST7590 reference design boards communicating with each other).

What to check:

a) Check that both reference design boards have the same PRIME GUI settings.

b) Verify the SNR of the communication. If the signal is too low or the noise is too high with respect to each other, the communication performance will be poor. Try to:

1. Check the SNR estimation of the receiving ST7590 device.

2. Measure the signal level S and the noise level N on the RX_IN line of the receiving board.

13 References

1. ST7590 datasheet: www.st.com/powerline
2. UM1038 - Hardware interconnection of the STM32™, SPEAr™3xx, and ST75xx user manual: www.st.com/powerline
3. STM32F103RG web page: www.st.com/internet/mcu/product/247494.jsp
4. AN2867 - Oscillator design guide for STM8S, STM8A and STM32F1 microcontrollers
5. ST “Virtual COM Port Driver”: http://www.st.com/st-web-ui/static/active/en/st_prod_software_internet/resource/technical/software/driver/stsw-stm32102.zip

14 Normative references

EN50065: Signaling on low voltage electrical installations in the frequency range 3 kHz to 148.5 kHz.

- Part 1: “General requirements, frequency bands and electromagnetic disturbances”
- Part 2 - 3: “Immunity requirements“
- Part 4 - 2: “Low voltage decoupling filters - Safety requirements”
- Part 7: “Equipment impedance”.

Appendix A

Main board layout

Figure 50. PCB layout - components

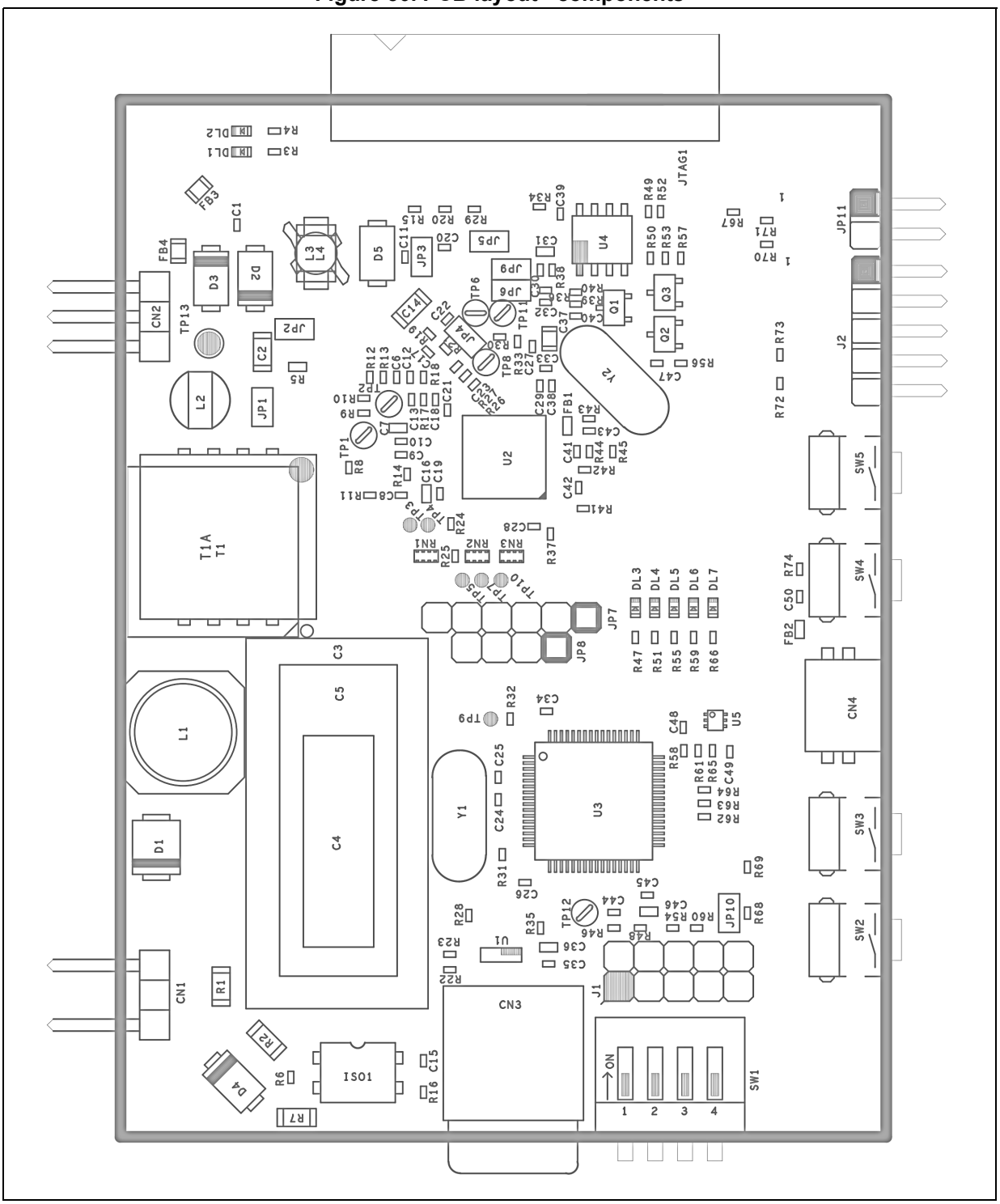


Figure 51. PCB layout - top view

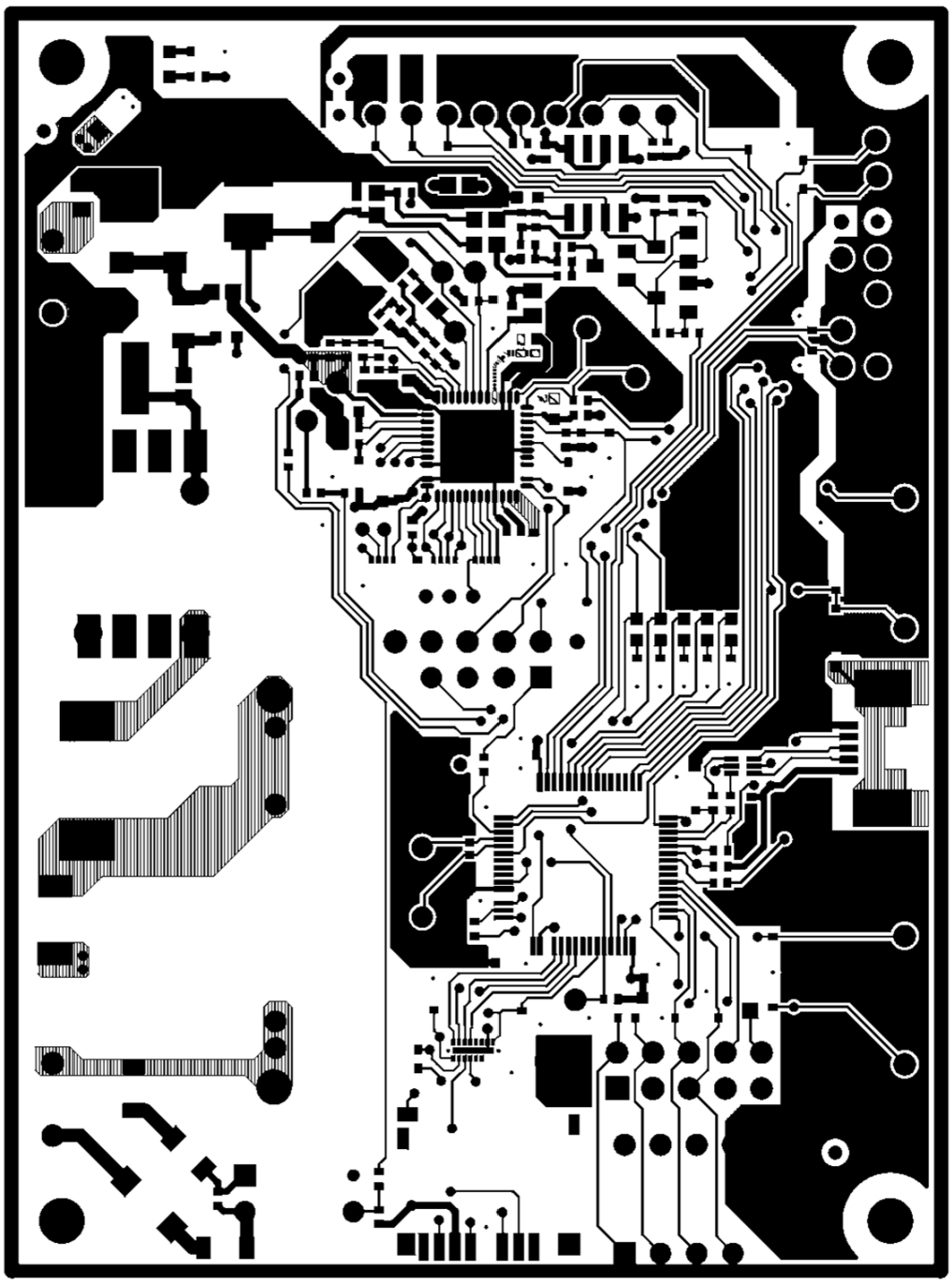
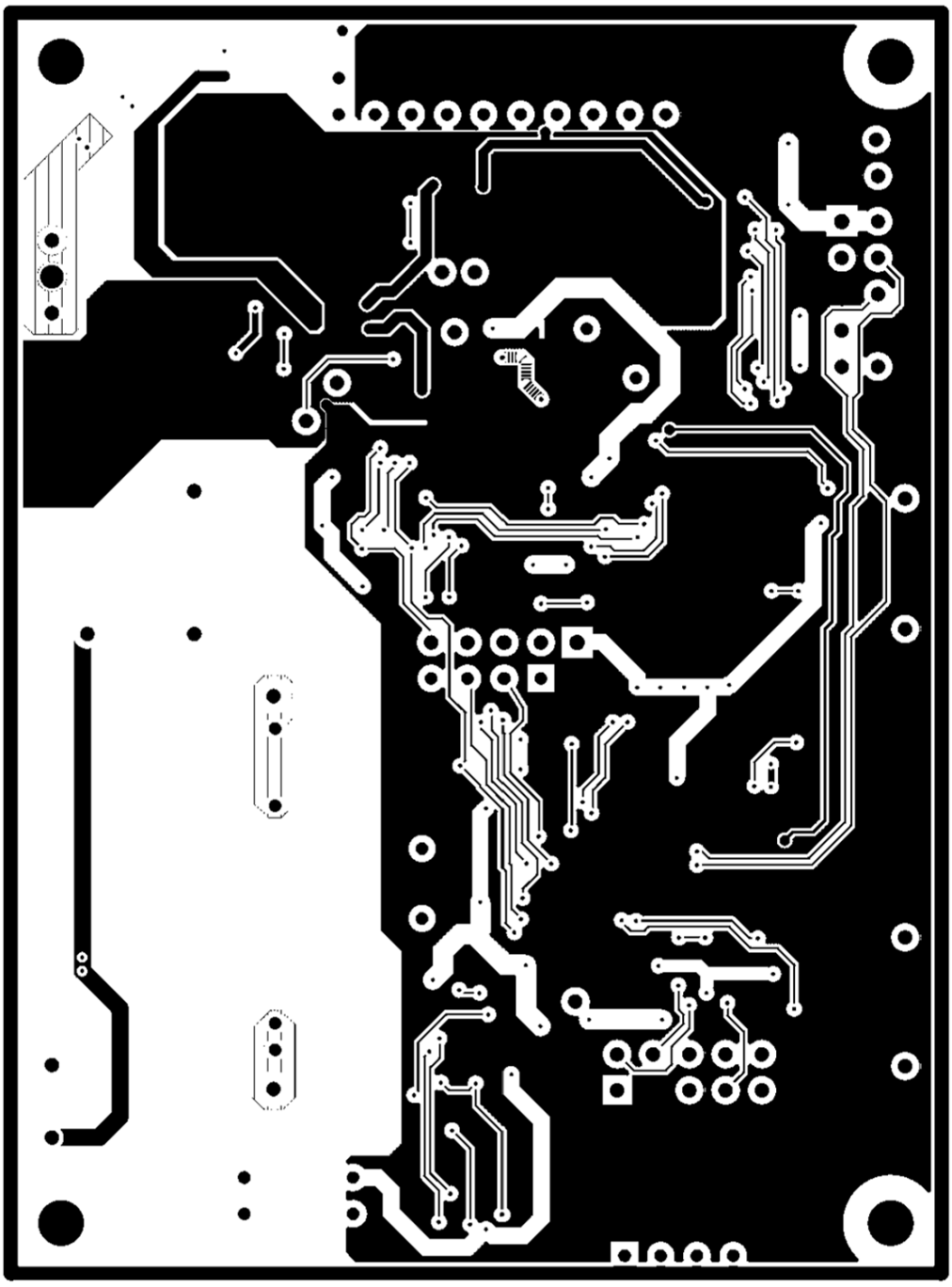


Figure 52. PCB layout - bottom view



Revision history

Table 8. Document revision history

Date	Revision	Changes
01-Sep-2014	1	Initial release.
30-Oct-2014	2	Updated title of *Figure 1: Main board with ST7590 and STM32 on page 1* and *Section 5: EVALKITST7590-Q1 description on page 12*. Updated title of *Section 8.2.3: Metrology interface to STM32* and *Section 8.2.4: General purpose push-buttons and LEDs on page 39*, replaced “main board with the ST7590 AND STM32” and “EVALST7590-Q1 main board with the ST7590 AND STM32” by “EVALKITST7590-Q1”. Updated title of *Figure 33: Maximum output level on EN50065 AMN measurement port on page 44*, and title of *Section : Main board layout on page 64* .