AN4467
Application note

Getting started with STM32L0xx hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use STM32L0xx product families and describes the minimum hardware resources required to develop an STM32L0xx application.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

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1 Power supplies

1.1 Introduction

The chip requires power supply on different power pins:

- V_{DD}= 1.65 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins. For V_{DD} below 1.8 V see *Section 1.3.3: Brownout reset (BOR)*
- V_{DDA} = V_{DD}: external analog power supply for ADC/DAC, Comparators, Reset blocks, RCs and PLL. The minimum voltage to be applied to V_{DDA} is 1.8 V when the DAC is used.The V_{DDA} voltage level must always be equal to V_{DD}, a maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and normal operation.
- V_{LCD}= 2.5 to 3.6 V when the LCD controller is powered externally. When the LCD is powered internally from the voltage generated by the embedded step-up converter, V_{LCD} pin must be connected to a capacitor. If the LCD is not used at all, this pin should be connected to V_{DDA}.
- V_{DD_USB} = 3.0 to 3.6 V, V_{DD_USB} is a dedicated independent USB power supply for USB transceivers. The minimum value of 3.0 V guarantees the USB signal voltage level. When USB is not used the application must supply V_{DD_USB} = 1.65 to 3.6 V.

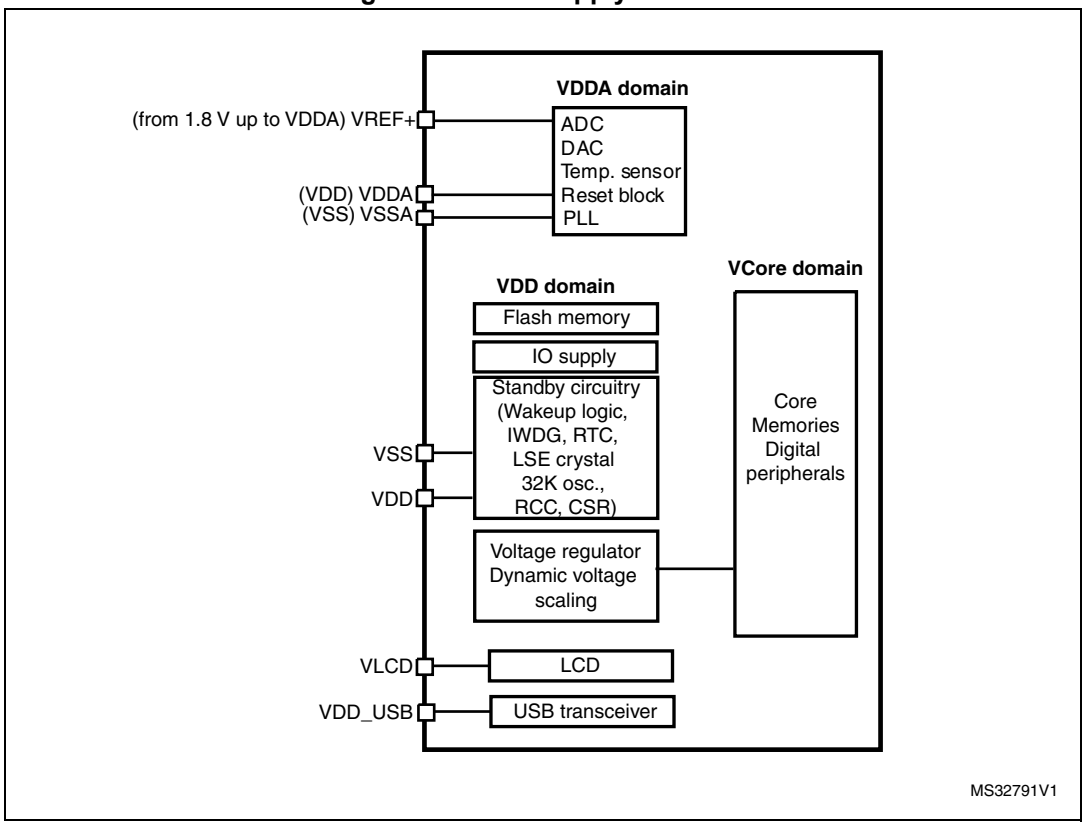
Digital power voltage (V_{CORE}) is provided with an embedded linear voltage regulator with three different programmable ranges from 1.2 to 1.8 V.

To be fully functional at full speed, the device requires a 1.71 to 3.6 V operating voltage supply (V_{DD}), making possible to reach the digital power voltage V_{CORE} close to 1.8 V (product voltage range 1).

Product voltage range 2 (V_{CORE} = 1.5 V) and 3 (V_{CORE} = 1.2 V) can be selected when the V_{DD} operates from 1.65 to 3.6 V. Therefore, frequency is limited to 16 MHz and 4.2 MHz, respectively.

When the DAC and brownout reset (BOR) are not used, the device can operate at power voltages below 1.8 V, down to 1.65 V.

Figure 1. Power supply overview



Note: V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.

1.1.1 Independent A/D converter supply and reference voltage

To improve conversion accuracy, the ADC and the DAC have an independent power supply that can be filtered separately, and shielded from noise on the PCB.

- The ADC voltage supply input is available on a separate V_{DDA} pin
- An isolated supply ground connection is provided on the V_{SSA} pin

V_{DDA} and V_{REF+} require a stable voltage. The consumption on V_{DDA} can reach several mA (see I_{DD}(ADCx), I_{DD}(DAC), I_{DD}(COMPx), and I_{DDA} in the product datasheets for further information).

When available (depending on the package), V_{REF-} must be tied to V_{SSA}. V_{SSA} and V_{REF-} must be tied to V_{SS} directly, without any filtering device, this avoids some ESD issues.

On some packages with the pin V_{REF+} to ensure a better accuracy on low-voltage inputs and outputs, the user can connect to V_{REF+} a separate external reference voltage which is lower than V_{DD}. V_{REF+} is the highest voltage, represented by the full scale value, for an analog input (ADC) or output (DAC) signal.

On packages without such a dedicated pin, V_{REF+} is internally connected to the ADC voltage supply (V_{DDA}).

1.1.2 Independent LCD supply (STM32L0x3 only)

The V_{LCD} pin is provided to control the contrast of the glass LCD. This pin can be used in two ways:

- It can receive, from an external circuitry, the desired maximum voltage that is provided on the segment and common lines to the glass LCD by the microcontroller.
- It can also be used to connect an external capacitor that is used by the microcontroller for its voltage step-up converter. This step-up converter is controlled by software to provide the desired voltage to the segment and common lines of the glass LCD. Refer to the specific product datasheet for the capacitor value.

The voltage provided to the segment and common lines defines the contrast of the glass LCD pixels. This contrast can be reduced when the dead time between frames is configured.

In case of LCD with big pixel, the high capacitance of the pixel might degrade the LCD signal shape. So the device offer the possibility to connect internal V_{LCD} rails (LCD_VLCD1, LCD_VLCD2, LCD_VLCD3) to optional capacitors. This improves the Segment and Common line signals shape with limited use of high drive resistor network, so it improves the signal shape without extra current consumption. The values of these decoupling capacitors must be tuned according to the LCD glass and the PCB capacitances. As a guideline the user can set the decoupling capacitor values to approximately 10 times the LCD and PCB capacitance. The LCD rail to be connected depends on the Bias configuration.

Table 1. V_{LCD} rails connections to GPIO pins

Rail	Bias			Pin selected by CAPA[2:0] bits
	1/2	1/3	1/4	
LCD_VLCD3	Not used	Not used	3/4 V_{LCD}	PB0 or PE12
LCD_VLCD2	1/2 V_{LCD}	2/3 V_{LCD}	2/4 V_{LCD}	PB2
LCD_VLCD1	Not used	1/3 V_{LCD}	1/4 V_{LCD}	PB12 or PE11

1.1.3 Voltage regulator

The internal voltage regulator is always enabled after reset. It can be configured to provide the core with three different voltage ranges. Choosing a range with low V_{core} reduces the consumption but lowers the maximum acceptable core speed. Consumption ranges in decreasing consumption order are as follows:

- Range 1, available only for V_{DD} above 1.71 V, allows maximum speed;
- Range 2 allows CPU frequency up to 16 MHz;
- Range 3 allows CPU frequency up to 4.2 MHz.

Note: In Range 1, when V_{DD} is below 2.0 V, the CPU frequency in run mode must be managed to prevent any changes exceeding a ratio of 4 in one shot. A delay of 5 µs must be respected between 2 changes. There is no limitation when waking up from low-power mode.

Voltage regulator works in three different modes depending on the application:

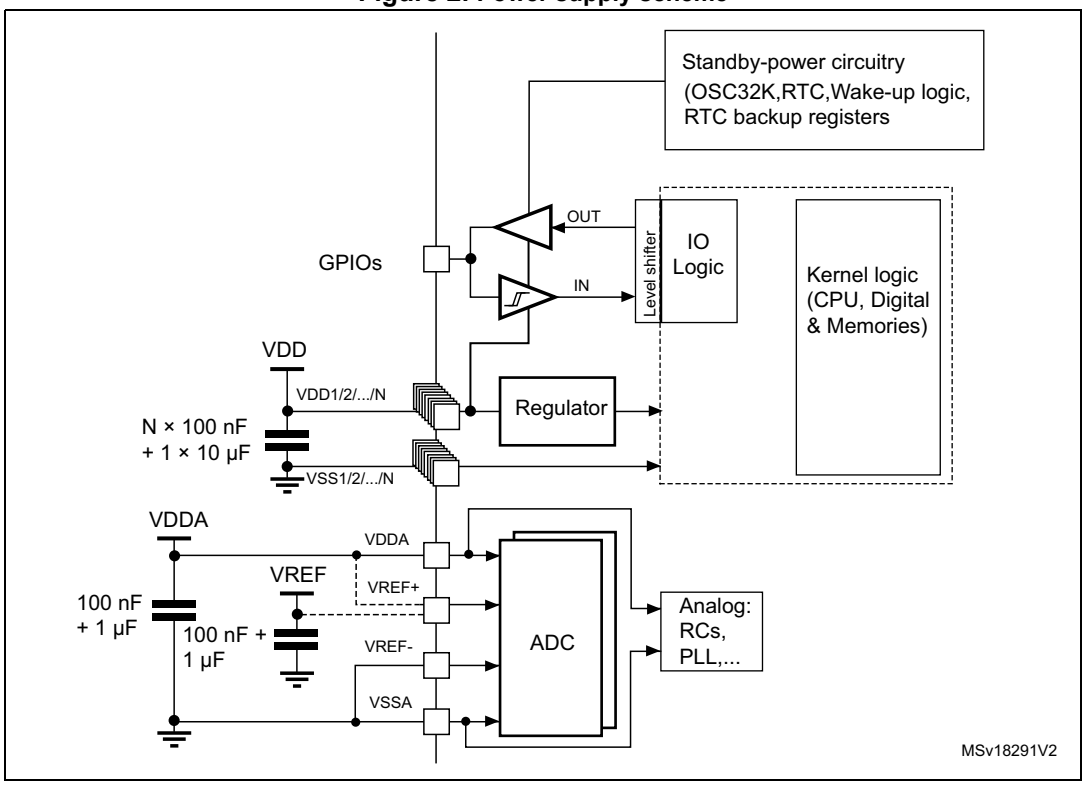
- in Run mode, the regulator supplies full power to the V_{core} domain (core, memories and digital peripherals);
- in Stop mode, low-power run and low-power wait modes, the regulator supplies low-power to the V_{core} domain, preserving the contents of the registers and SRAM;
- in Standby mode, the regulator is powered off. The contents of the registers and SRAM are lost except for those powered with the Standby circuitry.

1.2 Power supply schemes

The circuit is powered by a stabilized power supply, V_{DD}.

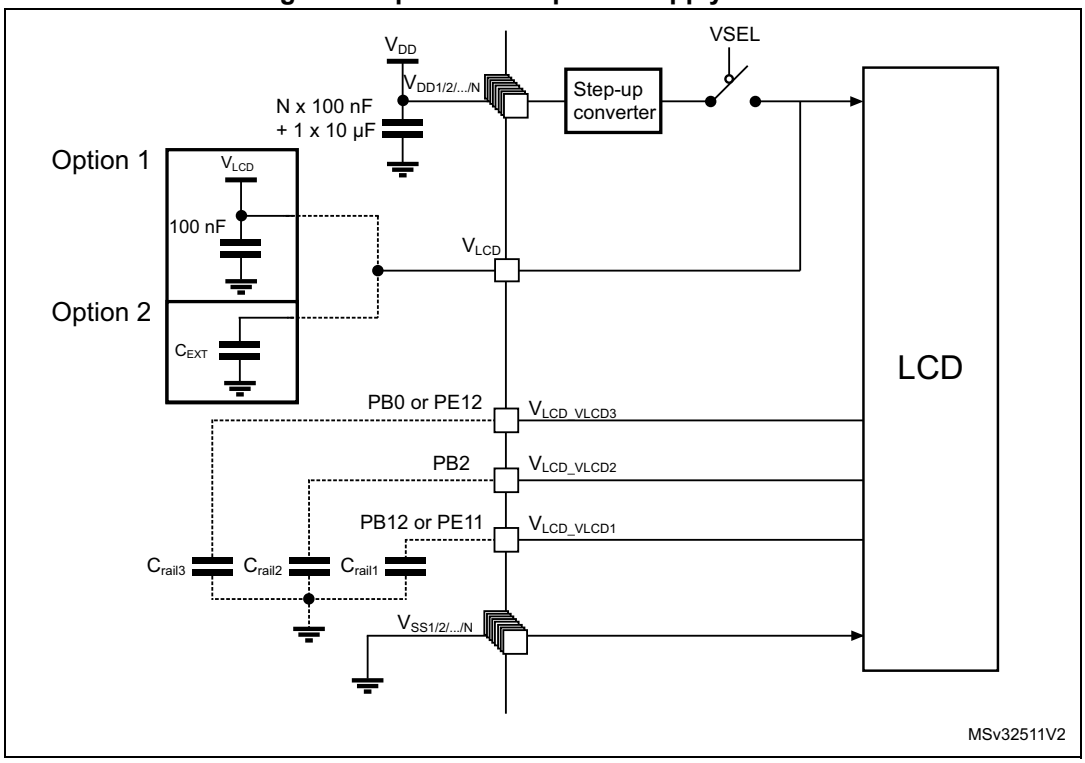
- The V_{DD} pins must be connected to V_{DD} with external decoupling capacitors; one single tantalum or ceramic capacitor (minimum 4.7 µF, typically 10 µF) for the package + one 100 nF ceramic capacitor for each V_{DD} pin).
- The V_{DDA} pin must be connected to two external decoupling capacitors (100 nF ceramic capacitor + 1 µF tantalum or ceramic capacitor).
- The V_{REF+} pin can be connected to the V_{DDA} external power supply. If a separate, external reference voltage is applied on V_{REF+}, a 100 nF and a 1 µF capacitor must be connected on this pin. To compensate peak consumption on Vref, the 1 µF capacitor may be increased up to 10 µF when the sampling speed is high. When ADC or DAC is used, V_{REF+} must remain between 1.8 V and V_{DDA}. V_{REF+} can be grounded when ADC and DAC are not active; this enables the user to power down an external voltage reference.
- Additional precautions can be taken to filter digital noise: V_{DDA} can be connected to V_{DD} through a ferrite bead. In this case take care to keep a (V_{DDA}- V_{DD}) difference lower than 300 mV.

Figure 2. Power supply scheme



1. V_{REF+} is either connected to V_{DDA} or to V_{REF-}.
2. N is the number of V_{DD} and V_{SS} inputs.

Figure 3. Optional LCD power supply scheme



- **Option 1**: LCD power supply is provided by a dedicated V_{LCD} supply source, V_{SEL} switch is open.
- **Option 2**: LCD power supply is provided by the internal step-up converter, V_{SEL} switch is closed, an external capacitance is needed for correct behavior of this converter.

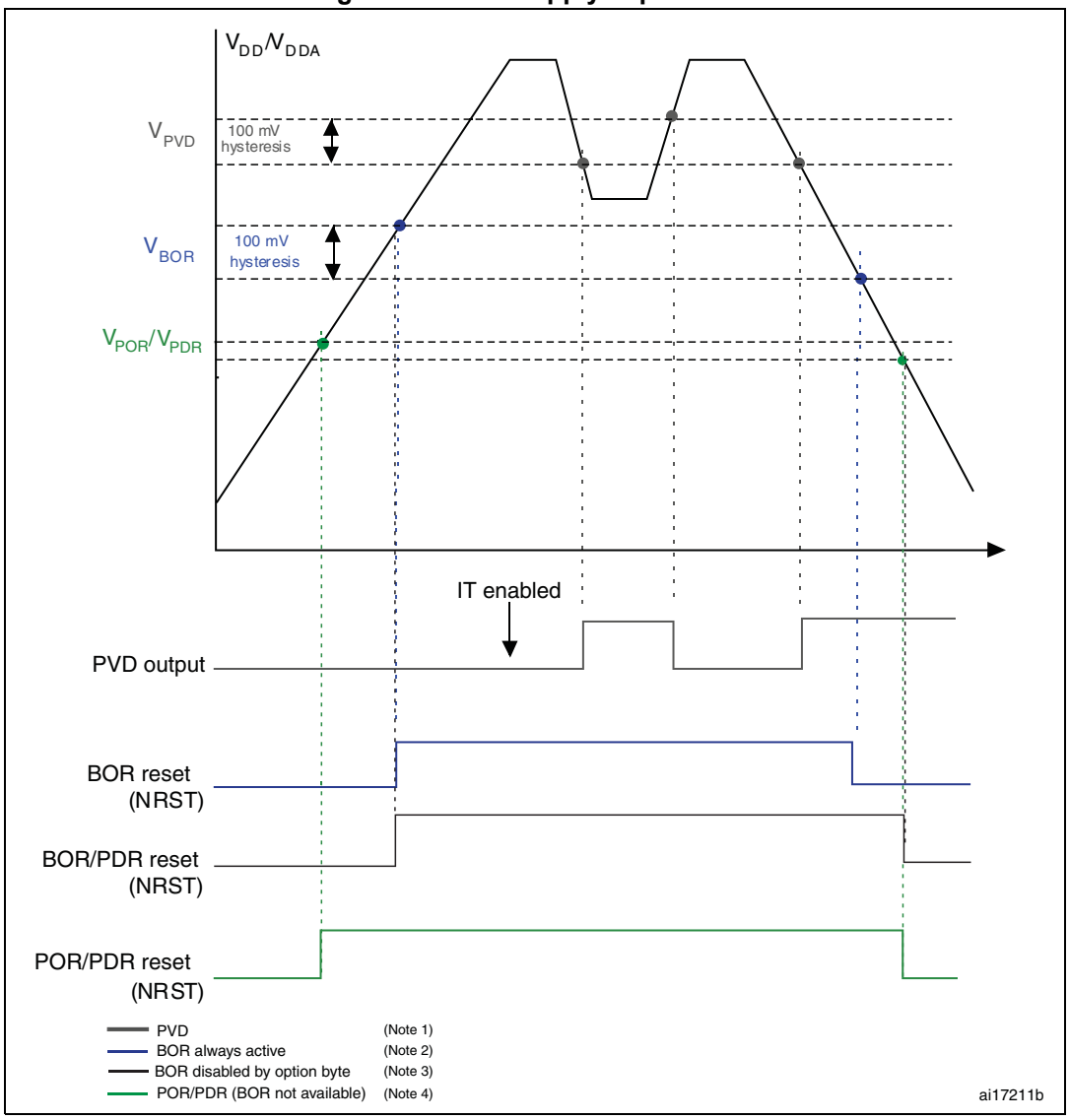
Note: The availability of the V_{LCD} rails depend on device package.

1.3 Reset and power supply supervisor

The input supply to the main and low-power regulators is monitored by a power-on/power-down/brownout reset circuit. Power-on/power-down reset are a null power monitoring with fixed threshold voltages, whereas brownout reset gives the choice between several thresholds with a very low, but not null, power consumption.

In addition, the STM32L0xx embeds a programmable voltage detector that compares the power supply with the programmable threshold. An interrupt can be generated when the power supply drops below the V_{PVD} threshold and/or when the power supply is higher than the V_{PVD} threshold. The interrupt service routine then generates a warning message and/or puts the MCU into a safe state.

Figure 4. Power supply supervisors



1. The PVD is available on all STM32L devices and it is enabled or disabled by software.
2. The BOR is available only on devices operating from 1.8 to 3.6 V, and unless disabled by option byte it masks the POR/PDR threshold.
3. When the BOR is disabled by option byte, the reset is asserted when V_{DD} goes below PDR level.
4. For devices operating from 1.65 to 3.6 V, there is no BOR and the reset is released when V_{DD} goes above POR level and asserted when V_{DD} goes below PDR level.

1.3.1 Power-on reset (POR) / Power-down reset (PDR), Brownout reset (BOR)

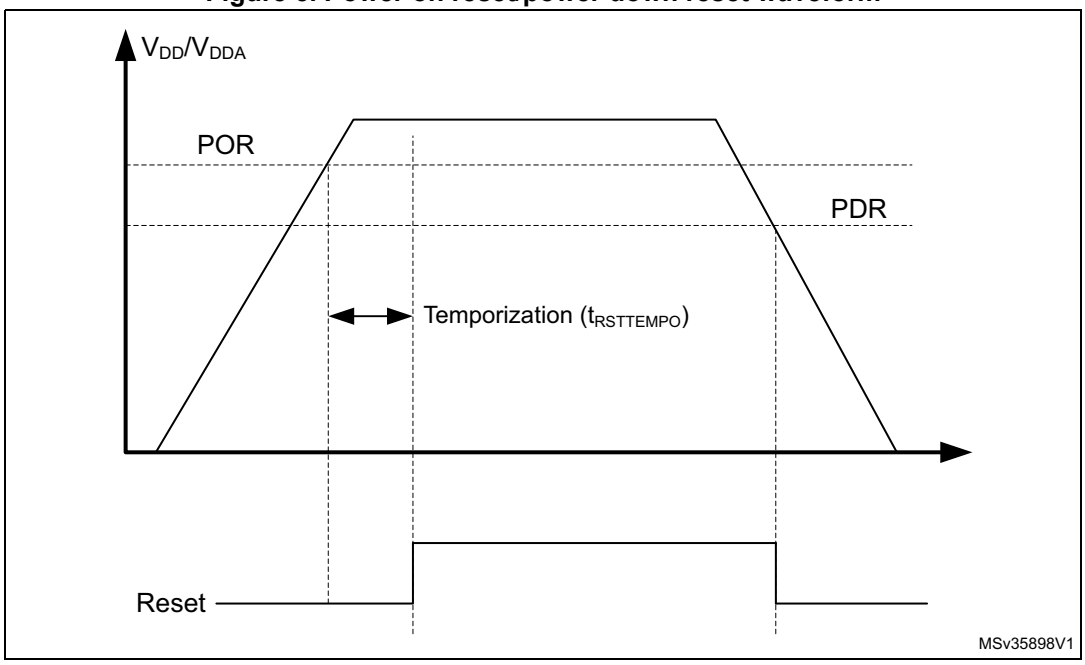
The monitoring voltage begins at 0.7 V.

During power-on, for devices operating between 1.8 and 3.6 V, the BOR keeps the device under reset until the supply voltages (V_{DD} and V_{DDA}) come close to the lowest acceptable voltage (1.8 V). At power-up this internal reset is maintained during ~ 1 ms to wait for the supply to reach its final value and stabilize.

At power-down the reset is activated as soon as the power drops below the lowest limit (i.e. 1.65 V).

At power-on, a defined reset should be maintained below 0.7 V. The upper threshold for a reset release is defined in the electrical characteristics section of the product datasheets.

Figure 5. Power on reset/power down reset waveform



For a programmable threshold above the chip lowest limit, a brownout reset can be configured to the desired value. The BOR can also be used to detect a power voltage drop earlier. The threshold values of the BOR can be configured through the FLASH_OBR option byte.

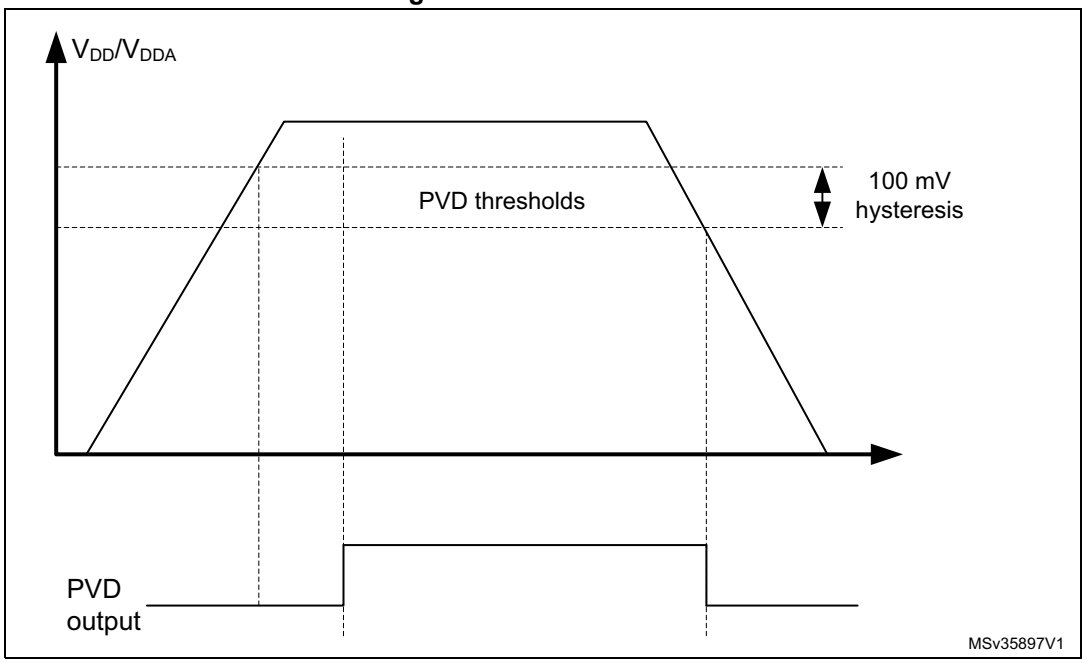
1.3.2 Programmable voltage detector (PVD)

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. Seven different PVD levels can be selected by software between 1.85 and 3.05 V, with 200 mV steps.

An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when it's higher than the V_{PVD} threshold. The interrupt service routine then generates a warning message and/or puts the MCU into a safe state.

The PVD is enabled by software configuration. As an example, the service routine can perform emergency shutdown tasks.

Figure 6. PVD thresholds



1.3.3 Brownout reset (BOR)

During power on, the brownout reset (BOR) keeps the device under reset until the supply voltage reaches the specified V_{BOR} threshold.

For devices operating from 1.65 to 3.6 V, the BOR option is not available and the power supply is monitored by the POR/PDR. As the POR/PDR thresholds are at 1.5 V, a “grey zone” exists between the V_{POR} / V_{PDR} thresholds and the minimum product operating voltage 1.65 V.

For devices operating from 1.8 to 3.6 V, the BOR is always active at power on and its threshold is 1.8 V.

When the system reset is released, the BOR level can be reconfigured or disabled by option byte loading.

If the BOR level is kept at the lowest level, 1.8 V at power-on and 1.65 V at power down, the system reset is fully managed by the BOR and the product operating voltages are within safe ranges.

When the BOR option is disabled by option byte, the power down reset is controlled by the PDR and a “grey zone” exists between the 1.65 V and V_{PDR}.

V_{BOR} is configured through device option bytes. By default, lowest level 0 threshold is activated. Five programmable V_{BOR} thresholds can be selected (see product datasheets for actual V_{BOR0} to V_{BOR4} thresholds).

When the supply voltage (V_{DD}) drops below the selected V_{BOR} threshold, a device reset is generated. When the V_{DD} is above the V_{BOR} upper limit the device reset is released and the system can start.

BOR can be disabled by programming the device option bytes. To disable the BOR function, V_{DD} must have been higher than V_{BOR0} to start the device option byte programming

sequence. The power-on and power-down is then monitored by the POR and PDR (see power-on reset (POR)/power-down reset (PDR) section in the product datasheets).

The BOR threshold hysteresis is ~100 mV (between the rising and the falling edge of the supply voltage).

1.3.4 System reset

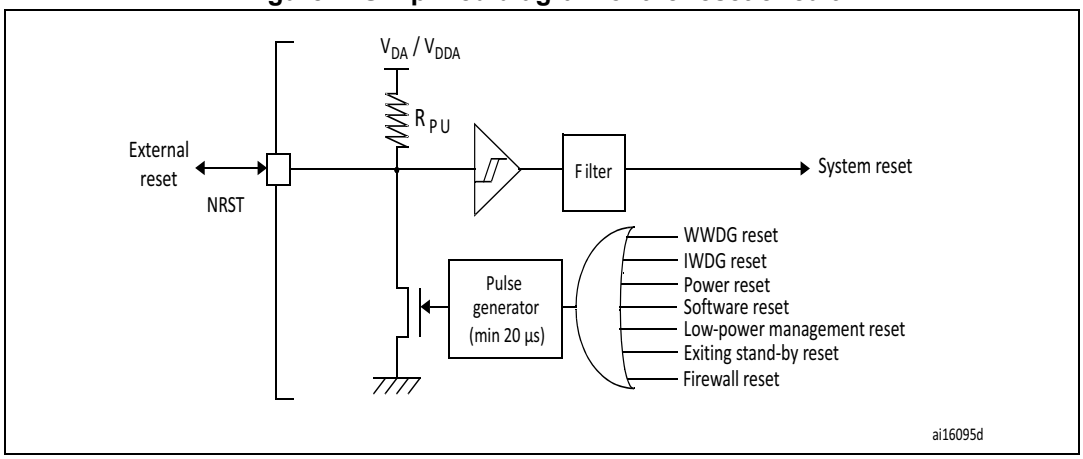
A system reset sets all registers to their reset values except for the RTC, backup registers and RCC control/status register, RCC_CSR.

A system reset is generated when one of the following events occurs:

1. A low level on the NRST pin (external reset)
2. Window watchdog end-of-count condition (WWDG reset)
3. Independent watchdog end-of-count condition (IWDG reset)
4. A reset bit set by software (SWreset)
5. Entering Standby or Stop mode configured to generate a reset (Low-power management reset)
6. Option byte loader reset
7. Exiting Standby mode
8. Firewall reset.

The reset source can be identified by checking the reset flags in the Control/Status register, RCC_CSR.

Figure 7. Simplified diagram of the reset circuit



The STM32L does not require an external reset circuit to power-up correctly. Only a pull-down capacitor is recommended to improve EMS performance by protecting the device against parasitic resets (see *Figure 7*).

Charging/discharging the pull-down capacitor through the internal resistor adds to the device power consumption. The recommended value of 100 nF for the capacitor can be reduced to 10 nF to limit power consumption.

2 Clocks

Four different clock sources can be used to drive the system clock (SYSCLK):

- HSI16 (high-speed internal) oscillator clock
- HSE (high-speed external) oscillator clock
- PLL clock
- MSI (multispeed internal) oscillator clock

The MSI is used as a system clock source after startup from reset, wake-up from Standby low-power modes.The MSI, HSI16 or HSI16 divided by four, are used as a system clock source after wake-up from Stop low-power mode.

The devices have the following two secondary clock sources:

- 37 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for auto-wakeup from Stop/Standby mode.
- 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the real-time clock (RTCCLK)

The STM32L0x2 and STM32L0x3 have HSI48 (high-speed internal) oscillator clock available for USB and Random generator. This permits a USB communication without the need for external clock source.

Each clock source can be switched on or off independently when not used, to optimize power consumption.

Refer to the STM32L0xx reference manuals (RM0367, RM0376, RM0377) for a description of the clock tree.

2.1 MSI clock

The MSI clock signal is generated from an internal RC oscillator. Its frequency range can be adjusted by software through the RCC_ICSCR register. Seven frequency ranges are available: 65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.1 MHz (default value) and 4.2 MHz, all are multiple values of 32.768 kHz.

The MSI clock is used as a system clock after a restart from reset.

The MSI RC oscillator has the advantage of providing a low-cost (no external components) low-power clock source. It is used as a wakeup clock in low-power modes to reduce power consumption and wakeup time.

The MSIRDY flag in the RCC_CR register indicates wether the MSI RC is stable or not. At startup, the MSI RC output clock is not released until this bit is set by hardware.

The MSI RC can be switched on and off through the RCC_CR register (default is on).

Calibration

If the application is subject to voltage or temperature variations, this may affect the RC oscillator speed. You can trim the MSI frequency in the application through the RCC_ICSCR register. Typically, this uses the HSE or LSE as reference (see RM0367/376/377 for details on clock measurement with TIM21). For more information refer to AN3300 *“How to calibrate an STM32Lxx internal RC oscillator”*.

2.2 HSE OSC clock

The high-speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE user external clock (see *Figure 8*)
- HSE external crystal/ceramic resonator (see *Figure 9*)

Figure 8. External clock

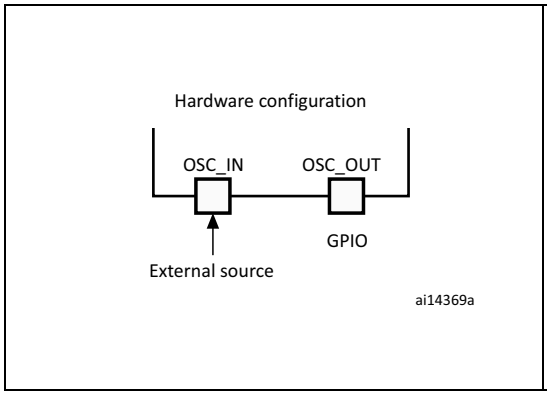
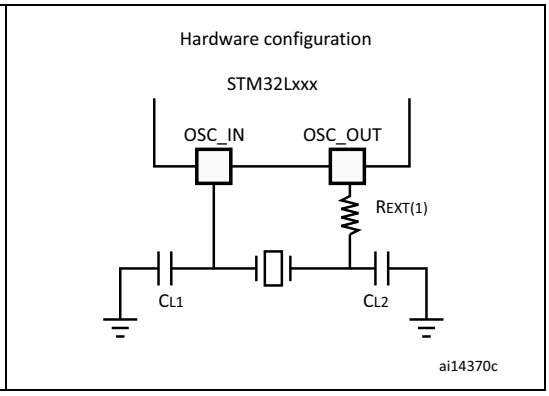


Figure 9. Crystal/ceramic resonators



1. The value of R_{EXT} depends on the crystal characteristics. A typical value is in the range of 5 to 6 R_S (resonator series resistance).To fine tune the REXT value ,refer to AN2867(*Oscillator design guide for ST microcontrollers*)
2. Load capacitance, C_L, has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where: C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. Please refer to *Section 5.4: Decoupling* to minimize its value.

2.2.1 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 32 MHz.

The external clock signal (square, sine or triangle) with a duty cycle of about 50%, has to drive the OSC_IN pin, while the OSC_OUT pin can be used as a GPIO. For Category 2 devices, when the package does not provide OSC_IN, PA0 can receive the external clock source, see CK_IN definition in RM0377. From current consumption standpoint a square signal is preferred (see *Figure 8*).

When HSE Bypass is used with V_{DD} below 2.0 V and in range 1, take care of the frequency drop as explained in *Section 1.1.3: Voltage regulator*.

2.2.2 External crystal/ceramic resonator (HSE crystal)

The external oscillator frequency ranges from 1 to 25 MHz.

The external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in *Figure 9*.

The resonator and the load capacitors have to be connected as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The load capacitance values must be adjusted according to the selected oscillator.

For C_{L1} and C_{L2} it is recommended to use high-quality ceramic capacitors in the 5 to 25 pF range (typical), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. C_{L1} and $C_{L2,}$ are usually the same value. The

crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. The PCB and MCU pin capacitances must be included when sizing C_{L1} and C_{L2} (10 pF can be used as a rough estimate of the combined pin and board capacitance).

Refer to the electrical characteristics sections in the datasheet of your product for more details, and to application note AN2867 “*Oscillator design guide for STM microcontrollers*”.

2.3 LSE OSC clock

The LSE crystal is a 32.768 kHz Low Speed External crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

2.3.1 External crystal/ceramic resonator (LSE crystal)

The LSE crystal is switched on and off using the LSEON bit in RCC control/status register (RCC_CSR). The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits (in RCC_CSR register) to obtain the best compromise between robustness and short start-up time on one side and low-power consumption on the other (see *Figure 10*).

The LSERDY flag (in RCC_CSR) indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated, if enabled, in the Clock interrupt enable register (RCC_CIER).

2.3.2 External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. You select this mode by setting the LSEBYP and LSEON bits (in RCC_CSR). The external clock signal (square, sinus or triangle) has to drive the OSC32_IN pin, from current consumption standpoint a square signal is preferred. The OSC32_OUT pin can be used as GPIO (see *Figure 10*)

Figure 10. External clock

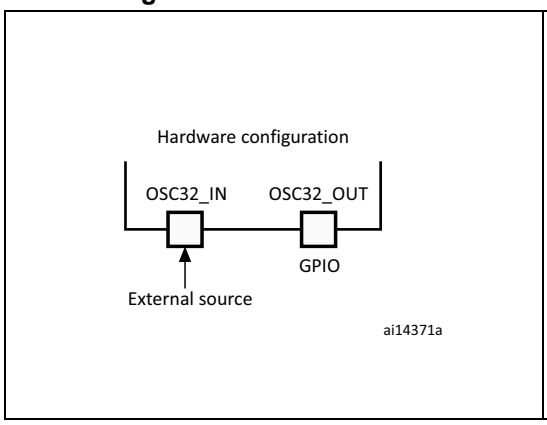
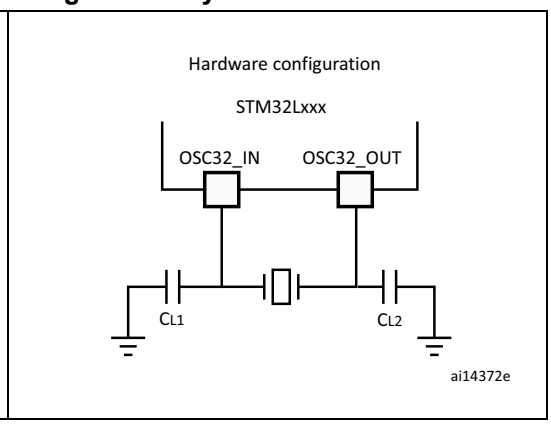


Figure 11. Crystal/ceramic resonators



1. OSC32_IN and OSC_OUT pins can be also used as GPIOs, but it is recommended not to use them as both RTC and GPIO pins in the same application.

2.4 Clock security system on HSE (CSSHSE)

The clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped. If a failure is detected on the HSE oscillator clock, this oscillator is automatically disabled and an interrupt is generated to inform the software about the failure (clock security system on HSE interrupt, CSSHSEI), allowing the MCU to perform rescue operations. The CSSHSEI is linked to the Cortex®-M0+ NMI (non-maskable interrupt) exception vector.

If the HSE oscillator is used directly or indirectly as the system clock (indirectly means: it is used as the PLL input clock, and the PLL clock is used as the system clock), a detected failure causes the system clock to switch to the MSI oscillator and the external HSE oscillator to be disabled. If the HSE oscillator clock is the clock entry of the PLL used as the system clock when the failure occurs, the PLL is also disabled.

For details, see the STM32L0xx reference manuals (RM0367, RM0376, RM0377).

2.5 HSI16 clock

The HSI16 clock signal is generated from an internal 16 MHz RC oscillator and can be used directly as a system clock or can used as PLL input. The HSI16 RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator. However, even with calibration, the frequency is less accurate than an external crystal oscillator or ceramic resonator.

Calibration

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations, This is why each device is factory calibrated by ST for 1% accuracy at T_A = 25°C.

If the application is subject to voltage or temperature variations, the RC oscillator speed will be impacted. You can trim the HSI16 frequency in the application through the RCC_ICSCR register. Typically, this uses the HSE or LSE as reference (see RM0367/376/377 for details on clock measurement with TIM21). For more information refer to AN3300 *“How to calibrate an STM32Lxx internal RC oscillator”*.

2.6 LSI clock

The LSI RC acts as an low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and RTC. The clock frequency is around 40 kHz (between 30 and 60 kHz). For more details, refer to the electrical characteristics section of the datasheets.

3 Boot configuration

3.1 Boot mode selection

In the Root part number 1, three different boot modes can be selected through the BOOT0 pin and nBOOT1 option bit, as shown in *Table 2*.

Table 2. Boot modes

BOOT mode selection pins		Boot mode	Aliasing
BOOT1(1)	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM	Embedded SRAM is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 option bit.

The values on the BOOT0 pin and nBOOT1 bit are latched on the 4th rising edge of SYSCLK after a reset. The user must set nBOOT1 and BOOT0 to select the required boot mode.

BOOT0 is a dedicated pin.The BOOT0 pin and nBOOT1 bit are also resampled when exiting Standby mode. Consequently, they must be kept in the required Boot mode configuration in Standby mode. After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, and starts code execution from the boot memory starting from 0x0000 0004.

Depending on the selected boot mode, main Flash program memory, system memory or SRAM is accessible as follows:

- Boot from main Flash memory: the main Flash program memory is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x0800 0000). In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from System memory: the system memory is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x1FFF EC00).
- Boot from embedded SRAM: the SRAM is aliased in the boot memory space (0x0000 0000), but is still accessible from its original memory space (0x2000 0000).

3.2 Embedded boot loader

The embedded boot loader is located in the System memory, programmed by ST during production. It is used to reprogram the Non Volatile memory using one of the interfaces listed in *Table 3*.

Table 3. Interfaces for different device categories

Interface	Ports	Device category
USART1	PA9/PA10	Cat 3 Cat 5
USART2	PA9/PA10	Cat 2
	PA2/PA3	Cat 3 Cat 5
SPI1	PA4/PA5/PA6/PA7	Cat 2/3 Cat 5 (without USB)
SPI2	PB12/PB13/PB14/PB15	Cat 3 Cat 5 (without USB)
USB	PA11/PA12	Cat 5 (with USB)
I2C1	PB6/PB7	Cat 5 (without USB)
I2C2	PB10/PB11	Cat 5 (without USB)

For additional information, refer to application note AN2606.

3.3 BOOT0 pin connection

The BOOT0 pin of the Root part number 1 has a lower V_{IL} than the other GPIO (for details see datasheet I/O static characteristics), thus as it does not fit CMOS requirement, when driven by another CMOS circuit the signal level must be verified.

4 Debug management

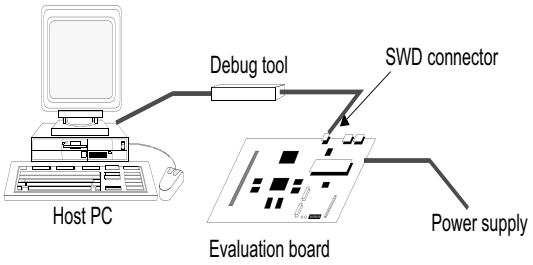
4.1 Introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a SW connector and a cable connecting the host to the debug tool.

Figure 12 shows the connection of the host to a development board.

The Nucleo demonstration board embeds the debug tools (ST-LINK) so it can be directly connected to the PC through an USB cable.

Figure 12. Host-to-board connection



4.2 SWD debug port (serial wire)

The STM32L0xx core integrates the serial wire debug port (SW-DP). It is an ARM® standard CoreSight™ debug port with a 2-pin (clock + data) interface to the debug access port.

4.3 Pinout and debug port pins

The STM32L0xx MCUs are offered in various packages with varying numbers of pins.

4.4 Serial wire debug (SWD) pin assignment

The same SWD pin assignment is available on all STM32L0xx packages.

Table 4. SWD port pins

SWD pin name	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	Serial wire clock	PA14

4.4.1 SWD pin assignment

After reset (SYSRESETn or PORESETn), the pins used for the SWD are assigned as dedicated pins which are immediately usable by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for general-purpose I/O (GPIO) usage. For more details on how to disable SWD port, refer to the section on I/O pin alternate function multiplexer and mapping of reference manuals RM0367/ 0376 / 0377.

4.4.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of these pins. The reset states of the GPIO control registers put the I/Os in the equivalent states:

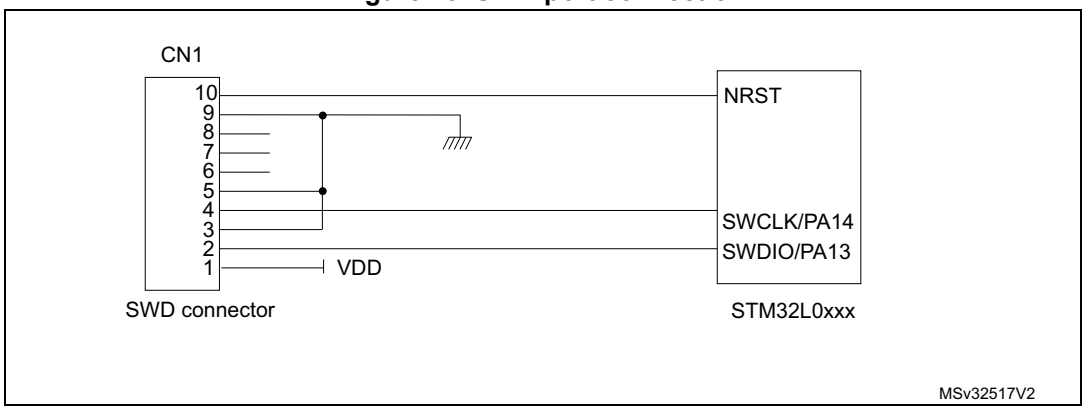
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

4.4.3 SWD port connection with standard SWD connector

Figure 13 shows the connection between the STM32L0xx and a standard SWD connector.

Figure 13. SWD port connection



5 Recommendations

5.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

5.2 Component position

A preliminary layout of the PCB must make separate:

- high-current circuits
- low-voltage circuits
- digital component circuits
- circuits separated according to their EMI contribution. This will reduce cross-coupling on the PCB that introduces noise.

5.3 Ground and power supply (V_{SS}, V_{DD}, V_{SSA}, V_{DDA})

Every block (noisy, low-level sensitive, digital, etc.) should be grounded individually, and all ground returns should be to a single point. Loops must be avoided or have a minimum area. In order to improve analog performance, you must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device. The power supplies should be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

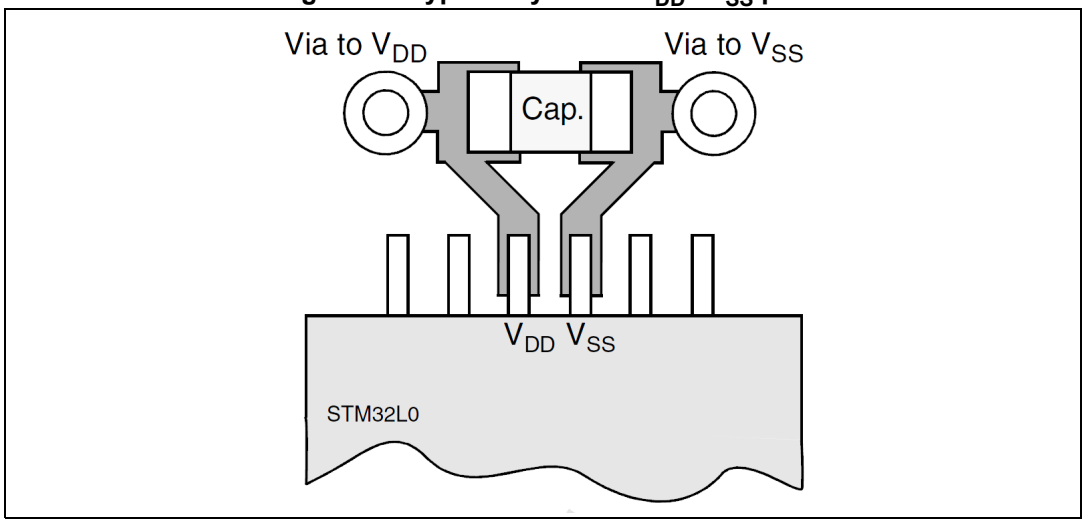
5.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors C (100 nF) and a tantalum or ceramic capacitor C of about 10 µF connected in parallel on the Root part number 1 device. Some package use a common V_{SS} for several V_{DD} instead of a pair of power supply (one V_{SS} for each V_{DD}), in that case the capacitors must be between each V_{DD} and the common V_{SS}.These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 to 100 nF, but exact values depend on the application needs.

Figure 14 shows the typical layout of such a V_{DD} / V_{SS} pair.

Figure 14. Typical layout for V_{DD} / V_{SS} pair



5.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (which is the case for interrupts and handshaking strobe signals but, not the case for LED commands).
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
  For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (example, clock)
- Sensitive signals (example, high impedance)

5.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance and avoid extra power consumption, unused clocks, counters or I/Os, should not be left free. I/Os should be connected to a fixed logic level of 0 or 1 by an external or internal pull-up or pull-down on the unused I/O pin. The other option is to configure GPIO as output mode using software. Unused features should be frozen or disabled, which is their default value.

6 Reference design

6.1 Description

The reference design shown in *Figure 15*, is based on the STM32L053RBT6.

This reference design can be tailored to any Root part number 1 device with a different package, using the pin correspondence given in *Table 7: Reference connection for all packages*.

6.1.1 Clock

Two clock sources are used for the microcontroller:

- LSE: X2– 32.768 kHz crystal for the embedded RTC
- HSE: X1– 8 MHz crystal for the Root part number 1 microcontroller

Refer to *Section 2: Clocks*.

6.1.2 Reset

The reset signal in *Figure 15* is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to *Section 1.3: Reset and power supply supervisor*.

6.1.3 Boot mode

The boot option is configured by setting switches SW1 (Boot 0). Refer to *Section 3: Boot configuration*.

Note: When waking up from Standby mode, the Boot pin is sampled. In this situation, you need to pay attention to its value.

6.1.4 SWD interface

The reference design shows the connection between the Root part number 1 and a standard SWD connector. Refer to *Section 4: Debug management*.

Note: It is recommended to connect the reset pins so as to be able to reset the application from the tools.

6.1.5 Power supply

Refer to *Section 1: Power supplies*.

6.2 Component references

Table 5. Mandatory components

Reference	Component name	Value	Quantity	Comments
U1A	Microcontroller	STM32L053R8(T6)	1	64-pin package
C8, C9, C10, C13	Capacitor	100 nF	3 ... 5	Ceramic capacitors (decoupling capacitors)
C11	Capacitor	4.7 µF	1	Tantalum / chemical / ceramic capacitor (decoupling capacitor)
C6, C12	Capacitor	1 µF	2	Ceramic capacitor (LCD booster or decoupling capacitor)

Table 6. Optional components

Reference	Component name	Value	Quantity	Comments
R1	Resistor	390 Ω	1	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
C5	Capacitor	100 nF	1	Ceramic capacitor
C1, C2	Capacitor	6.8 pF	2	Used for LSE: the value depends on the crystal characteristics. Fits for MC-306 32.768K-E3, which has a load capacitance of 6 pF.
C3, C4	Capacitor	20 pF	2	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
X1	Quartz	8 MHz	1	Used for HSE
X2	Quartz	32.764 kHz	1	Used for LSE
CN1	SWD connector	HE10	1	-
SW1	Switch	-	2	Used to select the right boot mode
B1	Push-button	-	1	-
L1	Ferrite bead	-	1	For EMC reduction on V_{DDA} supply, can be replaced by a direct connection between V_{DD} and V_{DDA}

Figure 15. Reference design (based on STM32L053RBT6)

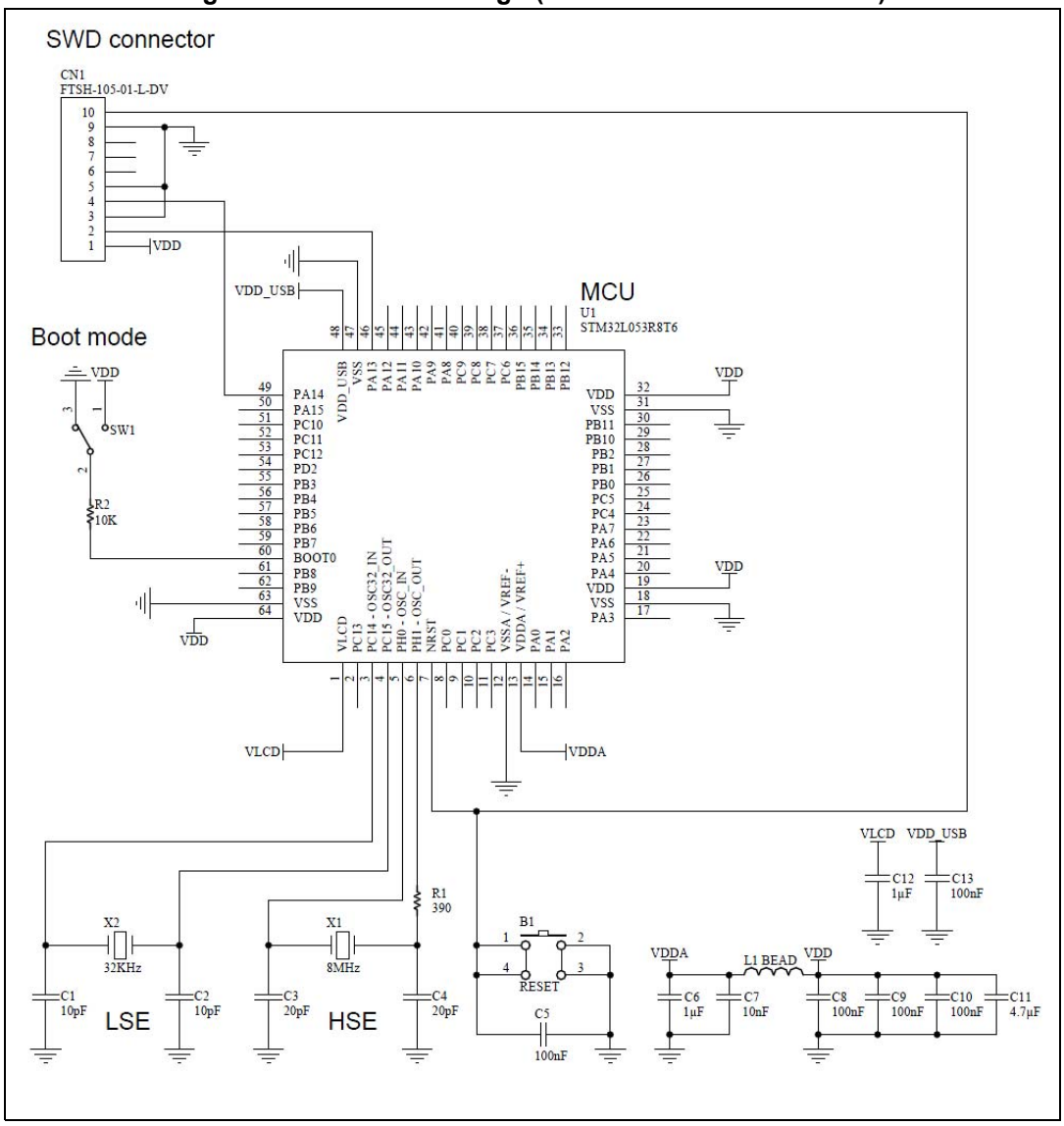


Table 7. Reference connection for all packages

Package	LQFP				BGA		CSP			QFN		
Number of pins	32	48	64	100	64	100	25	36	49	28	32(1)	32(2)
V_{LCD}	-	1	1	6	B2	E2	-	-	B6	-	-	-
PC14-OSC32_IN	2	3	3	8	A1	D1	A5	A6	C6	2	2	1
PC15-OSC32_OUT	3	4	4	9	B1	E1	B5	B6	C7	3	3	2
PH0-OSC_IN	-	5	5	12	C1	F1	-	-	D6	-	-	-
PH1-OSC_OUT	-	6	6	13	D1	G1	-	-	D7	-	-	-
NRST	4	7	7	14	E1	H2	C5	C6	D5	4	4	3
V_{SSA}	-	8	12	19	F1	J1	-	-	-	-	-	4
V_{REF-}	-	-	-	20	-	K1	-	-	-	-	-	-
V_{REF+}	-	-	-	21	G1	L1	-	E6	E6	-	-	-
V_{DDA}	5	9	13	22	H1	M1	D4	D5	F7	5	5	5
V_{SS_4}	-	-	18	27	C2	E3	-	-	-	-	-	-
V_{DD_4}	-	-	19	28	D2	H3	-	-	-	-	-	-
V_{SS_1}	16	23	31	49	D5	F12	-	-	D4	-	-	16
V_{DD_1}	17	24	32	50	E5	G12	-	F1	G2	-	17	17
PA13	23	34	46	72	A8	A11	A1	A1	C2	21	23	23
V_{DD_5}	-	-	-	73	-	C11	-	-	-	-	-	-
V_{SS_2}	-	35	47	74	D6	F11	D5	-	-	-	-	-
V_{DD_USB}	-	36	48	75	E6	G11	-	-	A1	-	-	24
PA14	24	37	49	76	A7	A10	C2	B2	B2	22	24	25
BOOT0	31	44	60	94	B4	A4	C4	C5	A5	1	31	30
V_{SS_3}	32	47	63	99	D4	D3	-	D6	-	-	-	31
V_{DD_3}	1	48	64	100	E4	C4	-	A5	A7	-	1	32

1. Cat 2/3 devices
2. Cat 5 devices

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
24-Apr-2014	1	Initial release
22-Jan-2015	2	Updated *Section 1.1: Introduction*, *Section 1.1.1: Independent A/D converter supply and reference voltage*, *Section 1.1.3: Voltage regulator* and *Section 2.2.1: External source (HSE bypass)*. Added *Table 3: Interfaces for different device categories*. Updated *Table 1: VLCD rails connections to GPIO pins* and *Table 7: Reference connection for all packages*.

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