AN4602
Application note

LIS3MDL: three-axis digital output magnetometer

Introduction

This document is intended to guide in the usage of and to provide useful details related to ST’s LIS3MDL 3-axis digital magnetometer.

The LIS3MDL is a three-axis high-performance magnetic sensor with a 16-bit resolution and a full scale of ±4/±8/±12/±16 gauss (user-selectable).

Sensor low-power consumption combined with power saving operating modes enables targeting handheld portable applications such as cell phones and tablets.

The ultra-small size and weight of its small, thin, plastic, land grid array package (LGA-12 2x2x1) make it an ideal choice for any application where reduced package size and weight are required, helping to optimize placement on the board.

Thermal stability of the device is guaranteed, internally compensating sensitivity drift over temperature variations using an advanced embedded algorithm.

To support integration in smart applications, the device may be configured to generate interrupt signals using thresholds programmable by the end user on the fly.

External communication is managed by a digital I^2C/SPI serial interface standard output.

The device is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

ST software support available for the LIS3MDL includes drivers, a tilt-compensated electronic compass, dynamic magnetometer calibration, 6-axis virtual gyro and complete 9-axis sensor fusion.

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1 Registers

Table 1: Registers

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OFFSET_X_REG_L_M	05h	XOFF7	XOFF6	XOFF5	XOFF4	XOFF3	XOFF2	XOFF1	XOFF0
OFFSET_X_REG_H_M	06h	XOFF15	XOFF14	XOFF13	XOFF12	XOFF11	XOFF10	XOFF9	XOFF8
OFFSET_Y_REG_L_M	07h	YOFF7	YOFF6	YOFF5	YOFF4	YOFF3	XOFF2	YOFF1	YOFF0
OFFSET_Y_REG_H_M	08h	YOFF15	YOFF14	YOFF13	YOFF12	YOFF11	YOFF10	YOFF9	YOFF8
OFFSET_Z_REG_L_M	09h	ZOFF7	ZOFF6	ZOFF5	ZOFF4	ZOFF3	ZOFF2	ZOFF1	ZOFF0
OFFSET_Z_REG_H_M	0Ah	ZOFF15	ZOFF14	ZOFF13	ZOFF12	ZOFF11	ZOFF10	ZOFF9	ZOFF8
WHO_AM_I	0Fh	0	0	1	1	1	1	0	1
CTRL_REG1	20h	TEMP_EN	OM1	OM0	DO2	DO1	DO0	FAST_ODR	ST
CTRL_REG2	21h	0	FS1	FS0	0	REBOOT	SOFT_RST	0	0
CTRL_REG3	22h	0	0	LP	0	0	SIM	MD1	MD0
CTRL_REG4	23h	0	0	0	0	OMZ1	OMZ0	BLE	0
CTRL_REG5	24h	FAST_READ	BDU	0	0	0	0	0	0
STATUS_REG	27h	ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
OUT_X_L	28h	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
OUT_X_H	29h	XD15	XD14	XD13	XD12	XD11	XD10	XD9	XD8
OUT_Y_L	2Ah	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
OUT_Y_H	2Bh	YD15	YD14	YD13	YD12	YD11	YD10	YD9	YD8
OUT_Z_L	2Ch	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
OUT_Z_H	2Dh	ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8
TEMP_OUT_L	2Eh	TMPO7	TMPO6	TMPO5	TMPO4	TMPO3	TMPO2	TMPO1	TMPO0
TEMP_OUT_H	2Fh	TMPO7	TMPO6	TMPO5	TMPO4	TMPO3	TMPO2	TMPO1	TMPO0
INT_CFG	30h	XIEN	YIEN	ZIEN	0	0	IEA	LIR	IEN

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
INT_SRC	31h	PTH_X	PTH_Y	PTH_Z	NTH_X	NTH_Y	NTH_Z	MROI	INT
INT_THS_L	32h	THSL7	THSL6	THSL5	THSL4	THSL3	THSL2	THSL1	THSL0
INT_THS_H	33h	THSH7	THSH6	THSH	THSH4	THSH3	THSH2	THSH1	THSH0

2 General configuration

Various features of the LIS3MDL can be configured by using CTRL_REG1, CTRL_REG2, CTRL_REG3 and CTRL_REG4.

- Output data rate (ODR)
  - Register CTRL_REG1; bits DO2, DO1, DO0, FAST_ODR
- Operating modes
  - Register CTRL_REG1: bits OM1, OM0
  - Register CTRL_REG4: bits OMZ1, OMZ0
- Full-scale
  - Register CTRL_REG2: bits FS1, FS0
- Measurement mode
  - Mode register (CTRL_REG3): bits MD1, MD0

2.1 Full scale

The LIS3MDL provides a selectable full scale to adjust the input dynamic range of the device to the amplitude of the magnetic field to be measured.

Full-scale configuration is selected by setting bits FS1, FS0 (register CTRL_REG2).

Table 2: Full-scale selection

FS1	FS0	Full-scale [G]	Gain@16-bit (LSB/G)
0	0	±4	6842
0	1	±8	3421
1	0	±12	2281
1	1	±16	1711

2.2 Operating modes

The LIS3DML allows four possible operating modes: low-power, medium-performance, high -performance and ultra-high-performance.

Operating modes on the X/Y axes can be chosen independently from the operating mode on the Z-axis:

- X/Y axes operating mode can be selected by setting bits OM1, OM0 (register CTRL_REG1)
- Z-axis operating mode by using bits OMZ1, OMZ0 (register CTRL_REG4)

Table 3: X/Y axes operating mode selection

Operating mode	OM1	OM0
Low-power	0	0
Medium-performance	0	1
High-performance	1	0
Ultra-high-performance	1	1

Table 4: Z-axis operating mode selection

Operating mode	OMZ1	OMZ0
Low-power	0	0
Medium-performance	0	1
High-performance	1	0
Ultra-high-performance	1	1

The output noise is strictly related to the operating mode. The noise level sets the minimum detectable field. In the following table noise is given for different operating modes.

Table 5: Noise in operating modes (average per axis)

Operating mode	RMS noise [mgauss]
Ultra-high-performance	3.5
High-performance	4.0
Medium-performance	4.6
Low-power	5.3

2.2.1 Output data rate

Register CTRL_REG1 (bits DO2, DO1, DO0,FAST_ODR) allows selecting ODR frequency.

A higher ODR can be selected by configuring bit 1 of CTRL_REG1.

Table 6: Data rate configuration

DO2	DO1	DO0	FODR	ODR [Hz]	OM
0	0	0	0	0.625	X
0	0	1	0	1.25	X
0	1	0	0	2.5	X
0	1	1	0	5	X
1	0	0	0	10	X
1	0	1	0	20	X
1	1	0	0	40	X
1	1	1	0	80	X
X	X	X	1	1000	LP
X	X	X	1	560	MP
X	X	X	1	300	HP
X	X	X	1	155	UHP

2.3 Measurement mode

The system goes to idle mode:

- automatically at the end of startup procedure
- automatically, if single-measurement mode has been selected at the end of the measurement process

Idle mode can also be forced by the user, setting the MD1 bit equal to 1 (mode register CTRL_REG3) . In idle mode (current consumption around 1 uA) the system is waiting for startup configuration commands. (Refer also to *Section 2.4: "Current consumption"*, and *Section 3: "Reading output data"*). Single/Continuous measurement mode can be selected by configuring bits MD1, MD0 of mode register (CTRL_REG3).

Table 7: System modes

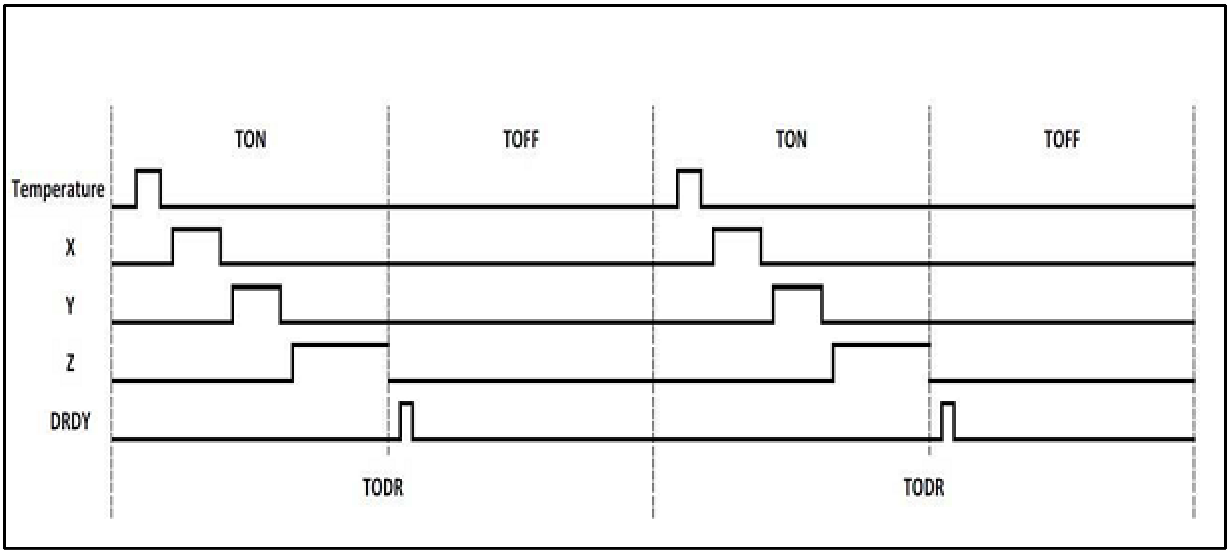
MD1	MD0	Mode
0	0	Continuous-measurement mode
0	1	Single-measurement mode
1	0	Idle mode
1	1	Idle mode

During single-measurement mode, the device performs a single measurement and writes the measured data in the data output register. After the measurement has been completed and the output data registers are updated, the device is reset to idle mode: the Mode register is consequently changed to idle mode (bit MD1 = 1).

During continuous-measurement mode, the device continuously performs measurements and writes measured data in the data output registers. In order to reduce average power consumption, the device is configured in a state similar to idle mode (called TOFF) between two consecutive measurements.

In TOFF mode average power consumption is reduced to a few µA by switching off the main blocks.

Figure 1: Sampling timing in continuous mode



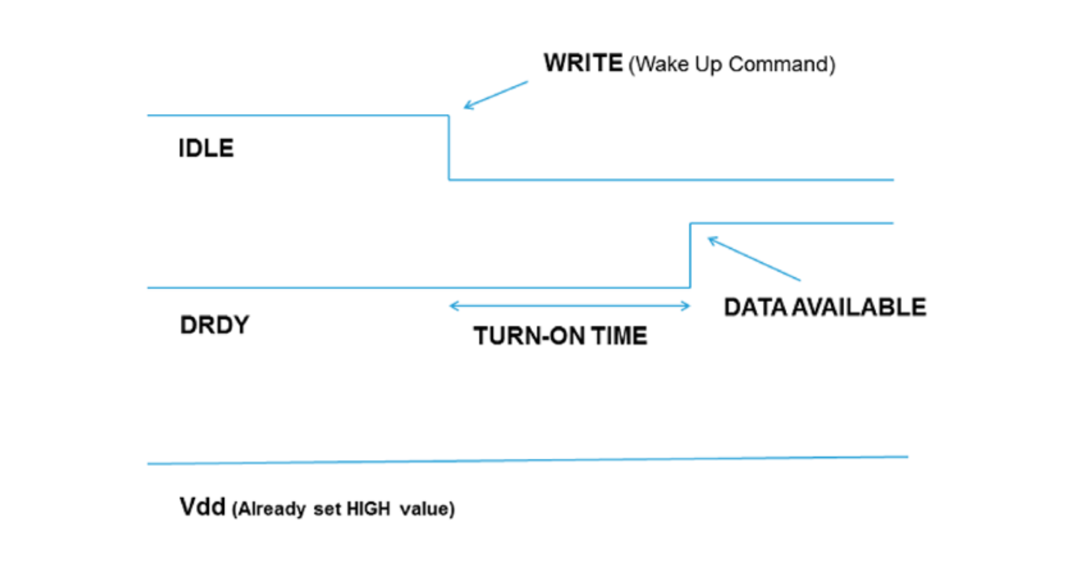
In the figure above we can see that the duty cycle is equal to TON/(TON + TOFF) = TON*ODR (where ODR=1/(TON + TOFF). Therefore the average power consumption is strictly dependent on the selected ODR (see *Table 10: "Current consumption (µA)"*).

Moreover, please note that different TON durations correspond to different operating modes which correspond to different duty cycles, therefore current consumption depends on both OM and ODR (see *Section 2.4: "Current consumption"*).

2.3.1 Turn-on time

Turn-on time is the interval between the wakeup command and data availability.

Figure 2: Turn-on time



The following table gives the turn-on time for each operating mode.

Table 8: Turn-on time

Operating mode	Startup time [ms]
Low-power	1.2
Medium-performance	1.91
High-performance	3.48
Ultra-high-performance	6.65

2.3.2 Switching modes

If the LIS3MDL device has been configured in continuous measurement, it is possible to change OM and/or ODR without switching to idle mode.

In this case (see *Table 9: "TON for operating modes"*) the system will reach the new configuration after a time interval given by the sum of the TON related to the old configuration and the TON related to the new configuration. For instance if we move from MP to UHP, the system will reach the new configuration after 1.65 ms + 6.4 ms = 8.05 ms .

All the performed measurements are valid and no data has to be deleted.

The following table gives TON duration for different OMs.

Table 9: TON for operating modes

Operating mode	TON [ms]
LP	0.9
MP	1.65
HP	3.23
UHP	6.4

2.4 Current consumption

The following tables summarize typical consumption for the different ODR allowed in each operating mode. Fast ODR consumption is summarized in the last four rows.

Table 10: Current consumption (µA)

ODR (Hz)	LP	MP	HP	UHP
0.625	6	7	10	15
1.25	7	10	15	25
2.5	10	15	25	40
5	15	25	40	75
10	25	40	75	145
20	40	75	145	270
40	80	145	285	565
80	150	290	565	1125
155	-	-	-	1950
300	-	-	1870	-
560	-	1720	-	-
1000	1500	-	-	-

When the system is in idle mode (bit MD1 of CTRL_REG3 equal to 1) current consumption is around 1 µA .

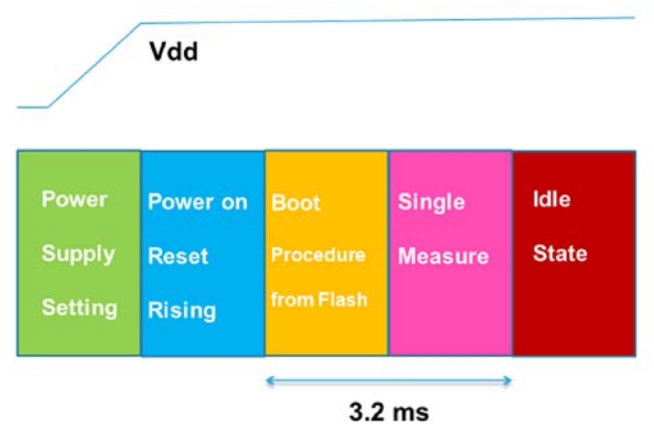
3 Reading output data

3.1 Startup sequence

After “Power-on reset rising” all the configuration/calibration parameters are loaded from FTP memory, then a single measure is performed and valid data are written in the output registers. At this stage the system goes to idle mode waiting for further commands through the I^2C/SPI interface. Please note that during the startup sequence, the DRDY pin is set to low.

The startup sequence can be summarized in the following figure.

Figure 3: Startup sequence



A typical wakeup sequence is summarized as follows:

1. Write 40h in CTRL_REG2. Sets full scale ±12 Hz.
2. Write FCh in CTRL_REG1. Sets UHP mode on the X/Y axes, ODR at 80 Hz and activates temperature sensor.
3. Write 0Ch in CTRL_REG4. Sets UHP mode on the Z-axis.
4. Write 00h in CTRL_REG3. Sets continuous-measurement mode.

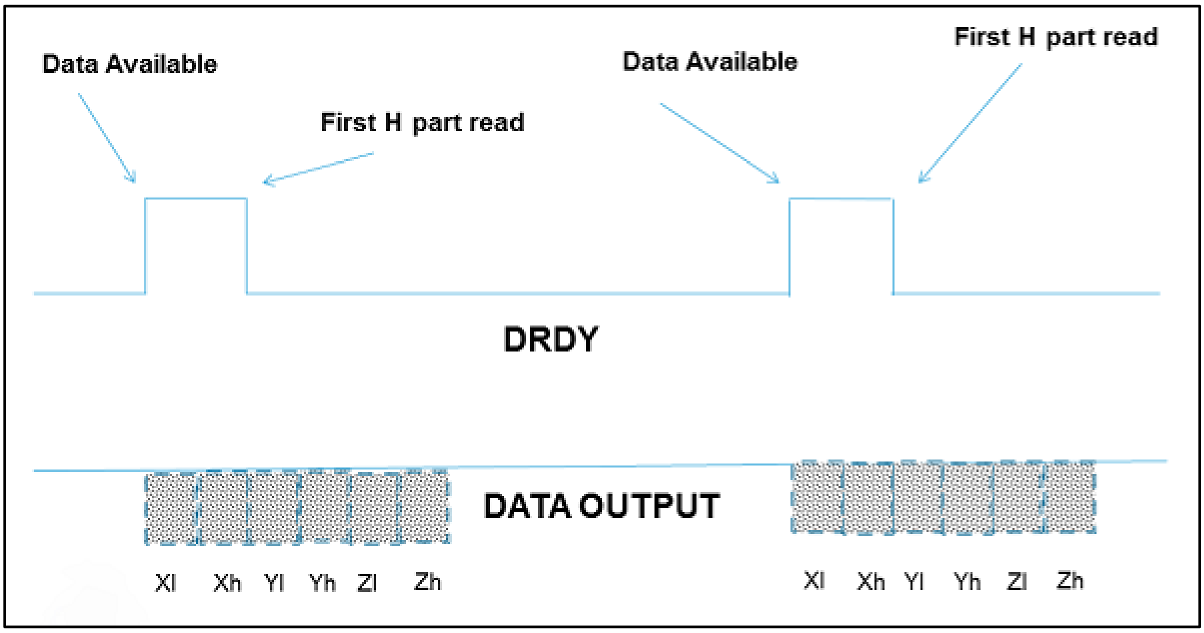
3.2 Reading magnetometer data

Data can be read in two ways: accessing directly the DRDY pin (pin 8) or reading bit 3 of STATUS_REG.

3.2.1 Using the data-ready (DRDY) signal

Pin 8 (DRDY) represents the content of the XYZDA bit of the STATUS_REG register. The data-ready signal rises to 1 when a new set of data has been generated and is available for reading. As soon as the first “High part” of the output data is read, DRDY goes low.

Figure 4: DRDY flow



Summarizing the read from the DRDY pin:

1. Read the DRDY pin
2. If DRDY = 0, then go to step 1
3. Read OUT_X_L
4. Read OUT_X_H
5. Read OUT_Y_L
6. Read OUT_Y_H
7. Read OUT_Z_L
8. Read OUT_Z_H
9. Data processing
10. Go to step 1

3.2.2 Using the STATUS_REG register

Directly polling the STATUS_REG register allows checking bit 7 (overrun). If bit 7 is set to 1, the reading rate is not adequate compared to the data production rate. If one or more magnetometer samples have been overwritten by new data because of an excessively slow reading rate, the ZYXOR bit of the STATUS_REG register is set to 1.

Reading from the STATUS_REG can be summarized as follows:

1. Read STATUS_REG
2. If STATUS_REG(3) = 0, then go to step 1
3. If STATUS_REG(7) = 1, some data have been overwritten
4. Read OUT_X_L
5. Read OUT_X_H
6. Read OUT_Y_L
7. Read OUT_Y_H
8. Read OUT_Z_L
9. Read OUT_Z_H
10. Data processing
11. Go to step 1

3.2.3 Using the block data update (BDU) feature

If the reading of the magnetic data cannot be synchronized with the XYZDA bit in the STATUS_REG register, it is strongly recommended to set the BDU (block data update) bit to 1 in CTRL_REG5 register.

This feature avoids the reading of values (most significant and least significant parts of the magnetic data) related to different samples. In particular, when the BDU is activated, the data registers related to each channel always contain the most recent magnetic data produced by the device, but, in case the reading of a given pair (i.e. OUT_X_H and OUT_X_L, OUT_Y_H and OUT_Y_L, OUT_Z_H and OUT_Z_L) is initiated, the refresh for that pair is blocked until both MSB and LSB parts of the data are read.

BDU only guarantees that OUT_X(Y, Z)_L and OUT_X(Y,Z)_H have been sampled at the same moment. For example, if the reading speed is too low, it may read X and Y sampled at T1 and Z sampled at T2.

3.2.4 FAST_READ option

Reading of output data occurs through the I^{2}C Interface. To accelerate the reading process the I^{2}C interface can be configured to allow reading of multiple bytes: data stored in all the data output registers will be transferred in the same transaction. At this point, if we are interested in H values only, it is not efficient to read L values.

By activating the FAST_READ option we allow the transfer of the high part of the output data only and we can disregard the low part of the output data.

For details concerning the I^{2}C interface, please refer to section 5.1 of the LIS3MDL datasheet.

The FAST_READ option can be selected by setting bit7 of CTRL_REG5 equal to 1..

3.3 Understanding magnetic data

The magnetic data are sent to the OUT_X_H, OUT_X_L, OUT_Y_H, OUT_Y_L, OUT_Z_H, and OUT_Z_L registers. These registers contain, respectively, the most significant part and the least significant part of the magnetic signals acting on the X, Y, and Z axes.

Complete data for the X (Y, Z) channel is given by the concatenation OUT_X_H & OUT_X_L (OUT_Y_H & OUT_Y_L, OUT_Z_H & OUT_Z_L) and it is expressed as a two’s complement number.

Magnetic data are represented as 16-bit numbers and are left-justified.

3.3.1 Big-little endian selection

The LIS3MDL allows swapping the content of the lower and the upper part of the data registers (i.e. OUT_X_H with OUT_X_L), to be compliant with both little-endian and big-endian data representations.

“Little Endian” means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. (The little end comes first). This mode corresponds to bit BLE (in CTRL_REG4 register) reset to 0 (default configuration).

On the contrary, “Big Endian” means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.

In the following table some examples showing the use of bit BLE are given.

Table 11: Output data registers content vs. magnetic values (FS = 4 G)

Data values [G]	BLE = 0		BLE = 1	
	29h	28h	29h	28h
4	6Ah	E8h	E8h	6Ah
2	35h	74h	74h	35h
1	1Ah	BAh	BAh	1Ah
0.5	0Dh	5Dh	5Dh	0Dh
0	00h	00h	00h	00h
-0.5	F2h	A3h	A3h	F2h
-1.0	E5h	46h	46h	E5h
-2.0	CAh	8Ch	8Ch	CAh
-4.0	95h	18h	18h	95h

4 Interrupt generation

The LIS3MDL interrupt signal can be configured in a very flexible way, allowing to recognize when magnetic data exceeds a threshold value. This signal can be driven on the INT pin

(pin 7).

The registers involved in the interrupt generation behavior are INT_CFG, INT_THS_L, INT_THS_H and INT_SRC.

Registers INT_THS_L and INT_THS_H are used to enter the threshold value used for interrupt generation. Register INT_CFG allows interrupt generation on a single axis, two axes, or for all the three axes. Finally the INT_SRC register allows understanding where the interrupt signal occurred.

4.1 Interrupt configuration

Table 12: INT_CFG (30h) register

XIEN	YIEN	ZIEN	0	0	IEA	LIR	IEN

Table 13: INT_CFG description

XIEN	Enable interrupt generation on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
YIEN	Enable interrupt generation on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
ZIEN	Enable interrupt generation on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured rate value higher than preset threshold)
IEA	Control the polarity on INT when an interrupt occurs. Default value: 0 (0: low; 1: high)
LIR	Latch interrupt request. Default value: 0 (0: interrupt request latched; 1: interrupt request not latched) Once latched, the INT pin remains in the same state until INT_SRC (31h) is read.
IEN	Interrupt enable on INT pin. Default value: 0 (0: disabled; 1: enabled)

The LIR bit allows deciding if the interrupt request must be latched or not. If the LIR bit is ‘1’, the interrupt signal goes high when the interrupt condition is satisfied and returns to low immediately if the interrupt condition cannot be verified. Otherwise, if the LIR bit is ‘0’, when an interrupt condition is applied, the interrupt signal remains high (even if the condition returns to a non-interrupt status) until a read of the INT_SRC register is performed.

4.2 Interrupt threshold

The threshold registers INT_THS_L and INT_THS_H define the magnetic data values used by the interrupt generation circuitry.

Defined threshold values are the same for all three axes.

In case the interrupt mechanism has been enabled for more than one axis, please note that this mechanism acts like a logical OR.

The threshold has to be expressed in absolute value; it is converted to LSB and has to be written in the INT_THS register (unsigned code). The device detects both positive and negative thresholds.

As previously seen, LSB depends on the full scale, refer to *Table 2: "Full-scale selection"* (sensitivity vs. FS table).

Table 14: INT_THS_H (33h) register

ITHRH7	ITHRH6	ITHRH5	ITHRH4	ITHRH3	ITHRH2	ITHRH1	ITHRH0

Table 15: INT_THS_L (32h) register

ITHRL7	ITHRL6	ITHRL5	ITHRL4	ITHRL3	ITHRL2	ITHRL1	ITHRL0

4.3 Interrupt source register

As already stated, the INT_SRC register indicates the cause that generated the interrupt.

The MROI bit switches on when an overflow data is detected.

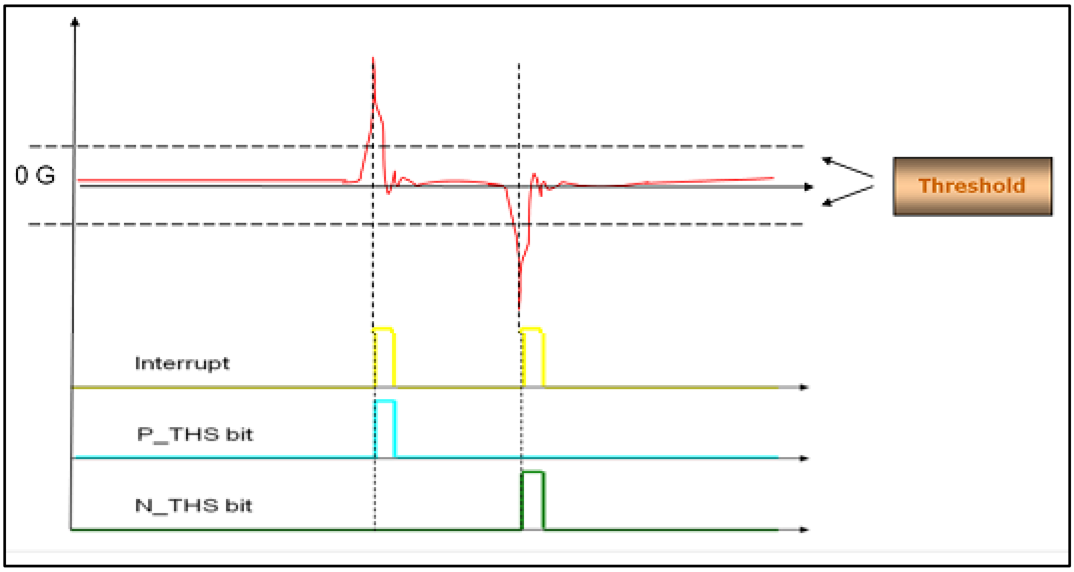
Table 16: INT_SRC description

PTH_X	Value on X-axis exceeds the threshold on the positive side. Default value: 0.
PTH_Y	Value on Y-axis exceeds the threshold on the positive side. Default value: 0.
PTH_Z	Value on Z-axis exceeds the threshold on the positive side. Default value: 0.
NTH_X	Value on X-axis exceeds the threshold on the negative side. Default value: 0.
NTH_Y	Value on Y-axis exceeds the threshold on the negative side. Default value: 0.
NTH_Z	Value on Z-axis exceeds the threshold on the negative side. Default value: 0.
MROI	Internal measurement range overflow on magnetic value. Default value: 0.
INT	This bit signals when interrupt event occurs.

Pin 7 (INT) is directly linked to the INT bit (INT_SRC register) which indicates that an interrupt event occurred.

The following graph shows one view of the interrupt mechanism.

Figure 5: Interrupt mechanism



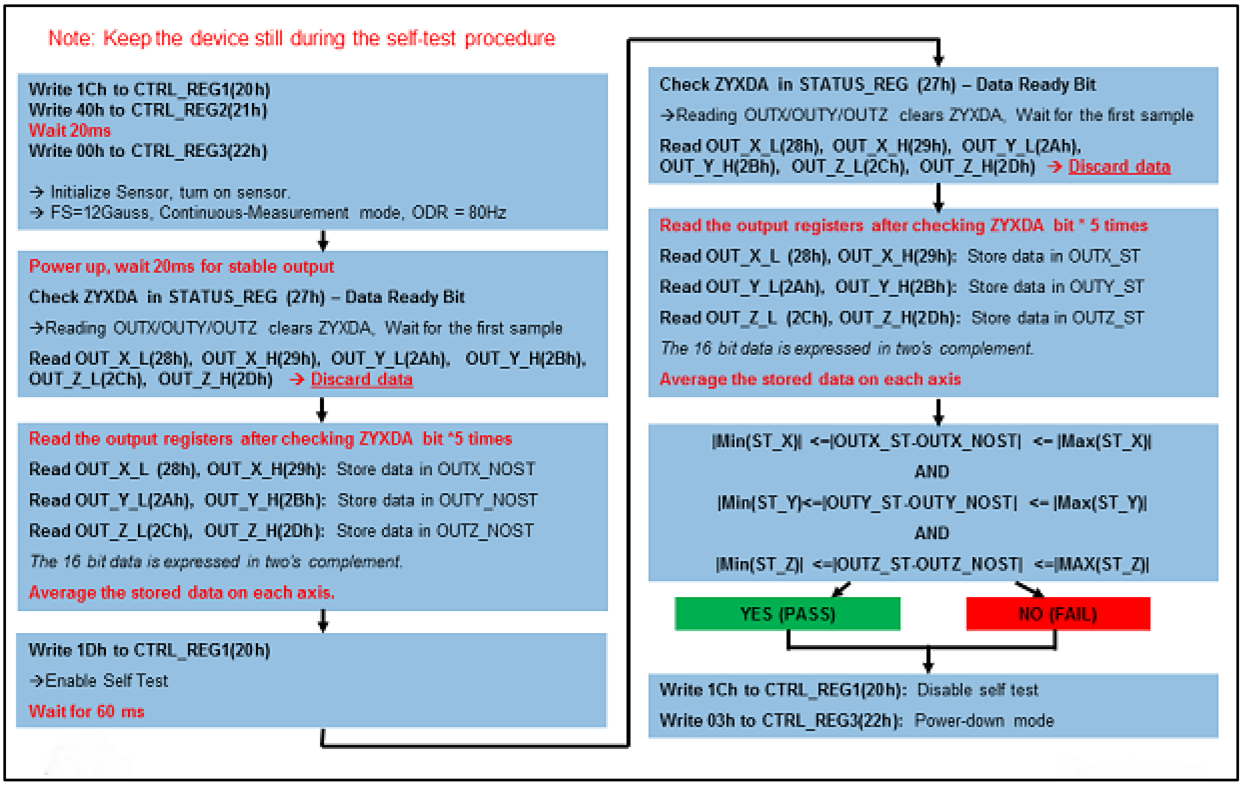
5 Self-test

In order to test the sensor the LIS3MDL device provides a self-test feature.

This test is enabled by setting bit 0 to ‘1’ in the CTRL_REG1 (20h) register.

The self-test procedure is indicated in the following figure.

Figure 6: Self-test sequence



The following table provides the self-test limits.

Table 17: Self-test limits (FS = 12 gauss)

Axis	ST min [gauss]	ST max [gauss]
X-axis	1.0	3.0
Y-axis	1.0	3.0
Z-axis	0.1	1.0

6 Temperature sensor and temperature compensation

The LIS3MDL is provided with an internal temperature sensor that is suitable for delta temperature measurement. Temperature data are generated with a frequency equal to the ODR and are stored inside the TEMP_OUT_L/TEMP_OUT_H registers: these values are 16-bit, 2’s complement.

The nominal sensitivity is 8 LSB/°C and 0 output means T=25 °C.

The temperature sensor can be enabled/disabled by setting the TEMP_EN bit (CTRL_REG1 register) equal to 1 or 0, respectively.

The sensitivity of the magnetic sensor changes when the temperature changes. A temperature compensation digital block is introduced to compensate for the effect of temperature.

7 Offset management

The LIS3MDL provides six registers dedicated to erase possible offset in the output data. Typical usage of these registers is to compensate for hard-iron effects:

OFFSET_X_REG_L_M (05h) ;

OFFSET_X_REG_H_M (06h) ;

OFFSET_Y_REG_L_M (07h) ;

OFFSET_Y_REG_H_M (08h) ;

OFFSET_Z_REG_L_M (09h) ;

OFFSET_Z_REG_H_M (0Ah) ;

Offset values have to be written in the registers as 16-bit, 2's complement (the sensitivity value is the same used for the magnetic data, please refer to *Table 2: "Full-scale selection"*).

The content of the OFFSET register is subtracted from the output of the device:

OUT = OUT(measured) - OFFSET

8 Revision history

Table 18: Document revision history

Date	Revision	Changes
17-Dec-2014	1	Initial release