AN4616
Application note

Migrating from STM32F401 and STM32F411 lines to STM32L4 Series and STM32L4+ Series microcontrollers

Introduction

For designers of the STM32 microcontroller applications, being able to easily replace one microcontroller type by another in the same product family is an important asset. Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note presents the required steps to migrate an existing design from the STM32F401 and STM32F411 lines microcontrollers to the STM32L4 Series and STM32L4+ Series devices. Three aspects must be considered for the migration: hardware, peripherals and firmware.

This document lists the full set of features available for the STM32F401 and STM32F411 lines, and the equivalent features on the STM32L4 Series and STM32L4+ Series (some products may have less features depending on their part number).

To fully benefit from this application note, the user must be familiar with the STM32 microcontrollers documentation available on *www.st.com* with a particular focus on:

- STM32F401 and STM32F411 lines reference manuals:
  - RM0368 (STM32F401xB/C and STM32F401xD/E)
  - RM0383 (STM32F411xC/E)
- STM32F401 and STM32F411 lines datasheets
- STM32L4 Series reference manuals:
  - RM0351 (STM32L4x5xx, STM32L4x6xx)
  - RM0394 (STM32L41xxx, STM32L42xxx, STM32L43xxx, STM32L44xxx, STM32L45xxx, STM32L46xxx)
  - RM0392 (STM32L471xx)
- STM32L4 Series datasheets
- STM32L4+ Series reference manual:
  - RM0432 (STM32L4Rxxx, STM32L4Sxxx)
- STM32L4+ Series datasheets.

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1 STM32L4 Series and STM32L4+ Series overview

The STM32L4 Series and STM32L4+ Series devices have a perfect fit in terms of ultra-low-power, performances, memory size and peripherals at a cost effective price.

STM32L4 Series and STM32L4+ Series enable a high frequency and a high performance operation, including the Arm®(a) Cortex®-M4 @ up to 120 MHz and an optimized Flash memory access through the adaptive real-time memory accelerator (ART Accelerator™).

The STM32L4 Series and STM32L4+ Series products increase the low-power efficiency in a Dynamic mode (µA/MHz) and still reach a very low level of static power consumption on the various available low-power modes.

The detailed list of available features and packages for each product is available in the respective datasheets.

The STM32L4 Series and STM32L4+ Series include a larger set of peripherals with advanced features compared to the STM32F401 and STM32F411 lines products, such as:

- Advanced encryption hardware accelerator (AES)
- Touch sensing controller (TSC)
- Controller area network (bxCAN)
- Single-wire protocol interface (SWPMI) (not available on STM32L4+ Series)
- Serial audio interface (SAI)
- Low-power UART (LPUART)
- Infrared interface (IRTIM)
- Low-power timer (LPTIM)
- Liquid crystal display controller (LCD) (not available on STM32L4+ Series)
- Digital filter for sigma delta modulators (DFSDM) (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L47xxx/48xxx and STM32L45xxx/46xxx)
- Operational amplifiers (OPAMP)
- Voltage reference buffer (VREFBUF)
- Digital to analog converter with low power Sample and Hold feature (DAC)
- Quad-SPI interface (QUADSPI) (not available on STM32L4+ Series)
- Flexible memory controller (FMC) (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx)
- Firewall (FW)
- Clock recovery system (CRS) for USB (for STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx).
- Hash processor (HASH) (for STM32L4R9xx/4S9xx and STM32L49xxx/4Axxx)
- Digital camera interface (DCMI) (for STM32L4+ Series and STM32L49xxx/4Axxx)
- Chrom-ART Accelerator™ controller (DMA2D) (for STM32L4+ Series and STM32L49xxx/4Axxx)

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- SRAM1 size is different on the various STM32L4 Series and STM32L4+ Series devices:
  - 192 Kbytes for STM32L4+ Series
  - 256 Kbytes for STM32L49xxx/4Axxx
  - 96 Kbytes for STM32L47xxx/48xxx
  - 128 Kbytes for STM32L45xxx/46xxx
  - 48 Kbytes for STM32L43xxx/44xxx
  - 32 Kbytes for STM32L41xxx/44xxx
- Additional SRAM2 with data preservation in Standby mode:
  - 64 Kbytes for STM32L4+ Series and STM32L49xxx/4Axxx
  - 32 Kbytes for STM32L47xxx/48xxx and STM32L45xxx/46xxx
  - 16 Kbytes for STM32L43xxx/44xxx
  - 8 Kbytes for STM32L41xxx/42xxx
- Additional SRAM3 for STM32L4+ Series:
  - 384 Kbytes
- Dual bank boot and 8-bit ECC on Flash memory (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx)
- Optimized power consumption and enriched set of low-power modes.

The STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices implement an USB FS device only. They also implement reduced Flash memory size (512 Kbytes for STM32L45xxx/46xxx, 256 Kbytes for STM32L43xxx/44xxx and 128 Kbytes for STM32L41xxx/42xxx).

This migration guide is only covering the migration from STM32F401 and STM32F411 lines to STM32L4 Series / STM32L4+ Series. As a consequence, new features present on STM32L4 Series and STM32L4+ Series but not already present on STM32F401 and STM32F411 lines are not covered in this document. Refer to the STM32L4Series reference manuals and datasheets for an exhaustive picture.

Table 1. STM32L4 Series / STM32L4+ Series memory availability

Part number	Flash size		RAM size			Feature level
	Size	Bank	SRAM1	SRAM2	SRAM3	
STM32L4S9xx	2 Mbytes	Dual	192 Kbytes	64 Kbytes	384 Kbytes	9+crypto
STM32L4R9xx						9
STM32L4S7xx						7+crypto
STM32L4R7xx						7
STM32L4S5xx						5+crypto
STM32L4R5xx						5
STM32L496xx	1 Mbyte		256 Kbytes	64 Kbytes	NA	6
STM32L4A6xx						6+crypto
STM32L471xx			96 Kbytes	32 Kbytes		1
STM32L475xx						5
STM32L476xx						6
STM32L486xx						6+crypto
STM32L451xx	512 Kbytes	Single	128 Kbytes	32 Kbytes		1
STM32L452xx						2
STM32L462xx						2+crypto
STM32L431xx	256 Kbytes		48 Kbytes	16 Kbytes		1
STM32L432xx						2
STM32L442xx						2+crypto
STM32L433xx						3
STM32L443xx						3+crypto
STM32L412xx	128 Kbytes		32 Kbytes	8 Kbytes		2
STM32L422xx						2+crypto

2 Hardware migration

The WLCSP packages in STM32F401 and STM32F411 lines are not equivalent to the WLCSP packages in the STM32L4 Series / STM32L4+ Series (different die sizes for both products).The list of available packages in the STM32L4 Series and STM32L4+ Series is given in *Table 2*.

Table 2. Packages available on STM32L4 Series and STM32L4+ Series

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
UFQFPN32	-	-	-	-	X	X	(5 x 5)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L432xx, STM32L442xx
LQFP32	-	-	-	-	-	X	(5 x 5)	STM32L412xx, STM32L422xx
LQFP48	-	-	-	-	X	X	(7 x 7)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx
UFQFPN48	-	-	-	X	X	X	(7 x 7)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx
WLCSP36	-	-	-	-	-	X	(2.85 x 3.07)	STM32L412xx, STM32L422xx
WLCSP49	-	-	-	-	X	-	(3.141 x 3.127)	STM32L431xx, STM32L433xx, STM32L443xx
WLCSP64	-	-	-	-	X	-	(3.141 x 3.127)	STM32L431xx, STM32L433xx, STM32L443xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
LQFP64	-	X	X	X	X	X	(10 x 10)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx
UFBGA64	-	-	-	X	X	X	(5 x 5)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx
WLCSP64	-	-	-	X	-	-	(3.357 x 3.657)	STM32L451xx, STM32L452xx, STM32L462xx
WLCSP72	-	-	X	-	-	-	(4.4084 x 3.7594)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx
WLCSP81	-	-	X	-	-	-	(4.4084 x 3.7594)	STM32L476xx
WLCSP100	-	X	-	-	-	-	(4.618 x 4.142)	STM32L496xx, STM32L4A6xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
LQFP100	X	X	X	X	X	-	(14 x 14)	STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx
UFBGA100	-	-	X	X	X	-	(7 x 7)	STM32L431xx, STM32L433xx, STM32L443xx
UFBGA132	X	X	X	-	-	-	(7 x 7)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4S5xx
UFBGA144	X	-	-	-	-	-	(10 x 10)	STM32L4R9xx, STM32L4S9xx
LQFP144	X	X	X	-	-	-	(20 x 20)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx

Table 2. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
WLCSP144	X	-	-	-	-	-	(5.24 x 5.24)	STM32L4R5xx, STM32L4R7xx, STM32L4R9xx, STM32L4S5xx, STM32L4S7xx, STM32L4S9xx
UFBGA169	X	X	-	-	-	-	(7 x 7)	STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx

1. X = supported.

Table 3 shows the pinout differences for packages available in both families.

Other packages in STM32F401 and STM32F411 lines are not available in STM32L4 Series / STM32L4+ Series.

STM32L4 Series / STM32L4+ Series, STM32F401 line and STM32F411 line devices share a high level of pin compatibility. Most peripherals share the same pins.

The transition from STM32F401 and STM32F411 lines to STM32L4 Series and STM32L4+ Series is simple since only a few pins are impacted.

Table 3. Pinout differences between STM32F401 line, STM32F411 line and STM32L4 Series/ STM32L4+ Series

STM32F401 and STM32F411 lines					STM32L4 Series / STM32L4+ Series				
QFP 64	QFP 100	QFPN 48	BGA 100[1]	Pinout	QFP 64	QFP 100	QFPN 48	BGA 100	Pinout
-	19	-	-	**VDD**	-	19	-	-	**VSSA**
30	48	22	L11	**VCAP1**	30	48	22	L11	**PB11**
-	73	-	C11	**VCAP2**	-	73	-	C11	**VDDUSB[2]**
48	-	36	-	**VDD**	48	-	36	-	**VDDUSB[2]**
-	-	-	K9	**PB11**	-	-	-	K9	**PD8**
-	-	-	H3	**PDR_ON**	-	-	-	H3	**VDD**
60	94	44	A4	**BOOT0**	60	94	44	A4	**PH3-BOOT0[3]**

1. Only for STM32F401xx devices.
2. VDDUSB pin can be connected externally to VDD.
3. Only for STM32L4R5xx/4S5xx, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx.

Note: STM32L4R9xx/4S9xx are not compatible with STM32L4 Series / STM32L4+ Series, for more details refer to application note Migration between STM32L476xx/486xx and STM32L4+ Series microcontrollers (AN5017).

Recommendations to migrate from the STM32F401 and STM32F411 lines board to the STM32L4 Series and STM32L4+ Series boards

The VDD pin (number 19 on the QFP100 package) is now used as VSSA pin in the STM32L4 Series / STM32L4+ Series devices.

A dedicated V_{DDUSB} supply is used in STM32L4 Series and STM32L4+ Series. This supply must be connected to the VDDUSB pin, which is the pin 48 on QFP64, pin 73 on QFP100 (for STM32L4R9xx/4S9xx refer to the application note *Migration between STM32L476xx/486xx and STM32L4+ Series microcontrollers* (AN5017)), pin 36 on QFPN48 and pin C11 on BGA100.

In the STM32F401 and STM32F411 lines devices, the pin was used for VCAP2 on QFP100 and BGA100 or for VDD on QFP64 and QFPN48, and is not needed for the STM32L4 Series / STM32L4+ Series devices.

The VCAP1 and the VCAP2 pins are used in the STM32F401 and STM32F411 lines for regulator stabilization through an external capacitor, and are not needed in the STM32L4 Series / STM32L4+ Series devices. Those pins are now mapped onto PB11 and VDDUSB (see *Table 3*).

The PB11 GPIO is present in the K9 ball of the BGA100 on the STM32F401 line (it is not available in other packages of the STM32F401 line). The K9 ball is mapped onto the PD8 pinout for the STM32L4x3xx devices in BGA100. The PD8 pinout is not available for the STM32F401 line in BGA100.

The PDR_ON pin, used to enable the power-supply supervisor on the STM32F401 line devices in BGA100 is not needed on the STM32L4 Series / STM32L4+ Series devices and is connected to the VDD pin, which is the pin H3 on BGA100.

The boot pins are different on both families. BOOT0 is multiplexed with the PH3 GPIO on the STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices. Refer to *Section 3: Boot mode selection* for more details. Those changes do not impact the design of the board.

Figure 1 to *Figure 4* show some examples of board designs migrating from STM32F401 and STM32F411 lines to STM32L4 Series and STM32L4+ Series.

Figure 1. LQFP100 compatible board design

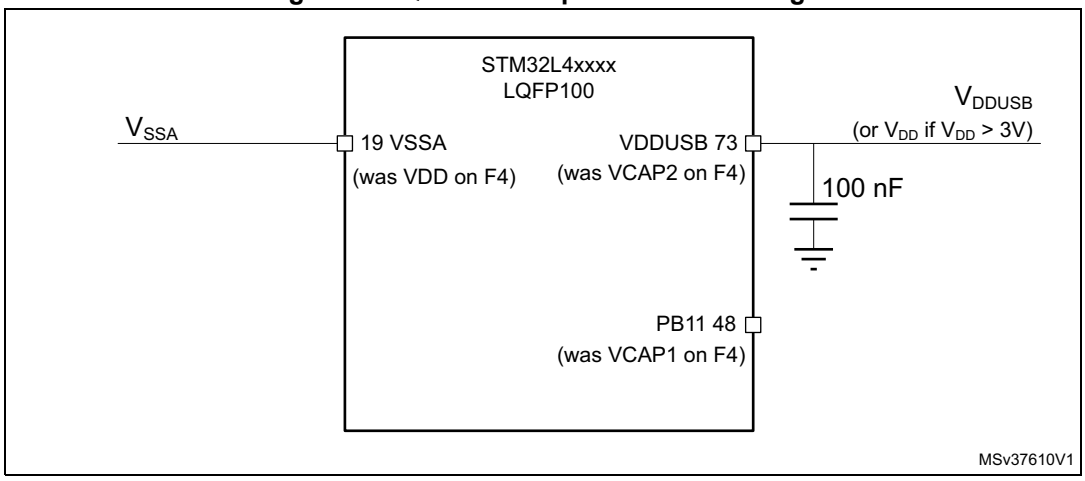


Figure 2. LQFP64 compatible board design

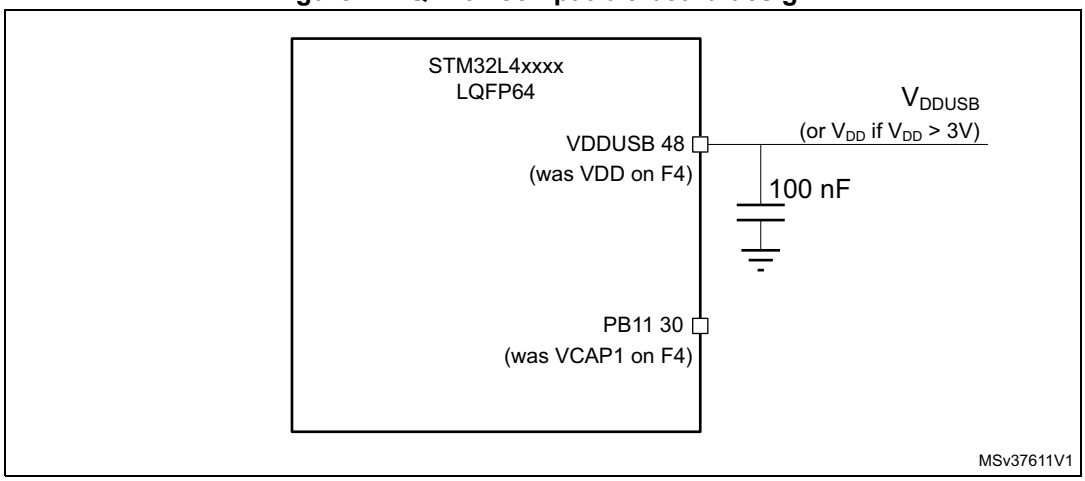


Figure 3. BGA100 compatible board design

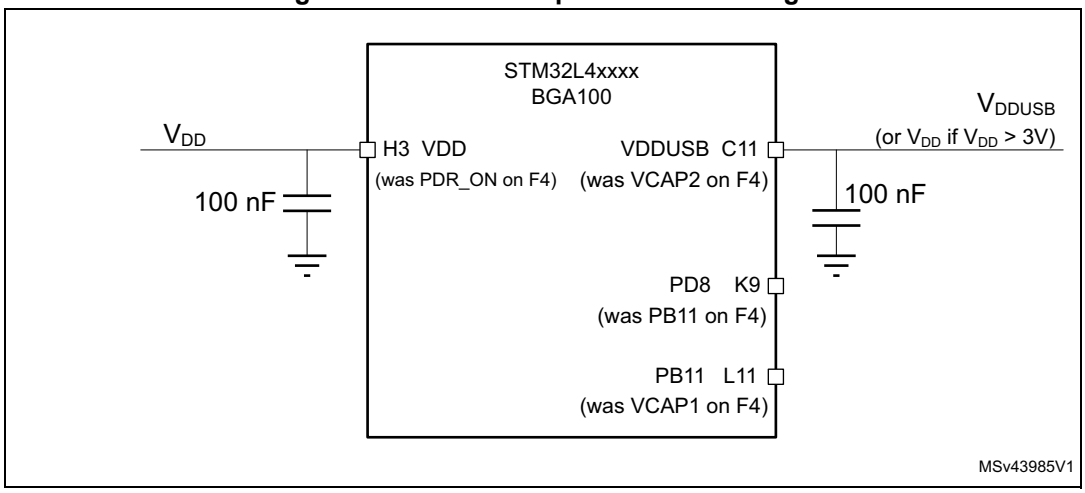
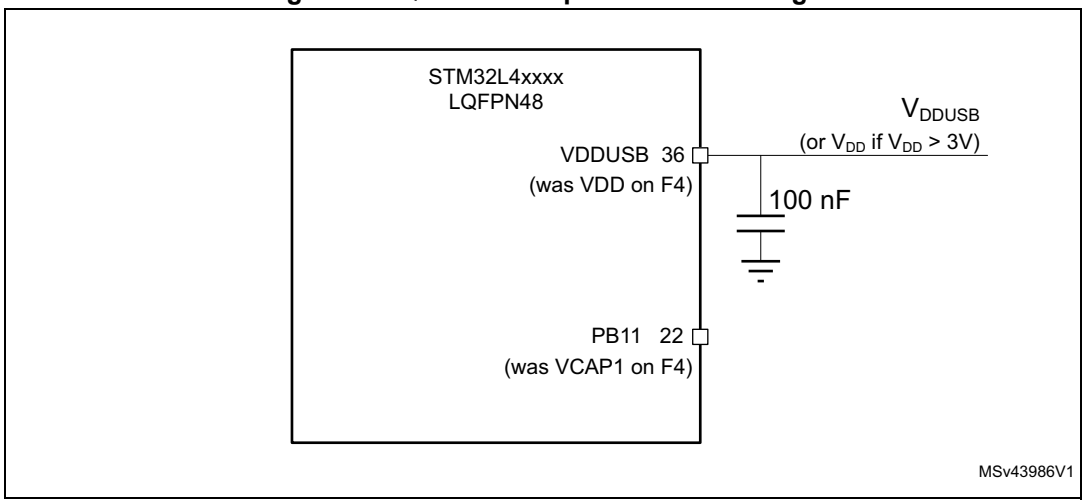


Figure 4. LQFPN48 compatible board design



SMPS packages

Some STM32L4 Series and STM32L4+ Series devices offer a package option allowing the connection of an external SMPS.

This is done through two VDD12 pins that are replacing two existing pins in the baseline package.

Compatibility is kept between derivatives of STM32L4 Series / STM32L4+ Series regarding those two VDD12 pins (the pins replaced are different across package types but are the same for all derivatives on similar packages).

Refer to the product datasheets for more details.

3 Boot mode selection

The STM32F401 and STM32F411 lines devices as and the STM32L4 Series / STM32L4+ Series devices can select boot modes between three options: boot from main Flash memory, boot from SRAM or boot from system memory. However, the way to select the boot mode differs between the products.

In the STM32F401 and STM32F411 lines, the boot mode is selected with two pins: BOOT0 and BOOT1.

In STM32L47xxx/48xxx devices, the boot mode is selected with one pin (BOOT0) and with the nBOOT1 option bit located in the user option bytes at the memory address 0x1FFF 7800.

In STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, the boot mode is selected with nBOOT1 option bit and with the BOOT0 pin or the nBOOT0 option bit depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register as shown in *Table 4*.

Table 4 and *Table 5* summarize the different configurations available for selecting the boot mode.

Table 4. Boot modes for STM32L47xxx/48xxx devices, STM32F401 line and STM32F411 line

Boot mode selection(1)		Boot mode	Aliasing
BOOT1(2)	BOOT0		
X	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM1	Embedded SRAM1 is selected as boot space

1. X = equivalent to 0 or 1.
2. The BOOT1 value is the opposite of the nBOOT1 option bit for STM32L47xxx/48xxx devices.

Table 5. Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and add STM32L41xxx/42xxx devices(1)

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main Flash empty(2)	Boot Memory Space Alias
X	X	0	1	0	Main Flash memory is selected as boot area
X	X	0	1	1	System memory is selected as boot area
X	1	X	0	X	Main Flash memory is selected as boot area
0	X	1	1	X	Embedded SRAM1 is selected as boot area

Table 5. Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and add STM32L41xxx/42xxx devices(1)

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main Flash empty(2)	Boot Memory Space Alias
0	0	X	0	X	Embedded SRAM1 is selected as boot area
1	X	1	1	X	System memory is selected as boot area
1	0	X	0	X	System memory is Selected as boot area

1. X = equivalent to 0 or 1.
2. For STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, a Flash empty check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed (0xFFFF FFFF) and if the boot selection was configured to boot from the main Flash memory.

Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during production. This bootloader is used to reprogram the Flash memory using one of the serial interfaces listed in *Table 6*.

Table 6. Bootloader interfaces on STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

Peripheral(1)	Pin	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
DFU	USB_DM (PA11) USB_DP (PA12)	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	X	-
	USART2_TX (PA2) USART2_RX (PA3)	-	X
USART3	USART3_TX (PB10) USART3_RX (PB11)	X	-
USART3	USART3_TX (PC10) USART3_RX (PC11)	X	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	X	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	X	X

Table 6. Bootloader interfaces on STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral[1]	Pin	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
I2C3	I2C3_SCL (PA8) I2C3_SDA (PB4)	X	-
	I2C3_SCL (PC0) I2C3_SDA (PC1)	-	X
I2C4	I2C4_SCL (PD12) I2C4_SDA (PD13)	-	X[2]
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	X	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	X	X
SPI3	SPI3_NSS (PA15) SPI3_SCK (PC10) SPI3_MISO (PC11) SPI3_MOSI (PC12)	X	-
CAN1	CAN1_RX (PB8) CAN1_TX (PB9)	-	X[3]
CAN2	CAN2_RX (PB5) CAN2_TX (PB6)	-	X[4]

1. X = supported.
2. Only for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L45xxx/46xxx devices.
3. Not available on STM32L41xxx/42xxx devices.
4. Only for STM32L49xxx/4Axxx devices.

Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details on the bootloader.

For smaller packages, it is important to check the pin and peripheral availability.

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 MCUs embed a set of peripherals that are classified in three groups:

- The first group is for the peripherals that are common to all products. Those peripherals are identical on all products, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second group is for the peripherals that present minor differences from one product to another (usually differences due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third group is for peripherals which have been considerably modified from one product to another (new architecture, or new features). For this group of peripherals, the migration requires a new development at application level.

Table 7 gives a general overview of this classification.

The software compatibility mentioned in *Table 7* refers only to the register description for low-level drivers.

The STMCube™ hardware abstraction layer (HAL) is compatible between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series.

Table 7. Peripheral compatibility analysis between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

<table>
<tr><th rowspan="2">Peripheral</th><th colspan="7">Number of instances in STM32</th><th colspan="3">Compatibility with STM32L4 Series / STM32L4+ Series</th></tr>
<tr><th>F401/ F411</th><th>L4Rxxx /4Sxxx</th><th>L49xxx /4Axxx</th><th>L47xxx /48xxx</th><th>L45xxx /46xxx</th><th>L43xxx /44xxx</th><th>L41xxx /42xxx</th><th>Software</th><th>Pinout</th><th>Comments</th></tr>
<tr><td>SPI</td><td>4/5</td><td colspan="5">3</td><td>2</td><td rowspan="2">Partial</td><td rowspan="2"></td><td rowspan="2">– I2S is no longer supported by SPI but replaced by dedicated Serial Audio Interface (SAI) in STM32L4 Series / STM32L4+ Series
– Some alternate function not mapped on same GPIO for SPI2/SPI3</td></tr>
<tr><td>I2S (full duplex)</td><td>2</td><td colspan="6">0</td></tr>
</table>

Table 7. Peripheral compatibility analysis between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	Number of instances in STM32							Compatibility with STM32L4 Series / STM32L4+ Series		
	F401/ F411	L4Rxxx /4Sxxx	L49xxx /4Axxx	L47xxx /48xxx	L45xxx /46xxx	L43xxx /44xxx	L41xxx /42xxx	Software	Pinout	Comments
WWDG	1	1						Full	NA	-
IWDG	1	1								
DBGMCU	1	1								
CRC	1	1						Partial		– Additional features in STM32L4 Series / STM32L4+ Series
EXTI	1	1						Partial	Full	– PH2 GPIO only available on STM32L49xxx/4Axxx devices for BGA169 package
USB OTG FS	1	1			0			Partial		– More endpoints in L4 – A few register controls are different – V_{DDUSB} merged with V_{DD} in STM32F401 and STM32F411 lines
USB FS	0	0			1			NA		USB device FS only on STM32L45xxx/46xxx and STM32L43xxx/44xxx
DMA	2	2						None	NA	Different features and DMA mapping requests differ (see *Section 4.3: Direct memory access controller (DMA)*)
TIM Basic General P. Advanced Low-power IRTIM	 0 7 1 0 0	 2 7 2 2 1			 2 4 1 2 1	 2 3 1 2 1	 1 3 1 2 1	Full	Partial	– Some pins not mapped on the same GPIO – Timer instance names may differ – Internal connections may differ
SDIO/ SDMMC	1	1					0	Full		Some pins are not mapped on the same GPIO

Table 7. Peripheral compatibility analysis between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	Number of instances in STM32							Compatibility with STM32L4 Series / STM32L4+ Series		
	F401/ F411	L4Rxxx /4Sxxx	L49xxx /4Axxx	L47xxx /48xxx	L45xxx /46xxx	L43xxx /44xxx	L41xxx /42xxx	Software	Pinout	Comments
PWR	1	1						Partial	NA	-
RCC	1	1						Partial		
USART **UART** **LPUART**	3 0 0	3 2 1			3 1 1	3 0 1		Partial	Full	– Additional features in STM32L4 Series / STM32L4+ Series – Fully compatible pinout for USART1/2/3
I2C	3	4		3	4	3		None	Partial	– Fully compatible pinout for I2C1/2 – I2C3 mapped on different GPIOs – Additional features in STM32L4 Series / STM32L4+ Series
ADC	1	1	3		1		2			– Additional features in STM32L4 Series / STM32L4+ Series – Some pins mapped on different GPIOs
RTC	1	1						Partial	Full	Additional features in STM32L4 Series and STM32L4+ Series
FLASH	1	1	2		1			None	NA	New peripheral
GPIO	Up to 82 IOs	Up to 140	Up to 136	Up to 114	Up to 83		Up to 52	Full		At reset, STM32F401 and STM32F411 lines devices are configured in Input-floating mode, the STM32L4 Series and STM32L4+ Series ones are in analog mode
SYSCFG	1	1						Partial	NA	-

Color key:

= No compatibility (new feature or new architecture)

= Partial compatibility (minor changes)

= Not applicable

4.2 Memory mapping

The peripheral address mapping has been changed in STM32L4 Series and STM32L4+ Series compared to STM32F401 and STM32F411 lines.

Table 8 provides the peripheral address mapping differences between the STM32F401 line, the STM32F411 line and the STM32L4 Series / STM32L4+ Series devices.

Table 8. Peripheral address mapping differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

Peripheral	STM32F401 and STM32F411 lines		STM32L4 Series / STM32L4+ Series	
	Bus	Base address	Bus	Base address(1)
USB OTG FS	AHB2	0x50000000	AHB2	0x5000 0000
DMA2	AHB1	0x40026400	AHB1	0x4002 0400
DMA1		0x40026000		0x4002 0000
Flash interface reg.		0x40023C00		0x4002 2000
RCC		0x40023800		0x4002 1000
CRC		0x40023000		0x4002 3000
GPIOH		0x40021C00	AHB2	0x4800 1C00
GPIOE		0x40021000		0x4800 1000
GPIOD		0x40020C00		0x4800 0C00
GPIOC		0x40020800		0x4800 0800
GPIOB		0x40020400		0x4800 0400
GPIOA		0x40020000		0x4800 0000
SPI5	APB2	0x4001 5000	NA	
TIM11		0x40014800		
TIM10		0x40014400		
TIM9		0x40014000		
EXTI		0x40013C00	APB2	0x4001 0400
SYSCFG		0x40013800		0x4001 0000
SPI4		0x40013400	NA	
SPI1		0x40013000	APB2	0x4001 3000
SDIO/SDMMC		0x40012C00		– 0x4001 2800 – 0x5006 2400 (AHB2) on STM32L4+ Series
ADC1 - ADC2 - ADC3		0x40012000	AHB2	0x5004 0000
USART6		0x40011400	NA	
USART1		0x40011000	APB2	0x4001 3800
TIM1		0x40010000		0x4001 2C00

Table 8. Peripheral address mapping differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	STM32F401 and STM32F411 lines		STM32L4 Series / STM32L4+ Series	
	Bus	Base address	Bus	Base address(1)
PWR	APB1	0x40007000	APB1	0x4000 7000
I2C3		0x40005C00		0x4000 5C00
I2C2		0x40005800		0x4000 5800
I2C1		0x40005400		0x4000 5400
USART2		0x40004400		0x4000 4400
I2S3ext		0x40004000	NA	
SPI3 / I2S3		0x40003C00	APB1	0x4000 3C00
SPI2 / I2S2		0x40003800		0x4000 3800
I2S2ext		0x40003400	NA	
IWDG		0x40003000	APB1	0x4000 3000
WWDG		0x40002C00		0x4000 2C00
RTC (inc. BKP registers)		0x40002800		0x4000 2800
TIM5		0x40000C00		0x4000 0C00
TIM4		0x40000800		0x4000 0800
TIM3		0x40000400		0x4000 0400
TIM2		0x40000000		0x4000 0000
QUADSPI	NA		AHB3(2) AHB4	0xA000 1000
FMC			AHB3	0xA000 0000
RNG			AHB2	0x5006 0800
HASH				0x5006 0400
AES				0x5006 0000
DCMI				0x5005 0000
GPIOI				0x4800 2000
GPIOG				0x4800 1800
GPIOF				0x4800 1400
DMA2D			AHB1	0x4002 B000
TSC				0x4002 4000
DFSDM			APB2	0x4001 6000
SAI2				0x4001 5800
SAI1				0x40015400
TIM17				0x4001 4800

Table 8. Peripheral address mapping differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	STM32F401 and STM32F411 lines		STM32L4 Series / STM32L4+ Series	
	Bus	Base address	Bus	Base address(1)
TIM16	NA		APB2	0x4001 4400
TIM15				0x4001 4000
TIM8				0x4001 3400
FIREWALL				0x4001 1C00
COMP				0x4001 0200
VREF				0x4001 0030
LPTIM2			APB1	0x4000 9400
SWPMI1				0x4000 8800
I2C4				0x4000 8400
LPUART1				0x4000 8000
LPTIM1				0x4000 7C00
OPAMP				0x4000 7800
DAC				0x4000 7400
CAN2				0x4000 6800
CAN1				0x4000 6400
UART5				0x4000 5000
UART4				0x4000 4C00
USART3				0x4000 4800
LCD				0x4000 2400
TIM7				0x4000 1400
TIM6				0x4000 1000
USB SRAM				0x4000 6C00
USB FS				0x4000 6800
CRS				0x4000 6000
OCTOSPI2			AHB3	0xA000 1400
OCTOSPI1				0xA000 1000
OCTOSPIM			AHB2	0x5006 1C00
GFXMMU			AHB1	0x4002 C000
DMAMUX1				0x4002 0800

Table 8. Peripheral address mapping differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	STM32F401 and STM32F411 lines		STM32L4 Series / STM32L4+ Series	
	Bus	Base address	Bus	Base address(1)
DSIHOST	NA		APB2	0x4001 6C00
LCD-TFT				0x4001 6800

Color key:

= Base address or bus change

= Not applicable (NA)

1. On STM32L4 Series / STM32L4+ Series devices on which the peripheral is not implemented, the memory address is reserved.
2. AHB3 for STM32L47xxx/48xxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, AHB4 for STM32L49xxx/4Axxx devices.

The system memory mapping has been updated between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series. For more details, refer to reference manuals or datasheets.

In STM32F401 and STM32F411 lines, only one SRAM1 is available, while in STM32L4 Series / STM32L4+ Series, three SRAMs are implemented: SRAM1, SRAM2 and SRAM3 (available only in STM32L4+ Series).

The SRAM2 (64 Kbytes for STM32L4+ Series and STM32L49xxx/4Axxx, 32 Kbytes for STM32L47xxx/48xxx and STM32L45xxx/46xxx, 16 Kbytes for STM32L43xxx/44xxx, 8 Kbytes for STM32L41xxx/42xxx) includes the additional features listed below:

- Maximum performance through ICode bus access without physical remap
- Parity check option (32-bit + 4-bit parity check)
- Write protection with 1-Kbyte granularity
- Read protection (RDP)
- Erase by system reset (option byte) or by software
- Content preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, Stop 2 modes
- Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).

4.3 Direct memory access controller (DMA)

STM32F401 and STM32F411 lines implement an enhanced DMA compared to STM32L4 Series and STM32L4+ Series.

For STM32L4+ Series, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer. In STM32L476xx/486xx, the DMA request line is connected directly to the peripherals.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routine function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique

DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

Table 9 shows the main differences.

Table 9. DMA differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

DMA	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Architecture	Dual AHB master: – 1 DMA controller for memory accesses – 1 DMA controller for peripheral accesses	Both DMA controllers can access memory and peripherals
Streams	– 8 streams per controller – 8 channels per stream	– 7 channels per controller (“streams” in STM32F401 and STM32f411 lines) – 8 requests per channel (“channels” in STM32F401 and STM32F411)
Data management	Four-word depth 32 first-in, first-out memory buffers (FIFOs) per stream, which can be used in FIFO mode or Direct mode.	NA
Color key: = Feature not available (NA) = Differences		

Table 10 presents the differences between the peripheral DMA requests in the STM32F401 line, the SMTM32F411 line and the STM32L4 Series / STM32L4+ Series.

Table 10. DMA request differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

Peripheral	DMA request	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series (1)
ADC	ADC1	DMA2_Stream0 DMA2_Stream4	DMA1_Channel1 DMA2_Channel3
	ADC2	NA	DMA1_Channel2 DMA2_Channel4
	ADC3		DMA1_Channel3 DMA2_Channel5
DAC	DAC1_CH1		DMA1_Channel3 DMA2_Channel4
	DAC1_CH2		DMA1_Channel4 DMA2_Channel5
DFSDM	DFSDM0		DMA1_Channel4
	DFSDM1		DMA1_Channel5
	DFSDM2		DMA1_Channel6
	DFSDM3		DMA1_Channel7
SPI1	SPI1_Rx	DMA2_Stream0 DMA2_Stream2	DMA1_Channel2 DMA2_Channel3
	SPI1_Tx	DMA2_Stream3 DMA2_Stream5	DMA1_Channel3 DMA2_Channel4
SPI2	SPI2_Rx SPI2_Tx	DMA1_Stream3 DMA1_Stream4	DMA1_Channel4 DMA1_Channel5
SPI3	SPI3_Rx	DMA1_Stream0 DMA1_Stream2	DMA2_Channel1
	SPI3_Tx	DMA1_Stream5 DMA1_Stream7	DMA2_Channel2
SPI4	SPI4_Rx	DMA2_Stream0 DMA2_Stream3	NA
	SPI4_Tx	DMA2_Stream1 DMA2_Stream4	
SPI5	SPI5_Rx SPI5_Tx	DMA2_Stream5(2) DMA2_Stream6(2)	
QUADSPI	QUADSPI	NA	DMA1_Channel5 DMA2_Channel7

Table 10. DMA request differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series (1)
USART1	**USART1_Rx**	DMA2_Stream2 DMA2_Steam5	DMA1_Channel5 DMA2_Channel7
	USART1_Tx	DMA2_ Stream7	DMA1_Channel4 DMA2_Channel6
USART2	**USART2_Rx** **USART2_Tx**	DMA1_Stream5 DMA1_Stream6	DMA1_Channel6 DMA1_Channel7
USART3	**USART3_Rx**	NA	DMA1_Channel3
	USART3_Tx		DMA1_Channel2
UART4	**UART4_Rx** **UART4_Tx**		DMA2_Channel5 DMA2_Channel3
UART5	**UART5_Rx** **UART5_Tx**		DMA2_Channel2 DMA2_Channel1
USART6	**USART6_Rx**	DMA2_Stream1 DMA2_Stream2	NA
	USART6_Tx	DMA2_Stream6 DMA2_Stream7	
LPUART	**LPUART_RX** **LPUART_TX**	NA	DMA2_Channel7 DMA2_Channel6
I2C1	**I2C1_Rx**	DMA1_Stream0 DMA1_Stream5	DMA1_Channel7 DMA2_Channel6
	I2C1_Tx	DMA1_Stream6 DMA1_Stream7	DMA1_Channel6 DMA2_Channel7
I2C2	**I2C2_Rx**	DMA1_Stream2 DMA1_Stream3	DMA1_Channel5
	I2C2_Tx	DMA1_Stream7	DMA1_Channel4
I2C3	**I2C3_Rx**	DMA1_Stream1 DMA1_Stream2	DMA1_Channel3
	I2C3_Tx	DMA1_Stream4 DMA1_Stream5	DMA1_Channel2
I2C4	**I2C4_Rx** **I2C4_Tx**	NA	DMA2_Channel1 DMA2_Channel2
SDIO **SDMMC**	**SDIO**	DMA2_Stream3 DMA2_Stream6	NA
	SDMMC	NA	DMA2_Channel4 DMA2_Channel5

Table 10. DMA request differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series (1)
TIM1	**TIM1_UP**	DMA2_Stream5	DMA1_Channel6
	TIM1_TRIG	DMA2_Stream0 DMA2_Stream4	DMA1_Channel4
	TIM1_COM	DMA2_Stream4	DMA1_Channel4
	TIM1_CH1	DMA2_Stream1 DMA2_Stream3	DMA1_Channel2
	TIM1_CH2	DMA2_Stream2	DMA1_Channel3
	TIM1_CH3	DMA2_Stream6	DMA1_Channel7
	TIM1_CH4	DMA2_Stream4	DMA1_Channel4
TIM2	**TIM2_UP**	DMA1_Stream1 DMA1_Stream7	DMA1_Channel2
	TIM2_CH1	DMA1_Stream5	DMA1_Channel5
	TIM2_CH2	DMA1_Stream6	DMA1_Channel7
	TIM2_CH3	DMA1_Stream1	DMA1_Channel1
	TIM2_CH4	DMA1_Stream6 DMA1_Stream7	DMA1_Channel7
TIM3	**TIM3_UP** **TIM3_TRIG** **TIM3_CH1** **TIM3_CH2** **TIM3_CH3** **TIM3_CH4**	DMA1_Stream2 DMA1_Stream4 DMA1_Stream4 DMA1_Stream5 DMA1_Stream7 DMA1_Stream2	DMA1_Channel3 DMA1_Channel6 DMA1_Channel6 NA DMA1_Channel2 DMA1_Channel3
TIM4	**TIM4_UP** **TIM4_CH1** **TIM4_CH2** **TIM4_CH3**	DMA1_Stream6 DMA1_Stream0 DMA1_Stream3 DMA1_Stream7	DMA1_Channel7 DMA1_Channel1 DMA1_Channel4 DMA1_Channel5
TIM5	**TIM5_UP**	DMA1_Stream0 DMA1_Stream6	DMA2_Channel2
	TIM5_CH1	DMA1_Stream2	DMA2_Channel5
	TIM5_CH2	DMA1_Stream4	DMA2_Channel4
	TIM5_CH3	DMA1_Stream0	DMA2_Channel2
	TIM5_CH4	DMA1_Stream1 DMA1_Stream3	DMA2_Channel1
	TIM5_TRIG	DMA1_Stream1 DMA1_Stream3	DMA2_Channel1
	TIM5_COM	NA	DMA2_Channel1

Table 10. DMA request differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series (1)
TIM6	**TIM6_UP**	NA	DMA1_Channel3 DMA2_Channel4
TIM7	**TIM7_UP**		DMA1_Channel4 DMA2_Channel5
TIM8	**TIM8_CH1** **TIM8_CH2** **TIM8_CH3** **TIM8_CH4** **TIM8_UP** **TIM8_TRIG** **TIM8_COM**		DMA2_Channel6 DMA2_Channel7 DMA2_Channel1 DMA2_Channel2 DMA2_Channel1 DMA2_Channel2 DMA2_Channel2
TIM15	**TIM15_CH1** **TIM15_UP** **TIM15_TRIG** **TIM15_COM**		DMA1_Channel5 DMA1_Channel5 DMA1_Channel5 DMA1_Channel5
TIM16	**TIM16_CH1** **TIM16_UP** **TIM16_CH1** **TIM16_UP**		DMA1_Channel3 DMA1_Channel3 DMA1_Channel6 DMA1_Channel6
TIM17	**TIM17_CH1** **TIM17_UP** **TIM17_CH1** **TIM17_UP**		DMA1_Channel1 DMA1_Channel1 DMA1_Channel7 DMA1_Channel7
SAI	**SAI1_A**		DMA2_Channel1 DMA2_Channel6
	SAI1_B		DMA2_Channel2 DMA2_Channel7
	SAI2_A		DMA1_Channel6 DMA2_Channel3
	SAI2_B		DMA1_Channel7 DMA2_Channel4
SWPMI	**SWPMI_RX**		DMA2_Channel1
	SWPMI_TX		DMA2_Channel2
AES	**CRYP_OUT**		NA
	CRYP_IN		
	AES_OUT		DMA2_Channel3 DMA2_Channel2
	AES_IN		DMA2_Channel5 DMA2_Channel1

Table 10. DMA request differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series (1)
I2S	**I2S2_EXT_Rx** **I2S2_EXT_Tx** **I2S3_EXT_Rx** **I2S3_EXT_Tx**	DMA1_Stream3 DMA1_Stream4 DMA1_Stream0 DMA1_Stream2 DMA1_Stream5	NA
DCMI	**DCMI**	NA	DMA2_Channel7 DMA2_Channel5
HASH	**HASH_IN**		DMA2_Channel7
Color key: = Feature not available (NA)			

1. On STM32L4 Series / STM32L4+ Series devices on which the peripheral is not implemented, the DMA request is reserved.
2. Not applicable for STM32F401 line.

4.4 Interrupts

Table 11 presents the interrupt vectors in the STM32F401 and STM32F411 lines versus STM32L4 Series / STM32L4+ Series.

Table 11. Interrupt vector differences between STM32F401 line, STM32F411 line and the STM32L4 Series / STM32L4+ Series

Position	STM32F401 and SMTM32F411 lines	STM32L4 Series / STM32L4+ Series(1)
0	WWDG	WWDG
1	PVD	PVD / PVM
2	TAMP_ STAMP	TAMPER / CSS
3	RTC_WKUP	RTC_WKUP
4	FLASH	FLASH
5	RCC	RCC
6	EXTI0	EXTI0
7	EXTI1	EXTI1
8	EXTI2	EXTI2
9	EXTI3	EXTI3
10	EXTI4	EXTI4
11	DMA1_Stream0	DMA1_Channel1
12	DMA1_Stream1	DMA1_Channel2
13	DMA1_Stream2	DMA1_Channel3
14	DMA1_Stream3	DMA1_Channel4

Table 11. Interrupt vector differences between STM32F401 line, STM32F411 line and the STM32L4 Series / STM32L4+ Series (continued)

Position	STM32F401 and SMTM32F411 lines	STM32L4 Series / STM32L4+ Series(1)
15	DMA1_Stream4	DMA1_Channel5
16	DMA1_Stream5	DMA1_Channel6
17	DMA1_Stream6	DMA1_Channel7
18	ADC	ADC1_2
19	NA	CAN1_TX
20		CAN1_RX0
21		CAN1_RX1
22		CAN1_SCE
23	EXTI9_5	EXTI9_5
24	TIM1_BRK / TIM9	TIM1_BRK / TIM15
25	TIM1_UP / TIM10	TIM1_UP / TIM16
26	TIM1_TRG_COM / TIM11	TIM1_TRG_COM / TIM17
27	TIM1_CC	TIM1_CC
28	TIM2	TIM2
29	TIM3	TIM3
30	TIM4	TIM4
31	I2C1_EV	I2C1_EV
32	I2C1_ER	I2C1_ER
33	I2C2_EV	I2C2_EV
34	I2C2_ER	I2C2_ER
35	SPI1	SPI1
36	SPI2	SPI2
37	USART1	USART1
38	USART2	USART2
39	NA	USART3
40	EXTI15_10	EXTI15_10
41	RTC_Alarm	RTC_Alarm
42	USB_FS_WKUP	DFSDM3
43	NA	TIM8_BRK
44		TIM8_UP
45		TIM8_TRG_COM
46		TIM8_CC
47	DMA1_Stream7	ADC3

Table 11. Interrupt vector differences between STM32F401 line, STM32F411 line and the STM32L4 Series / STM32L4+ Series (continued)

Position	STM32F401 and SMTM32F411 lines	STM32L4 Series / STM32L4+ Series(1)
48	NA	FMC
49	SDIO	SDMMC
50	TIM5	TIM5
51	SPI3	SPI3
52	NA	UART4
53		UART5
54		TIM6_DACUNDER
55		TIM7
56	DMA2_Stream0	DMA2_Channel1
57	DMA2_Stream1	DMA2_Channel2
58	DMA2_Stream2	DMA2_Channel3
59	DMA2_Stream3	DMA2_Channel4
60	DMA2_Stream4	DMA2_Channel5
61	NA	DFSDM0
62		DFSDM1
63		DFSDM2
64	NA	COMP
65		LPTIM1
66		LPTIM2
67	OTG_FS	– OTG_FS (STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) – USB_FS (STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
68	DMA2_Stream5	DMA2_CH6
69	DMA2_Stream6	DMA2_CH7
70	DMA2_Stream7	LPUART1
71	USART6	– QUADSPI – OCTOSPI 1 (for STM32L4+ Series)
72	I2C3_EV	I2C3_EV
73	I2C3_ER	I2C3_ER

Table 11. Interrupt vector differences between STM32F401 line, STM32F411 line and the STM32L4 Series / STM32L4+ Series (continued)

Position	STM32F401 and SMTM32F411 lines	STM32L4 Series / STM32L4+ Series(1)
74	NA	SAI1
75		SAI2
76		– SWPMI1 – OCTOSPI2 (for STM32L4+ Series)
77		TSC
78		– LCD – DSIHOST (for STM32L4R9xx/4S9xx)
79		AES
80		RNG
81	FPU	FPU
82	NA	HASH and CRS
83		I2C4_EV
84		I2C4_ER
85		DCMI
86		CAN2_TX
87		CAN2_RX0
88		CAN2_RX1
89		CAN2_SCE
90		DMA2D
91	NA	LCD-TFT
92		LCD-TFT_ER
93		GFXMMU
94		DMAMUX1_OVR

Color key:

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Differences

1. On STM32L4 Series and STM32L4+ Series devices on which the peripheral is not implemented, the interrupt is not applicable.

4.5 Reset and clock control (RCC)

The main RCC differences between STM32L4 Series / STM32L4+ Series, STM32F401 line and STM32F411 line are presented in *Table 12*.

Table 12. RCC differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

RCC	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
MSI	NA	– MSI is a low power oscillator with programmable frequency up to 48 MHz
HSI16	16 MHz RC factory and user trimmed	
LSI	32 kHz	– 32 kHz RC – Lower consumption, higher accuracy
HSE	4 to 26 MHz	4 to 48 MHz
LSE	– 32.768 kHz – Configurable drive/consumption (not in STM32F401 line)	
HSI48	NA	– 48 MHz RC (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx) – Can drive USB Full Speed, SDMMC and RNG
PLL	– Main PLL for system – 1 PLL (PLLI2S) for I2S – The PLL sources are HSI, HSE.	– Main PLL for system: x2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG FS clock (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) x1 PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (for STM32L45xxx/46xxx and STM32L43xxx/44xxx) – Each PLL can provide up to 3 independent outputs – The PLL multiplication/division factors are different from the STM32F401and STM32F411 lines ones – PLL clock sources: MSI, HSI16, HSE

Table 12. RCC differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

RCC	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
PLL	– Main PLL for system – 1 PLL (PLLI2S) for I2S – The PLL sources are HSI, HSE.	– Main PLL for system: x2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG FS clock (for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) x1 PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (for STM32L45xxx/46xxx and STM32L43xxx/44xxx) – Each PLL can provide up to 3 independent outputs – The PLL multiplication/division factors are different from the STM32F401and STM32F411 lines ones – PLL clock sources: MSI, HSI16, HSE
System clock source	HSI, HSE or PLL	MSI, HSI16, HSE or PLL
System clock frequency	– Up to 84 MHz (STM32F401 line), 100 MHz (STM32F411 line) – 16 MHz after reset using HSI	– Up to 80 MHz or 120 MHz for STM32L4+ Series – 4 MHz after reset using MSI
AHB frequency	Up to 84 MHz (STM32F401 line), 100 MHz (STM32F411 line)	Up to 80 MHz or 120 MHz for STM32L4+ Series
APB1 frequency	Up to 42 MHz (STM32F401 line), 50 MHz (STM32F411 line)	Up to 80 MHz or 120 MHz for STM32L4+ Series
APB2 frequency	Up to 84 MHz (STM32F401 line), 100 MHz (STM32F411 line)	Up to 80 MHz or 120 MHz for STM32L4+ Series
RTC clock source	LSI, LSE or HSE (1 MHz) using 1/2, 1/3, ¼ clock pre-divider	LSI, LSE or HSE/32
MCO clock source	– MCO1 pin (PA8): HSI, LSE, HSE, PLLCLK – MCO2 pin (PC9): HSE, PLLCLK, SYSCLK, PLLI2S – With configurable prescaler, 1, 2, 3, 4, 5 for each output.	– MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI or HSI48 (for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx) – With configurable prescaler, 1, 2, 4, 8 or 16 for each output.
CSS	CSS (clock security system) on HSE and CSS on LSE	

Table 12. RCC differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

RCC	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Internal oscillator measurement / calibration	– LSE connected to TIM5 CH4 IC: can measure HSI with respect to LSE clock high precision – LSI connected to TIM5 CH4 IC: can measure LSI with respect to HSI or HSE clock precision – HSE connected to TIM11 CH1 IC: can measure HSE with respect to LSE/HSI clock	Mainly replacing TIM5/TIM11 in STM32F401/411 lines by TIM15/16/17 in STM32L4 Series / STM32L4+ Series – LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision – LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision – HSE/32 connected to TIM17 CH1 IC: can measure HSE with respect to LSE/HSI16 clock – MSI connected to TIM17 CH1 IC: can measure MSI with respect to HSI16/HSE clock – On STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx, HSE/32 and MSI are connected to TIM16 CH1 IC
Interrupt	– CSS (linked to NMI IRQ) – LSIRDY, LSERDY, HSIRDY, HSERDY, PLLRDY, PLLI2SRDY (linked to RCC global IRQ)	– CSS (linked to NMI IRQ) – LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, PLLSAI1RDY, PLLSAI2RDY (only on STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx) (linked to RCC global IRQ)
Color key: = New feature or new architecture = Same feature, but specification change or enhancement = Feature not available (NA) = Differences		

In addition to the differences described in *Table 12*, the following additional adaptation steps may be needed for the migration:

- Performance versus VCORE ranges
- Peripheral access configuration
- Peripheral clock configuration.

4.5.1 Performance versus V_{CORE} ranges

In STM32L4 Series / STM32L4+ Series, the maximum CPU clock frequency and the number of Flash memory wait state depend on the selected V_{CORE} voltage range. See *Table 13* for details.

Table 13. STM32L4 Series and STM32L4+ Series performance versus V_{CORE} ranges(1)

CPU performance	Power performance	VCORE Range	Typical value (V)	Max frequency (MHz)					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
STM32L4 Series									
High	Medium	1	1.2	-	80	64	48	32	16
Medium	High	2	1.0	-	26	26	18	12	6
STM32L4+ Series									
High	Medium	1 boost mode	1.28	120	100	80	60	40	20
		1 normal mode	1.2	-	-	80	60	40	20
Medium	High	2	1.0	-	-	-	26	16	8

1. WS = wait state.

In the STM32F401 and STM32F411 lines, the maximum CPU clock frequency and the number of Flash memory wait state depend on the selected V_{DD} voltage range. See *Table 14* and *Table 15* shows an example on the number of WS according to HCLK frequency.

Table 14. Number of wait states according to CPU clock (HCLK) frequency (STM32F401xB/C and STM32F401xD/E)

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 30	0 < HCLK ≤ 24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤ 60	24 < HCLK ≤ 48	18 < HCLK ≤ 36	16 < HCLK ≤ 32
2 WS (3 CPU cycles)	60 < HCLK ≤ 84	48 < HCLK ≤ 72	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	-	72 < HCLK ≤ 84	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	-	72 < HCLK ≤ 84	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	-	80 < HCLK ≤ 84

Table 15. Number of wait states according to CPU clock (HCLK) frequency (STM32F411xC/E)

Wait states (WS) (LATENCY)	HCLK (MHz)			
	Voltage range 2.7 V - 3.6 V	Voltage range 2.4 V - 2.7 V	Voltage range 2.1 V - 2.4 V	Voltage range 1.71 V - 2.1 V
0 WS (1 CPU cycle)	0 < HCLK ≤ 30	0 < HCLK ≤ 24	0 < HCLK ≤ 18	0 < HCLK ≤ 16
1 WS (2 CPU cycles)	30 < HCLK ≤ 64	24 < HCLK ≤ 48	18 < HCLK ≤ 36	16 <HCLK ≤ 32
2 WS (3 CPU cycles)	64 < HCLK ≤ 90	48 < HCLK ≤ 72	36 < HCLK ≤ 54	32 < HCLK ≤ 48
3 WS (4 CPU cycles)	90 < HCLK ≤ 100	72 < HCLK ≤ 96	54 < HCLK ≤ 72	48 < HCLK ≤ 64
4 WS (5 CPU cycles)	-	96 < HCLK ≤ 100	72 < HCLK ≤ 90	64 < HCLK ≤ 80
5 WS (6 CPU cycles)	-	-	90 < HCLK ≤ 100	80 < HCLK ≤ 96
6 WS (7 CPU cycles)	-	-	-	96 < HCLK ≤ 100

On top of the V_{DD} voltage range specified in the tables presented above, the maximum frequency is limited by the power-scale value indicated by software in the VOS[1:0] bits of the PWR_CR register.

Those bits modify the internal digital logic voltage from the power regulator.

This voltage scaling enables an optimization of the power consumption when the device is clocked below the maximum CPU frequency.

4.5.2 Peripheral access configuration

Since the address mapping of some peripherals has changed in STM32L4 Series and STM32L4+ Series compared to STM32F401 and STM32F411 lines, different registers must be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from Reset mode].

Table 16. RCC registers used for peripheral access configuration for STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

Bus	Register STM32F401 and STM32F411 lines	Register STM32L4 Series / STM32L4+ Series	Comments
AHB	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2)	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2) RCC_AHB3RSTR (AHB3)(1)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2)	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2) RCC_AHB3ENR (AHB3)(1)	Used to [enable/disable] the AHB peripheral clock
	RCC_AHB1LPENR RCC_AHB2LPENR	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3)	Used to [enable/disable] the AHB peripheral clock in Sleep mode
APB1	RCC_APB1RSTR	RCC_APB1RSTR1 RCC_APB1RSTR2(1)	Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR	RCC_APB1ENR1 RCC_APB1ENR2(1)	Used to [enable/disable] the APB1 peripheral clock
	RCC_APB1LPENR	RCC_APB1SMENR1 RCC_APB1SMENR2(1)	Used to [enable/disable] the APB1 peripheral clock in Sleep mode
APB2	RCC_APB2RSTR		Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR		Used to [enable/disable] the APB2 peripheral clock
	RCC_APB2LPENR	RCC_APB2SMENR	Used to [enable/disable] the APB2 peripheral clock in Sleep mode

1. Register configuring peripherals are not present in the STM32F401 and STM32F411 lines, so it is not needed from a migration-only stand point.

The configuration to access a given peripheral involves identifying the bus to which the peripheral is connected (see *Table 8*) and selecting the right register according the needed action (see *Table 16*).

For example, the USART1 is connected to the APB2 bus. In order to enable the USART1 clock, the RCC_APB2ENR register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_ENABLE();
```

In order to disable the USART1 clock during Sleep mode (to reduce power consumption) the RCC_APB2SMENR register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_SLEEP_ENABLE();
```

4.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source, independent from the system clock, which is used to generate the clock required for their operation.

- **USB**:
  - In the STM32F401 and STM32F411 lines, the USB 48 MHz clock is derived from the PLL48CLK main PLL “Q” output.
  - In STM32L4 Series and STM32L4+ Series, the USB 48 MHz clock is derived from one of the following sources:
    Main PLL VCO (PLLUSB1CLK), PLLSAI1 VCO (PLLUSB2CLK)
    MSI clock (when the MSI clock is auto-trimmed with the LSE, it can be used by the USB OTG FS device)
    HSI48 internal oscillator (only on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx).
- **SDIO/SDMMC:**
  - In STM32F401 and STM32F411 lines, the SDIO clock (SDIOCLK) is derived from the PLL48CLK main PLL “Q” output and must be less than 48 MHz.
  - In STM32L4 Series and STM32L4+ Series, the SDMMC clock is derived from one of the following sources:
    Main PLL VCO (PLLUSB1CLK)
    PLLSAI1 VCO (PLLUSB2CLK)
    MSI clock
    HSI48 internal oscillator (only on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx).
- **RTC**:
  - In STM32F401 and STM32F411 lines, the RTC clock is derived from one of the three following sources: LSE, LSI or HSE divided by prescaler (1 to 31) and must be equal to 1 MHz.
  - In STM32L4 Series and STM32L4+ Series, the RTC and the LCD glass clocks are derived from one of the three following sources: LSE clock, LSI clock, or HSE clock divided by 32. The PCLK frequency must always be greater than or equal to the RTC clock frequency.
- **ADC**:
  - In STM32F401 and STM32F411 lines, the ADC clock is the PCLK2 clock divided by a programmable factor (2, 4, 6, 8).
  - In STM32L4 Series and STM32L4+ Series, the input clock of the two ADCs (master and slave) can be selected between two different clock sources:
    Derived (selected by software) from system clock (SYSCLK), PLLSAI1 VCO[(a)] (PLLADC1CLK) or PLLSAI2 VCO[(b)] (PLLADC2CLK) (only on STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices). In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).
    Derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). In this mode, a programmable divider factor can be selected (1, 2

a. Not available on STM32L41xxx/42xxx, only SYSCLK could be used on those devices.

b. PLLSAI2VCO (PLLADC2CLK) is a clock source only on STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices.

or 4 according to bits CKMODE[1:0]). Refer to the STM32L4 Series and STM32L4+ Series reference manuals for more details.

- **DAC**:

  In STM32L4 Series and STM32L4+ Series, in addition to the PCLK1 clock, the LSI clock is used for the sample and hold operation.

- **U(S)ARTs:**
  - In STM32F401 and STM32F411 lines, the U(S)ART clock is APB1 or APB2 clock, depending on which APB bus is mapped to the U(S)ART)
  - In STM32L4 Series and STM32L4+ Series, the U(S)ART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, APB1 or APB2 clock (depending on which APB bus is mapped to the U(S)ART).

  Using a source clock independent from the system clock (like HSI16) allows to change the system clock on the fly without need to reconfigure the U(S)ART peripheral baud rate prescalers.

- **I2Cs**:
  - In STM32F401 and STM32F411 lines, the I2C clock is APB1 clock (PCLK1).
  - In STM32L4 Series and STM32L4+ Series, the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16 or APB1 (PCLK1).

  Using a source clock independent from the system clock (like HSI16) allows to change the system clock on the fly without need to reconfigure I2C peripheral timing register.

- **I2S/SAI:**
  - In STM32F401 and STM32F411 lines, the I2S clocks are derived from one of the two following sources: an external clock I2S_CKIN or PLLI2SCLK.
  - In STM32L4 Series and STM32L4+ Series, the I2S peripherals are not available and they are replaced by SAIs.
  - For STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices, the SAI clocks are derived from one of the four following sources:
    An external clock mapped on SAI1_EXTCLK or SAI2_EXTCLK
    PLLSAI1 VCO (PLLSAI1CLK)
    PLLSAI2 VCO (PLLSAI2CLK)
    A main PLL VCO (PLLSAI3CLK)
  - For STM32L45xxx/46xxx and STM32L43xxx/44xxx devices, the SAI clocks are derived from one of the four following sources:
    An external clock mapped on SAI1_EXTCLK for SAI1
    PLLSAI1 (P) divider output (PLLSAI1CLK)
    A main PLL (P) divider output (PLLSAI2CLK)
    HSI16 clock.

4.6 Power control (PWR)

In STM32L4 Series and STM32L4+ Series, the PWR controller presents some differences compared to the one on STM32F401 and STM32F411 lines. These differences are summarized in *Table 17*.

Table 17. PWR differences between STM32F401 line, STM32F411 line, and STM32L4 Series / STM32L4+ Series

PWR	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Power supplies	– V_{DD} = 1.7 to 3.6 V when internal voltage regulator is disabled	V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, Flash memory and
	– V_{CORE} = 1.2 V (scalable) – V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator – The voltage regulator requires one or two external capacitors connected to dedicated pins VCAP_1, VCAP_2 – In application Run mode, the voltage regulator output voltage can be scaled by software (lowered) to save power consumption when the device is clocked below the maximum frequency	– V_{CORE} = 1.0 to 1.28 V V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. It is generated by an internal voltage regulator – Two V_{CORE} ranges can be selected by software depending on target frequency
	V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present	V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present
	V_{DD} and V_{DDA} must be at the same voltage value	Independent power supplies (V_{DDA}, V_{DDUSB}, V_{DDIO2}) allow to improve power consumption by running MCU at lower supply voltage than analog and USB
	– V_{SSA}, V_{DDA}: 1.8 V to 3.6 V (1.7V with external power-supply supervisor) – V_{DDA} is the external analog power supply for A/D and D/A converters – V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively	– V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DAC/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V. – V_{DDA} is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators – The V_{DDA} voltage level is independent from the V_{DD} voltage
	NA	– V_{LCD} = 2.5 to 3.6 V – The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter

Table 17. PWR differences between STM32F401 line, STM32F411 line, and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Power supplies (continued)	– N/A – USB OTG FS powered by V_{DD} – V_{DD} must be > 3.0 V (or degraded electrical characteristic between 2.7 V to 3V)	– V_{DDUSB} = 3.0 to 3.6 V – V_{DDUSB} is the external independent power supply for USB transceivers – The V_{DDUSB} voltage level is independent from the V_{DD} voltage
	– N/A No VDDIO2 supply in STM32F401/411 lines	– V_{DDIO2} = 1.08 V to 3.6 V – V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]) – The V_{DDIO2} voltage level is independent from the V_{DD} voltage (not applicable for STM32L45xxx/46xxx, STM32L43xxx/44xxx nor STM32L41xxx/42xxx)
	NA	– Available only on SM32L4R9xx/4S9xx – VDDDSI is independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY – This supply must be connected to the global VDD
	NA	– Available only on SM32L4R9xx/4S9xx – VCAPDSI is the output of the DSI regulator (1.2V) which must be connected externally to VDD12DSI
	NA	– Available only on SM32L4R9xx/4S9xx – VDD12DSI is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins – An external capacitor of 2.2µF must be connected on the VDD12DSI pin
Battery backup domain	– RTC with backup registers (80 bytes) – LSE – PC13 to PC15 I/Os	– RTC with backup registers (128 bytes) – LSE – PC13 to PC15 I/Os
Power supply supervisor	– Integrated POR / PDR circuitry – Programmable voltage detector (PVD)	– Integrated POR / PDR circuitry – Programmable voltage detector (PVD)
	– Brownout reset (BOR) – BOR can be disabled after power-on	– Brownout reset (BOR) – BOR is always enabled, except in Shutdown mode
	NA	4 peripheral voltage monitoring (PVM): – PVM1 for VDDUSB – PVM2 for VDDIO2 (for STM32L49xxx/4Axxx and STM32L47xxx/48xxx only) – PVM3/PVM4 for VDDA (~1.65 V/ ~2.2 V)

Table 17. PWR differences between STM32F401 line, STM32F411 line, and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Low-power modes	Sleep mode	Sleep mode
	NA	Low-power run mode – System clock is limited to 2 MHz – I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz – Consumption is reduced at lower frequency thanks to LP regulator usage
		Low-power sleep mode – System clock is limited to 2 MHz – I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz – Consumption is reduced at lower frequency thanks to LP regulator usage
	Stop mode (all clocks are stopped)	Stop 0, Stop1 and Stop2 mode Some additional functional peripherals (cf wakeup source)
	Standby mode (V_{CORE} domain powered off)	Standby mode (V_{CORE} domain powered off) – Optional SRAM2 retention – Optional I/O pull-up or pull-down configuration
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off)
External SMPS	NA	– Support for external SMPS for high-power efficiency. Refer to AN4978

Table 17. PWR differences between STM32F401 line, STM32F411 line, and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Wake-up sources	Sleep mode Any peripheral interrupt/wakeup event	Sleep mode Any peripheral interrupt/wakeup event
	Stop mode – Any EXTI line event/interrupt – PVD, RTC	Stop 0, Stop 1 and Stop 2 mode – Any EXTI line event/interrupt – BOR, PVD, PVM, COMP, RTC, USB, IWDG, – U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
	Standby mode – WKUP pin (PA0) rising edge – RTC event – External reset in NRST pin – IWDG reset	Standby mode – Up to 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin – IWDG reset
	NA	Shutdown mode – Up to 5 WKUP pins rising or falling edge – RTC event – External reset in NRST pin
Wake-up clocks	Wake-up from Stop HSI 16 MHz	Wake-up from Stop HSI16 16 MHz or MSI (all ranges up to 48 MHz) allowing 5 µs wakeup at high speed without waiting for PLL startup time
	Wake-up from Standby HSI 16 MHz	Wake-up from Standby MSI (ranges from 1 to 8 MHz)
	NA	Wake-up from Shutdown MSI 4 MHz
Configuration	-	– In STM32L4 Series and STM32L4+ Series the registers are different – From 2 registers in STM32F401/411 lines up to 25 registers in STM32L4 Series / STM32L4+ Series 4 control registers 2 status registers 1 status clear register 2 registers per GPIO port (A,B,I) for controlling pull-up and pull-down – Most configuration bits from STM32F401 and STM32F411 lines can be found in STM32L4 Series / STM32L4+ Series (but sometime may have a different programming mode)

Table 17. PWR differences between STM32F401 line, STM32F411 line, and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Color key: = New feature or new architecture = Same feature, but specification change or enhancement = Feature not available (NA) = Differences		

4.7 Real-time clock (RTC)

STM32L4 Series / STM32L4+ Series, STM32F401 line and STM32F411 line implement almost the same features on the RTC. *Table 18* shows the differences.

Table 18. RTC differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

RTC	STM32F401and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Features	– Coarse digital calibration – Kept for compatibility only, new developments must only use smooth calibration	Only smooth calibration available
	1 tamper pin (available in VBAT)	3 tamper pins (available in VBAT)
	80 bytes backup registers	128 bytes backup registers
Configuration	-	Coarse digital calibration not available in STM32L4 Series / STM32L4+ Series: – RTC_CR/DCE not available – RTC_CALIBR register not available – RTC_TAFCR (F4) = RTC_TAMPCR (L4) except a few bits
Color key: = Same feature, but specification change or enhancement = Feature not available (NA)		

For more information about RTFC features on STM32L4 Series and STM32L4+ Series, refer to the RTC chapter of the STM32L4 Series and STM32L4+ Series reference manuals.

4.8 System configuration controller (SYSCFG)

The STM32L4 Series and STM32L4+ Series SYSCFG implements additional features compared to the STM32F401 and STM32F411 lines. *Table 19* shows the differences.

Table 19. SYSCFG differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

SYSCFG	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Features	– Remapping memory areas – Managing the external interrupt line connection to the GPIOs	– Remapping memory areas – Managing the external interrupt line connection to the GPIOs – Managing robustness feature – Setting SRAM2 write protection and software erase – Configuring FPU interrupts – Enabling the firewall – Enabling /disabling I2C Fast-mode Plus driving capability on some I/Os and voltage booster for I/Os analog switches
Configuration	-	– Most registers from STM32F401 and STM32F411 lines are identical to the ones in STM32L4 Series / STM32L4+ Series – A few bits are different and EXTI configuration may differ (number of GPIO is different depending on product)
Color key: = Same feature, but specification change or enhancement		

4.9 General-purpose I/O interface (GPIO)

The GPIO peripheral of the STM32L4 Series and STM32L4+ Series devices embeds identical features compared to the one present in the STM32F401 and STM32F411 lines.

The GPIO code written for the STM32F401 and STM32F411 lines may require minor adaptations for the STM32L4 Series and STM32L4+ Series devices. This is due to the mapping of particular functions on different GPIOs (refer to pinout differences in *Section 2: Hardware migration* and to the product's datasheet for detailed alternate function mapping differences).

Below are the main GPIO features:

- GPIO mapped on AHB bus for better performance
- I/O pin multiplexer and mapping: pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) connected to an I/O pin at a time. In this way, there cannot be any conflict between peripherals sharing the same I/O pin.

At reset, the GPIOs on the STM32F401 and STM32F411 lines are configured in Input-floating mode while the GPIOs on the STM32L4 Series and STM32L4+ Series are configured in analog mode (to avoid consumption through the IO Schmitt trigger).

For more information on the GPIO programming and usage on STM32L4 Series and STM32L4+ Series, refer to the “I/O pin multiplexer and mapping” section in the GPIO chapter of the STM32L4 Series and STM32L4+ Series reference manuals. For detailed description of the pinout and alternate function mapping, refer to the product’s datasheet.

4.10 Extended interrupts and events controller (EXTI) source selection

The external interrupt/event controller (EXTI) is very similar on STM32F401 line, STM32F411 line and on STM32L4 Series / STM32L4+ Series. *Table 20* shows the main differences.

Table 20. EXTI differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

EXTI	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Number of event/interrupt lines	Up to 23 configurable lines	Up to 41 lines: – 12 direct, 26 configurable on STM32L4+ Series – 15 direct, 26 configurable on STM32L49xxx/4Axxx – 14 direct, 26 configurable on STM32L47xxx/48xxx – 12 direct, 25 configurable on STM32L43xxx/44xxx and STM32L41xxx/42xxx
Configuration	-	Registers are slightly different to cope with different number of interrupts
Color key: = Same feature, but specification change or enhancement		

4.11 Flash memory

Table 21 presents the difference between the Flash memory interface of the STM32F401 and STM32F411 lines, and the one of the STM32L4 Series / STM32L4+ Series.

The STM32L4 Series and STM32L4+ Series instantiates a different Flash module both in terms of architecture/technology and interface, consequently the STM32L4 Series and STM32L4+ Series Flash memory programming procedures and registers are different compared to the ones of the STM32F401 and STM32F411 lines.

Any code written for the Flash interface in the STM32F401 and STM32F411 lines needs to be rewritten to run in the STM32L4 Series and STM32L4+ Series.

For more information on programming, erasing and protection of the STM32L4 Series and STM32L4+ Series Flash memory, refer to the STM32L4 Series and STM32L4+ Series reference manuals.

Table 21. FLASH differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

Flash	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Main/ Program memory	0x0800 0000 to (up to) 0x0807 FFFF	– 0x0800 0000 to up to 0x080F FFFF – 0x0800 0000 to up to 0x081F FFFF (only for STM32L4+ Series)
	– Up to 512 Kbytes – 4 sectors of 16 Kbytes – 1 sector of 64 Kbytes – 1 or 3 sectors of 128 Kbytes – Programming granularity: 8, 16, 32, 64-bit – Read granularity: 128-bit	– For STM32L4+ Series: Up to 2 Mbytes Split in 2 banks When dual bank is enabled each bank: 256 pages of 4 Kbytes and each page: 8 rows of 512 bytes When dual bank is disabled memory block contains 256 pages of 8 Kbytes and each page: 8 rows of 1024 bytes – For STM32L49xxx/4Axxx and STM32L47xxx/48xxx: Up to 1 Mbyte Split in 2 banks Each bank: 256 pages of 2 Kbytes Each page: 8 rows of 256 bytes – For STM32L45xxx/46xxx: Up to 512 Kbytes 1 bank 256 pages of 2 Kbytes Each page: 8 rows of 256 bytes – For STM32L43xxx/44xxx: Up to 256 Kbytes 1 bank 128 pages of 2 Kbytes Each page: 8 rows of 256 bytes – For STM32L41xxx/42xxx: Up to 128 Kbytes 1 bank 64 pages of 2 Kbytes Each page: 8 rows of 256 bytes – Programming and read granularity: 72-bit (including 8 ECC bits)
Features	NA	– Read while write (RWW) – Dual bank boot (only for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx)
		– ECC – Flash Empty check (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
Wait state	Up to 6 (depending on the supply voltage and frequency)	Up to 5 (depending on the core voltage and frequency)

Table 21. FLASH differences between STM32F401 line, STM32F411 line and STM32L4 Series (continued)/ STM32L4+ Series (continued)

Flash	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
ART Accelerator™	Allowing 0 wait state when executing from the cache	Allowing 0 wait state when executing from the cache
One time programmable (OTP)	512 OTP bytes	1 Kbyte OTP bytes (bank1)
Flash interface	NA	Different from STM32F401 and STM32F411 lines
Erase granularity	Sector and mass erase	Page erase (2 Kbytes), bank erase and mass erase (all banks)
Read protection (RDP)	– Level 0 no protection – RDP = 0xAA	– Level 0 no protection – RDP = 0xAA
	– Level 1 memory protection – RDP ≠ {0xAA, 0xCC}	– Level 1 memory protection – RDP ≠ {0xAA, 0xCC}
	Level 2 RDP = 0xCC(1)	Level 2 RDP = 0xCC(1)
Proprietary code readout Protection (PCROP)	Granularity: 1 sector	– 1 PCROP area per bank – Granularity: 64-bit – PCROP_RDP option: PCROP area preserved when RDP level decreased – For STM32L4+ Series: Dual bank: 1 PCROP area per bank Single bank: 2 PCROP area
Write protection (WRP)	Granularity: 1 sector	– 2 write protection area per bank – Granularity: 2 Kbytes – For STM32L4+ Series: Dual bank: 2 areas per bank Single bank: 4 areas

Table 21. FLASH differences between STM32F401 line, STM32F411 line and STM32L4 Series (continued)/ STM32L4+ Series (continued)

Flash	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
User-option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	NA	nRST_SHDW
	WDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
		WWDG_SW
	BOR_LEV[1:0]	BOR_LEV[2:0]
	NA	BFB2 (except for STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
		nBOOT1
		SRAM2_RST, SRAM2_PE
		DUAL BANK (except for STM32L4+ Series, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
User option bytes (continued)	SPRMOD	nBOOT0 (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xx)
	NA	nSWBOOT0 (only for STM32L4xxx/4Sxxx, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)
		DBANK (for STM32L4+ Series)
		DB1M (for STM32L4+ Series)

Color key:

= New feature or new architecture

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Differences

1. Memory read protection level 2 is an irreversible operation. When level 2 is activated, the level of protection cannot be decreased to level 0 or level 1.

4.12 Universal synchronous asynchronous receiver transmitter (U(S)ART)

The STM32L4 Series and STM32L4+ Series devices implement several new features on the U(S)ART compared to STM32F401 and the STM32F411 lines devices. *Table 22* shows the differences.

Table 22. U(S)ART differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

U(S)ART	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Instances	3 x USART	– 3 x USART – 2 x UART for STM32L49xxx/4Axxx and STM32L47xxx/48xxx – 1 x UART for STM32L45xxx/46xxx – 1 x LPUART
Baud rate	– Up to 2 x 10.5 Mbit/s + 1 x 5.25 Mbit/s (STM32F401 line) – Up to 2 x 12.5 Mbit/s + 1 x 6.25 Mbit/s (STM32F411 line)	Up to 10 Mbit/s (when the clock frequency is 80 MHz and oversampling is by 8)
Clock	Single clock domain	Dual clock domain allowing: – UART functionality and wakeup from Stop mode – Convenient baud rate programming independent from the PCLK reprogramming
Data	Word length: programmable (8 or 9 bits)	– Word length: programmable (7, 8 or 9 bits) – Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	– 14 interrupt sources with flags – 23 interrupt sources with flags for STM32L4+ Series

Table 22. U(S)ART differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series (continued)

U(S)ART	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Features	– Hardware flow control (CTS/RTS) – Continuous communication using DMA – Multiprocessor communication – Single-wire half-duplex communication – IrDA SIR ENDEC block – LIN mode – SPI master	
	– Smartcard mode T = 0 and T = 1 is to be implemented by software – Number of stop bits: 0.5, 1, 1.5, 2	– Smartcard mode T = 0 and T = 1 supported (features are added to support T = 1 such as receiver timeout, block length, end of block detection, binary data inversion, among others) – Number of stop bits: 1, 1.5, 2
	NA	– Wakeup from Stop mode (Start bit, received byte, address match) – Support for ModBus communication Timeout feature CR/LF character recognition – Receiver timeout interrupt – Auto baud rate detection – Driver Enable – Swappable Tx/Rx pin configuration – Two internal FIFOs for transmit and receive data (for STM32L4+ Series) – SPI slave (for STM32L4+ Series) LPUART does not support synchronous mode (SPI Master), Smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt, auto baud rate detection.
Features (continued)	NA	– STM32F401/411 lines registers and associated bits are not identical in STM32L4 Series / STM32L4+ Series – Refer to STM32L4 Series and STM32L4+ Series reference manuals for details

Color key:

= New feature or new architecture

= Same feature, but specification change or enhancement

= Feature not available (NA)

= Differences

4.13 Inter-integrated circuit (I2C) interface

The STM32L4 Series and STM32L4+ Series devices implement a different I2C peripheral which allows an easy software management. *Table 23* shows the differences.

Table 23. I2C differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

I2C	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Instances	x3	– x3 for STM32L47xxx/48xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx – x4 for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L45xxx/46xxx
Features	– 7-bit and 10-bit Addressing mode – SMBus – Standard mode (Sm, up to 100 kHz) – Fast mode (Fm, up to 400 kHz)	
	NA	– Fast mode Plus (Fm+, up to 1 MHz) – Independent clock – Wakeup from STOP on address match
Configuration	-	– Register configuration is very different in STM32F401 and STM32F411 lines compared to STM32L4 Series and STM32L4+ Series – Refer to STM32L4 Series and STM32L4+ Series reference manuals for details
Color key: = New feature or new architecture = Feature not available (NA) = Differences		

4.14 Serial peripheral interface (SPI) / IC to IC sound (I2S) /serial audio interface (SAI)

STM32L4 Series / STM32L4+ Series, STM32F401 line and STM32F411 line implement almost the same features on the SPI (apart from I2S). *Table 24* shows the differences.

Table 24. SPI differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

SPI	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Instances	– x4 (for STM32F401 line) – x5 (for STM32F411 line)	x3
Features	SPI + I2S	– I2S feature is not supported by SPI in STM32L4 Series / STM32L4+ Series – SAI interfaces are available instead: x2 (SAI1, SAI2) for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx x1 (SAI1) for STM32L45xxx/46xxx and STM32L43xxx/44xxx
Data size	Fixed, configurable to 8 or 16 bits	Programmable from 4 to 16-bit
Data buffer	Tx & Rx 16-bit buffers (single data frame)	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	No (16-bit access only)	Yes (8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds)
Mode	– SPI TI mode – SPI Motorola mode	– SPI TI mode – SPI Motorola mode – NSSP mode
Speed	– Up to 42 Mbit/s (core at 84 MHz) (for STM32F401 line) – Up to 50 Mbit/s (core at 100 MHz) (for STM32F411 line)	Up to 40 Mbit/s (APB at 80 MHz)
Configuration	-	The data size and Tx/Rx flow handling are different in STM32F401/411 lines and STM32L4 Series / STM32L4+ Series hence requiring different software sequence
Color key: = New feature or new architecture = Same feature, but specification change or enhancement = Differences		

Migrating from I2S to SAI

The STM32L4 Series and STM32L4+ Series devices do not include an I2S interface as part of the SPI peripheral, they include a serial audio interface (SAI) instead.

Table 25 shows the main differences between I2S and SAI. This comparison considers only the full duplex I2S instances.

Table 25. I2S/SAI differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

I2S/SAI	STM32F401 and STM32F411 lines (I2S)	STM32L4 Series / STM32L4+ Series (SAI)
Instances Full duplex I2S	x2	– x2 (SAI1, SAI2) for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx – x1 (SAI1) for STM32L45xxx/46xxx and STM32L43xxx/44xxx
Features	Full-duplex communication	Two independent audio sub-blocks (per SAI) which can be transmitters or
	Master or slave operations	– Synchronous or Asynchronous mode between the audio sub-blocks – Possible synchronization between multiple SAIs – Master or slave configuration independent for both audio sub-blocks
	8-bit programmable linear prescaler to reach accurate audio sample frequencies (from8 kHz to 192 kHz)	Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in Master mode

Table 25. I2S/SAI differences between STM32F401 line, STM32F411 line and STM32L4 Series (continued)/ STM32L4+ Series (continued)

I2S/SAI	STM32F401 and STM32F411 lines (I2S)	STM32L4 Series / STM32L4+ Series (SAI)
Features (continued)	– Data format may be 16-bit, 24-bit or 32-bit. – Data direction is always MSB first	– Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit. – First active bit position in the slot is configurable – LSB first or MSB first for data transfer
	Channel length is fixed to 16-bit (16-bit data size) or 32-bit (16-bit, 24-bit, 32-bit data size) by audio channel	– Up to 16 slots available with configurable size – Number of bits by frame can be configurable – Frame synchronization active level configurable (offset, bit length, level) – Stereo/Mono audio frame capability
	Programmable clock polarity (steady state)	Communication clock strobing edge configurable (SCK)
	16-bit register for transmission and reception with one data register for both channel sides	8-word integrated FIFOs for each audio sub-block (facilitating Interrupt mode)
	Supported I2S protocols: – I2S Philips standard – MSB-justified standard (left-justified) – LSB-justified standard (right-justified) – PCM standard (with short and long frame synchronization on 16-bit channel frame or 16-bit data frame extended to 32-bit channel frame)	Audio protocols: – I2S, LSB or MSB-justified, PCM/DSP, TDM (up to 16 channels), AC'97 – SPDIF output – Mute mode – PDM interface (for STM32L4Rxxx/L4Sxxx)
	DMA capability for transmission and reception (16-bit wide)	2-channel DMA per SAI
	– Master clock may be output to drive an external audio component Ratio is fixed at 256 × F_S (where F_S is the audio sampling frequency)	
	Interrupt sources when enabled: – Errors – Tx Buffer Empty, Rx Buffer not Empty	Interrupt sources when enabled: – Errors – FIFO requests
	Error flags with associated interrupts if enabled respectively: – Overrun and underrun detection – Anticipated frame synchronization signal detection in Slave mode – Late frame synchronization signal detection in Slave mode	Same than STM32F401 and STM32F411 lines + protection against misalignment in case of underrun and overrun

Table 25. I2S/SAI differences between STM32F401 line, STM32F411 line and STM32L4 Series (continued)/ STM32L4+ Series (continued)

I2S/SAI	STM32F401 and STM32F411 lines (I2S)	STM32L4 Series / STM32L4+ Series (SAI)
Configuration	-	– There is no compatibility between the I2S on STM32F401 and STM32F411 lines and the SAI on STM32L4 Series / STM32L4+ Series – User must configure the SAI interface for the target protocol – Refer to the STM32L4 Series and STM32L4+ Series reference manuals for details
Color key: = New feature or new architecture = Same feature, but specification change or enhancement = Differences		

The SAI peripheral improves robustness of communication in Slave mode compared to the I2S peripheral (in case of data clock glitch for example).

In Master mode, while migrating an application from the STM32F401 and STM32F411 lines to the STM32L4 Series / STM32L4+ Series devices, the user must review the possible master clock (MCLK), the data bit clock (SCK) and the frame synchronization (FS) frequency reachable.

The user must use the STM32L4 Series / STM32L4+ Series PLL multiplication factors and the SAI internal clock divider for a given external oscillator (which can be different than the ones on the STM32F401 and STM32F411 lines I2S).

In the STM32L4 Series / STM32L4+ Series, the SAI1 and SAI2 input clocks are derived (selected by software) from one of the following sources:

- For STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx:
  - An external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2
  - PLLSAI1 (P) divider output (PLLSAI1CLK)
  - PLLSAI2 (P) divider output (PLLSAI2CLK)
  - Main PLL (P) divider output (PLLSAI3CLK)
- For STM32L45xxx/46xxx and STM32L43xxx/44xxx:
  - An external clock mapped on SAI1_EXTCLK for SAI1
  - PLLSAI1 (P) divider output (PLLSAI1CLK)
  - Main PLL (P) divider output (PLLSAI2CLK)
  - HSI16 clock

When the clock is derived from one of the internal PLLs, the three PLL inputs are either HSI16, HSE or MSI (between 4 and 48 MHz) divided by a programmable factor PLLM (from 1 to 8 (or from1 to 16 for STM32L4+ Series)).

For STM32L4+ Series, when the clock is derived from one of the internal PLLs, the three PLL inputs are either HSI16, HSE or MSI divided by its own programmable factor (PLLM, PLLSAI1M and PLLSAI2M) (from 1 to 16).

This input is then multiplied by PLLN (from 8 to 86 (or from 8 to 127 for STM32L4+ Series)) to reach PLL VCO frequency (must be between 64 and 344 MHz).

It is finally divided by PLLP to provide the input clock of the SAI (max 80 MHz (or 120 MHz for STM32L4+ Series)):

- 7 or 17 on STM32L47xxx/48xxx devices
- [2...31] on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx and STM32L43xxx/44xxx devices

When the master clock MCLK is used by the external slave audio peripheral, the PLL output is divided by the SAI internal master clock divider factor (1, 2, 4, 6, 8, ..., 30) to provide the master clock (MCLK). The data bit clock is then derived from MCLK with the following formula:

$$SCK = MCLK \times (FRL + 1) / 256 = (MCLK) / (256 / (FRL + 1))$$

Where:

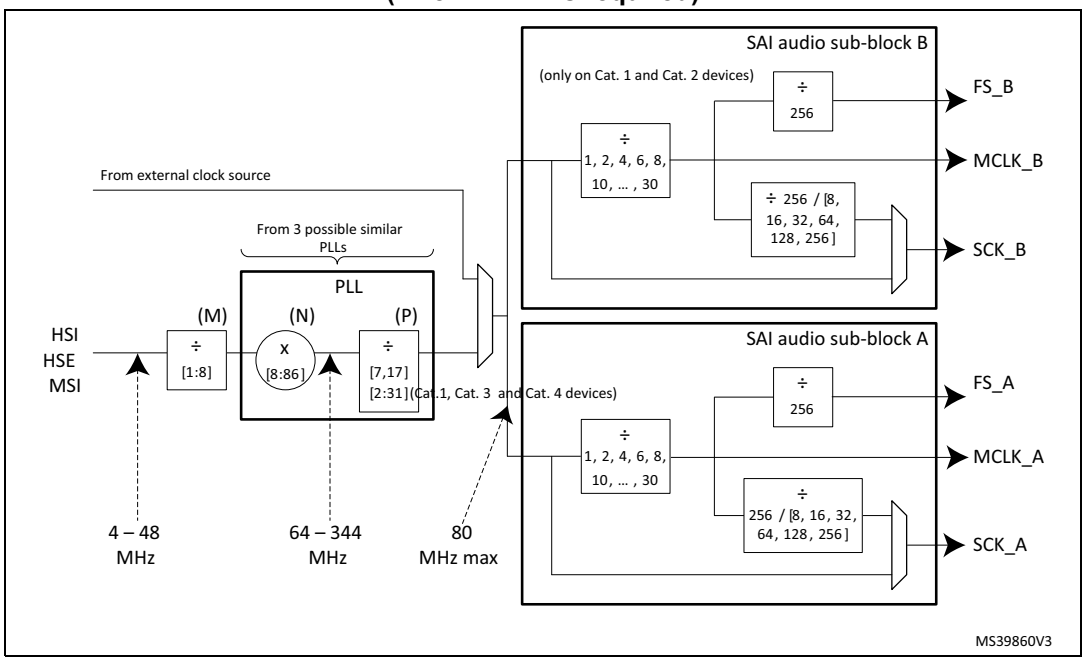
- FRL is the number of bit clock cycles - 1 in the audio frame (0 to 255)
- (FRL+ 1) must be a power of 2 higher or equal to 8
- (FRL + 1) = 8, 16, 32, 64, 128, 256

The SCK can also be directly connected to the input clock of the SAI when MCLK output is not needed.

The frame synchronization (FS) frequency is always MCLK / 256.

Figure 5 illustrates the clock generation scheme in the STM32L4 Series / STM32L4+ Series. Refer to the STM32L4 Series and STM32L4+ Series reference manuals for more details.

Figure 5. STM32L4 Series / STM32L4+ Series generation of clock for SAI Master mode (when MCLK is required)



4.15 Cyclic redundancy check calculation unit (CRC)

The CRC is very similar in STM32F401 line, STM32F411 line and in STM32L4 Series / STM32L4+ Series. *Table 26* shows the differences.

Table 26. CRC differences between STM32F401 line, STM32F411 line and STM32L4 Series/ STM32L4+ Series

CRC	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Features	– Single input/output 32-bit data register – CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size – General-purpose 8-bit register (can be used for temporary storage)	
	– Use CRC-32 (Ethernet) polynomial: 0x4C11DB7 – Handles 32-bit data size	– Fully programmable polynomial with programmable size (7, 8, 16, 32-bit) – Handles 8-,16-, 32-bit data size – Programmable CRC initial value – Input buffer to avoid bus stall during calculation – Reversibility option on input and output

Table 26. CRC differences between STM32F401 line, STM32F411 line and STM32L4 Series/ STM32L4+ Series (continued)

CRC	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series
Configuration	-	– Configuration registers in STM32F401 and STM32F411 lines are identical than the ones in STM32L4 Series / STM32L4+ Series – The STM32L4 Series and STM32L4+ Series devices include additional registers for new features – Refer to the STM32L4 Series and STM32L4+ Series reference manuals for details
Color key: = New feature or new architecture		

4.16 USB on-the-go full speed (USB OTG FS)

Very similar USB OTG FS peripherals are implemented on STM32L4+ Series, STM32L49xxx/4Axxx, STM32L47xxx/48xxx devices and in the STM32F401 and STM32F411 lines.

The key differences are listed in *Table 27*.

Table 27. USB OTG FS differences between STM32F401 line, 411 line and STM32L4+ Series

USB	STM32F401 and STM32F411 lines	STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx
Features	– Universal serial bus revision 2.0 – Full support for the USB on-the-go (USB OTG)	
	FS mode: – 1 bidirectional control endpoint – 3 IN endpoints (bulk, interrupt, isochronous) – 3 OUT endpoints (bulk, interrupt, isochronous)	FS mode: – 1 bidirectional control endpoint – 5 IN endpoints (bulk, interrupt, isochronous) – 5 OUT endpoints (bulk, interrupt, isochronous)
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	
	NA	– Attach detection protocol (ADP) – Battery charging detection (BCD)
		Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB
Mapping	AHB2	

Table 27. USB OTG FS differences between STM32F401 line, 411 line and STM32L4+ Series (continued)

USB	STM32F401 and STM32F411 lines	STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx
Buffer memory	– 1.25 Kbyte data FIFOs – Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO	– 1.25 Kbyte data FIFOs – Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO
Low-power modes	USB suspend and resume	– USB suspend and resume – Link power management (LPM) support
Configuration	-	– In STM32L4+ Series the registers are different – Refer to the STM32L4+ Series reference manuals for details
Color key: = New feature or new architecture = Same feature, but specification change or enhancement = Feature not available (NA) = Differences		

On the STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, the USB is full speed (FS) device only. The main features are listed in *Table 28*.

On the STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx devices, a clock recovery system (CRS) block is included. It can provide a precise clock to the USB peripheral.

When using the USB device mode, the CRS allows a crystal-less USB operation.

When using the USB host mode, the CRS allows a low-frequency crystal (32.768 kHz) USB operation.

Table 28. USB FS on the STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx

USB	STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx
Features	Universal Serial Bus (USB) revision 2.0, including link power management (LPM) support
	– Configurable number of endpoints from 1 to 8 – Cyclic redundancy check (CRC) generation/checking, Non-return-to-zero Inverted (NRZI) encoding/decoding and bit-stuffing – Isochronous transfers support – Double-buffered bulk/isochronous endpoint support – USB Suspend/Resume operations – Frame locked clock pulse generation

Table 28. USB FS on the STM32L45xxx/46xxx, STM32L43xxx/44xxx (continued)and STM32L41xxx/42xxx

USB	STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx
Features (continued)	– Attach detection protocol (ADP) – Battery charging detection (BCD) – USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)
	– Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB
Mapping	APB1
Buffer memory	1024 bytes of dedicated packet buffer memory SRAM
Low-power modes	– USB suspend and resume – Link power management (LPM) support

4.17 Analog-to-digital converters (ADC)

Table 29 details the differences between the ADC peripherals of the STM32F401 and STM32F411 lines compared to the STM32L4 Series / STM32L4+ Series devices. The main differences are a new digital interface and new architecture/features.

Table 29. ADC differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series

ADC	STM32F401 and STM32F411 lines	STM32L4 Series / STM32L4+ Series (1)
ADC type	SAR structure	SAR structure
Instances	1 instance	– x3 for STM32L49xxx/4Axxx and STM32L47xxx/48xxx – x2 for STM32L41xxx/42xxx – x1 for STM32L4+ Series, STM32L45xxx/46xxx and STM32L43xxx/44xxx
Max sampling frequency	2.4 Msps	– 5.1 Msps (fast channels) – 4.8 Msps (slow channels)
Number of channels	Up to 16 channels	Up to 19 channels per ADC
Resolution	12-bit	12-bit + digital oversampling up to 16-bit
Conversion modes	Single / Continuous / Scan / Discontinuous	Single / Continuous / Scan / Discontinuous Dual mode
DMA	Yes	Yes

Table 29. ADC differences between STM32F401 line, STM32F411 line and STM32L4 Series (continued)/ STM32L4+ Series (continued)

ADC	STM32F401 and STM32F411 lines		STM32L4 Series / STM32L4+ Series (1)	
External trigger	Yes		Yes	
	External event for regular group: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM2 CC3 TIM2 CC4 TIM2_TRGO TIM3_CH1 TIM3 TRGO TIM4 CC4 TIM5_CC1 TIM5_CC2 TIM5_CC3 EXTI line 11	External event for injected group: TIM1_CH4 TIM1_TRGO TIM2_CH1 TIM2_TRGO TIM3_CH2 TIM3_CH4 TIM4_CH1 TIM4_CH2 TIM4_CH3 TIM4_TRGO TIM5_CH4 TIM5_TRGO EXTI line 15	External event for regular group: TIM1 CC1 TIM1 CC2 TIM1 CC3 TIM2 CC2 TIM3 TRGO TIM4 CC4 EXTI line 11 TIM8_TRGO TIM8_TRGO2 TIM1_TRGO TIM1_TRGO2 TIM2_TRGO TIM4_TRGO TIM6_TRGO TIM15_TRGO TIM3_CC4	External event for injected group: TIM1 TRGO TIM1 CC4 TIM2 TRGO TIM2 CC1 TIM3 CC4 TIM4 TRGO EXTI line15 TIM8_CC4 TIM1_TRGO2 TIM8_TRGO TIM8_TRGO2 TIM3_CC3 TIM3_TRGO TIM3_CC1 TIM6_TRGO TIM15_TRGO
Supply requirement	1.8 V to 3.6 V (1.7 V with external power-supply supervisor)		– 1.62 V to 3.6 V – Independent power supply (V_{DDA})	
Reference voltage	External V_{DDA} - V_{REF+} < 1.2 V		Reference voltage for STM32L4 Series / STM32L4+ Series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)	
Electrical parameters	– 300 µA (Typ.) on V_{REF} DC current – 1.8 mA (Typ.) on V_{DDA} DC current		Consumption proportional to conversion speed: 200 µA/Msps	
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$		$V_{REF-} \leq V_{IN} \leq V_{REF+}$	
Color key: = New feature or new architecture = Same feature, but specification change or enhancement				

1. On STM32L4 Series and STM32L4+ Series devices on which the peripheral is not implemented, the external event is not applicable.

5 Revision history

Table 30. Document revision history

Date	Revision	Changes
21-Jul-2015	1	Initial release
23-Nov-2015	2	*Section 4.2: Memory mapping* updated: Stop 0 mode *added when content is preserved* *Table 16: PWR differences between STM32F401 line, STM32F411 line, and STM32L4 Series* updated: Stop 0 mode added
10-Mar-2016	3	*Section 1: STM32L4 Series overview*; added category 2 and 4 for STLM32L4.
20-Feb-2017	4	Updated: – Document title. – *Introduction*. – *Section 1: STM32L4 Series and STM32L4+ Series overview*. – *Section 2: Hardware migration* – *Figure 3*, – *Table 1*, *Table 2*, *Table 5*, *Table 6*, *Table 7*, *Table 9*, *Table 10*, *Table 16*, *Table 19*, *Table 20*, *Table 21*, *Table 28*. – Cat. 2 devices replaced by STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices. – Cat. 4 devices replaced bySTM32L45xxx/46xxx and STM32L43xxx/44xxx devices. Removed Table *Product category overview*.
01-Sep-2017	5	Updated the whole document to add the information about STM32L4+ Series devices.

Table 30. Document revision history (continued)

Date	Revision	Changes
11-Apr-2018	6	Updated – *Table 6: Bootloader interfaces on STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – DAC naming: 1 DAC with 2 channels instead of 2 DACs
18-Sep-2018	7	Added – Information related to STM32L41xxx/42xxx to the whole document – *Table 1: STM32L4 Series / STM32L4+ Series memory availability* Updated – Cover page – *Section 1: STM32L4 Series and STM32L4+ Series overview* – *Section 3: Boot mode selection* – *Section 4.2: Memory mapping* – *Section 4.16: USB on-the-go full speed (USB OTG FS)* – *Section 4.5.3: Peripheral clock configuration* – *Recommendations to migrate from the STM32F401 and STM32F411 lines board to the STM32L4 Series and STM32L4+ Series boards on page 13* – *Table 2: Packages available on STM32L4 Series and STM32L4+ Series* – *Table 3: Pinout differences between STM32F401 line, STM32F411 line and STM32L4 Series/ STM32L4+ Series* – *Table 5: Boot modes for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and add STM32L41xxx/42xxx devices* – *Table 6: Bootloader interfaces on STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – *Table 7: Peripheral compatibility analysis between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – *Table 8: Peripheral address mapping differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – *Table 12: RCC differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – *Table 17: PWR differences between STM32F401 line, STM32F411 line, and STM32L4 Series / STM32L4+ Series* – *Table 20: EXTI differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – *Table 21: FLASH differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – *Table 23: I2C differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series* – *Table 28: USB FS on the STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx* – *Table 29: ADC differences between STM32F401 line, STM32F411 line and STM32L4 Series / STM32L4+ Series*