Application note

PCB design guidelines for the BlueNRG and BlueNRG-MS devices

Introduction

The BlueNRG and BlueNRG-MS are very low power Bluetooth low energy (BLE) single-mode network processor devices, which can act as master or slave. Both devices embed a 2.4 GHz RF transceiver, a Cortex M0 microcontroller, and a by-passable DC-DC step-down converter to achieve optimum power consumption.

The BlueNRG/MS devices are housed in two different packages:

- QFN 32 pins
- WLCSP 34 balls

ST provides all necessary source files (reference designs) for those customers who want to speed-up their developing.

This application note is intended to accompany the reference designs and provides detailed information regarding the design decisions employed within STMicroelectronics designs. In addition, it details the design guidelines to develop a generic radio frequency application using a BlueNRG and BlueNRG-MS devices. As the layout guidelines are exactly the same for both devices, from now on we use the BlueNRG to refer to the two different devices.

The RF performance and the critical maximum peak voltage, spurious and harmonic emission, receiver matching strongly depend on the PCB layout as well as the selection of the matching network components.

For optimal performance, STMicroelectronics recommends the use of the PCB layout design hints described in the following sections. Last but not least, STMicroelectronics strongly suggests using the BOM defined in the reference design, BOM that guarantees, with a good PCB design, the correct RF performance.

For further information, visit the STMicroelectronics web site at www.st.com.

1 Reference schematics

Different application boards have been developed to show the BlueNRG device functionalities.

The schematics of the different application boards are reported in the following pictures and refer to the various possible combinations:

- QFN32 package, SMD discrete balun, DC-DC converter ON (Figure 1. QFN32 package, SMD discrete balun, DC-DC converter ON);
- QFN32 package, SMD discrete balun, DC-DC converter OFF (Figure 2. QFN32 package, SMD discrete balun, DC-DC converter OFF);
- QFN32 package, integrated balun , DC-DC converter ON (Figure 3. QFN32 package, integrated balun, DC-DC converter ON);
- CSP34 package, SMD discrete balun, DC-DC converter ON (Figure 4. CSP34 package, SMD discrete balun, DC-DC converter ON);
- CSP34 package, SMD discrete balun, DC-DC converter OFF (Figure 5. CSP34 package, SMD discrete balun, DC-DC converter OFF);
- CSP34 package , integrated balun , DC-DC converter ON (Figure 6. CSP34 package, integrated balun, DC-DC converter ON);

All the layout guidelines described in the next sections are to be applied to all these application boards.

Figure 1. QFN32 package, SMD discrete balun, DC-DC converter ON

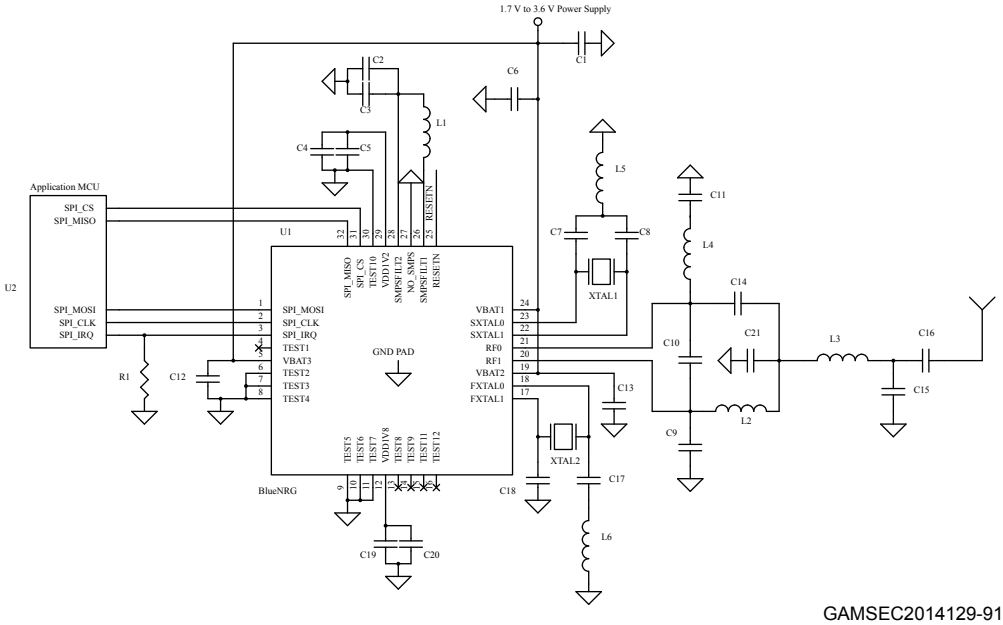

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Figure 2. QFN32 package, SMD discrete balun, DC-DC converter OFF

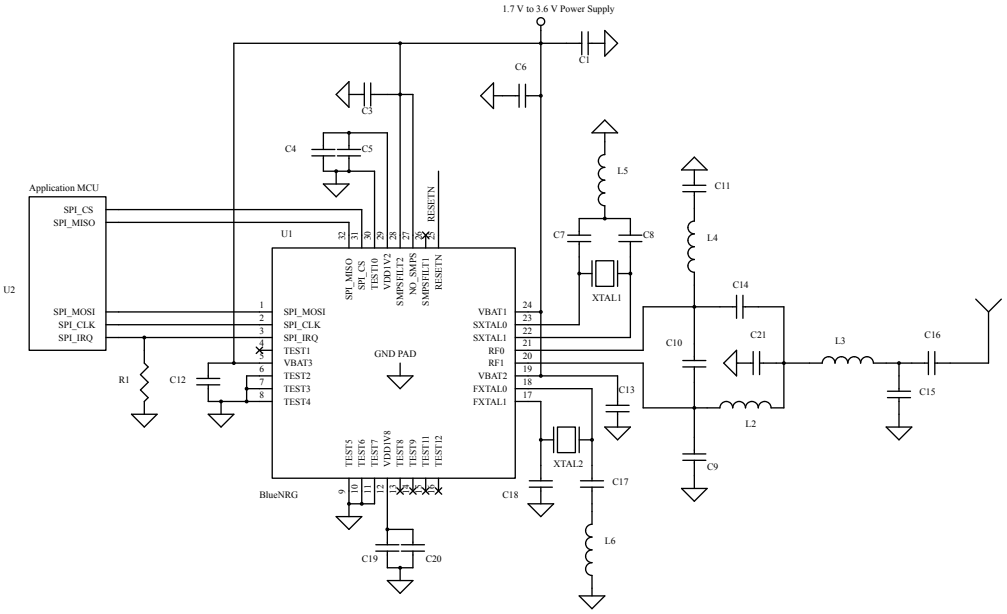

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Figure 3. QFN32 package, integrated balun, DC-DC converter ON

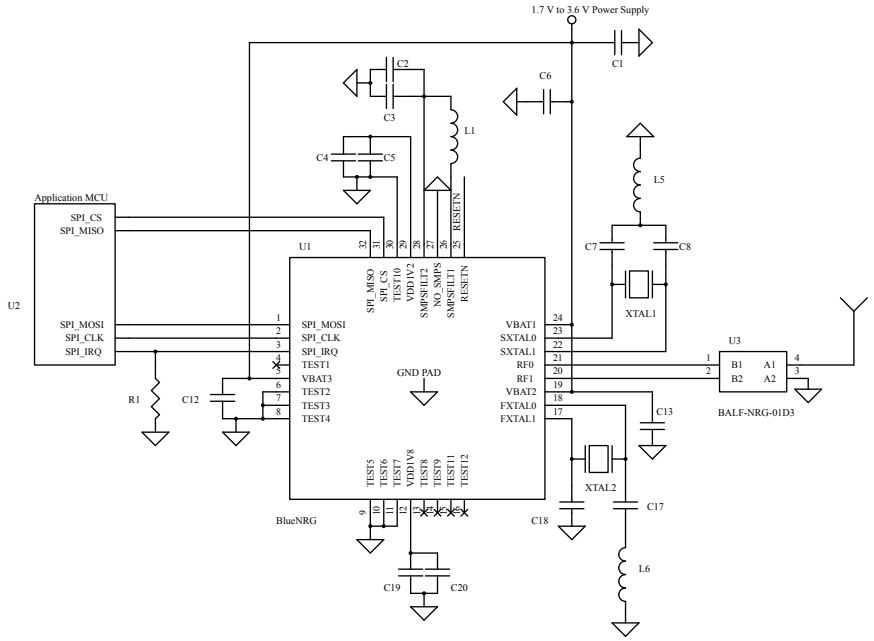

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Figure 4. CSP34 package, SMD discrete balun, DC-DC converter ON

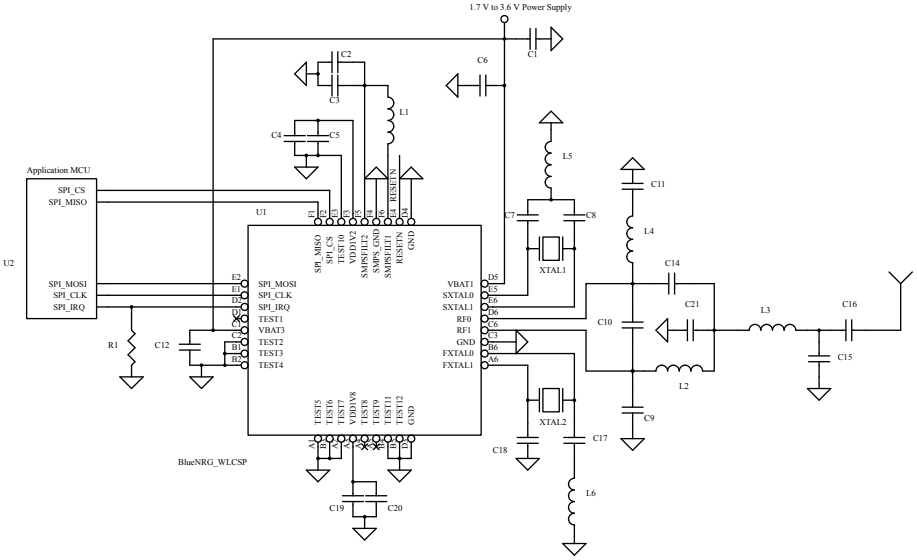

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Figure 5. CSP34 package, SMD discrete balun, DC-DC converter OFF

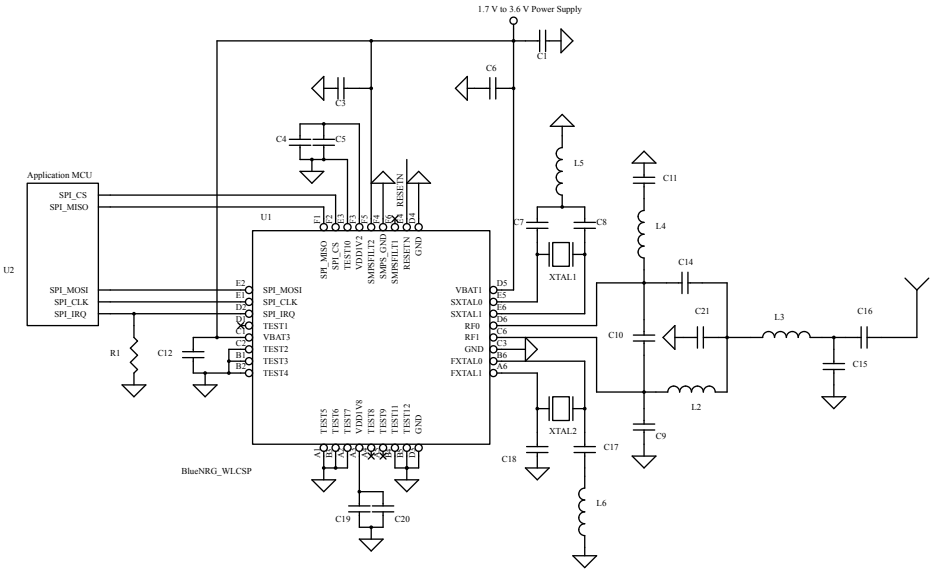

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Figure 6. CSP34 package, integrated balun, DC-DC converter ON

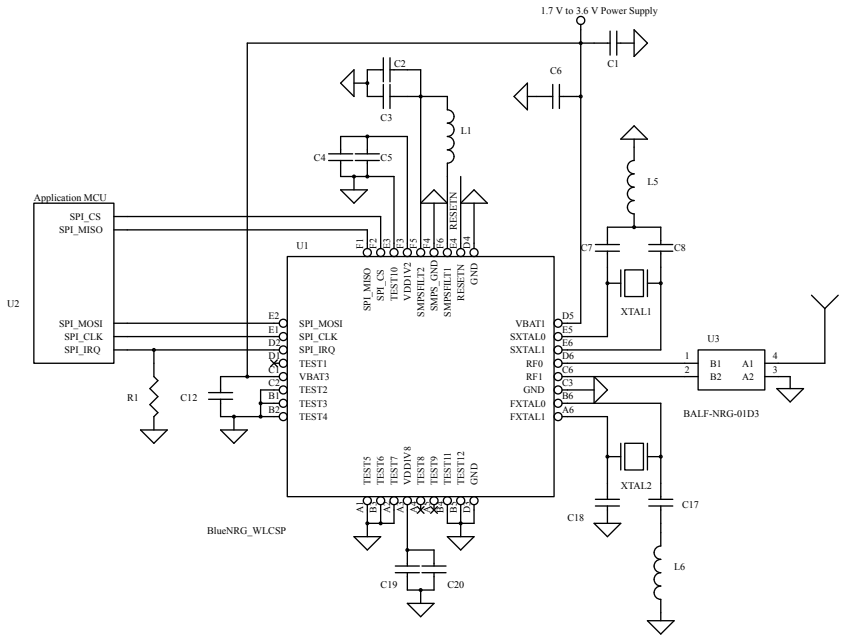

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Table 1. BlueNRG application board external components description

Components	Description
C1, C6, C12	Decoupling capacitors for battery voltage
C2, C3	DC-DC converter filtering capacitors
C4, C5	Decoupling capacitor for on-chip 1.2 V voltage regulator
C19, C20	Decoupling capacitor for on-chip 1.2 V voltage regulator
C9, C10, C11, C14, C15, C16, C21	RF discrete balun filter/matching capacitors
C7, C8	XTAL1 capacitors
C17, C18	XTAL2 capacitors
L1	DC-DC converter inductor
L2, L3, L4	RF discrete balun filter/matching inductors
L5	XTAL1 filtering inductor
L6	XTAL2 filtering inductor
R1	IRQ pull-down resistor
XTAL1	Low-frequency crystal
XTAL2	High-frequency crystal
U1	High-frequency crystal BlueNRG QFN/CSP device
U2	Micro controller
U3	Integrated balun

2 Component dimensioning

The choice of the external components is essential for the correct application functionality. In the next section, the description of the main components, their functionality and how to choose them are described.

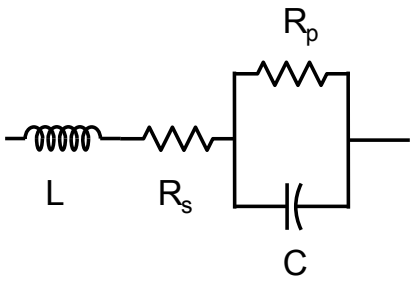
2.1 Capacitors

A capacitor is a passive electrical component used to store energy in an electrical field. The forms of practical capacitors vary widely, but all contain at least two electrical conductors separated by a dielectric.

Capacitors differ from each other in construction techniques and materials used to manufacture. A lot of different types of capacitors exist (double-layer, polyester, polypropylene and so on), but this document focuses on the surface mount versions of ceramics only. The other types of capacitors are not indicated neither for characteristics nor cost for the application targeted in this document.

A capacitor, as a practical device, exhibits not only capacitance but resistance and inductance as well. A simplified schematic for the equivalent circuit is shown in Figure 7. Capacitor equivalent circuit .

Figure 7. Capacitor equivalent circuit



Typically for the capacitors the ESR (equivalent series resistance) and the ESL (equivalent series inductance) are defined. The term ESR combines all losses, both series and parallel, in a capacitor at a given frequency so that the equivalent circuit is reduced to a simple R-C series connection. Same considerations for the ESL that is the equivalent series inductor comprised of three components: pad layout, capacitor height and power plane spreading inductance.

The main differences between ceramic dielectric types are the temperature coefficient of capacitance and the dielectric loss. COG and NP0 (negative-positive-zero, i.e ± 0) dielectrics have the lowest losses and are used for filtering, matching and so on.

For RF parts it is generally recommended multilayer (or monolithic) ceramic capacitors with a COG dielectric material, which is a highly stable class I dielectric offering a linear temperature coefficient, low loss and stable electrical properties over time, voltage and frequency.

For RF decoupling purposes select a capacitor value such that for the frequency to be decoupled is close to or just above the series resonant frequency (SRF) of the capacitor. At SRF the parasitic impedance resonates with the device capacitance to form a series tuned circuit and the impedance presented by the capacitor is the effective series resistance (ESR).

For DC blocking or coupling applications at RF, typically a capacitor with low insertion loss and a good quality factor is required. Since a capacitor's quality factor is inversely proportional to its ESR, select a capacitor with a low ESR and ensure that the SRF of the capacitor is greater than the frequency of operation. If the working frequency is above the SRF of the capacitor, it appears inductive.

Note: All the capacitors of the BlueNRG application board used for the matching network and for the crystals have to be C0G.

2.2 Inductors

An inductor is a passive electrical component used to store energy in its magnetic field. Any conductor has inductance. An inductor is typically made of wire or other conductor wound into a coil, to increase the magnetic field.

Inductors differ from each other for construction techniques and materials used to manufacture. A lot of different types of inductors exist (air core inductor, ferromagnetic core inductor, and variable inductor), but this document will focus on the inductors useful for RF only. Usually in RF the air core inductors are used. The term air core describes an inductor that does not use a magnetic core made of ferromagnetic material, but coil wound on plastic, ceramic, or another nonmagnetic form. They are lower inductance than ferromagnetic core coils but are used at high frequencies because they are free from energy losses called core losses.

Usually, the real circuit of an inductor is composed of a series resistance and a parallel capacitor. The parallel capacitor is considered to be the inter-winding capacitance that exists the turns of the inductor. If the inductor is placed over a ground plane then, this capacitance also includes the capacitance that exists between the inductor and the ground plane. The series resistor can be considered as the resistance of the inductor winding.

In term of circuit performance, as already mentioned for the capacitors, the self-resonant frequency and the quality factor are the main inductor parameters, especially for the circuit where the losses need to be minimized. At the self-resonant frequency, the inductor impedance is at maximum. For frequency above the self-resonance the inductor behavior change and it appears capacitive.

In general wire wound inductors have a higher quality factor than a multilayer equivalent. They also reflect and radiate more energy that can give rise to higher emission levels, especially in term of self-coupling. Inductive coupling can give rise to undesired circuit operation: to minimize coupling mount the inductors in sensitive circuit areas at 90 degrees to one another.

In the BlueNRG application board two different inductor types are used:

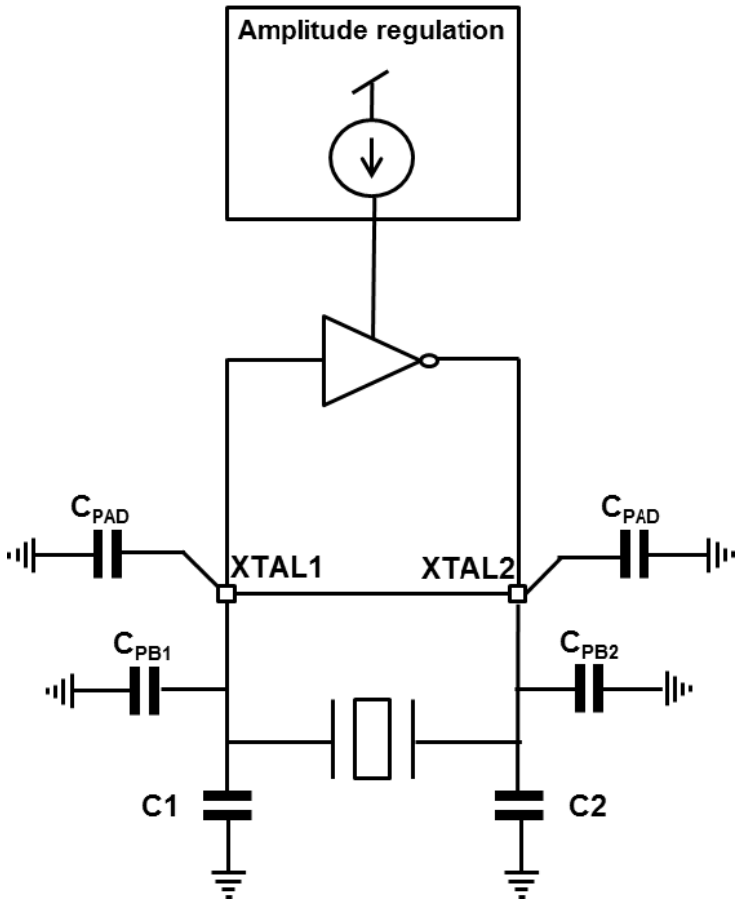
1. DC-DC converter coil: the BlueNRG supports 10 µH only, while the BlueNRG-MS supports 4.7 or 10 µH (program the desired configuration inside the IFR). The DCR has to be less than 1 ohm; the rated current has to be higher than 100 mA.
2. RF matching and filtering coil: in this case the best solutions are the high Q coils, but a good compromise between application cost versus RF performances is to choose an inductor with a medium Q.

2.3 External quarts

The BlueNRG includes a high frequency and a low-frequency integrated oscillators that required two external crystals.

The BlueNRG includes a fully integrated, low power 16/32 MHz Xtal oscillator with an embedded amplitude regulation loop. In order to achieve low power operation and good frequency stability of the Xtal oscillator, certain considerations with respect to the quartz load capacitance C0 need to be taken into account. Figure 8. Diagram of the BlueNRG amplitude regulated oscillator shows a simplified block diagram of the amplitude regulated oscillator used on the BlueNRG.

Figure 8. **Diagram of the BlueNRG amplitude regulated oscillator**



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Low power consumption and fast startup time are achieved by choosing a quartz crystal with a small load capacitance C0. A reasonable choice for capacitor C0 is 15 pF. To achieve good frequency stability, the following equation needs to be satisfied:

Equation 1

$$C_0 = \frac{C_1' * C_2'}{C_1' + C_2'}$$

Where C1'=C1+CPCB1+CPAD, C2'= C2+CPCB2+CPAD, where C1 and C2 are external (SMD) components, CPCB1 and CPCB2 are PCB routing parasites and CPAD is the equivalent small-signal pad-capacitance. The value of CPAD is around 0.5 pF for each pad. The routing parasites should be minimized by placing quartz and C1/C2 capacitors close to the chip, not only for an easier matching of the load capacitance C0, but also to ensure robustness against noise injection. Connect each capacitor of the Xtal oscillator to ground by a separate via.

Regarding the low-frequency crystal oscillator the same consideration has to be done.

It is important to underline that the BlueNRG and BlueNRG-MS integrate an internal low-frequency RC oscillator that works without external quartz. The internal low-frequency RC oscillator can be chosen as an alternative to the low-frequency crystal oscillator, which works with a 32 kHz crystal. The BlueNRG and BlueNRG-MS also integrate an internal high-frequency RC oscillator, but it is disabled after an initial system bootstrap, so it is necessary to use an external quartz for radio operations.

3 Two or multi-layer application boards

Different approach has to be taken into account when an application board is designed using the QFN32 or the WLCSP34 package.

3.1 QFN32 package

In this case the best solution is to use a two-layer application board.

Figure 9. QFN32 package application board stack-up layer

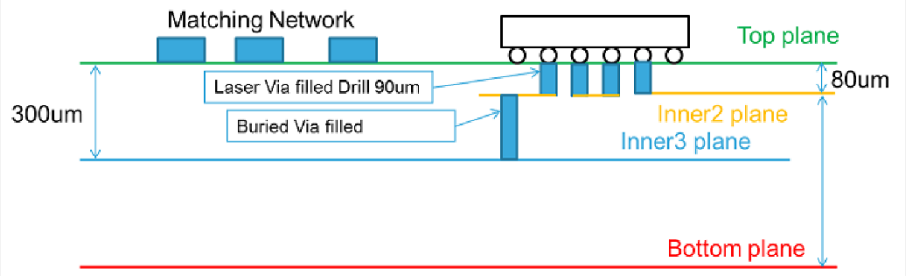
The two layers have to be so distributed:

1. TOP layer: used for routing.
2. BOTTOM layer: used for grounding under the RF zones and for routing on the rest.

3.2 WLCSP34 package

In this case, it is not possible to design a two-layer board and the stack-up layer is a multilayer due to the complexity of the package. In Figure 10. WLCSP34 package application board stack-up layer the suggested stack-up layer.

Figure 10. WLCSP34 package application board stack-up layer



In this case a four-layer solution is used. Also, a more complicated and expensive technology has to be used to connect the tracks to the internal balls. The four layers have to be distributed as follows:

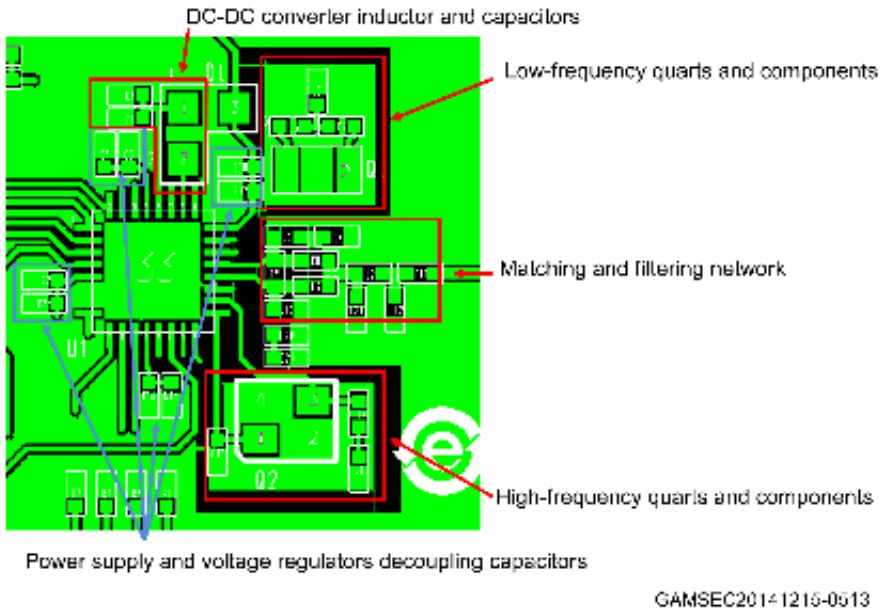
1. TOP layer: used for routing
2. INNER2 layer: used for routing
3. INNER3 layer: used only for ground
4. BOTTOM layer: used for routing

The filled laser vias and the buried vias have to be used in this case. The thickness between the TOP layer and the INNER2 layer has to be 80 um. The thickness between the TOP layer and the INNER3 layer has to be 300 um. The thickness between the INNER3 layer and the BOTTOM layer can be chosen according to the customer necessity.

4 Design recommendations when using QFN32 package

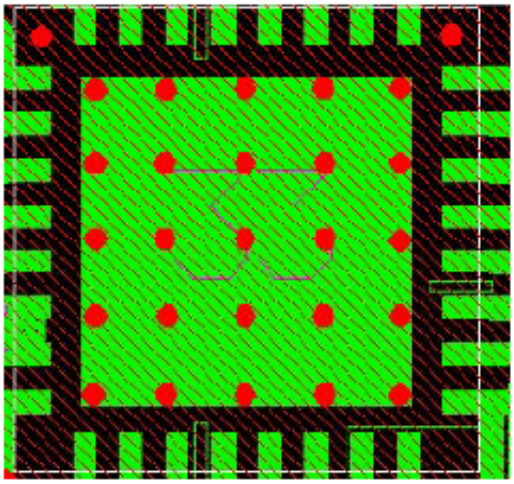
The application board TOP layer layout using the QFN32 package is shown in Figure 11. QFN32 package application board TOP layer.

Figure 11. QFN32 package application board TOP layer



It is crucial to connect very well the ground of the exposed pad of the QFN32 to the ground on the application board. So many vias are necessary to be sure that the parasitic inductor introduced from each via is negligible.

Figure 12. Vias on the exposed pad of the QFN32 package



The ground of the two external crystals has to be isolated from the ground of the RF part of the board. This is because the RF ground is “dirty” and this signal can disturb the correct functionality of the two crystals. Also to reduce the coupling effects some cunning have to be taken: In the high-frequency crystal the load capacitor of the FXTAL0, pin 18, has to be connected to ground in series with an inductor (see Figure 13. High-frequency crystal inductor); In the low-frequency crystal the ground part of two load capacitors have to be connected together and,

after, connected to the ground by an inductor. The two tracks that connect the low-frequency crystal to the SXTAL0 and SXTAL1, pins 23 and 22, have to be put in a layer different from the TOP.

Figure 13. High-frequency crystal inductor

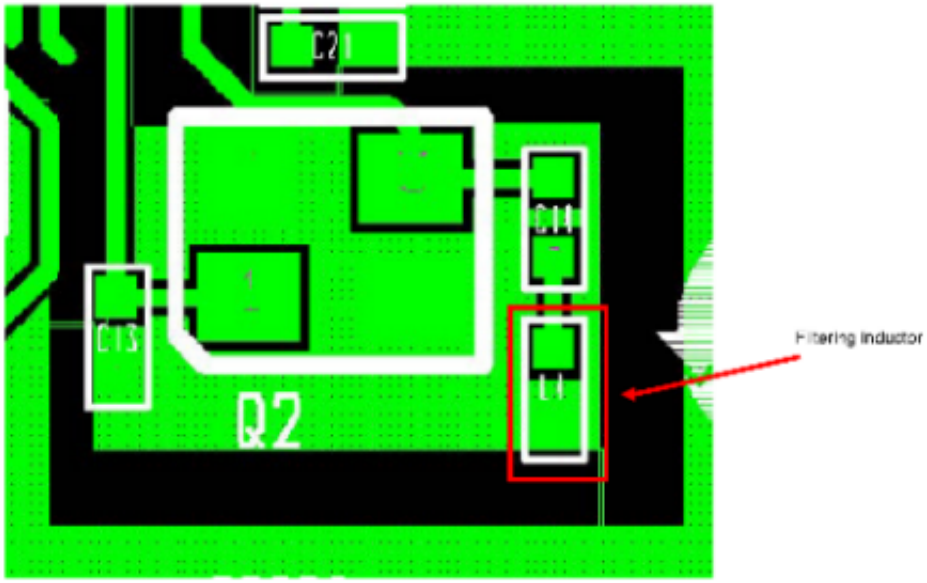
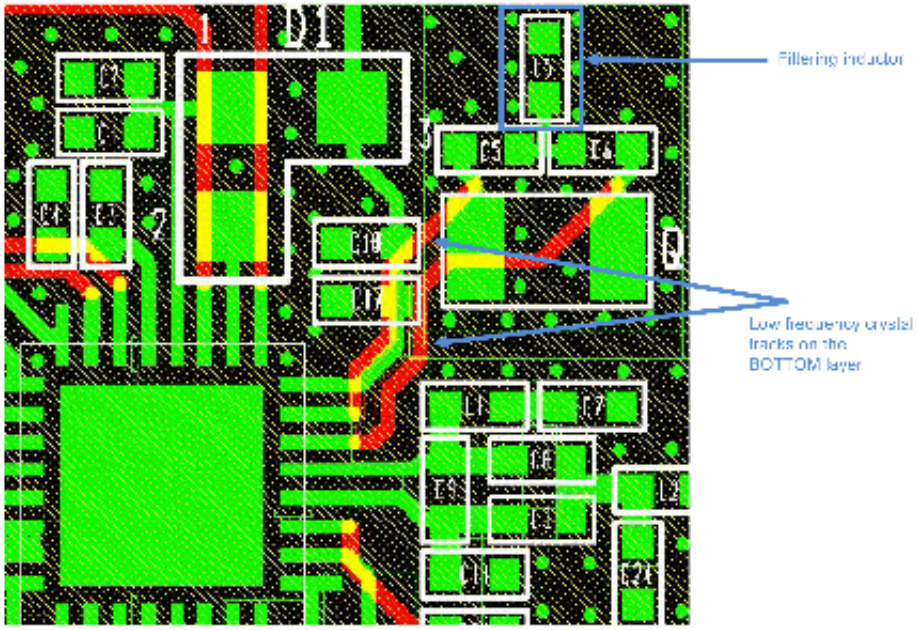
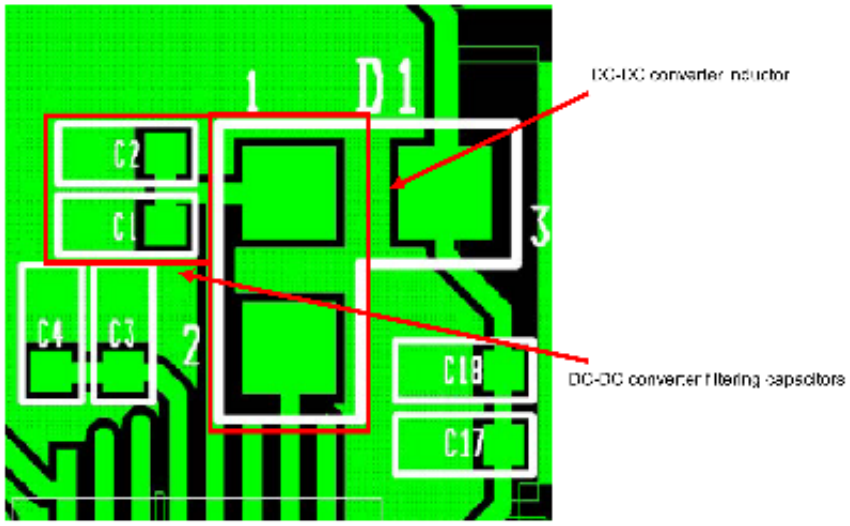


Figure 14. Low-frequency crystal inductor and tracks



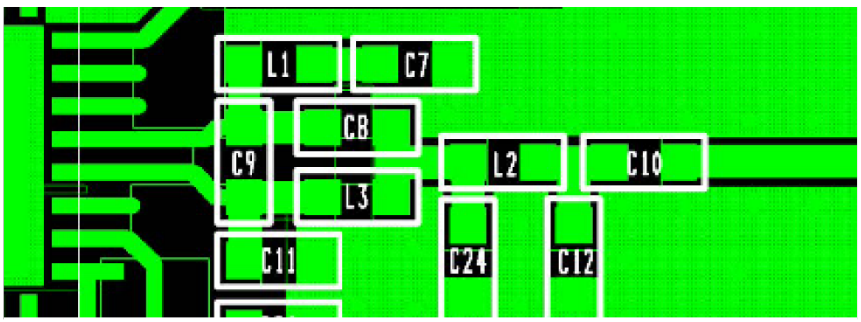
The DC-DC converter area is very sensitive, and it is necessary to pay attention to the layout of this part. This is because the DC-DC converter generates GND noise that can get coupled on surrounding ground reducing the sensitivity, and high-frequency components can be coupled onto RF part. So to ensure a correct layout it is necessary of: Providing efficient filtering by placing capacitors as close as possible from the BlueNRG; Reducing parasitic ensuring wide and short connections to BlueNRG. In Figure 15. DC-DC converter layout zone the suggested layout is shown DC-DC converter inductor DC-DC converter filtering capacitors

Figure 15. **DC-DC converter layout zone**



Particular care has to be taken in the placement of the supply voltage filtering capacitors. It is, in fact, important to ensure efficient filtering placing these capacitors as close as possible from their dedicated pins on the BlueNRG. The TX/RX part of the BlueNRG is a very sensitive part. The discrete balun has to be placed as close as possible to the TX/RX pins. The traces that connect the RF pins to the balun network (differential trace) should be of equal length. If the two differential signals are unbalanced, common-mode issues can be generated. The differential traces have to be routed firmly together. Differential receivers are designed to be sensitive to the difference between a pair of inputs, but also to be insensitive to a common-mode shift of those input. Therefore, if any external noise is coupled equally into the differential traces, the receiver will be insensitive to this (standard mode coupled) noise. More closely differential traces are routed together, more equal will any coupled noise be on each trace, therefore better will be the rejection of the noise in the circuit.The parallel inductors in the balun (and in general) should be mutually perpendicular to avoid mutual couplings. If no perpendicular position is possible, turn away their interposing capacitors or resistors.The interconnections between the elements are not considered transmission lines because their lengths are much shorter than the wavelength and, thus, their impedance is not critical. As results, their recommended width is smallest possible. In this way, the parasitic capacitances to ground can be minimized.

Figure 16. **Discrete balun layout zone**

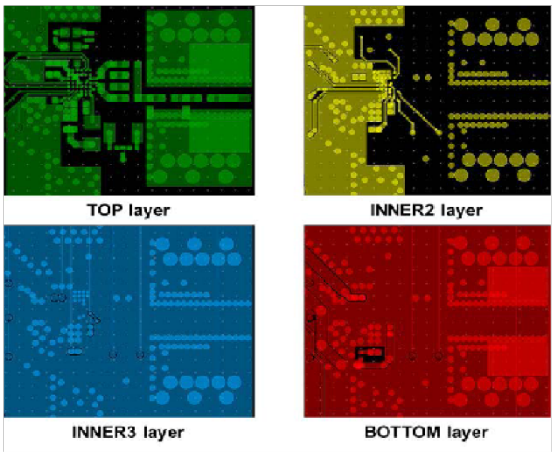


An application board using an integrated balun was also designed . The integrated balun was developed internally to STMicroelectronics and can be used only with the BlueNRG/MS device. It is mandatory to follow the layout rules described in the balun datasheet (BALF-NRG-01D3).

5 Design recommendations when using WLCSP34 package

The application board for the WLCSP34 package was designed in a four-layer due the more complexity to treat the CSP package. The print of the four layers is shown in Figure 17. WLCSP34 four-layer board.

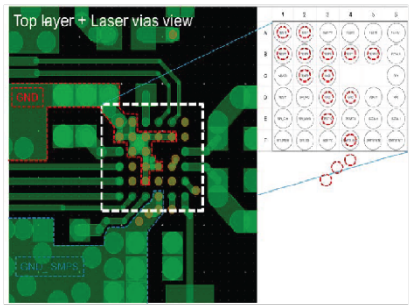
Figure 17. WLCSP34 four-layer board



A good ground connection is essential for the RF performances. This point is important for all RF devices in all packages, but it is critical in a CSP package due to the reduced dimension of the device. A good ground connection, that means low resistance between the ground balls of the device and the ground layer, produces a low cross talk among critical blocks that means RF performance not impacted.

The ground connection of the BlueNRG in WLCSP package on the TOP layer is shown in Figure 18. WLCSP34 ground connection (TOP layer view). Laser vias are used to connect TOP layer ground and INNER2 layer ground. The ground laser vias have to be put under GND balls, under the GND_SMPS ball and under the unused balls. In the TOP layer the GND_SMPS has to be kept separated from the GND.

Figure 18. WLCSP34 ground connection (TOP layer view)

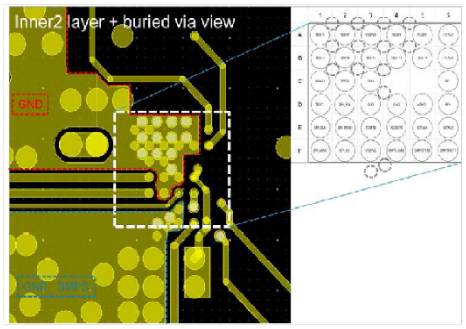


In the INNER2 layer, Figure 19. WLCSP34 ground connection (INNER2 layer view), buried filled vias have to be used to connect INNER2 layer ground and INNER 3 layer ground. The buried filled vias have to be put with 400 um of offset (both in x and y directions) respect to laser vias.

In the INNER2 layer the GND_SMPS has to be kept separated from the GND.

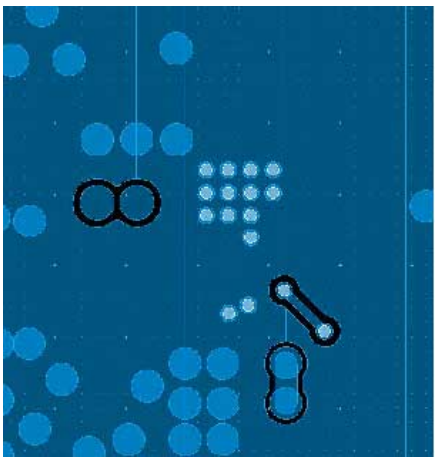
It is necessary not put ground layer under the RF discrete balun. This is because due to the very little distance between TOP and INNER2 layers; 80 um, the parasitic capacitances would be too big and would not be possible to find a working solution of the matching network.

Figure 19. WLCSP34 ground connection (INNER2 layer view)



In the INNER3 layer, Figure 20. WLCSP34 ground connection (INNER3 layer view), GND and GND_SMPS have to be connected together. This layer has to be kept as continue as possible to obtain a good ground that means less noise.

Figure 20. WLCSP34 ground connection (INNER3 layer view)



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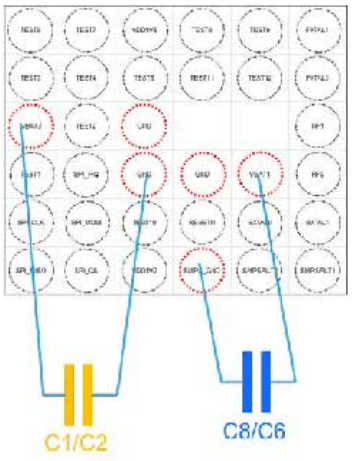
To guarantee the RF performances with the DC-DC converter ON it is important to have an effective filtering between VBAT1 and SMPS_GND pins. This filtering is obtained using some filtering capacitors are shown in Figure 21. Focus on power supply pins. The C6 and C8 capacitors between the VBAT1 and the SMPS_GND have to be put as close as possible to the WLCSP. The width of the connection tracks has to be increased as much as possible. The TOP layer or the INNER2 layer has to be used to route these tracks.

Figure 21. Focus on power supply pins



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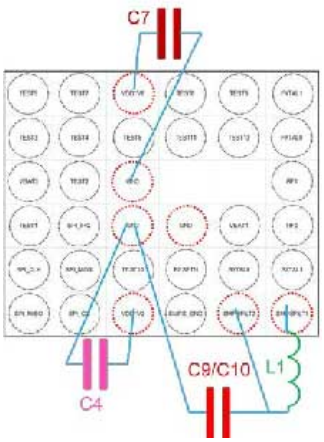
To guarantee the RF performances with the DC-DC converter ON it is important also to have an effective filtering between SMPSFILT2 and GND pins. This filtering is obtained using some filtering capacitors are shown in Figure 22. Focus on BlueNRG biasing pins. The C9 and C10 capacitors between the SMPSFILT2 and the GND have to be put as close as possible to the WLCSP. The width of the connection tracks has to be increased as much as possible. The TOP layer or the INNER2 layer has to be used to route these tracks. The L1 inductor has to be also put as close as possible to the BlueNRG device.

The capacitors C4 and C7 to filter the VDD_1V2 and VDD_1V8 balls have to be also put as near as possible to the device.

Figure 22. Focus on BlueNRG biasing pins



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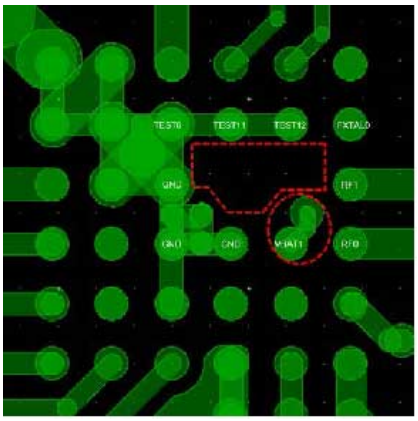
On TOP layer avoid putting metal inside the red zone. This zone is very sensible to the ground layer and the presence of a metal plane can affect the operation of the device.

The VBAT1 connection is improved using two laser filled vias.

Figure 23. Other TOP layer constraints



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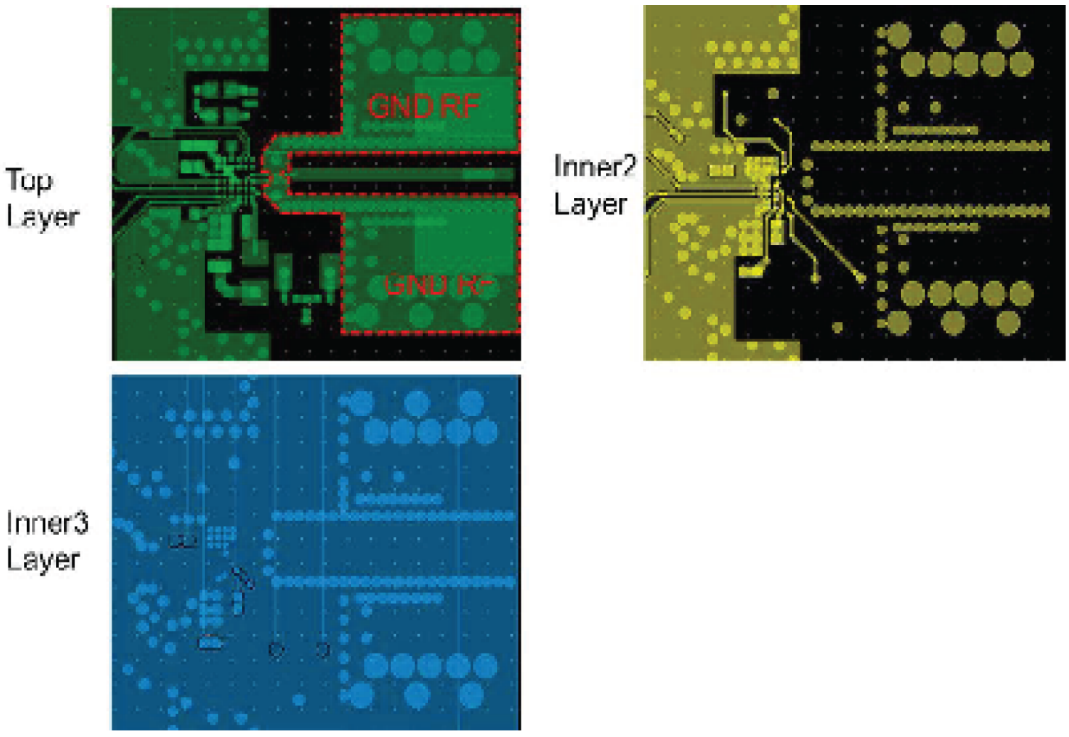
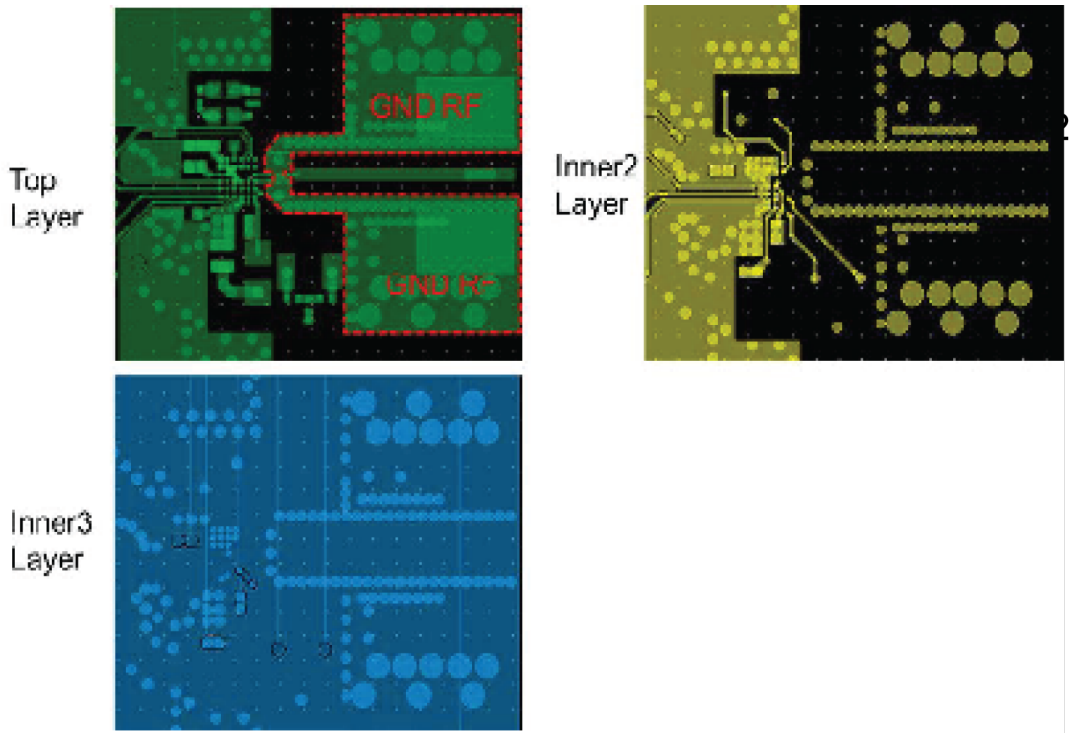
The RF ground in the TOP layer is “hot” so it could generate pulling power. To avoid this risk, it is necessary to not merge the RF ground to the others ground on the TOP and INNER2 layers, but merge all the different grounds in the INNER3 layer.

Figure 24. RF ground on the discrete balun application board



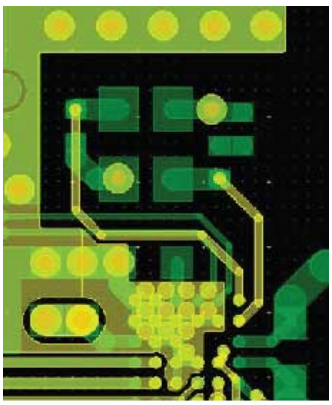
To design the board with the integrated balun as matching network all the above suggestions has to be implemented. The only difference is located in the balun zone where the datasheet recommendation has to be followed. Particular attention to the ground must be observed: also in this case the RF ground in the TOP layer is “hot” and it could generate pulling. The RF TOP layer ground has to be extended to the balun zone (see Figure 25. RF ground on the integrated balun application board), but has to be merged to the other ground on the INNER3 layer.

Figure 25. **RF ground on the integrated balun application board**



The high-frequency crystal has to be put as far as possible from the matching network. The tracks that connect the crystal pins to the BlueNRG FXTAL0 and FXTAL1 pins have to be routed as far as possible from the matching network, and also have to be kept as far as possible one from each other. The INNER2 layer has to be used to connect the crystal pins to the BlueNRG FXTAL0 and FXTAL1 pins. The INNER2 layer has to be keeping empty under the crystal. All these recommendations are shown in Figure 26. High-frequency crystal connection.

Figure 26. **High-frequency crystal connection**



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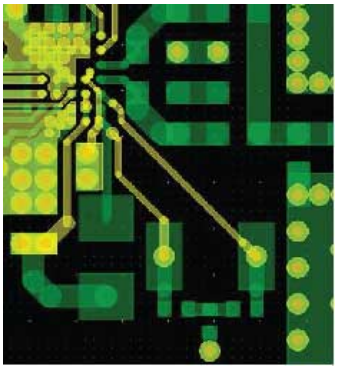
The low-frequency crystal has to be put as far as possible from the matching network. The tracks that connect the crystal pins to the BlueNRG SXTAL0 and SXTAL1 pins have to be routed as far as possible from the matching network, and also have to be kept as far as possible one from each other. The INNER2 layer has to be used to connect the crystal pins to the BlueNRG FXTAL0 and FXTAL1 pins. The INNER2 layer has to be keeping empty under the crystal. All these recommendations are shown in Figure 27. Low-frequency crystal connection.

Figure 27. Low-frequency crystal connection



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The DC-DC converter inductor has to be placed as close as possible to the BlueNRG. The INNER2 layer has to be kept empty under the DC-DC converter inductor. All these recommendations are shown in Figure 28. DC-DC converter inductor connection.

Figure 28. DC-DC converter inductor connection

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6 References

References

[1] BlueNRG datasheet
[2] BlueNRG-MS datasheet
[3] BALF-NRG-01D3 datasheet

Revision history

Table 2. **Revision history**

Date	Version	Changes
15-Jan-2015	1	Initial release.
20-Jul-2018	2	Updated Section 2.2 Inductors. Minor text changes.

Contents

List of figures