AN4685
Application note

12 V, 10 W isolated flyback converter based on VIPer25HD

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Introduction

This document describes the STEVAL-ISA162V1, a 12 V - 10 W power supply in isolated flyback topology with VIPer25HD, a new off line high voltage converter by STMicroelectronics, specifically designed to build quasi-resonant flyback converters.

The main features of the device are: 800 V avalanche rugged power section, PWM control, cycle by cycle current limit with adjustable set point, on board soft start and safe auto restart after a fault condition.

The available protections are: thermal shutdown with hysteresis, two levels of overcurrent protection, overvoltage and overload protections.

The present flyback converter is suitable for different applications. It can be used as an external adapter or as an auxiliary power supply in consumer equipment.

Figure 1. Evaluation board image: power supply board. Top layer

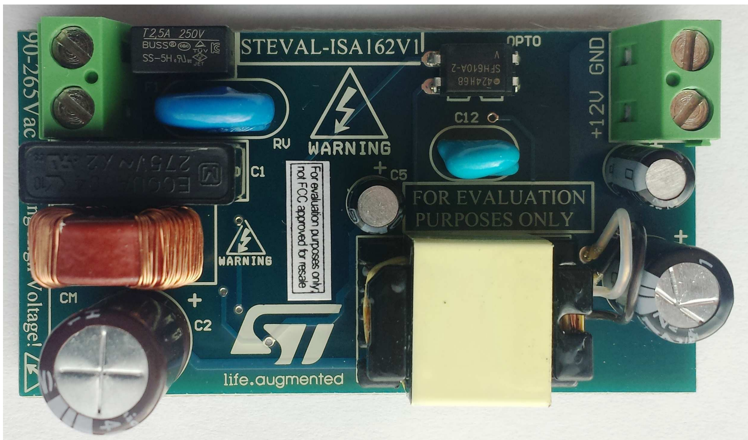
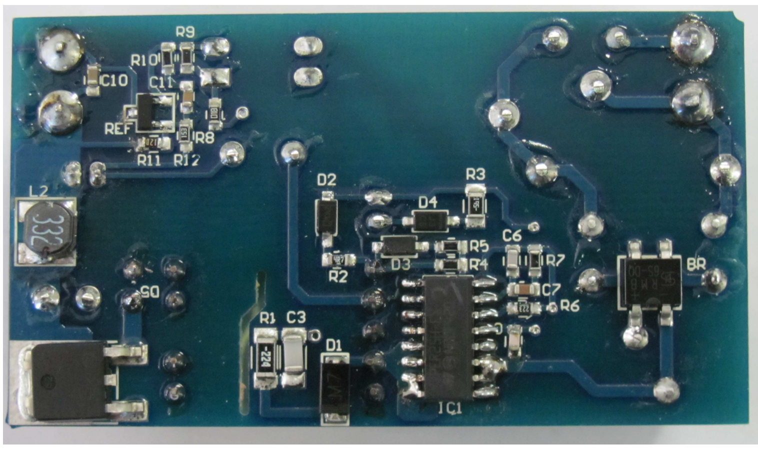


Figure 2. Evaluation board image: power supply board. Bottom layer



Contents

1 Test board: design and evaluation

The electrical specifications of the evaluation board are listed in *Table 1*.

Table 1. Electrical specifications

Parameter	Min.	Typ.	Max.	Unit
AC main input voltage	90		265	V_{AC}
Main frequency (f_L)	50		60	Hz
Output voltage	11.4	12	12.6	V
Output current			0.84	A
Output ripple voltage			50	mV
Rated output power		10		W
Standby input power @230 V_{AC}			40	mW
Active mode efficiency	83			%
Active mode at 10% load efficiency	73			%
Ambient operating temperature			60	ºC

The power supply is set in isolated flyback topology. The schematic is given in *Figure 3*, the bill of materials (BOM) in *Table 2*. Input section includes a diode bridge (BR), an X-capacitor (C1) for differential EMC suppression and a CM choke for common mode EMC suppression.

A clamp network (D1, R1, C3) is used for leakage inductance demagnetization.

The ZCD pin is responsible for the quasi resonant operation, being a transformer demagnetization sensing input triggering the MOSFET turn-on. A small LC filter has been added at the output in order to filter the high frequency ripple.

Figure 3. Electrical schematic

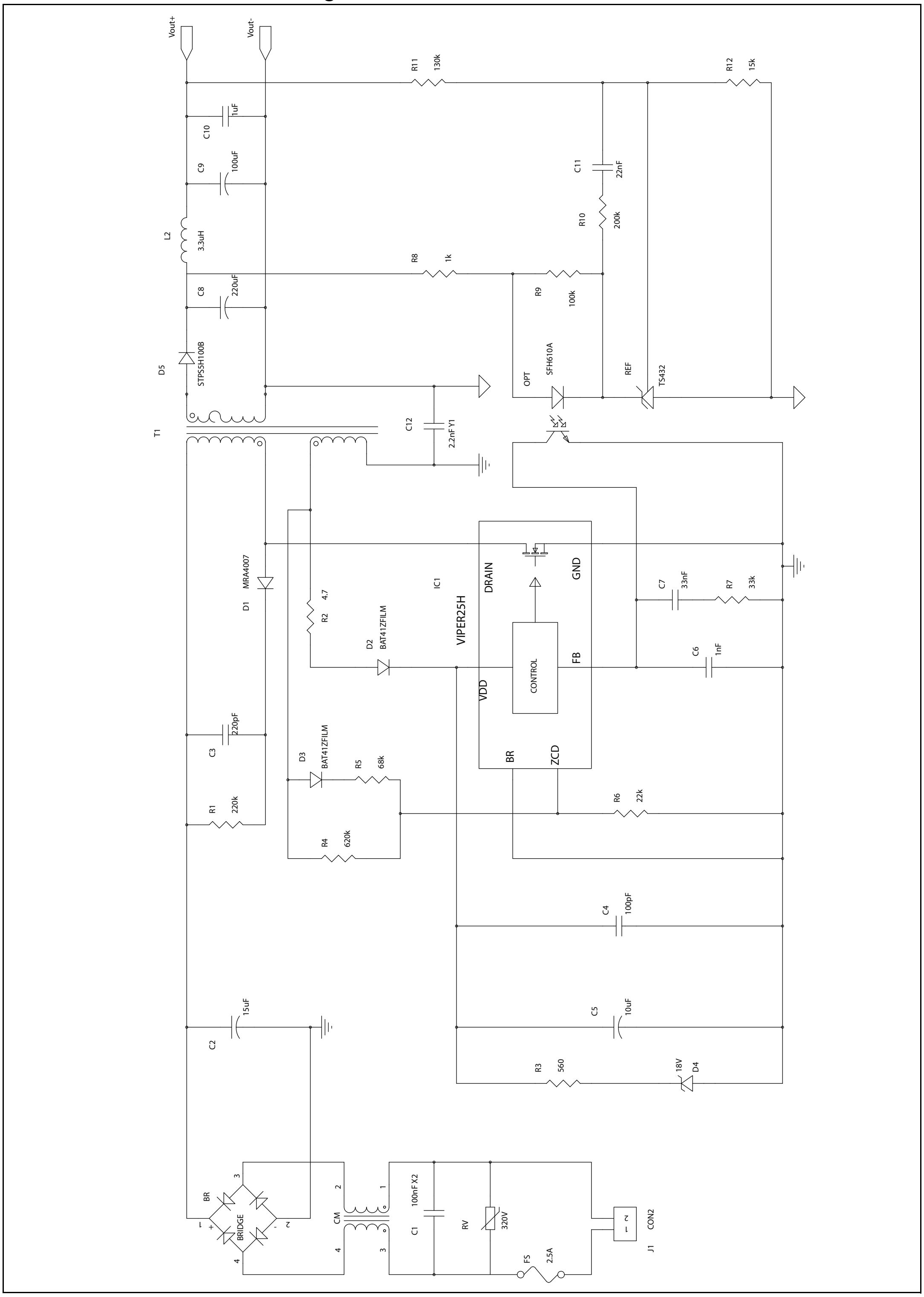


Table 2. Bill of material (BOM)

Reference	Part	Description	Note
BR	RMB6S	0.8 A - 600 V Bridge	Taiwan Semiconductor
RV	B72210S0321K101	Varistor - 320 V	EPCOS
FS	SS-5H-2-5A-BK	2.5 A - Fuse	Cooper Bussmann
R1	ERJ-P08J224V	220 kΩ - 0.33 W - 200 V Resistor	5% tolerance
R2	ERJ3RQF4R7V	4.7 Ω - 1/10 W Resistor	1% tolerance
R3	ERJT06J561V	560 Ω - 0.25 W Resistor	5% tolerance
R4	ERJP03F6203V	620 kΩ - 0.2 W Resistor	1% tolerance
R5	ERJP03F6802V	68 kΩ - 0.2 W Resistor	1% tolerance
R6	ERJP03F2202V	22 kΩ - 0.2 W Resistor	1% tolerance
R7	ERJP03F3302V	33 kΩ - 0.2 W Resistor	1% tolerance
R8	ERJ3GEYJ102V	1k Ω - 1/10 W Resistor	5% tolerance
R9	ERJP03F1003V	100 kΩ - 0.2 W Resistor	1% tolerance
R10	ERJP03F2003V	200 kΩ - 0.2 W Resistor	1% tolerance
R11	NTR06B1303CTR1KF	130 kΩ - 0.063 W Resistor	0.1% tolerance
R12	ERA3AEB153V	15 kΩ - 0.1 W Resistor	0.1% tolerance
C1	ECQUAAF104M	100 nF - 275 V Capacitor X2	Panasonic
C2	UVC2G150MPD	15 µF - Electrolytic capacitor 400 V	Nichicon
C3	GRM31A5C2J221JW01D	220 pF - Capacitor 630 V	Murata
C4	VJ0603A101JNAAO	100 pF - Capacitor 50 V	Vishay
C5	ECEA1VKS100	10 µF - Electrolytic capacitor 35 V	Panasonic
C6	GRM1885C1H102FA01D	1nF - Capacitor 50 V	Murata
C7	GRM188R71H333KA61D	33 nF - Capacitor 50 V	Murata
C8	25ZLG220MEFC8X11.5	220 µF - Electrolytic capacitor 25 V	Rubycon
C9	25YXJ100M5X11	100 µF - Electrolytic capacitor 25 V	Rubycon
C10	GRM188C81E105KAADD	1µF - Capacitor 25V	Murata
C11	GRM188R71H223KA01D	22 nF - Capacitor 50 V	Murata
C12	DE2E3KY222MA2BM01	2.2 nF - 250 V Capacitor X1/Y2	Murata
D1	MRA4007T3G	General purpose diode 1 A - 1000 V	Onsemi
D2, D3	BAT41ZFILM	Signal Schottky 0.2 A - 100 V	STM
D4	MMSZ5248B-V-GS08	Zener diode 18 V - 0.5 W	Vishay
D5	STPS5H100B	Power Schottky 100 V-5 A	STM
L2	SD43-332ML	3.3 µH – Power inductor	Coilcraft
CM	744821120	20 mH CM CHOKE	Wurth Elektronik
IC	VIPer25HD	Offline primary controller	STM

Table 2. Bill of material (BOM)

Reference	Part	Description	Note
OPT	SFH610A-2	Optocoupler	Vishay
REF	TS432ILT	Reference	STM
T1	YJ-310V600310	Flyback transformer	Yujingtech

The transformer characteristics are listed in the table below.

Table 3. Transformer characteristics

Parameter	Value
Manufacturer	Yujing Technology CO. LTD.
Part number	YJ-310V600310
Primary inductance	1.5 mH ± 10%
Leakage inductance	40 µH Max
Primary turns (N1+N3)	85
Secondary turns (N2)	15
Auxiliary turns (N4)	16
Core	EEE-13V
Ferrite	3C96 Ferroxcube

Figure 4. Dimensional drawing and pin placement diagram - bottom view

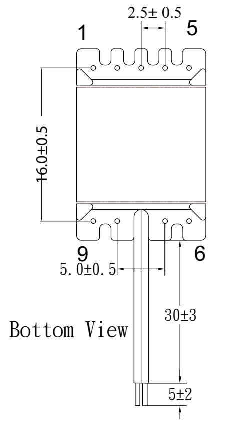


Figure 5. Dimensional drawing and pin placement diagram - electrical diagram

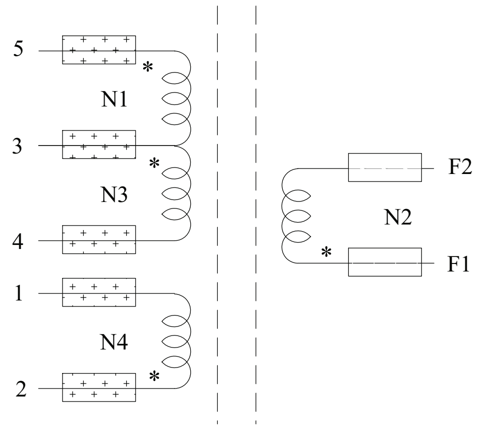
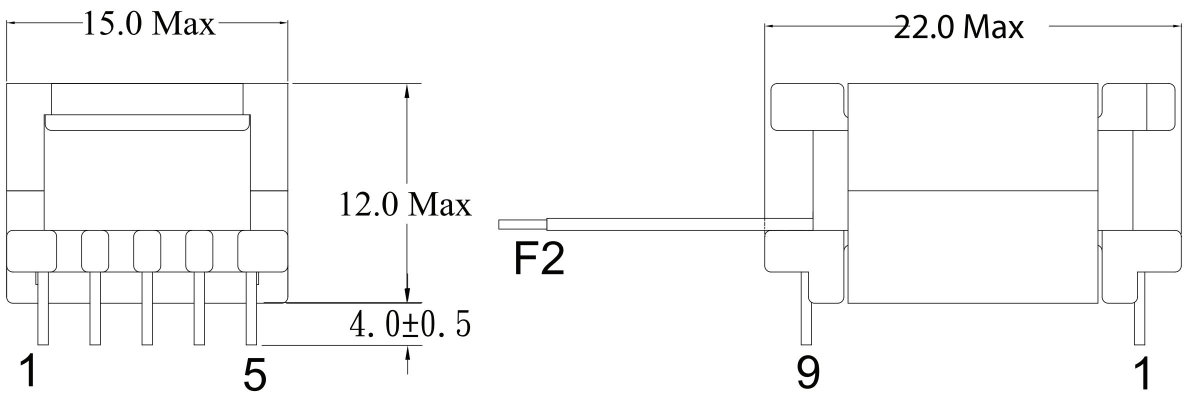


Figure 6. Dimensional drawing and pin placement diagram - side view



1.1 Output voltage characteristics

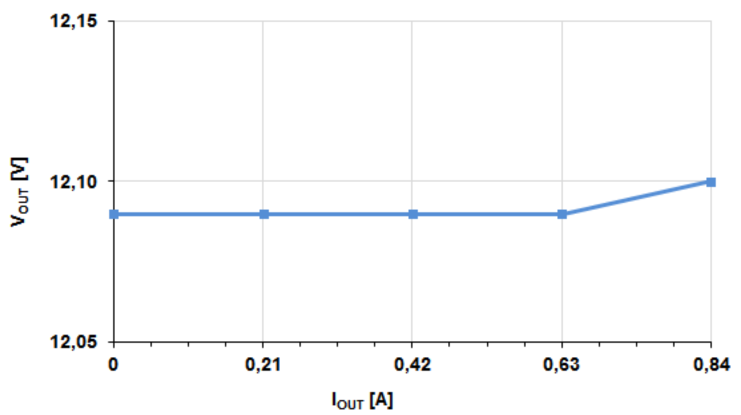
The output voltage of the board is measured in different line and load conditions. *Table 4* shows the results: the output voltage variation is negligible versus load and line variation.

As output voltage is low affected by line variations, just the load regulation at 230 V_{AC} is reported in *Figure 7*.

Table 4. Output voltage line-load regulation

V_{IN} [V_{AC}]	V_{OUT} (V)				
	No Load	0.21 A	0.42 A	0.63 A	0.84 A
90	12.09	12.09	12.09	12.09	12.10
115	12.09	12.09	12.09	12.09	12.10
150	12.09	12.09	12.09	12.09	12.10
180	12.09	12.09	12.09	12.09	12.10
230	12.09	12.09	12.09	12.09	12.10
265	12.09	12.09	12.09	12.09	12.10

Figure 7. Output voltage load regulation at 230V_{AC}



1.2 Efficiency measurements

Any external power supply (EPS) must be capable to meet the international regulation agency limits. The European code of conduct (EC CoC version 5) limit is taken as reference.

Since this power supply is considered a no low voltage power supply, the formula to calculate the minimum average efficiency is:

Table 5. EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies), Tier 2 (1 January 2016)

Nameplate output power (Pno)	Minimum average efficiency (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.5 *Pno+0.169
> 1 to ≤ 49 watts	≥ [0.071* ln (Pno)]-0.00115*Pno+ 0.670
> 49 watts	≥ 0.890

According to the above table, the minimum average efficiency is 82.25%, measured as average of the efficiencies at 25%, 50%, 75% and 100% of the rated output power at both 115V_{AC} and 230V_{AC}.

Another requirement is the efficiency measured at 10% of the rated output power, according to the below table:

Table 6. EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies) at 10% maximum output load, Tier 2 (1 January 2016)

Nameplate output power (Pno)	Minimum average efficiency (expressed as a decimal)
0 to ≤ 1 watt	≥ 0.5 *Pno+0.060
> 1 to ≤ 49 watts	≥ [0.071* In (Pno)]-0.00115*Pno+ 0.570
> 49 watts	≥ 0.790

For the considered application the minimum efficiency is 72.25%.

Table 7 to *Table 9* show all the efficiency measurement results.

Table 7. Average efficiency at 115 V_{AC}

%Load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.21	12.09	2.958	2.538	85.80
50%	0.42	12.09	5.845	5.078	86.88
75%	0.63	12.09	8.816	7.617	86.40
100%	0.84	12.10	11.900	10.164	85.41
Average efficiency					**86.12**

Table 8. Average efficiency at 230 V_{AC}

%Load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
25%	0.21	12.09	3.140	2.538	80.83
50%	0.42	12.09	6.103	5.078	83.20
75%	0.63	12.09	8.902	7.617	85.57
100%	0.84	12.10	11.810	10.164	86.06
Average efficiency					**83.92**

Table 9. Average efficiency at 10% of the max output load

V_{IN} [V_{AC}]	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency (%)
115	0.084	12.09	1.198	1.015	84.72
230	0.084	12.09	1.279	1.015	79.36

Figure 8. Efficiency vs. output current load

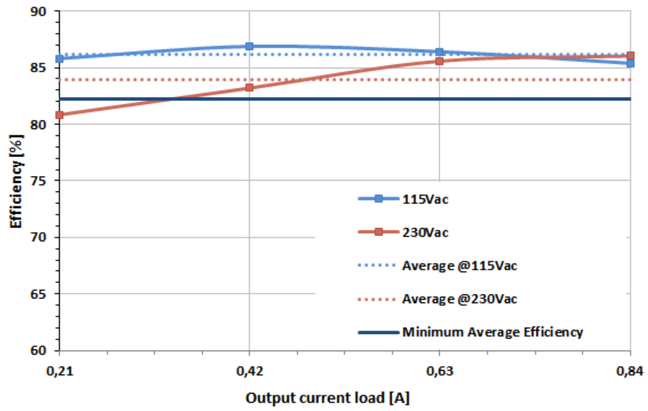
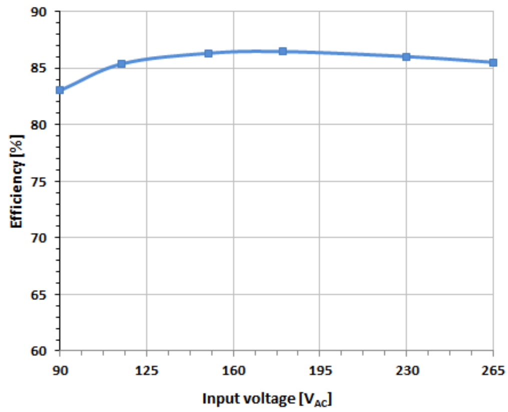


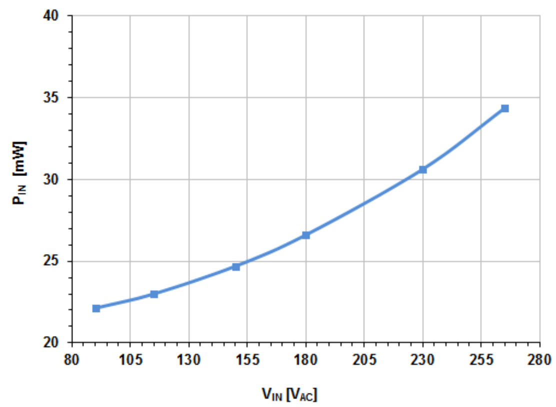
Figure 9. Efficiency (@ full load) vs. Input voltage



1.3 No load consumptions

The input power of the converter has been measured in no load, in this condition the converter works in burst mode so that the average switching frequency is reduced, thus minimizing the frequency related losses.

Figure 10. No load consumptions vs. input voltage



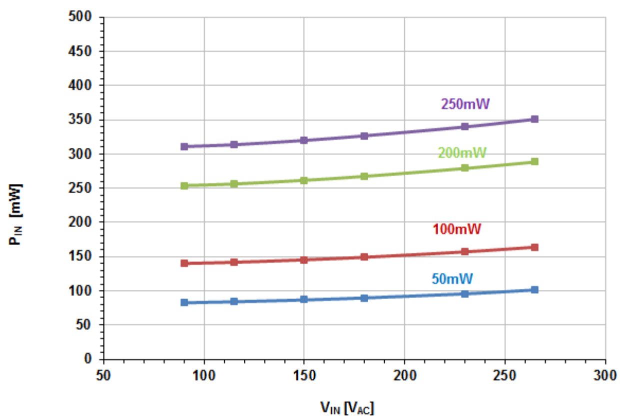
1.4 Light load consumption

Although the EC CoC hasn't other requirements regarding light load performance, in order to give quite complete information, the input power of the evaluation board in light load conditions is reported.

In particular, in order to be complying with EuP Lot 6, the EPS requires an efficiency higher than 50% when the output load is 250 mW.

The presented demo meets also this requirement.

Figure 11. Light load consumptions at different output power



2 Typical board waveforms

The drain voltage and current waveforms in full load condition are reported for minimum and maximum input voltage in *Figure 12* and *Figure 13*, and for the two nominal input voltages in *Figure 14* and *Figure 15* respectively.

Figure 12. Drain current and voltage at full load at 90 V_{AC}

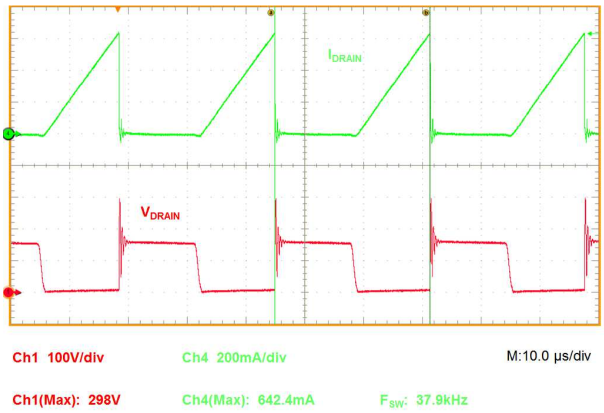


Figure 13. Drain current and voltage at full load at 265 V_{AC}

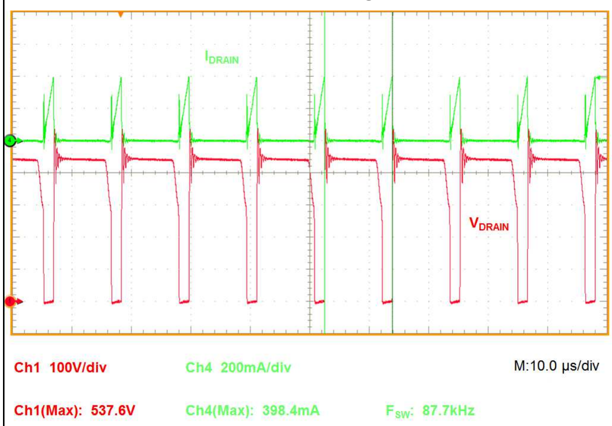


Figure 14. Drain current and voltage at full load at 115 V_{AC}

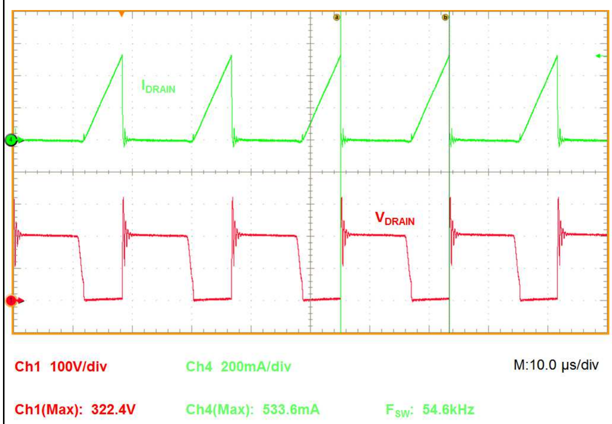
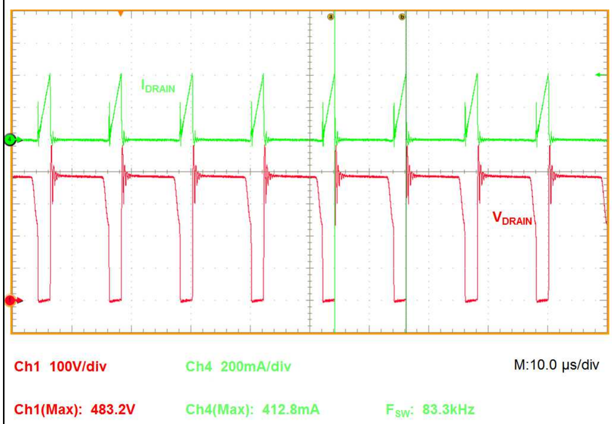


Figure 15. Drain current and voltage at full load at 230 V_{AC}



The output ripple at the switching frequency was also measured. The board is provided with LC filter, for further reduce the ripple without reducing the overall output capacitor's ESR.

The voltage ripple across the output connector (V_{OUT}) and before the LC filter (V_{OUT_PRE}) was measured, in order to verify the effectiveness of the LC filter. The following two figures show voltage ripple at 115 V_{AC} (*Figure 16*) and at 230 V_{AC} (*Figure 17*) at full load condition.

Figure 16. Output voltage ripple at full load at 115 V_{AC}

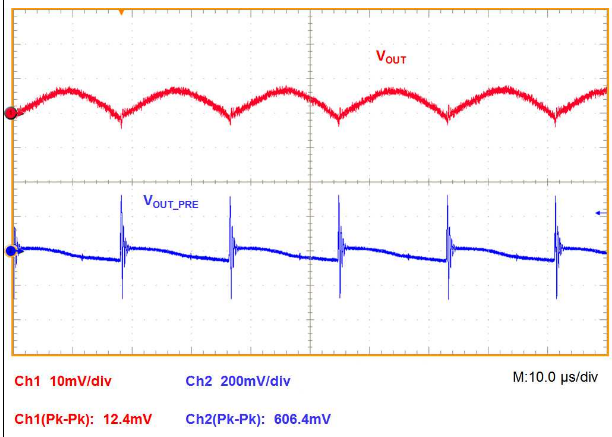
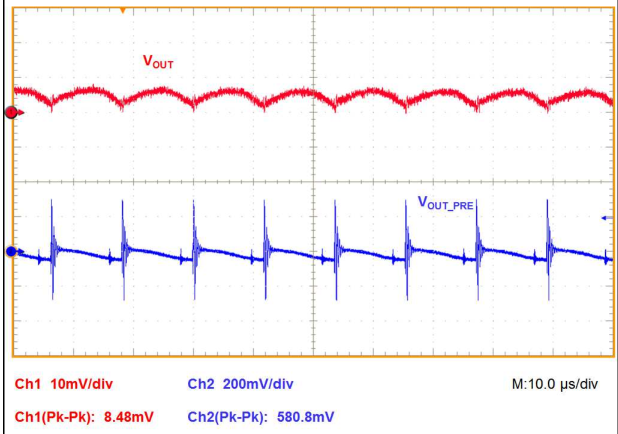


Figure 17. Output voltage ripple at full load at 230 V_{AC}



2.1 Dynamic step load regulation

In any power supply is important to measure the output voltage when the converter is submitted to dynamic load variations, in order to be sure that good stability is ensured and no overvoltage or undervoltage occurs.

The test has been performed, for both nominal input voltages, varying output load from 0 to 100% of nominal value.

In any tested conditions, no abnormal oscillations were noticed on the output and over/under shoot were well within acceptable values.

Figure 18. Dynamic step load (0 to 100% output load) at 115 V_{AC}

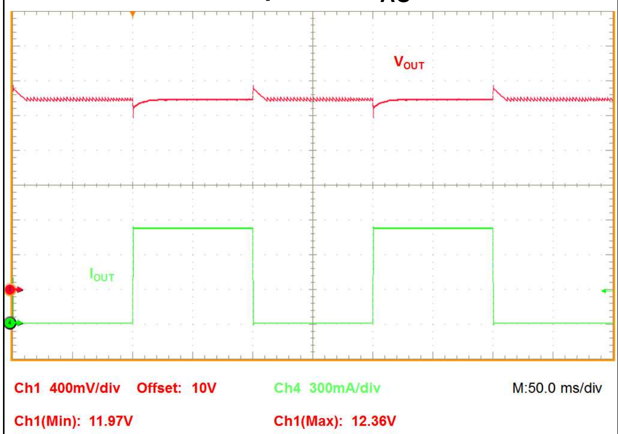
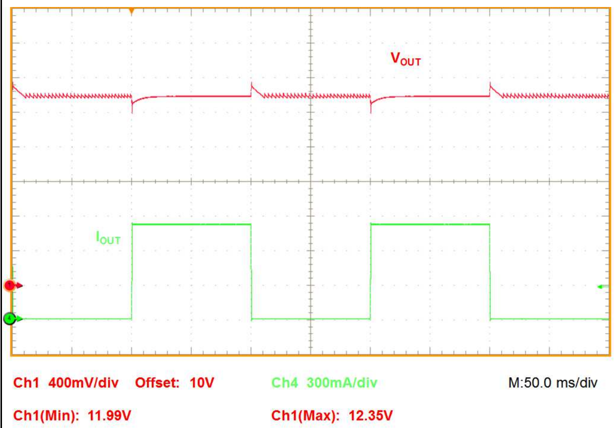


Figure 19. Dynamic step load (0 to 100% output load) at 230 V_{AC}

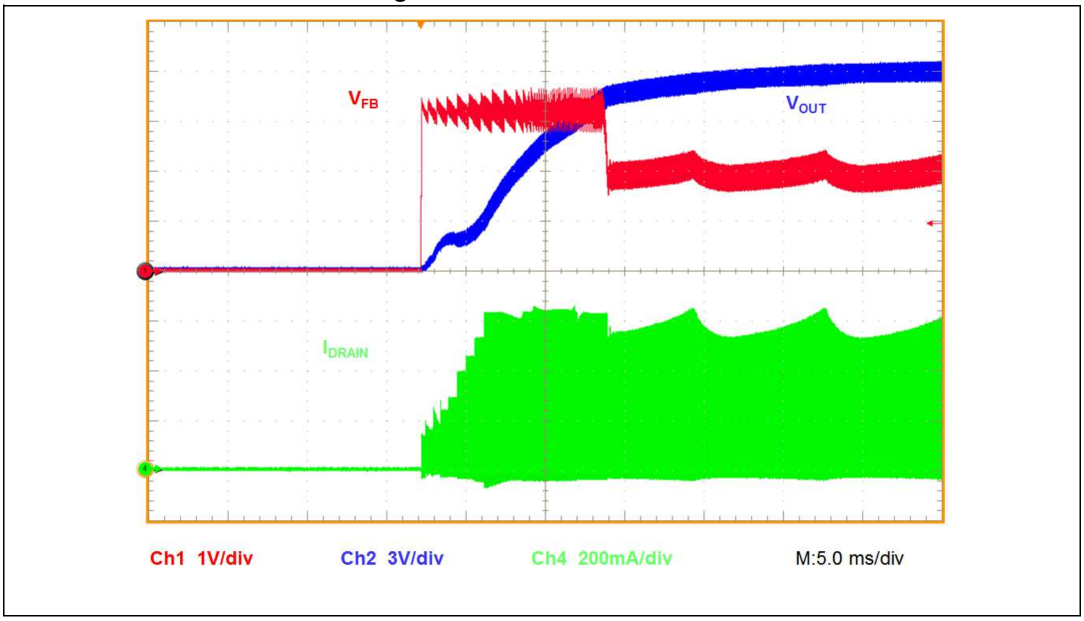


3 Soft-start

When the converter starts, the output capacitor is discharged and needs some time to reach the steady state condition. During this time, the voltage V_{ZCD} is not high enough to correctly arm the internal ZCD circuit. In this case, the power MOSFET is turned on with a fixed frequency ($F_{STARTER}$) determined by the internal oscillator. As soon as the voltage on ZCD pin is able to arm the ZCD circuit, the turn-on of the power MOSFET is driven by this circuit and is no more related to the internal oscillator.

The VIPer25 implements an internal soft-start feature. As the device starts to work, no matter the control loop request, the drain current is allowed to increase from zero to the maximum value (value that can be adjusted through an external resistor) gradually. The *Figure 20* shows the soft-start phase of the presented converter when it is operating at minimum line voltage and maximum load.

Figure 20. Soft-start feature



4 Protection features

In order to increase end-product safety and reliability, VIPer25 has some protection features: overload protection, overvoltage protection, shorted secondary rectifier detection and transformer saturation protection.

In the following sections these protections are tested and the results are presented.

4.1 Overload and short circuit protection

When the load power demand increases, the feedback loop reacts increasing the voltage on pin. In this way the PWM current set point increases and the power delivered to the output rises. This process ends when the delivered power equals the load power request.

In case of overload or output short circuit (see *Figure 21*), the voltage on FB pin reaches the V_{FBlin} value (3.3 V typical) and the drain current is limited to I_{Dlim} (or the one set by the user through the R_{LIM} resistor) by OCP comparator. In these conditions an internal current generator is activated and it charges the capacitor C7; when the voltage on FB pin reaches the V_{FBolp} threshold (4.8 V typical), the converter is turned off and is not allowed to switch again until the V_{DD} voltage falls below the $V_{DD\_RESTART}$ (4.5 V typical) and then rises to V_{DDon} (14 V typical).

Overload condition can be obtained shorting the output connector. After the V_{DD} voltage reaches the V_{DDon} value, if the short-circuit is not removed, the system starts to work in auto-restart mode (see *Figure 22*): in this case the MOSFET switches for a short period of time, where the converter tries to deliver to the output as much power as it can, and a longer period where the device is not switching and no power is processed.

As the duty cycle of power delivery is very low (around 3.92%), the average power throughput is also very low, resulting in a very safe operation.

Figure 21. Overload event, OLP triggering

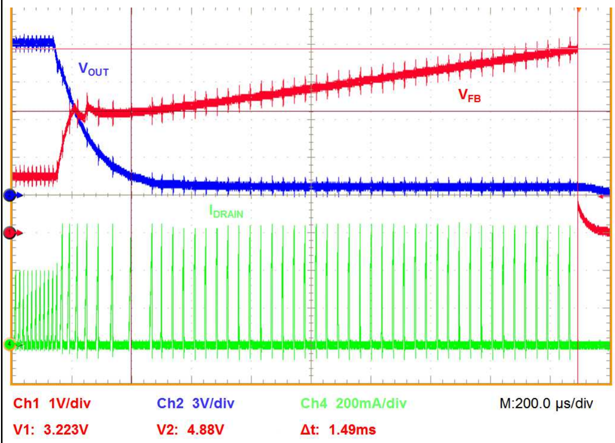
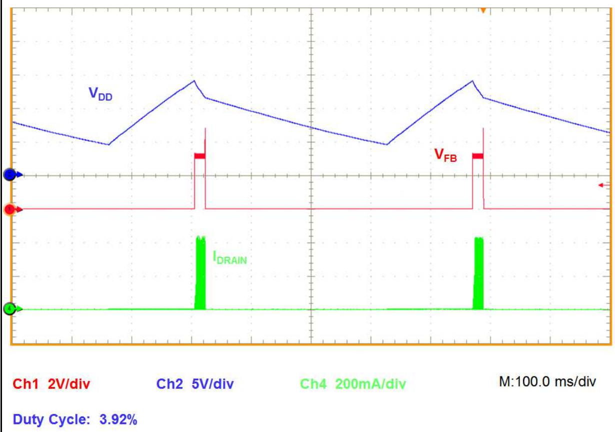


Figure 22. Overload event, continuous overload



4.2 Overvoltage protection

An output overvoltage protection is implemented monitoring the voltage across the auxiliary winding during the power MOSFET turn-off time, through the diode D3 and the resistor divider R5 and R6 connected on the ZCD pin. If this voltage exceeds the V_{OVP} (4.2 V typical) threshold, an overvoltage event is assumed and an internal counter is activated; if this event happens for four consecutive times, the controller recognizes an overvoltage condition and the device stops switching. This counter provides high noise immunity and avoids spikes erroneously tripping the protection. The counter is reset every time the OVP signal is not triggered in one oscillator cycle.

After the device has stopped switching, to re-enable operation, the V_{DD} voltage must be recycled.

The protection can be tested by opening the resistor connected to the output voltage (R11). In this way, the converter operates in open loop and the excess of power with respect to the load, charges the output capacitance increasing the output voltage until the OVP is tripped and the converter stops switching.

In *Figure 23* and *Figure 24* it is possible to see that output voltage increases, and consequentially, the ZCD pin voltage increases; as it reaches about 4.2 V the converter stops switching (at the same time the output voltage reaches about 14 V).

Figure 23. Overvoltage event

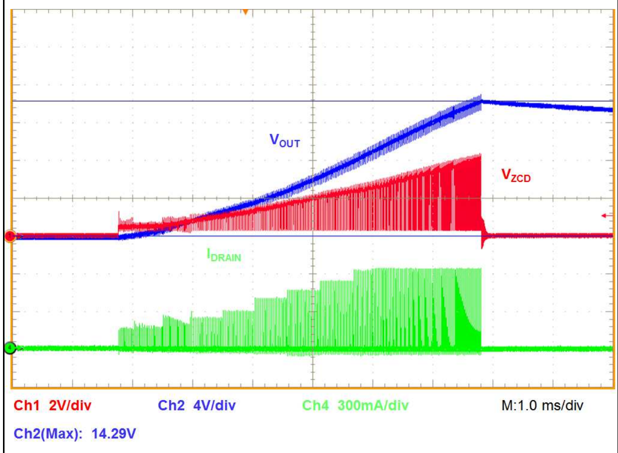
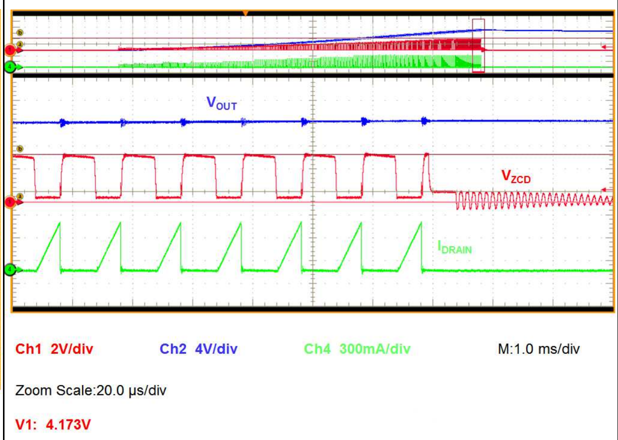


Figure 24. Overvoltage magnification



4.3 2nd level over current protection

The VIPer25 is protected against short circuit of the secondary rectifier, short circuit on the secondary windings or a hard saturation of flyback transformer. Such as anomalous condition is invoked when the drain current exceeds the threshold I_{DMAX} (1.2 A typical).

To distinguish a real malfunction from a disturbance, a warning state is entered after the first signal trip. If in the subsequent switching cycle the signal is not tripped, a temporary disturbance is assumed and the protection logic will be reset; otherwise if the I_{DMAX} threshold is exceeded for two consecutive switching cycles a real malfunction is assumed and the power MOSFET is turned off.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding; hence the V_{DD} capacitor decays till the V_{DD}

under voltage threshold (V_{DDoff}), which clears the latch. V_{DD} voltage recycles and if the fault condition is not removed the device enters in auto restart mode.

Figure 25. 2nd level over current event

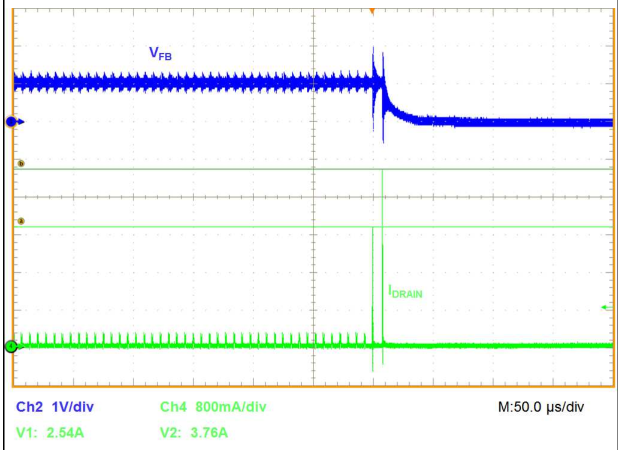
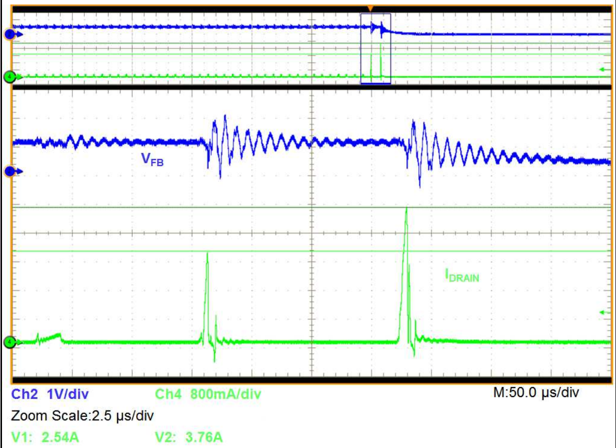


Figure 26. 2nd level over current event magnification



5 Conducted noise measurements

A pre-compliance test for the EN55022 (Class B) European normative was performed and average measurements of the conducted noise emissions at full load and nominal mains voltages are shown in *Figure 27* and *Figure 28*. As seen in the diagrams, in all test conditions there is a good margin for the measurements with respect to the limits.

Figure 27. CE average measurement at 115 V_{AC} full load

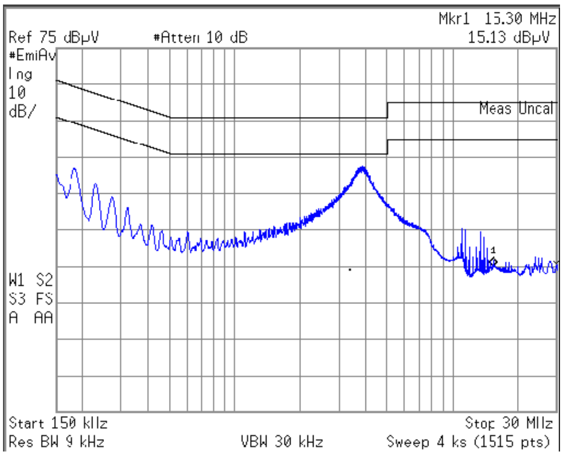
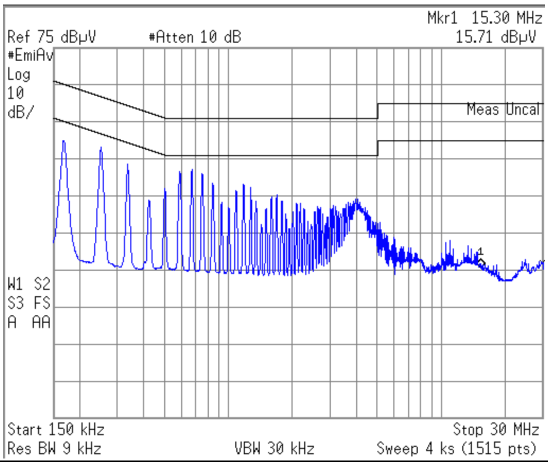


Figure 28. CE average measurement at 230 V_{AC} full load



6 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for the two nominal input voltages (115 V_{AC} and 230 V_{AC}) in full load condition. The results are shown in *Figure 29* to *Figure 32* and summarized in *Table 10*.

Figure 29. Thermal map at 115 V_{AC} full load. Bottom layer

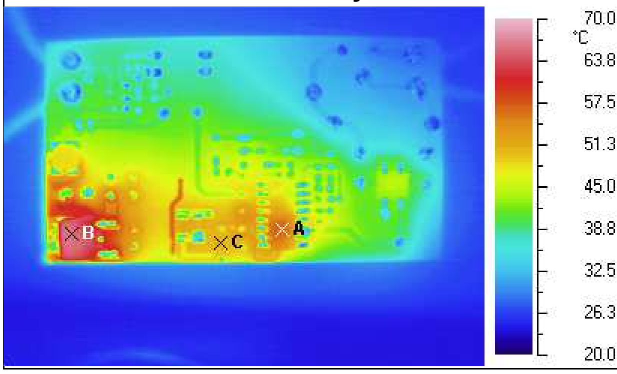


Figure 30. Thermal map at 115 V_{AC} full load. Top layer

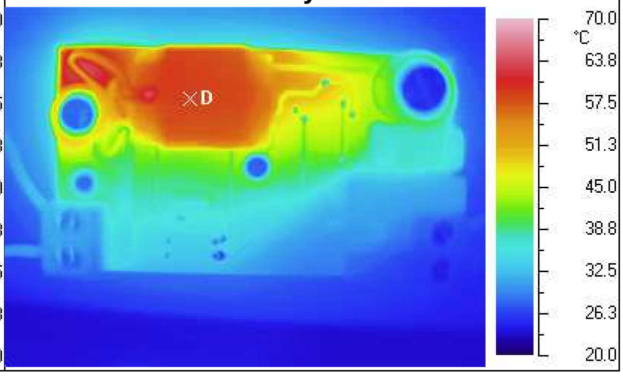


Figure 31. Thermal map at 230 V_{AC} full load. Bottom layer

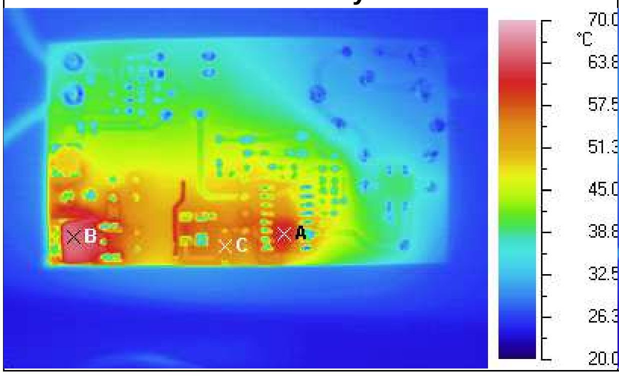


Figure 32. Thermal map at 230 V_{AC} full load. Top layer

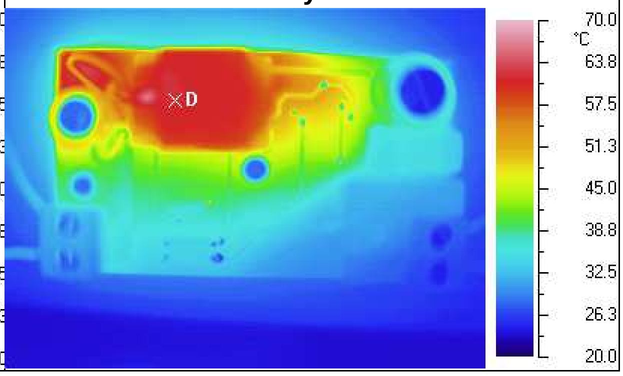


Table 10. Temperature of key components (T_{amb} = 25 °C, emissivity = 0.95 for all points)

Point	Temp (°C)		Reference
	115V_{AC}	230V_{AC}	
A	56.8	61.5	VIPer25HD
B	66.3	66.2	Output diode
C	50.4	55.2	Snubber diode
D	59.0	61.9	Transformer

7 Conclusions

In this document a flyback has been described and characterized. Special attention was paid to efficiency and low load performances and the bench results were good with very low input power in light load condition. The efficiency performance have been compared with requirements of the EC CoC and DoE regulation programs for external AC/DC adapter with very good results, being the measured active mode efficiency always higher respect the minimum required.

Also the EMI emission are quite low, even is using low cost input filter.

8 Demonstration tools and documentation

The VIPer25HD evaluation board order code is: STEVAL-ISA162V1.

Further information about this product is available in the VIPer25 datasheet at www.st.com.

9 Revision history

Table 11. Document revision history

Date	Revision	Changes
12-Jun-2015	1	Initial release.