AN4695
Application note

Thermal dissipation and how to clear diagnostic registers in case of under-voltage

Introduction

This application note is intended to integrate the information provided in the L9959 product datasheet so as to facilitate the comprehension of:

- Theoretical calculus for Thermal Dissipation produced on integrated MOS due to the driving of a DC motor;
- Diagnostic registers clearing at the device power up or in case of V_S under-voltage.

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1 Thermal dissipation

This is a section regarding the theoretical calculus for Thermal Dissipation produced on integrated MOS due to the driving of a DC motor (rotating RL load).

We drive the bridge through PWM input signal and DIR input signal. In our case, we assume that the H-bridge is working in forward mode.

Figure 1: PWM mode current flow

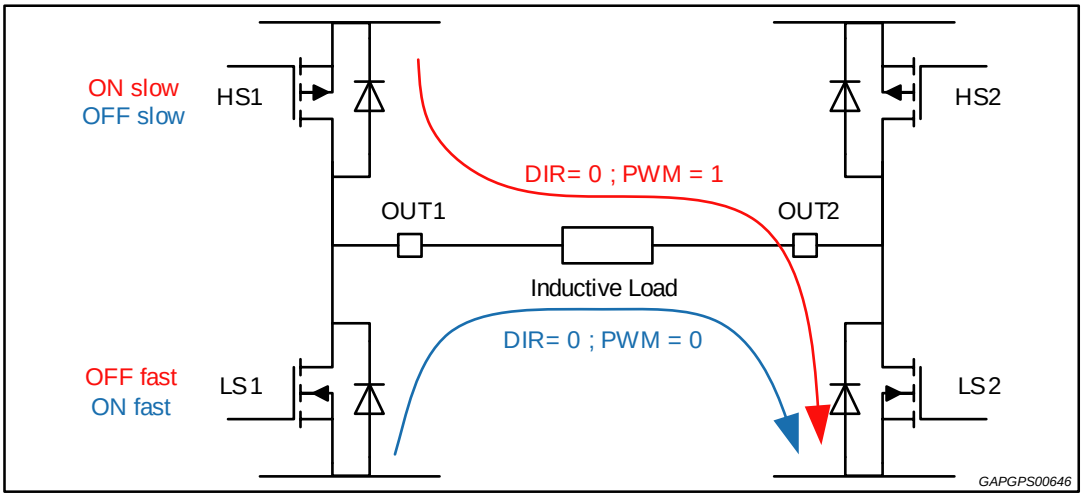

Figure 2: Boundaries diagram

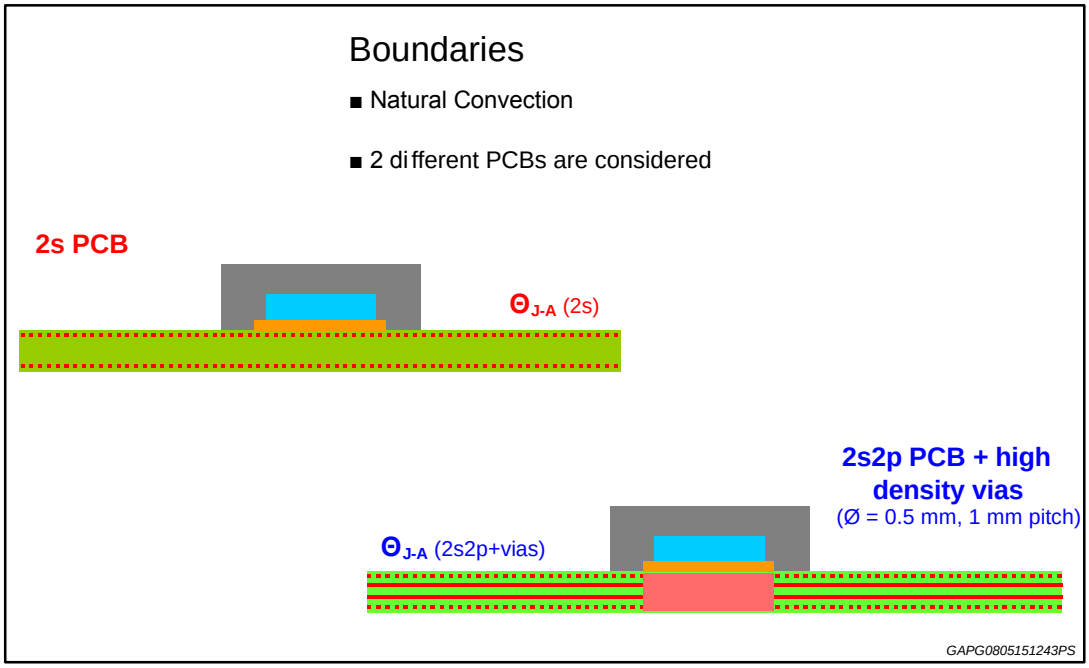

Table 1: Thermal simulation results summary

Package type	Exp. Pad Size (mm^2)	Die Size (mm^2)	$\Theta_{j\text{-}amb}$ (°C/W) on 2s PCB	$\Theta_{j\text{-}amb}$ (°C/W) on 2s PCB
PowerSSO8/12	3.5 x 2.6	4	92	36
PowerSSO24/36	6.5 x 4.4	16	65	23
		9	66	24

1.1 Average power dissipation - the theoretical model

The total average power PAV per PWM cycle can be calculated by using the below set of worst case conditions:

- Parameter
  - DT
  - a_{sw}
  - f_{pwm}
  - I_{load}
  - V_{ps}
  - R_{dsonH0}
  - R_{dsonL1}
  - VSR slow
  - ISR slow
  - T_{amb}
  - R_{thja}

We calculate the power dissipation PAV single due to a Single die contribution which works in the above table reported conditions. The parameter L_{sw} takes into account the switching time which must be subtracted to the nominal Duty Cycle (DT).

$$HSD_0 : \begin{cases} P_{static-on-H0} = R_{dsonH0} * I_{load}^2 * (DT - \alpha_{sw}) & (1) \\ \text{where} : \alpha_{sw} = \frac{\sum_{i=0}^{3} tsw_i}{T} & \\ P_{sw-H0} = (I_{load} * V_{ps}) * \left(\frac{V_{ps}}{VSR} + \frac{I_{load}}{ISR}\right) * f_{pwm} & (2) \end{cases}$$

$$LSD_1 : P_{static-on-L1} = R_{dsonL1} * I_{load}^2 \quad (3)$$

$$HSD_1 : P_{static-on-H1} = 0 \quad \text{(i.e. always off)} \quad (4)$$

$$LSD_0 : P_{static-on-L0} = R_{dsonL0} * I_{load}^2 * (1-DT) \quad (5)$$

Switching times tswi (i = 0; 1; 2; 3) are timings defined both in function of the maximum power peak on HSD0 in a PWM cycle Pa, and the power dissipation in conduction Pb.

$$P_a = I_{load} * V_{ps} \quad (6)$$

$$P_b = I_{load}^2 * R_{dsonH0} \quad (7)$$

Based upon the foregoing partial contributions, for the Single option we have an average power consumption:

$$P_{AVsingle} = P_{sw} + P_{static} = (1) + (2) + (3) + (4) + (5) \quad (8)$$

In case we use the Twin option (both dies simultaneously working), we have to consider both die contributions:

$$P_{AVtwin} = 2 * P_{AVsingle} \quad (9)$$

Juntion temperature calculation for Twin option is defined as:

$$T_j = T_{amb} + (R_{thja} * P_{AVtwin}) \quad (10)$$

2 How to clear diagnostic registers in case of under-voltage

Diagnostic registers clearing at the device power up or in case of Vs under-voltage require to consider different sentences present in different sections of the datasheet. It could be useful to summarize here the standard approach necessary to implement for having DIA_REG1 and DIA_REG2 with no fault condition present inside. The diagnostic of the device has to be performed in steady-state. The device internally implements several fault diagnostic functions and the main ones are:

- Short circuit to ground at OUT1
- Short circuit to ground at OUT2
- Short circuit to battery at OUT1
- Short circuit to battery at OUT2
- Short circuit over load
- Short circuit to battery at disable output
- Short circuit to ground at disable output
- Under voltage at V_S
- Over temperature

For safety reasons, a double Fault registers (DIA_REG1/ DIA_REG2) strategy has been implemented. Under voltage at V_S has higher priority versus all the other faults. To maintain full visibility of all the other possible faults conditions also in case of $V_S < V_{uv}$, the effect of the command DIACLR1 has been differentiated from the standard procedure: move fault bits from DIA_REG1 to DIA_REG2 and clear DIA_REG1 (for $V_S > V_u$) , and what has been implemented ($V_S < V_{uv}$) is a simple move from DIA_REG1 to DIA_REG2 but not a clear. The aim of the previous approach is to permit when the under voltage conditions will be recovered, to have the full visibility of all the other (mutual exclusive) possible fault reasons, giving additional information otherwise masked. In case V_{DD} is already present at the rising edge of V_S, the suggested sequence to obtain a full clear of the two different fault registers is:

- Wait until V_S overcome V_{uv}
- Enable the command DIACLR1 writing the relative bit in the register STATCON_REG
- Enable the command DIACLR2 writing the relative bit in the register STATCON_REG

3 Revision history

Table 2: Document revision history

Date	Revision	Changes
09-Oct-2015	1	Initial release.

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