AN4720
Application note

Half bridge resonant LLC converters and primary side MOSFET selection

Alfio Scuto

Introduction

These days, vast amounts of data are stored and shared by innumerable users around the world, leading to the vertiginous increase of data centers that house clusters of servers, storage devices, networks and telecommunications systems servicing users around the world.

The conflicting requirement of limiting or reducing total carbon emissions deriving from the enormous corresponding energy demand imposes the need to constantly improve the efficiency of the associated electronic systems.

The power supplies that feed all of these systems are pivotal in this respect and are required to satisfy the following requirements:

- higher efficiency
- higher power density
- higher component density

Among several types of switched-mode power supplies, resonant power converters with LLC half-bridge configurations are receiving a lot of interest because of their intrinsic capacity to lower switching losses while increasing switching frequencies.

LLC resonant converters convert power with frequency modulation and Zero Voltage Switching (ZVS) for power MOSFETs.

They require switching frequencies as close as possible to the resonant frequency, as any deviation increases the current circulating in the resonant tank which translates into increased electrical losses, compromising the advantages of this topology.

In addition, current and/or voltage peaks can further stress the MOSFET devices when the circuit works in resonance.

The challenge, therefore, is to select the right power MOSFETs to simultaneously satisfy low switching loss and high reliability requirements.

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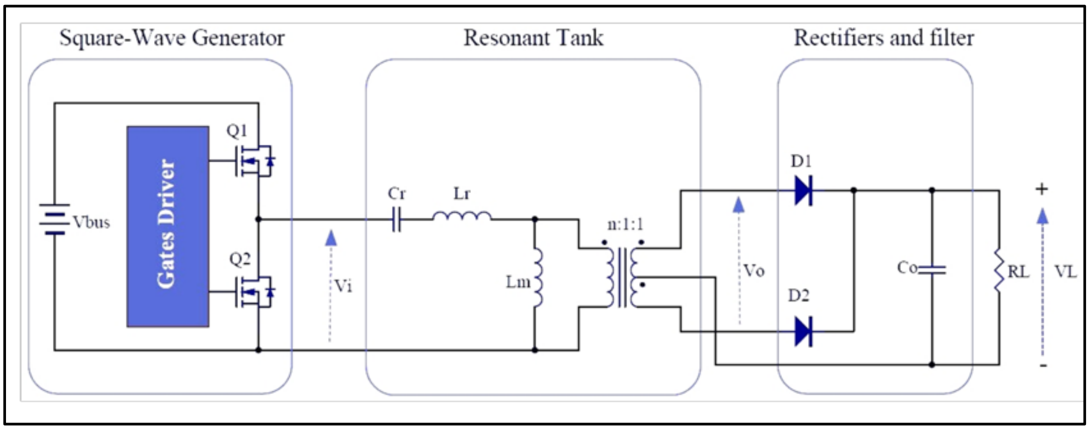
1 LLC resonant half-bridge converters: topology and characteristics

A basic LLC resonant half-bridge converter is shown below.

Figure 1: Basic LLC resonant half-bridge converter



The circuit consists of:

- **A square-wave generator**: two power MOSFETs, Q_1 (High Side) and Q_2 (Low Side), are configured to produce a unipolar square-wave voltage. To prevent any cross-conduction through ground and allow sufficient time to realize the ZVC, the two devices are driven with a small dead time T_d.
- **Resonant Tank**: the resonant network is formed by capacitor C_r and inductors L_r and L_m. In particular, L_m represents the transformer's magnetizing inductance. The LLC resonant converter looks very similar to an LC series resonant converter (SRC), apart from the addition of the inductor Lm.
- **Rectifier and filter**: on the secondary side of a converter, the rectifier consists of two diodes for full-wave rectification and an output capacitor C_o to smooth the rectified voltage to the load R_L. In some "synchronous rectification" configurations, the two diodes are replaced with MOSFETs to help reduce conduction losses, especially in low-voltage and high current applications.

2 Circuit analysis and operation

LLC converters have been the subject of extensive research, with various developments in analysis and modeling techniques.

Fundamental harmonic analysis (FHA) represents a consolidated method to derive the transfer function of the resonant tank and the output rectifier stage *[1]*. The FHA frequency domain method sacrifices model accuracy to simplify the topology through sinusoidal waveform approximations and AC equivalent circuits.

Assuminga 50% duty-cycle (180° saturation and 180° cut-off for each MOSFET) for Q_1 e $Q_{2,}$ the voltage applied to the resonant tank is a periodical square-wave voltage between 0 and V_{bus}.

Using the Fourier series, we can break up the square-wave voltage in input and output through their harmonic components (see *Figure 2: "Fundamental Harmonic Analysis (FHA)"*)

When the resonance tank operates at its series resonance frequency, we can assume that the bulk of the energy is transferred to the output through the fundamental component of this square wave.

Moreover, if we consider a Q-factor of the resonator tank high enough to neglect the high order harmonics, the current in the cell can be considered as purely sinusoidal.

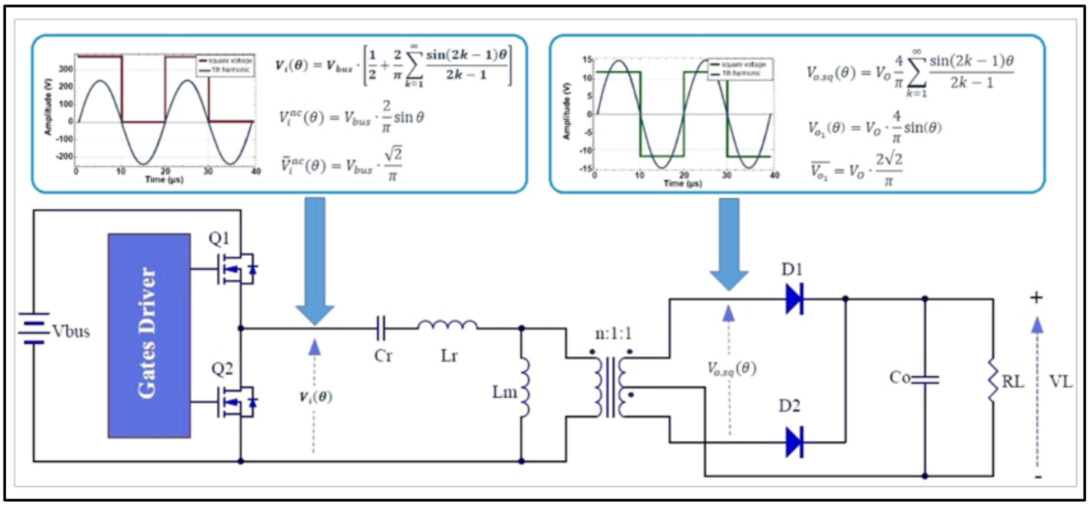
At resonance, the amount of energy provided to the resonator tank is mainly dependent on the value of the resonant circuit impedance at that frequency for a given load impedance R_L.

In power amplifiers, the configuration of the two MOSFETs and the electrical characteristics of Figure 1 determine what is known as a ‘quasi-complementary Class D’ circuit because it uses two identical transistors (N-channel MOSFETs). A true-complementary configuration would require N- and P-channel MOSFETs.

The second side of the transformer is center tapped and the square-wave voltage is bipolar.

Figure 2: "Fundamental Harmonic Analysis (FHA)" shows the input and output voltages when implementing the FHA hypothesis at resonance frequency.

Figure 2: Fundamental Harmonic Analysis (FHA)



To include the load resistance in the AC circuit, it needs to be converted to an equivalent AC impedance on the primary side of the transformer (see *Figure 3*).

As the frequency of the square-wave generator is varied, the resonant circuit impedance varies. In the LLC, the circuit peak resonance frequency is a function of the load. When there is no load, the resonance frequency of the circuit is f_p. As the load increases, the circuit resonance frequency approaches the f_0 limit representing a short-circuit load.

Hence, LLC impedance adjustment follows a family of curves with $f_p \leq f_{res} \leq f_0$ during the normal operation of the circuit.

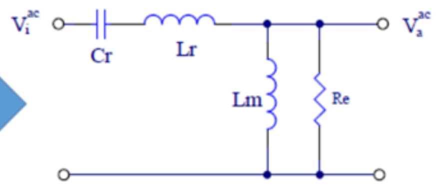
Figure 3: AC equivalent circuit for the LLC resonant converter

$$R_e = \frac{8 \cdot n^2}{\pi^2} R_L$$

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}$$

$$f_p = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}}$$

$$Q_e = \frac{1}{R_e} n^2 \sqrt{\frac{L_r + L_m}{C_r}}$$



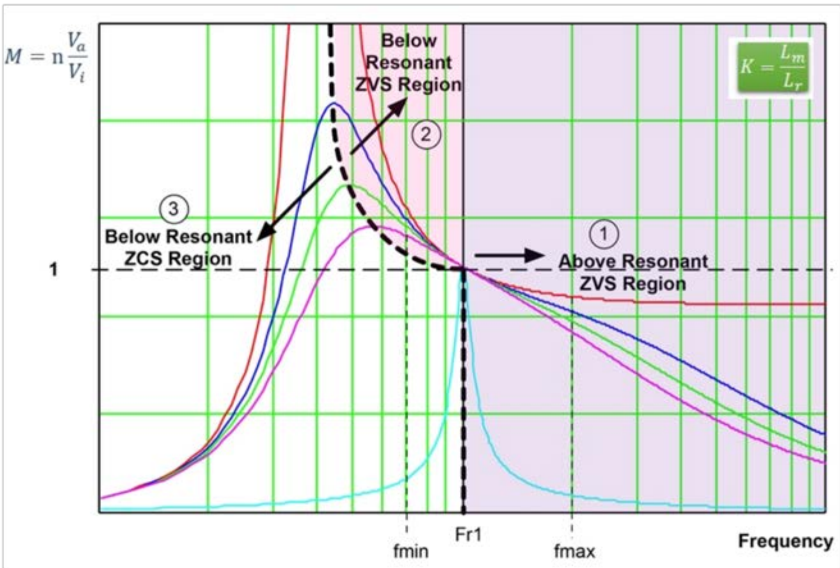
From the equivalent AC circuit in *Figure 3: "AC equivalent circuit for the LLC resonant converter"*, the DC voltage gain can be derived using the FHA.

In *Figure 4: "Operating regions for an LLC resonant converter"*, the operating regions of the LLC resonant converter are divided into two primary switching type regions: the ZCS region and the ZVS region. When the converter switches at higher than resonant frequencies f_{r1}, it always runs in ZVS mode. When the converter switches at lower than resonant frequencies f_{r2}, it always runs in ZCS mode.

When the converter is switching between the resonant frequencies f_{r1} and f_{r2}, the load condition determines whether the converter operates in ZVS or ZCS mode.

Under normal operating conditions, the LLC resonant converter operates at slightly higher than the resonant frequency f_{r1}, which is optimal for high efficiency.

Figure 4: Operating regions for an LLC resonant converter



One interesting feature of the gain curves is that they all converge on the point where the switching frequency is equal to the resonant frequency; in other words, this unity gain point is load independent and the converter operating at this point does not need to change its switching frequency for any level of output power as long as the input voltage is the same.

The principal features of the FHA model are:

- The resonant tank responds primarily to fundamental component of the applied square-wave voltage, then tank waveforms are approximated into their fundamental components.
- A secondary rectifier + low-pass filter effect is incorporated into load.

The disadvantages of the FHA model are:

- It does not accurately predict operation frequency and tank current amplitude, especially in Discontinuous Conduction Mode (DCM).
- The FHA model is not sufficiently accurate for overcurrent or overpower protection design, so appropriate design margins need to be considered.

3 The role of MOSFETs in achieving the ZVS condition

Having briefly analyzed the resonant tank circuit, we can now focus on how to drive the MOSFETs to create the ZVS condition for soft-switching at turn-on.

In *Figure 1: "Basic LLC resonant half-bridge converter"*, the body diodes of Q1 and Q2 are highlighted because they play an important role in the functionality of the circuit.

Moreover, the drain-to-source capacitances C_{oss1} and C_{oss2} provide an additional contribution to the voltage transient of the node HB (midpoint between Q_1 and Q_2).

It is important to bear in mind that C_{oss1} and C_{oss2} are nonlinear capacitors; their value is a function of the drain-to-source voltage *[2]*.

4 MOSFET output capacitance (C_{OSS})

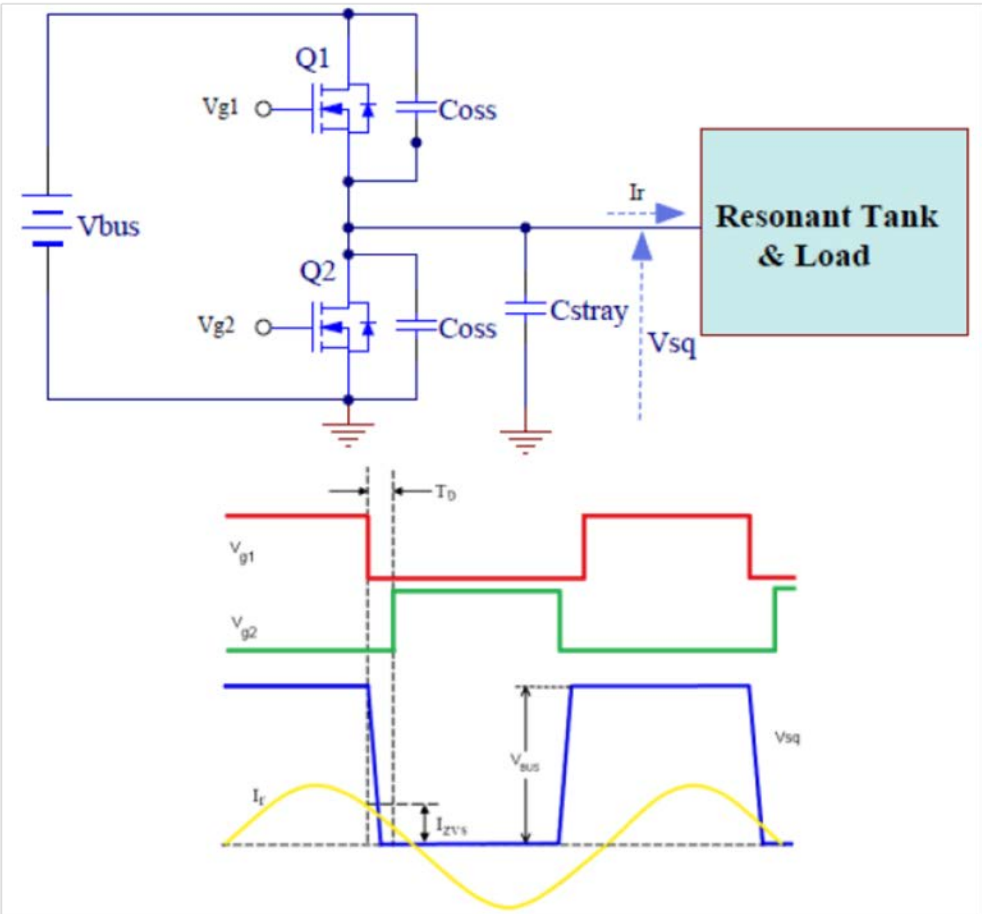
At the HB midpoint node, the total capacitance C_{zvs} is the sum of the output MOSFET capacitors C_{OSS} and the parasitic capacitance C_{stray} of the power MOSFET cases, the heat sink, the intra-winding capacitance of the resonant inductor, etc.

Equation 1

$$C_{zvs} = 2C_{oss} + C_{stray}$$

Let's see how the capacitance C_{zvs} can influence the ZVS condition through the Q quality factor *[3]*.

Figure 5: Role of capacitor C_{OSS} and dead time T_D



4.1 Q for ZVS at full load and min Vin

In order to guarantee ZVS, the tank current at the end of the first half cycle (see *Figure 5: "Role of capacitor Coss and dead time TD"*) must exceed the minimum value necessary to deplete the equivalent capacitance within the dead time interval T_D.

Equation 2

$$I_{zvs} = (2C_{oss} + C_{stray})\frac{V_{BUS}}{T_D}$$

This current equals the peak value of the reactive current flowing through the resonant tank and determines the reactive power level.

Moreover, the RMS component of the tank current associated with the active power is:

Equation 3

$$I_{act} = \frac{P_{in}}{V_{i,FHA}}$$

From Equation 2, Equation 3 and the resonant tank input impedance $Z_n(f_n, K, Q)$ we obtain:

Equation 4

$$\frac{Im[Zn(fn,K,Q)]}{Re[Zn(fn,K,Q)]} \geq \frac{C_{zvs}}{\pi T_D}\frac{V_{BUS}^2}{P_{in}}$$

Solving Equation 4, we determine the quality factor Q_{zvs1} that ensures ZVS behavior at full load and minimum input voltage.

4.2 Q for ZVS at no load and max Vin

The ZVS condition also needs to be satisfied under no load and maximum input voltage. For this operating condition, it is possible to find an additional constraint for the maximum quality factor to guarantee ZVS.

If $Z_{in\ OL}$ is the impedance of the resonance tank under no load, the condition to operate in ZVS is:

Equation 5

$$\frac{V_{i,FHA\ max}}{Z_{in\ OL}(f_{n,max}, K, Q)} \geq \frac{I_{zvs\ (V_{BUS})}}{\sqrt{2}}$$

The above equation forms the constraint for obtaining the quality factor Q_{zvs2} for the ZVS under no load and maximum input voltage, thus:

Equation 6

$$Q_{zvs2} \leq \frac{2}{\pi}\frac{f_{n,max}}{(1+K)f_{n,max}{}^2 - 1}\frac{T_D}{R_{ac}C_{ZVS}}$$

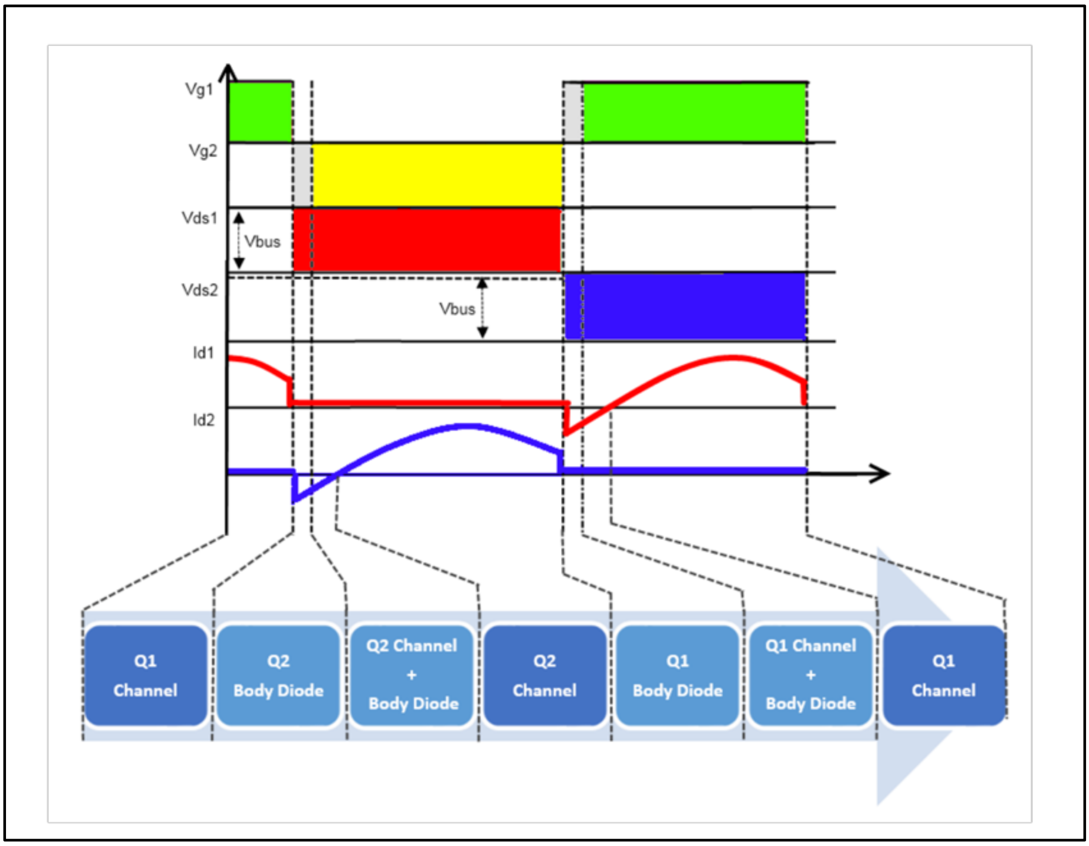
Therefore, in order to guarantee ZVS over the whole operating range of the resonant converter, we have to choose a maximum quality factor value lower than the smaller of Q= min [Q_{zvs1}; Q_{zvs2}]

5 MOSFET body diodes

In *Figure 6: "Typical waveforms for ZVS"*, we see the two gate signals with the added dead time to avoid Q_1 and Q_2 being ON simultaneously.

During this delay time, the current flows through the body diode of the each MOSFET to guarantee ZVS operation, while during the ON state the body diodes are OFF.

Figure 6: Typical waveforms for ZVS

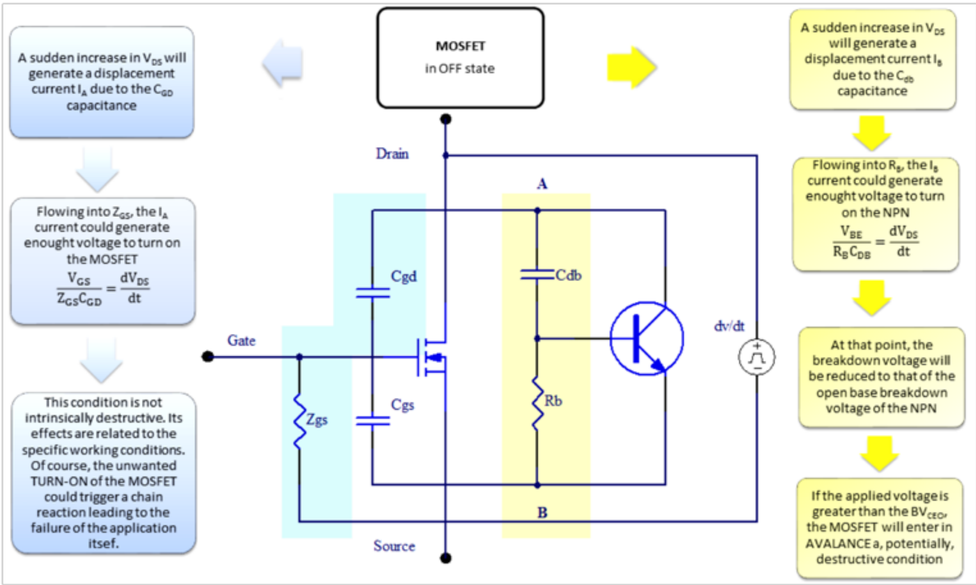


6 Power MOSFET failure mechanisms

Figure 7: "MOSFET device with its parasitic components" shows the MOSFET device and its parasitic components.

6.1 Failure mode 1: static dv/dt associated with the parasitic BJT

Figure 7: MOSFET device with its parasitic components



6.2 Failure mode 2: reverse recovery dv/dt

The load current is negative while the MOSFET is ON and thus flows through the source-drain diode in the MOSFET structure (see *Figure 7: "MOSFET device with its parasitic components"*).

The base-emitter junction is reverse biased and the parasitic BJT is OFF.

When the MOSFET is turned OFF, a voltage step with a certain dv/dt is applied across D-S. The resulting displacement current I_D flows through the drain-base capacitance C_{DB} and the P-base finite resistance R_B.

At the same time, the diode reverse recovery I_{RR} flows through R_B itself in order to remove the charge stored in the drain region; I_{RR} is not generated by dV/dt, but accompanies it.

The parasitic bipolar could be turned ON. This would reduce the clamping voltage and potentially cause the device to enter an avalanche state.

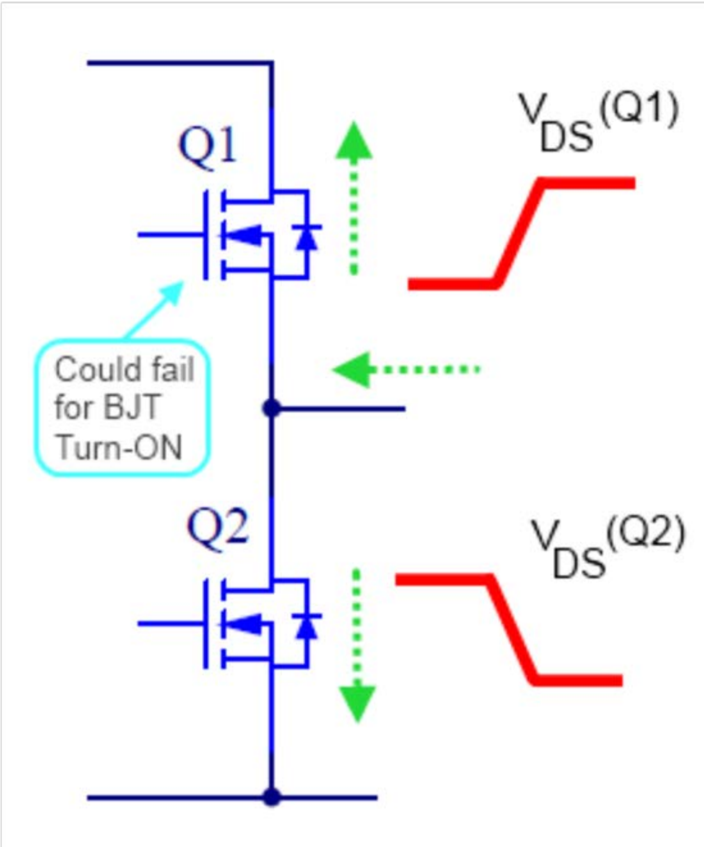
As these dV/dt issues are common for bridge topologies, we need to carefully control the switching speed of the MOSFET. In the HB, the switching MOSFET generates the V_{DS} variation across the device in the OFF state (see *Figure 8: "HB switching "*).

Q_1 is ON and the current is flowing through the parasitic diode of Q_1 (D_1) due to its direction; when Q_1 is turned OFF, the load current still flows through D1 for the whole dead-time duration.

Q_2 is turned ON with a high |dv/dt| (the dv/dt is negative on Q_2 and depends on $R_{G\text{-}ON}(Q_2)$) so the current switches from D_1 to Q_2. The same |dv/dt | with a positive value is applied to Q_1.

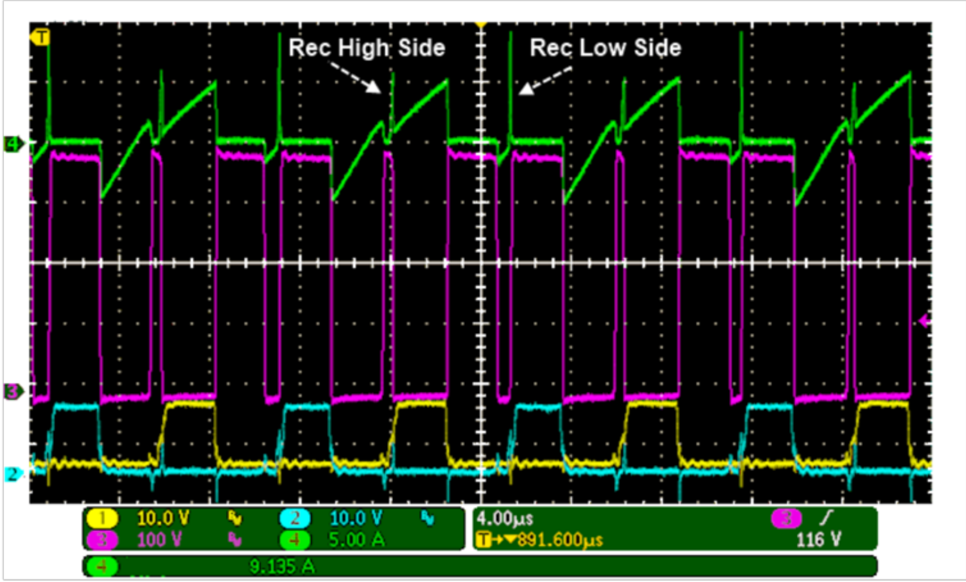
The base-drain diode reverse recovery increases the risk of parasitic BJT turn-on, so the dv/dt could be very dangerous and cause Q_1 failure. The same problem could affect Q_2 during Q_1 turn-on.

Figure 8: HB switching



Generally, MOSFETs with fast recovery diodes are not necessary for normal ZVS operation, but MOSFET failure in LLC resonant converters can sometimes be caused by high current spikes (shoot through) due to the poor reverse recovery characteristics of the body diode at particular instants (see *Figure 9: "Current spikes in HB"*).

Figure 9: Current spikes in HB

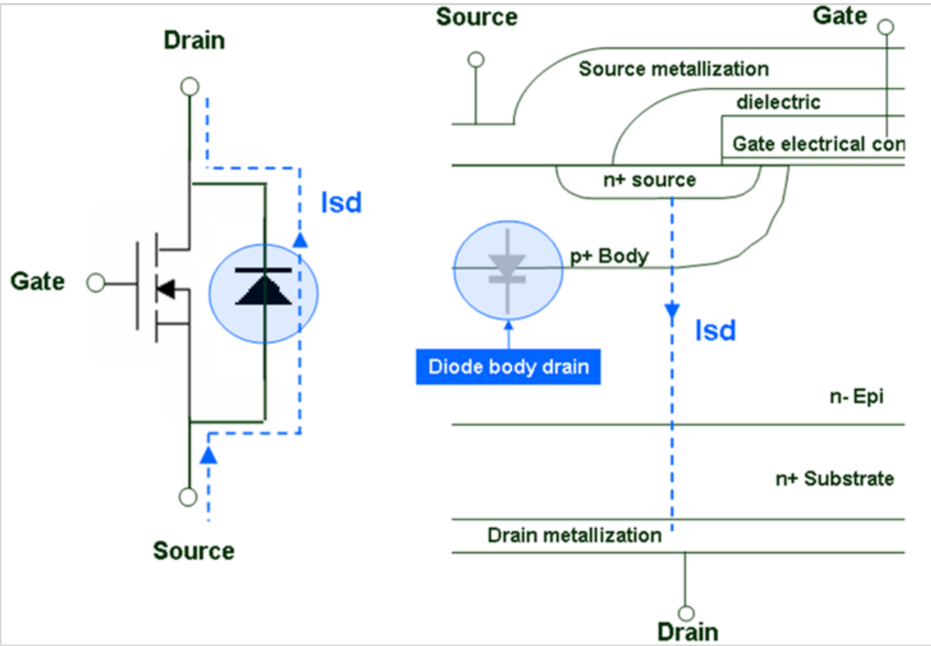


CH	1	2	3	4
	Low-side Vgs	High-side Vgs	Low-side Vds	Low-Side MOSFET current

6.2.1 Body diode reverse recovery

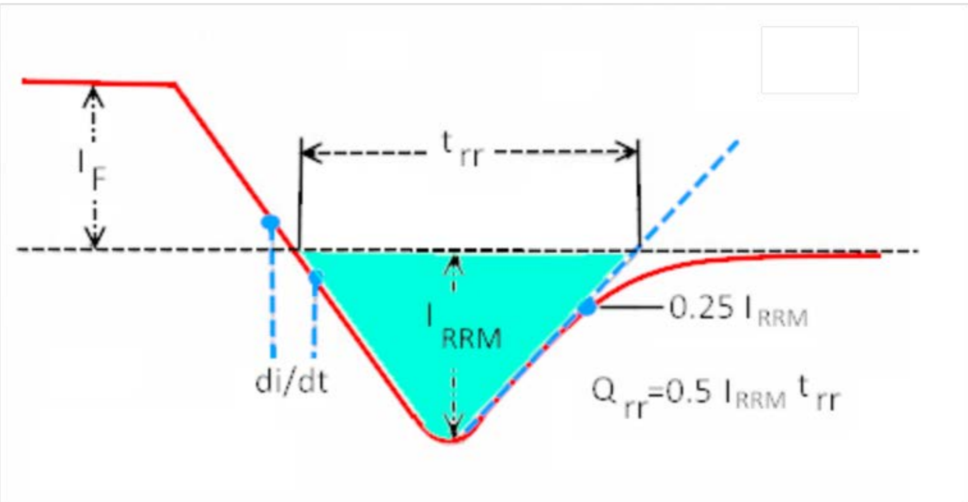
Figure 10: "Current through body diode" shows the cross section of a MOSFET device with the intrinsic diode between the body and drain.

Figure 10: Current through body diode



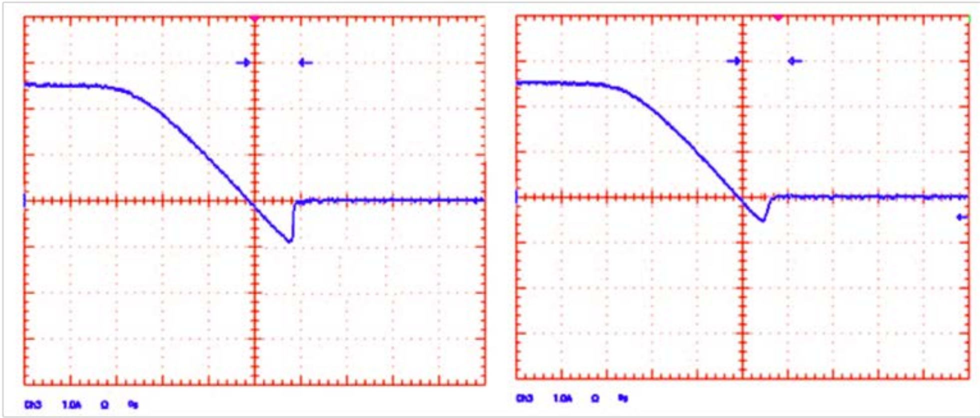
MOSFET parasitic body diode reverse recovery occurs during diode switching from the ON to the OFF state because its stored minority charges must be removed either actively via negative current or passively via recombination inside the device. The typical dynamic parameters listed in the datasheet for diode reverse recovery are depicted in *Figure 11: "Figure 11: Body diode reverse recovery charge"*.

Figure 11: Body diode reverse recovery charge



The highlighted area in the picture represents the body diode reverse recovery charge (Q_{rr}). *Figure 12: "MOSFETs with standard (left) and fast intrinsic body diodes (right)"* shows a comparison between MOSFETs with standard intrinsic diodes and MOSFETs with fast intrinsic diodes (low Q_{rr}).

Figure 12: MOSFETs with standard (left) and fast intrinsic body diodes (right)



As already mentioned, MOSFETs with fast recovery diodes are not necessary in normal ZVS operation, which is why STMicroelectronics has developed the MDmesh™ M2 and MDmesh™ M2-EP series.

Both series are well suited for LLC applications and the MDmesh™ M2-EP series in particular has advanced features to maximize power system efficiency with special emphasis on high frequency operation and low load conditions.

7 Non-standard operations in LLC resonance HB

For specific situations where it is not possible to ensure safe device operation, STMicroelectronics offers the special MDmesh™ DM2 series with improved body diode performance, offering both very low reverse recovery charge (Q_{rr}) and short recovery time (t_{rr}).

7.1 Capacitive region operations

An example case is when the system operates in steady state under a low load. In this condition, the system frequency is near the lower resonant frequency and the ZVS is obtained.

If the load changes from a low to a high value, the switching frequency should follow the new resonant frequency; if this doesn't occur we might fall into region 3 (see *Figure 4: "Operating regions for an LLC resonant converter"*)

The MOSFET is turned OFF while the current is circulating through the body diode and, since the antagonist MOSFET is turning ON, a body diode recovery can occur *[4]*.

In this case, there is additional power dissipation due to the current and voltage of the conducting body diode.

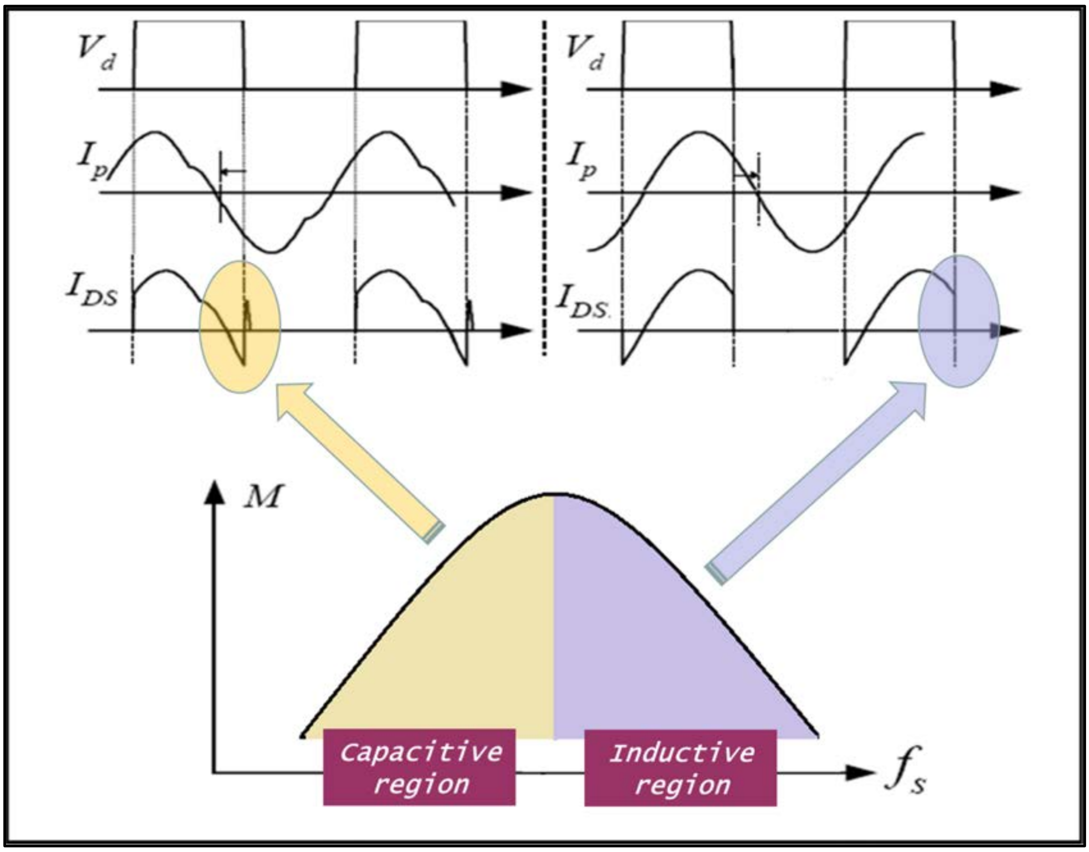
This gives rise to a potentially lethal shoot-through condition for the half-bridge led, due to the simultaneous parasitic turn-on of both MOSFETs; moreover, the recovery of the body diodes generates large and energetic positive current spikes.

In order to reduce this kind of risk, several solutions are implemented. Dedicated gate driver controllers able to manage the dead time or appropriate network circuits able to increase the dead time or higher R_{gate} values can generally resolve this problem.

Chip manufacturers can also help solve this problem with dedicated MOSFET devices featuring short recovery times. The STMicroelectronics MDmesh™ DM2 MOSFET technology re[resents a robust solution with enhanced body diode recovery time performance, rated at less than 200ns.

As previously mentioned, a resonant converter operates in capacitive and inductive regions, as depicted below in *Figure 13: "capacitive and inductive areas"*.

Figure 13: capacitive and inductive areas

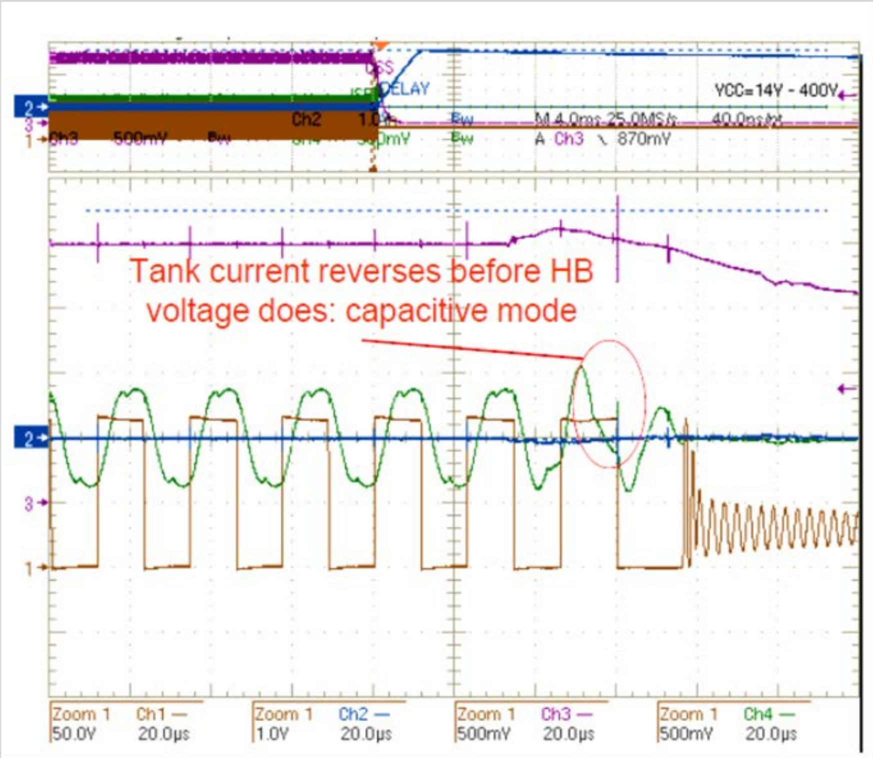


When the system operates in the inductive region, the switching is in ZVS and during the transition where the main switch passes from the ON to the OFF state, its current I_p has a positive value (violet area) and flows from drain to source. When the system functions in the capacitive region, the operations occur at ZCS. In this case (yellow area), the current on the main switch goes from source to drain, also involving the physical diode on the MOSFET structure.

The LLC system can experience capacitive mode operation in the following circumstances:

- Soft capacitive mode: occurs when the tank current phase progressively approaches zero, for example at power down, with max load when the input voltage goes low. Generally, resonant controllers like the L6699A *[5]* by STMicroelectronics have an advanced protection feature (anti capacitive mode) that increase the switching frequency as if there were an overload condition, thus raising the tank current phase.
- Hard capacitive mode: this can occur when the tank current phase becomes zero or negative from one cycle to another as in the case of a short at the output (see *Figure 14: "Hard capacitive mode"*). In this situation, the MOSFET is turned OFF and the converter is stopped and no hard switching takes place.

Figure 14: Hard capacitive mode



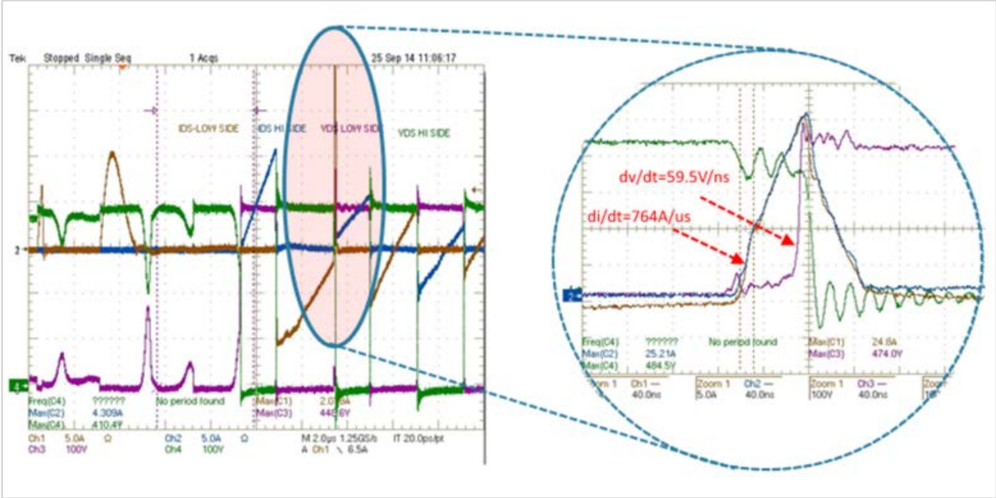
7.2 Hard switching at start-up

During start-up, the ZVS condition can be lost and the MOSFETs will undergo hard-switching, potentially causing a very high diode reverse recovery current.

At start-up, the voltage across resonant capacitor is initially discharged and needs a number of switching cycles before being charged to the steady-state value $V_{in}/2$. During the initial transient, abnormally high tank current peak values may appear. The tank current does not reverse during the first one or two switching cycles. In this condition, we may experience the potentially hazardous capacitive-mode and hard-switching operations, even if for a very short time interval. The MOSFETs could exceed their maximum dv/dt and di/dt ratings (*Figure 15: "Dangerous operating conditions exceeding datasheet maximum ratings"*), leading to potential failures.

This issue is also addressed in the L6699A resonant controller thanks to an enhanced soft-start procedure to smooth the start-up.

Figure 15: Dangerous operating conditions exceeding datasheet maximum ratings

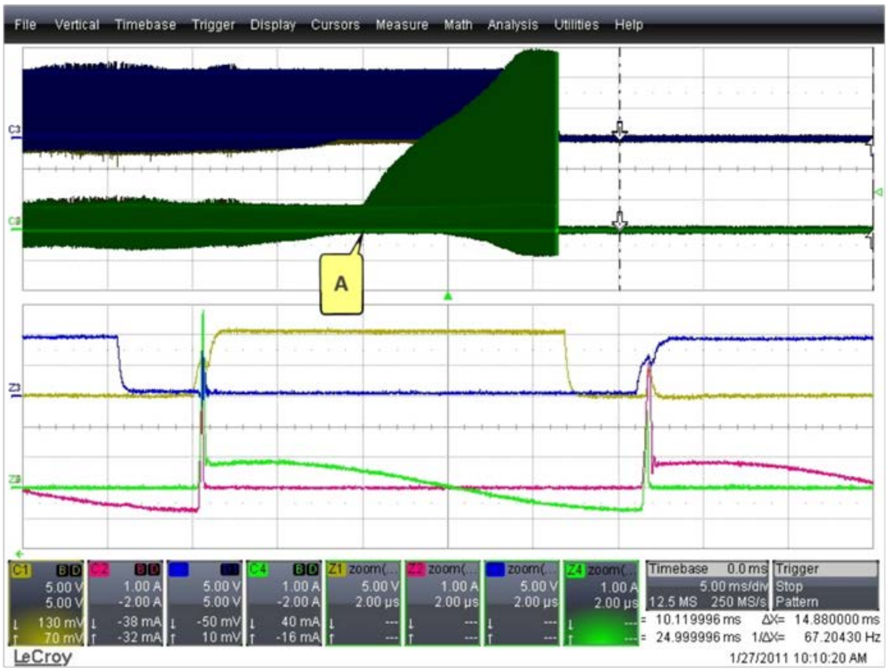


Another possible solution to these potential failures is to slow down the dynamics of the circuit using a combination of a diode and resistors in series with the two gates.

7.3 Hard switching caused by supply disconnection

Hard switching can also occur during normal SMPS operation. In fact, if the main supply is disconnected, the system could be forced to operate in capacitive mode, as shown in *Figure 16: "Hard switching caused by supply disconnection"*.

Figure 16: Hard switching caused by supply disconnection

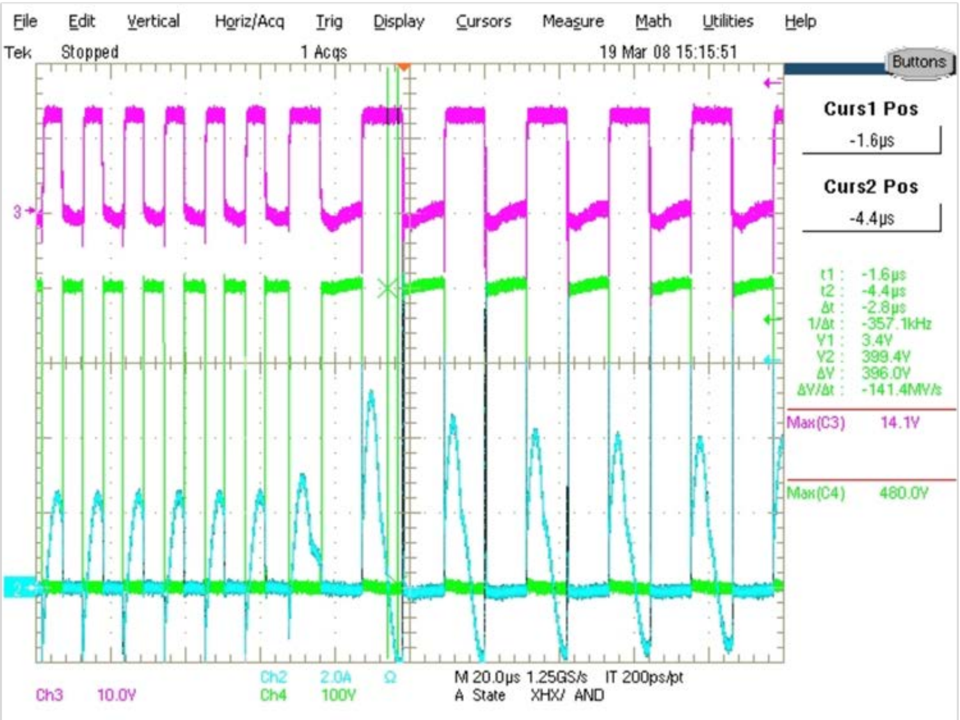


The figure shows that when the main supply is removed (point A), the dead-time fixed by the driver is not enough to maintain inductive operation, so the current continues to rise due to the shoot-through between the two devices.

8 Hard switching caused by fast load transition

In this case, the system might not change the switching frequency quickly enough and so allow capacitive mode operation for the time required by the control system to restore normal inductive operation of the SMPS.

Figure 17: Hard switching caused by fast load transition



In the above figure, the purple V_{gs}signal shows how the working frequency changes when there is a fast load transition. On the left side of the figure, the current (cyan line) has a typical shape for a resonant LLC, while on the right side, the voltage V_{ds} (green line) lags the current, which is typical of a capacitive network.

9 Conclusions

This application note reviews the underlying theories for the characteristics of a resonance LLC topology and, in particular, the key role of MOSFET devices in circuit operation.

Particular attention was paid to the operating conditions that could determine potential failures of the MOSFETs. For these special situations, STMicroelectronics suggests its dedicated DM2 series with improved body diode performance.

From this report, it is clear that special consideration should be given to MOSFET selection for new LLC designs requiring body diodes with fast recovery times, low voltage drops and rugged, dynamic dv/dt parameters.

In the context of the above requirements for soft and resonant applications, important benefits are offered by the MDmesh™ M2-EP series technology, which optimizes both the shape and the absolute value of the output capacitance, proven to be key requirements in high efficiency SMPS applications.

For additional information regarding the MDmesh™ M2-EP series technology, please refer to AN4742 *[9]*

10 References

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11 Revision history

Table 1: Document revision history

Date	Revision	Changes
05-Aug-2015	1	Initial release.