AN4754
Application note

Migrating between STM32L486xx/476xx and STM32L443xx/433xx microcontrollers

Introduction

For more and more applications using STM32 microcontrollers, it is important to easily migrate a project to a different microcontroller in the same product family.

Migrating an application to a different microcontroller is needed, for instance, when product requirements grow, putting extra demands on memory size, or requiring an increase in the number of I/Os. On the other hand, cost reduction objectives may force to switch to cheaper components and towards shrinking the PCB area.

This application note is intended to help the user to analyze the steps needed to migrate from existing designs based on STM32L486xx/476xx microcontrollers to STM32L443xx/433xx microcontrollers. It groups together the most important information and lists the key items to address.

In this document the comparisons are carried out for the “full feature” variants of the STM32L486xx/476xx and STM32L443xx/433xx microcontrollers. The user must consider that some products may have less features (depending on actual part number).

Migrating between two devices within the same family can require in some cases hardware and/or software changes: the required changes are described in this document.

To benefit fully from the information in this application note, the user should be familiar with the STM32 microcontroller family.

This application note has to be read in conjunction with STM32L486xx/476xx and STM32L443xx/433xx microcontrollers reference manuals (RM0351 and RM0394, respectively) and microcontrollers datasheets, all available at *www.st.com*.

Table 1. Applicable products

Type	Product RPNs
Microcontrollers	STM32L433CC, STM32L433RC, STM32L433VC, STM32L433CB, STM32L433RB
	STM32L443CC, STM32L443RC, STM32L443VC
	STM32L476RG, STM32L476JG, STM32L476MG, STM32L476ME, STM32L476VG, STM32L476QG, STM32L476ZG, STM32L476RE, STM32L476JE, STM32L476VE, STM32L476QE, STM32L476ZE, STM32L476RC, STM32L476VC
	STM32L486JG, STM32L486QG, STM32L486RG, STM32L486VG, STM32L486ZG

Contents

List of tables

List of figures

1 Hardware migration guide

1.1 PCB design compatibility

The STM32L486xx/476xx microcontrollers do not share all the packages with the STM32L443xx/433xx microcontrollers. The *Table 2* illustrates for each common package the pinout/ballout compatibility.

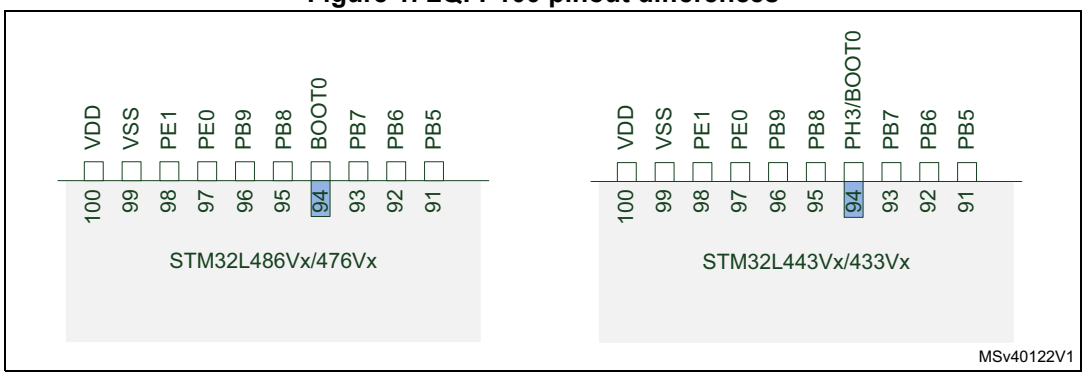
Table 2. Package availability and PCB design compatibility

Package	STM32L443xx STM32L433xx	STM32L486xx STM32L476xx	Pinout/ballout difference	PCB design modification
LQFP144 (20 x 20)	-	X	-	-
LQFP100 (14 x14)	X	X	Weak	Not Mandatory(1)
LQFP64 (10 x 10)	X	X	Weak	Not Mandatory(1)
LQFP48 (7 x 7)	X	-	-	-
UFQFPN48 (7 x 7)	X	-	-	-
UFQFPN32 (5 x 5)	X -(2)	-	-	-
UFBGA132 (7 x 7)	-	X	-	-
UFBGA100 (7 x 7)	X	-	-	-
UFBGA64 (5 x 5)	X	-	-	-
WLCSP81	-	X -(3)	-	-
WLCSP72	-	X	-	-
WLCSP64	X	-	-	-
WLCSP49	X	-	-	-

1. There is no change required from an application moving from STM32L486xx/476xx microcontrollers to STM32L443xx/433xx microcontrollers. For a migration from STM32L443xx/433xx microcontrollers to STM32L486xx/476xx microcontrollers, the PH3 GPIO is lost. Note that there is no alternate function attached to this IO for the STM32L443xx/433xx microcontrollers.
2. This package is not available for this microcontrollers since the VLCD pin is not present. The feature is introduced for the 32-pin package for the STM32L442xx, STM32L432xx and STM32L431xx microcontrollers.
3. Only for the STM32L476xx microcontrollers.

1.1.1 LQFP100 package

Figure 1. LQFP100 pinout differences



For the highlighted (blue) terminals, BOOT0 pin for the STM32L486Vx/476Vx microcontrollers is replaced by a BOOT0 pin shared with a GPIO for the STM32L443Vx/433Vx microcontrollers, in order to offer a maximum of flexibility if managing the BOOT0 function by option bytes for these last products.

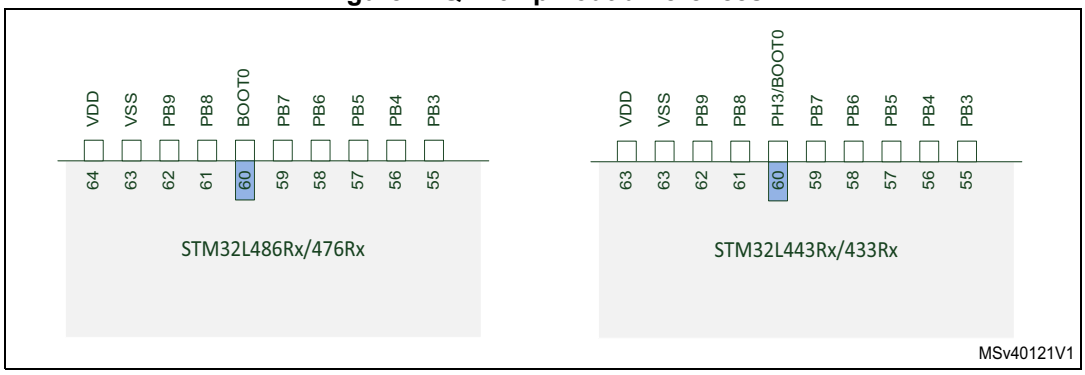
By default, the STM32L443Vx/433Vx microcontrollers are configured to use this pin as boot0 pin like for the STM32L486Vx/476Vx microcontrollers, in order to keep direct compatibility with the STM32L486Vx/STM32L76Vx PCB.

Table 3. List of LQFP100 pinout differences

Terminal	STM32L486Vx/476Vx	STM32L443Vx/433Vx
94	BOOT0	PH3/BOOT0

1.1.2 LQFP64 package

Figure 2. QFP64 pinout differences



For the highlighted (blue) terminals, BOOT0 pin for the STM32L486Rx/476Rx microcontrollers is replaced by a BOOT0 pin shared with a GPIO for the STM32L443Rx/433Rx microcontrollers, in order to offer a maximum of flexibility if managing the BOOT0 function by option bytes for these last products.

By default, the STM32L443Rx/433Rx microcontrollers are configured to use this pin as boot0 pin like for the STM32L486Rx/476Rx microcontrollers, in order to keep direct compatibility with the STM32L486Rx/476Rx PCB.

Table 4. List of LQFP64 pinout differences

Terminal	STM32L486Vx/476Vx	STM32L443Vx/433Vx
60	BOOT0	PH3/BOOT0

2 Peripheral migration guide

2.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals which can be classified in three categories:

1. Peripherals which are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
2. Peripherals which are shared by all products but have only minor differences (in general to support new features), so migration from one product to another is very easy and does not need any significant new development effort.
3. Peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, migration will require new development at application level.

Table 5 summarizes the available peripherals and their compatibility for the STM32L486xx/476xx and STM32L443xx/433xx microcontrollers.

Table 5. Peripheral compatibility analysis between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers

Peripherals		STM32L443xx/ STM32L433xx	STM32L486/ STM32L476xx	Compatibility	
				Software	Comments
Flash memory(1)	Size (byte)	256 K	1 M	-	-
	Bank	Single	Dual	-	-
SRAM (Kbyte)	SRAM1	48	96	-	The SRAM2 may be contiguous to the SRAM1 (physical address is still in 0x1000 0000) in the STM32L443xx/433xx microcontrollers only
	SRAM2(2)	16	32	-	
FMC (external memory controller for static memory)		NO	YES	-	-
QUADSPI(3)		YES	YES	YES	Dual flash mode features added + 1 additional bit DHHC to delay data output into the STM32L443xx/433xx microcontrollers only

Table 5. Peripheral compatibility analysis between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers (continued)

Peripherals		STM32L443xx/ STM32L433xx	STM32L486/ STM32L476xx	Compatibility	
				Software	Comments
Timers[4]	Advanced control	1 (16-bit)	2 (16-bit)	YES	-
	General purpose	2 (16-bit) 1 (32-bit)	5 (16-bit) 2 (32-bit)	YES YES	Infrared feature is using TIMER15 + 16 instead of TIMER16 +17 (because there is no timer 17). -
	Basic	2 (16-bit)	2 (16-bit)	YES	-
	Low power	2 (16-bit)	2 (16-bit)	YES	-
	Systick timer	1	1	YES	-
	Independent watchdog timer	1	1	YES	-
	Window watchdog timer	1	1	YES	-
Communication interfaces	SPI	3	3	YES	-
	I2C	3	3	YES	-
	USART UART LPUART	3 0 1	3 2 1	YES - YES	Additional features[5] - -
	SAI	1	2	YES	-
	CAN	1	1	YES	-
	USB	FS device with clock recovery	OTG FS without clock recovery	NO	The USB peripheral is completely different as well as memory map for the peripheral Additional clock source (HSI48).
	SDMMC	YES	YES	YES	Additional clock source (HSI48)
	SWPMI	YES	YES	YES	-
RTC		YES	YES	YES	APB clock control added (see RCC)[6]
Tamper pins		YES up to 3	YES up to 3	YES	-
LCD		YES	YES	YES	-
Random generator		YES	YES	YES	Additional clock source (HSI48)

Table 5. Peripheral compatibility analysis between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers (continued)

Peripherals		STM32L443xx/ STM32L433xx	STM32L486/ STM32L476xx	Compatibility	
				Software	Comments
GPIOs wake up pins I/Os down to 1.08 V		YES up to 83 YES up to 5 NO	YES up to 114 YES up to 5 YES up to 14	YES YES -	Additional I/O PH3 multiplexed with BOOT0(7)
Capacitive sensing		YES up to 21	YES up to 24	YES	-
DFSDM		NO	YES	-	-
12-bit ADC	Instance	1	3	MOSTLY (8)	Internal channel connections mapping changes slightly
	number of channels	16	24		
12-bit DAC		2	2	YES	-
Internal voltage reference buffer		1	1	YES	VREFBUF is disabled for package lower than 100-pin
Analog comparator		2	2	YES	-
operational amplifiers		1	2	YES	-
EXTI		YES	YES	YES	-
RCC		YES	YES	YES	New bit: – To stop the APB clock of the RTC keeping ON the RTC kernel clock in sleep or run modes – New HSI48 to manage the clock recovery for USB. It can be the clock source for the RNG and the SDMMC as well – HSI16 can be connected to SAI when there is no PLL ON (audio flow detection) – MCO can also output HSI48 – PLL P dividers – More bit to calibrate HSITRIM
PWR(9)		YES	YES	YES	No more power voltage monitoring on V_{DDIO2} (PVM2) Pull-up/pull-down control bit for stand-by mode for PH3
SYSCFG(10)		YES	YES	YES	SRAM2 write protection area reduced due to lower SRAM2 size

1. Refer to the *Section 2.3* for more details
2. Refer to the *Section 2.5* for more details
3. Refer to the *Section 2.6* for more details

4. Refer to the *Section 2.11* for more details
5. Refer to the *Section 2.12* for more details
6. Refer to the *Section 2.13* for more details
7. Refer to the *Section 2.14* for more details
8. Refer to the *Section 2.18* for more details
9. Refer to the *Section 2.9* for more details
10. Refer to the *Section 2.10* for more details

Most of known bugs for the STM32L486xx/476xx microcontrollers have been corrected for the STM32L443xx/433xx microcontrollers. Please refer to the corresponding product erratasheets to find out the remaining bugs.

2.2 Register boundary addresses of peripherals

Table 6 compares the peripherals register boundary addresses for STM32L443xx/433xx versus STM32L486xx/476xx microcontrollers.

Table 6. Peripherals register boundary addresses comparison

Peripheral	Bus	STM32L443xx/433xx base address	STM32L486xx/476xx base address
OTG_FS	AHB2	NA	0x50000000 - 0x5003FFFF
GPIOG	AHB2	NA	0x48001800 - 0x48001BFF
GPIOF	AHB2	NA	0x48001400 - 0x480017FF
DFSDM	APB2	NA	0x40016000 - 0x400163FF
SAI2	APB2	NA	0x40015800 - 0x40015BFF
TIM17	APB2	NA	0x40014800 - 0x40014BFF
TIM8	APB2	NA	0x40013400 - 0x400137FF
USB SRAM	APB1	0x40006C00 - 0x40006FFF	NA
USB FS	APB1	0x40006800 - 0x40006BFF	NA
CRS	APB1	0x40006000 - 0x400063FF	NA
UART5	APB1	NA	0x40005000 - 0x400053FF
UART4	APB1	NA	0x40004C00 - 0x40004FFF
TIM5	APB1	NA	0x40000C00 - 0x40000FFF
TIM4	APB1	NA	0x40000800 - 0x40000BFF
Color key: = not applicable			

2.3 Flash memory

The flash interface differences between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers are indicated in *Table 7*.

Table 7. Flash memory comparison

Flash	STM32L443xx/433xx	STM32L486xx/476xx
Main/Program memory	0x08000000 up to 0x0803FFFF	0x08000000 up to 0x080FFFFF
	Up to 256 Kbyte Split in 1 bank 128 pages of 2 KB	up to 1Mbyte Split in 2 banks 256 pages of 2 KB per bank
Features	Single bank boot	Read while write (RWW) Dual bank boot
Wait states	Up to 4 (depending on the supply voltage and the frequency)	
Flash empty check	YES	NO
Protections	Write protection: 2 areas 1 PCROP area	Write protection: 2 areas per bank 1 PCROP area per bank
One Time Programmable (OTP) memory	1 Kbyte	1 Kbyte
Interface	0x4002 2000 - 0x4002 23FF	

Table 7. Flash memory comparison (continued)

Flash	STM32L443xx/433xx	STM32L486xx/476xx
Option bytes	0x1FFF 7800 - 0x1FFF 780F	Bank 1: 0x1FFF 7800 - 0x1FFF 780F Bank 2: 0x1FFF F800 - 0x1FFF F80F
	nBOOT0	NA
	nSWBOOT0	NA
	SRAM2_RST	SRAM2_RST
	SRAM2_PE	SRAM2_PE
	nBOOT1	nBOOT1
	NA	DUALBANK
	NA	BFB2
	WWDG_SW	WWDG_SW
	IWDG_STDBY	IWDG_STDBY
	IWDG_STOP	IWDG_STOP
	IWDG_SW	IWDG_SW
	nRST_SHDW	nRST_SHDW
	nRST_STDBY	nRST_STDBY
	nRST_STOP	nRST_STOP
	BOR_LEV	BOR_LEV
	RDP	RDP
	PCROP1_STRT	PCROP1_STRT
	PCROP1_END	PCROP1_END
	WRP1A_STRT	WRP1A_STRT
	WRP1A_END	WRP1A_END
	WRP1B_STRT	WRP1B_STRT
	WRP1B_END	WRP1B_END
	NA	PCROP2_STRT
	NA	PCROP2_END
	NA	WRP2A_STRT
	NA	WRP2A_END
	NA	WRP2B_STRT
	NA	WRP2B_END
Color key: = not applicable		

Table 8 to *Table 11* show in pink which are the new bit specified for the STM32L443xx/433xx microcontrollers, and in green the ones defined in the STM32L486xx/476xx microcontrollers only.

Table 8. User and read protection option bytes(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	nBOOT0	nSWBOOT0	SRAM2_RST	SRAM2_PE	nBOOT1	Res	DUALBANK	BFB2	WWDG_SW	IWDG_STDBY	IWDG_STOP	IWDG_SW
-	-	-	-	r	r	r	r	r	-	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	nRST_SHDW	nRST_STDBY	nRST_STOP	Res	BOR_LEV[2:0]			RDP[7:0]							
-	r	r	r	-	r	r	r	r	r	r	r	r	r	r	r

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.
Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

The STM32L443xx/433xx microcontrollers embed a new features named “Flash empty check”. When the device boots from flash, a hardware mechanism can detect if the flash is empty or not. If the flash is not empty and if the user wants to boot from flash, the device will boot from flash. If the flash is empty (@0x08000 0000 equal to 0xFFFF FFFF), the device will be forced to boot from the system flash and not the main flash as requested.

Table 9. FLASH_SR register (1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	PEMPTY	BSY
-	-	-	-	-	-	-	-	-	-	-	-	-	-	rs	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPTVERR	RDERR	Res	Res	Res	Res	FASTERR	MISERR	PGSERR	SIZERR	PGAERR	WRPERR	PROGERR	Res	OPERR	EOP
rc_w1	rc_w1	-	-	-	-	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	-	rc_w1	rc_w1

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

Table 10. FLASH_CR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK	OPTLOCK	Res	Res	OBL_LAUNCH	RDERRIE	ERRIE	EOPIE	Res	Res	Res	Res	Res	FSTPG	OPTSTRT	STRT
rs	rs	-	-	rc_w1	rw	rw	rw	-	-	-	-	-	rw	rs	rs
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MER2	Res	Res	Res	BKER	PNB[7:0]								MER1	PER	PG
rw	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

Table 11. FLASH_ECCR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ECCD	ECCC	Res	Res	Res	Res	Res	ECC CIE	Res	Res	Res	SYSF_ ECC	BK_ ECC	ADDR_ECC[18:16]		
rc_w1	rc_w1	-	-	-	-	-	rw	-	-	-	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_ECC[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

2.4 Boot modes

The boot mode selection changes slightly between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers. The aim of this improvement is to share BOOT0 input pin with a GPIO (PH3) and to add option bits to choose if BOOT0 value is coming from the IO pin or from the option bit value. The pink text highlights what is new in STM32L443xx/433xx microcontrollers.

Table 12. STM32L443xx/433xx microcontrollers boot modes(1)

Boot memory space	nBOOT1 option bit	nBOOT0 option bit	BOOT0 pin (PH3)	nSWBOOT0 option bit	Main flash empty(2)
Main flash	don't care	don't care	0	1	0
System flash	don't care	don't care	0	1	1
Main Flash	don't care	1	don't care	0	don't care
embedded SRAM1	0	don't care	1	1	don't care
embedded SRAM1	0	0	don't care	0	don't care
system flash	1	don't care	1	1	don't care
system flash	1	0	don't care	0	don't care

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.
2. Please refer to *Section 2.3* to get more details.

Table 13. STM32L486xx/476xx microcontrollers boot modes

Boot memory space	BOOT1	BOOT0 pin
main flash	don't care	0
system flash	0	1
embedded SRAM1	1	1

2.5 SRAM2 memory

There are very few differences between the STM32L443xx/433xx and the STM32L486xx/476xx microcontrollers concerning the SRAM2 memory.

Table 14. SRAM2 features comparison

-	STM32L443xx/433xx	STM32L486xx/476xx
Size	16 KB	32 KB
address	0x1000 0000 - 0x1000 3FFF	0x1000 0000 - 0x1000 7FFF
Parity check	YES	YES
Write protection	YES - 1 KB granularity	YES - 1 KB granularity
Read protection	RDP	RDP
SRAM2 Erase	System reset or Software reset	System reset or Software reset
SRAM2 contiguous with SRAM1	YES	NO

The following STM32L486xx/476xx limitation has been fixed for the STM32L443xx/433xx microcontrollers: if a read occurs during an erase operation, the CPU will not be stalled and the value returned is deterministic and equal to 0x0000 0000

2.6 QUADSPI peripheral

The main difference between the STM32L443xx/433xx and the STM32L486xx/476xx QUADSPI peripheral is the dual flash mode that is available only on the STM32L443xx/433xx microcontrollers. This feature allows to read two serials memories simultaneously.

The number of QUADSPI alternate functions is higher on STM32L443xx/433xx microcontrollers, since there are five additional dedicated alternate functions for the second memory interface (BK2_NCS, BK2_IO0, BK2_IO1, BK2_IO2, BK2_IO3). This feature is not available on 32-pin packages. Please refer to the corresponding datasheets.

Table 15. STM32L443xx/433xx versus STM32L486xx/476xx microcontrollers QUADSPI comparison

QUADSPI features	STM32L443xx/433xx	STM32L486xx/476xx
Dual flash mode	YES	NO

Table 16 and *Table 17* highlight in pink the bits that are different between the STM32L443xx/433xx and the STM32L486xx/476xx microcontrollers.

Table 16. QUADSPI_CR register for the STM32L443xx/433xx microcontrollers(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRESCALER								PMM	APMS	Res	TOIE	SMIE	FTIE	TCIE	TEIE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	FTHRES				FSEL	DFM	Res	SSHIFT	TCEN	DMAEN	ABORT	EN
-	-	-	-	rw	rw	rw	rw	rw	rw	-	rw	rw	w1s	rw	w1s

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

Table 17. QUADSPI_CCR register for the STM32L443xx/433xx microcontrollers(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DDRM	DHHC	Res	SIOO	FMODE[1:0]		DMODE		Res	DCYC[4:0]					ABSIZE	
rw	rw	-	rw	rw	rw	rw	rw	-	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABMODE		ADSIZE		ADMODE		IMODE		INSTRUCTION[7:0]							
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

The bit DHHC, available only for the STM32L443xx/433xx microcontrollers, allows to delay the data on the data lines by 1/4 of a QUADSPI output clock cycle.

2.7 Interrupt vector

Table 18 presents differences between the STM32L443xx/433xx and the STM32L486xx/476xx microcontrollers, in terms of interrupt vectors.

Table 18. Interrupt vector differences between the STM32L443xx/433xx and STM32L486xx/476xx microcontrollers

Position	STM32L443xx/433xx	STM32L486xx/476xx
26	TIM1_TRG_COM	TIM1_TRG_COM/TIM17
29	NA	TIM3
30	NA	TIM4
42	NA	DFSDM3
43	NA	TIM8_BRK
44	NA	TIM8_UP
45	NA	TIM8_TRIG_COM
46	NA	TIM8_CC
47	NA	ADC3
48	NA	FMC
50	NA	TIM5
52	NA	UART4
53	NA	UART5
61	NA	DFSDM0
62	NA	DFSDM1
63	NA	DFSDM2
75	NA	SAI2

Table 18. Interrupt vector differences between the STM32L443xx/433xx and STM32L486xx/476xx microcontrollers (continued)

Position	STM32L443xx/433xx	STM32L486xx/476xx
82	CRS	NA
Color key: = not applicable		

2.8 Reset and Clock Control (RCC)

Table 19 highlights the main differences related to RCC (reset and clock controller) between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers.

Table 19. RCC differences between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers

Peripherals	STM32L443xx/433xx	STM32L486xx/476xx
	Clock sources	
USB FS	– MSI clock – PLL /Q – PLLSAI1 /Q – HSI48	NA
USB OTG FS	NA	– MSI clock – PLL /Q – PLLSAI1 /Q
RNG/SDMMC	– MSI clock – PLL /Q – PLLSAI1 /Q – HSI48	– MSI clock – PLL /Q – PLLSAI1 /Q
USARTs	USART1: – APB2 clock – HSI16 – LSE – SYSCLK USART 2 & 3: – APB1 clock – HSI16 – LSE – SYSCLK	
	NA	USART 4 & 5: – APB1 clock – HSI16 – LSE – SYSCLK

Table 19. RCC differences between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers (continued)

Peripherals	STM32L443xx/433xx	STM32L486xx/476xx
	Clock sources	
LPUART1	– APB1 clock – HSI16 – LSE – SYSCLK	
I2Cs	– APB1 – HSI16 – STSCLK	
SPIs	– APB2 Clock for SPI1 – APB1 clock for SPI2 and SPI3	
SAI1	– HSI16 for audio flow detection – PLLSAI1 clock /P divider – PLL clock /P divider	– PLLSAI1 clock /P divider – PLLSAI2 clock /P divider – PLL clock /P divider
SAI2	NA	– PLLSAI1 clock /P divider – PLLSAI2 clock /P divider – PLL clock /P divider
QUADSPI	– AHB clock	
IWDG	– LSI clock	
WWDG	– APB1 clock	
ADC	– SYSCLK – PLLSAI1 R divider	
SWPMI	– HSI16 clock – PB1 clock	
RTC	– HSE/32 – LSE – LSI – Register clock disabling (not the kernel one) in run or sleep modes – RTCAPBEN in RCC_APB1ENR1 register – RTCAPBSMEN in RCC_APB1SMENR1 register	– HSE/32 – LSE – LSI
LCD	– HSE/32 – LSE – LSI	

Table 19. RCC differences between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers (continued)

Peripherals	STM32L443xx/433xx	STM32L486xx/476xx
	Clock sources	
MCO	– LSI – LSE – SYSCLK – HSI16 – HSE – PLLCLK – MSI – HSI48	– LSI – LSE – SYSCLK – HSI16 – HSE – PLLCLK – MSI
PLL	2 PLLs (PLL, PLLSAI1)	3 PLLs (PLL, PLLSAI1, PLLSAI2)
PLLP divider	PLLSAI1_PDIV[4:0] from 2 to 31	PLLP: 7 or 17
HSI16	HSITRIM[6:0]	HSITRIM[4:0]
HSI48	RC with clock recovery used for USB/RNG/SDMMC	NA
Color key: = not applicable		

The modifications done at register level for the STM32L443xx/433xx microcontrollers are illustrated in pink text in *Table 20* whereas the bits present for the STM32L486xx/476xx microcontrollers and no more available into the STM32L443/433 microcontrollers are written in green text in the register map.

Table 20. RCC register map(1)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	RCC_CR	Res.	Res.	PLLSAI2RDY	PLLSAI2ON	PLLSAI1RDY	PLLSAI1ON	PLLRDY	PLLON	Res.	Res.	Res.	Res.	CSSON	HSEBYP	HSERDY	HSEON	Res.	Res.	Res.	Res.	HSIASFS	HSIRDY	HSIKERON	HSION	MSI RANGE [3:0]				MSIRGSEL	MSIPLLEN	MSIRDY	MSION
	Reset value	-	-	0	0	0	0	0	0	-	-	-	-	0	0	0	0	-	-	-	-	0	0	0	0	0	1	1	0	0	0	1	1
0x04	RCC_ICSCR	Res.	HSITRIM[6:0]							HSICAL[7:0]								MSITRIM[7:0]								MSICAL[7:0]							
	Reset value	-	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
0x08	RCC_CFGR	Res.	MCO PRE [2:0]			MCOSEL [3:0]				Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	STOPWUCK	Res.	PPRE2 [2:0]			PPRE1 [2:0]			HPRE [3:0]				SWS [1:0]		SW [1:0]	
	Reset value	-	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	RCC_PLL CFGR	PLLP DIV[4:0]					PLLR [1:0]		PLLREN	Res.	PLLQ [1:0]		PLLQEN	Res.	Res.	PLLP	PLLPEN	Res.	PLLN [6:0]							Res.	PLLM [2:0]			Res.	Res.	PLL SRC [1:0]		
	Reset value	0	0	0	0	0	0	0	0	-	0	0	0	-	-	0	0	-	0	0	1	0	0	0	0	-	0	0	0	-	-	0	0

Table 20. RCC register map[1] (continued)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x10	RCC_ PLLSAI1 CFGR	PLLSAI1P DIV[4:0]					PLL SAI1R [1:0]		PLLSAI1REN	Res.	PLL SAI1 Q [1:0]		PLLSAI1QEN	Res.	Res.	PLLSAI1P	PLLSAI1PEN	Res.	PLLSAI1N [6:0]							Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	Reset value	0	0	0	0	0	0	0	0	-	0	0	0	-	-	0	0	-	0	0	1	0	0	0	0	-	-	-	-	-	-	-	-
0x14	RCC_ PLLSAI2 CFGR	Res.	Res.	Res.	Res.	Res.	PLL SAI2R [1:0]		PLLSAI2REN	Res.	PLL SAI2 Q [1:0]		PLLSAI2QEN	Res.	Res.	PLLSAI2P	PLLSAI2PEN	Res.	PLLSAI2N [6:0]							Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	Reset value	-	-	-	-	-	0	0	0	-	0	0	0	-	-	0	0	-	0	0	1	0	0	0	0	-	-	-	-	-	-	-	-
0x18	RCC_CIER	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HSI48RDYIE	LSECSSIE	Res.	PLLSAI2RDYIE	PLLSAI1RDYIE	PLLRDYIE	HSERDYIE	HSIRDYIE	MSIRDYIE	LSERDYIE	LSIRDYIE
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	-	0	0	0	0	0	0	0	0
0x1C	RCC_CIFR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HSI48RDYF	LSECSSF	CSSF	PLLSAI2RDYF	PLLSAI1RDYF	PLLRDYF	HSERDYF	HSIRDYF	MSIRDYF	LSERDYF	LSIRDYF
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0
0x20	RCC_CICR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HSI48RDYC	LSECSSC	CSSC	PLLSAI2RDYC	PLLSAI1RDYC	PLLRDYC	HSERDYC	HSIRDYC	MSIRDYC	LSERDYC	LSIRDYC
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0	0	0	0
0x28	RCC_ AHB1RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	TSCRST	Res.	Res.	Res.	Res.	CRCRST	Res.	Res.	FLASHRST	Res.	Res.	Res.	Res.	Res.	Res.	DMA2RST	DMA1RST
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	0	-	-	0	-	-	-	-	-	-	0	0
0x2C	RCC_ AHB2RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RNGRST	Res.	AESRST	Res.	Res.	ADCRST	OTGFSRST	Res.	Res.	Res.	Res.	GPIOHRST	GPIOGRST	GPIOFRST	GPIOERST	GPIODRST	GPIOCRST	GPIOBRST	GPIOARST
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	0	-	-	0	0	-	-	-	-	0	0	0	0	0	0	0	0
0x30	RCC_ AHB3RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	QSPIRST	Res.	Res.	Res.	Res.	Res.	Res.	Res.	FMCRST
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	-	-	0
0x38	RCC_ APB1RSTR1	LPTIM1RST	OPAMPRST	DAC1RST	PWRRST	Res.	USBFSRST	CAN1RST	CRSRST	I2C3RST	I2C2RST	I2C1RST	UART5RST	UART4RST	USART3RST	USART2RST	Res.	SPI3RST	SPI2RST	Res.	Res.	Res	Res.	Res.	LCDRST	Res.	Res.	Res.	TIM7RST	TIM6RST	TIM5RST	TIM4RST	TIM3RST	TIM2RST
	Reset value	0	0	0	0	.	0	0	0	0	0	0	0	0	0	0	-	0	0	-	-	-	-	-	-	-	-	0	0	0	0	0	0

Table 20. RCC register map[1] (continued)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x3C	RCC_ APB1RSTR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LPTIM2RST	Res.	Res.	SWPMI1RST	Res.	LPUART1RST
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	0	-	0
0x40	RCC_ APB2RSTR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DFSDMRST	Res.	SAI2RST	SAI1RST	Res.	Res.	TIM17RST	TIM16RST	TIM15RST	Res.	USART1RST	TIM8RST	SPI1RST	TIM1RST	SDMMCRST	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	SYSCFGRST
	Reset value	-	-	-	-	-	-	-	0	-	0	0	-	-	0	0	0	-	0	0	0	0	0	-	-	-	-	-	-	-	-	-	0
0x48	RCC_AHB1 ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	TSCEN	Res.	Res.	Res.	Res.	CRCEN	Res.	Res.	FLASHEN	Res.	Res.	Res.	Res.	Res.	Res.	DMA2EN	DMA1EN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	0	-	-	1	-	-	-	-	-	-	0	0
0x4C	RCC_AHB2 ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RNGEN	Res.	AESEN	Res.	Res.	ADCEN	OTGFSEN	Res.	Res.	Res.	Res	GPIOHEN	GPIOGEN	GPIOFEN	GPIOEEN	GPIODEN	GPIOCEN	GPIOBEN	GPIOAEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	0	-	-	0	0	-	-	-	-	0	0	0	0	0	0	0	0
0x50	RCC_AHB3 ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	QSPIEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	FMCEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	-	-	-	-	-	0
0x58	RCC_ APB1ENR1	LPTIM1EN	OPAMPEN	DAC1EN	PWREN	Res.	USBFSEN	CAN1EN	CRSEN	I2C3EN	I2C2EN	I2C1EN	UART5EN	UART4EN	USART3EN	USART2EN	Res.	SP3EN	SPI2EN	Res.	Res.	WWDGEN	RTCAPBEN	LCDEN	Res.	Res.	Res.	Res.	TIM7EN	TIM6EN	TIM5EN	TIM4EN	TIM3EN	TIM2EN
	Reset value	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	-	0	0	-	-	0	1	0	-	-	-	0	0	0	0	0	0
0x5C	RCC_ APB1ENR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LPTIM2EN	Res.	Res.	SWPMI1EN	Res.	LPUART1EN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	0	-	-	0	-	0
0x60	RCC_ APB2ENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DFSDMEN	Res.	SAI2EN	SAI1EN	Res.	Res.	TIM17EN	TIM16EN	TIM15EN	Res.	USART1EN	TIM8EN	SPI1EN	TIM1EN	SDMMC1EN	Res.	Res.	Res.	FIREWALLEN	Res.	Res.	Res.	Res.	Res.	SYSCFGEN
	Reset value	-	-	-	-	-	-	-	0	-	0	0	-	-	0	0	0	-	0	0	0	0	0	-	-	-	0	-	-	-	-	-	0
0x68	RCC_ AHB1SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	TSCSMEN	Res.	Res.	Res.	Res.	CRCSMEN	Res.	SRAM1SMEN	FLASHSMEN	Res.	Res.	Res.	Res.	Res.	Res.	DMA2SMEN	DMA1SMEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	1	-	1	1	-	-	-	-	-	-	1	1

Table 20. RCC register map[1] (continued)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x6C	RCC_ AHB2SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RNGSMEN	Res.	AESSMEN	Res.	Res.	ADCFSSMEN	OTGFSSMEN	Res.	Res.	SRAM2SMEN	Res.	GPIOHSMEN	GPIOGSMEN	GPIOFSMEN	GPIOESMEN	GPIODSMEN	GPIOCSMEN	GPIOBSMEN	GPIOASMEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	1	-	-	1	1	-	-	1	-	1	1	1	1	1	1	1	1
0x70	RCC_ AHB3SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	QSPISMEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	FMCSEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	-	-	-	-	-	1
0x78	RCC_ APB1SM ENR1	LPTIM1SMEN	OPAMPSMEN	DAC1SMEN	PWRSMEN	Res.	USBFSSMEN	CAN1SMEN	CRSSMEN	I2C3SMEN	I2C2SMEN	I2C1SMEN	UART5SMEN	UART4SMEN	USART3SMEN	USART2SMEN	Res.	SP3SMEN	SPI2SMEN	Res.	Res.	WWDGSMEN	RTCAPBENSMEN	LCDSMEN	Res.	Res.	Res.	TIM7SMEN	TIM6SMEN	TIM5SMEN	TIM4SMEN	TIM3SMEN	TIM2SMEN
	Reset value	1	1	1	1	-	1	1	1	1	1	1	1	1	1	1	-	1	1	-	-	1	1	1	-	-	-	1	1	1	1	1	1
0x7C	RCC_ APB1SM ENR2	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LPTIM2SMEN	Res.	Res.	SWPMI1SMEN	Res.	LPUART1SMEN
	Reset value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1	-	-	1	-	1
0x80	RCC_ APB2SMENR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DFSDMSMEN	Res.	SAI2SMEN	SAI1SMEN	Res.	Res.	TIM17SMEN	TIM16SMEN	TIM15SMEN	Res.	USART1SMEN	TIM8SMEN	SPI1SMEN	TIM1SMEN	SDMMCSMEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	SYSCFGSMEN
	Reset value	-	-	-	-	-	-	-	1	-	1	1	-	-	1	1	1	-	1	1	1	1	1	-	-	-	-	-	-	-	-	-	-	1
0x88	RCC_CCIPR	DFSDMSEL	SWPMI1SEL	ADCSEL		CLK48SEL		SAI2SEL		SAI1SEL		LPTIM2SEL		LPTIM1SEL		I2C3SEL		I2C2SEL		I2C1SEL		LPUART1SEL		USART5SEL		USART4SEL		USART3SEL		USART2SEL		USART1SEL	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x90	RCC_BDCR	Res.	Res.	Res.	Res.	Res.	Res.	LSCOSEL	LSCOEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	BDRST	RTCEN	Res.	Res.	Res.	Res.	Res.	RTC SEL [1:0]		LSECSSD		LSECSSON	LSE DRV [1:0]		LSEBYP	LSERDY	LSEON
	Reset value	-	-	-	-	-	-	0	0	-	-	-	-	-	-	-	0	0	-	-	-	-	-	0	0	-	0	0	0	0	0	0	0
0x94	RCC_CSR	LPWRSTF	WWDGRSTF	IWDGRSTF	SFTRSTF	BORRSTF	PINRSTF	OBLRSTF	FIREWALLRSTF	RMVF	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	MSIS RANGE[3:0]				Res.	Res.	Res.	Res.	Res.	Res.	LSIRDY	LSION
	Reset value	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	0	1	1	0	-	-	-	-	-	-	0	0

Table 20. RCC register map(1) (continued)

Off-set	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x98	RCC_CRRCR	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	HSI48CAL[8:0]									Res	Res	Res	Res	Res	HSI48RDY	HSI48ON
	Reset value																	X	X	X	X	X	X	X	X	X						0	0

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.
Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

CLK48SEL = 0x00 into the RCC_CCIPR register selects now HSI48 as 48 MHz clock source for USB, RNG or SDMMC in the STM32L443xx/433xx microcontrollers.

2.9 Power controller

Table 21 shows the PVM differences between the STM32L443xx/433xx and the STM32L486xx/476xx microcontrollers

Table 21. PVM differences between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers

PVM	STM32L443xx/433xx	STM32L486xx/476xx
PVM1	Power: VDDUSB VPVM1 (Around 1.2V) EXTI line 35	
PVM2	NA	Power: VDDIO2 VPVM2 (Around 0.9V) EXTI line 36
PVM3	Power: VDDA VPVM3 (Around 1.65V) EXTI line 37	
PVM4	Power: VDDA VPVM4 (Around 2.2V) EXTI line 38	
Color key: = not applicable		

The green text from the *Table 22* to the *Table 25* presents the bit available in the STM32L486xx/476xx microcontrollers only. The text in pink illustrates the bit available only in the STM32L443xx/433xx microcontrollers.

Table 22. PWR_CR2 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	USV	IOSV	Res	PVM4	PVM3	PVM2	PVM1	Res	Res	Res	SYSCFG SMEN
-	-	-	-	-	rw	rw	-	rw	rw	rw	rw	-	-	-	rw

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

Table 23. PWR_SR2 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PVMO4	PVMO3	PVMO2	PVMO1	PVDO	VOSF	REGLPF	REGLPS	Res	Res	Res	Res	Res	Res	Res	Res
r	r	r	r	r	r	r	r	-	-	-	-	-	-	-	-

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

There are no more PWR_PUCRF, PWR_PDCRF and PWR_PUCRG, PWR_PDCRG registers in the STM32L443xx/433xx microcontrollers.

Table 24. PWR_PUCRH register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	PU3	Res	PU1	PU0
-	-	-	-	-	-	-	-	-	-	-	-	rw	-	rw	rw

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

Table 25. PWR_PDCRH register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	PD3	Res	PD1	PD0
-	-	-	-	-	-	-	-	-	-	-	-	rw	-	rw	rw

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

2.10 System configuration controller (SYSCFG)

Table 26 and *Table 27* shows in green the bit only available in the STM32L486xx/476xx microcontrollers.

Table 26. SYSCFG_MEMRMP register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	FB_MODE	Res	Res	Res	Res	Res	MEM_MODE		
-	-	-	-	-	-	-	rw	-	-	-	-	-	rw	rw	rw

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

Table 27. SYSCFG_SWPR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P31WP	P30WP	P29WP	P28WP	P27WP	P26WP	P25WP	P24WP	P23WP	P22WP	P21WP	P20WP	P19WP	P18WP	P17WP	P16WP
rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15WP	P14WP	P13WP	P12WP	P11WP	P10WP	P9WP	P8WP	P7WP	P6WP	P5WP	P4WP	P3WP	P2WP	P1WP	P0WP
rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs	rs

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

2.11 Timers peripherals

Few differences are listed in this section between the STM32L443xx/433xx and the STM32L486xx/476xx microcontrollers. There are mainly linked to the number of timers present into each product.

Table 28 below provides the timers availability for each product.

Table 28. Timers availability depending on products

Timers	STM32L443xx/433xx	STM32L486xx/476xx
TIM1 - Advanced control	YES	
TIM8 - Advanced control	NO	YES
TIM2 - General purpose 32-bit timers	YES	
TIM3 - General purpose 16-bit timers	NO	YES
TIM4 - General purpose 16-bit timers	NO	YES
TIM5 - General purpose 32-bit timers	NO	YES

Table 28. Timers availability depending on products (continued)

Timers	STM32L443xx/433xx	STM32L486xx/476xx
TIM6 - Basic timer (16-bit)	YES	
TIM7 - Basic timer (16-bit)	YES	
TIM15 - General purpose 16-bit timer	YES	
TIM16 - General purpose 16-bit timer	YES	
TIM17 - General purpose 16-bit timer	NO	YES
Systick timer	YES	
WWDG timer	YES	
IWDG timer	YES	
LPTIMER1	YES	
LPTIMER2	YES	

There are few differences concerning the internal connections between the timers to fit specific features depending on the products.

Infrared interface (IRTIM)

Table 29 illustrates the infrared interface comparison between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers.

Table 29. Infrared interface comparison between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers

-	STM32L443xx/433xx	STM32L486xx/476xx
Infrared interface (IRTIM)	TIM15_OC1 + TIM16_OC1	TIM16_OC1 + TIM17_OC1

TIMER16

TIM16 input capture 1 multiplexer receives more inputs within the STM32L443xx/433xx microcontrollers than within the STM32L486xx/476xx microcontrollers. *Table 30* shows the differences. It is mainly linked to the fact that the STM32L443xx/433xx microcontrollers do not have TIM17. In order to keep all the functions available in STM32L486xx/476xx microcontrollers, the signals connected to TIM17 input capture 1 are added to TIM16 input capture 1 in the STM32L443xx/433xx microcontrollers.

Table 30. Input capture 1 multiplexer comparison between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers

Timers	STM32L443xx/433xx	STM32L486xx/476xx
TIM17	NA	I/O MSI HSE/32 MCO
TIM16	I/O LSI LSE RTC wakeup MSI HSE/32 MCO	I/O LSI LSE RTC wakeup
Color key: = not applicable		

Table 31 presents with pink text the modifications brought in the STM32L443xx/433xx microcontrollers. The TI1_RMP[2:0] is extended by one additional bit to cover the remap of the input captures connected to the timer 17 in the STM32L486xx/476xx microcontrollers, but that are no more present in the STM32L443xx/433xx microcontrollers.

Table 31. TIM16_OR1 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	TI1_RMP[2:0]		
-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

2.12 USART peripheral

The difference between the STM32L443xx/433xx and the STM32L486xx/476xx microcontrollers is mainly due to the USART additional feature supporting the ISO7816-3 smartcard protocol.

Table 32, *Table 33* and *Table 34* presents with pink text the new bits present in the STM32L443xx/433xx microcontrollers registers compared to the STM32L486xx/476xx microcontrollers.

Table 32. USARTx_CR3 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	TCBGTIE	Res	WUFIE	WUS		SCARCNT[2:0]			Res
-	-	-	-	-	-	-	rw	-	rw	rw	rw	rw	rw	rw	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEP	DEM	DDRE	OVRDIS	ONEBIT	CTSIE	CTSE	RTSE	DMAT	DMAR	SCEN	NACK	HDSEL	IRLP	IREN	EIE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

Table 33. USARTx_ISR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	TCBGT	Res	Res	REACK	TEACK	WUF	RWU	SBKF	CMF	BUSY
-	-	-	-	-	-	r	-	-	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABRF	ABRE	Res	EOBF	RTOF	CTS	CTSIF	LBDF	TXE	TC	RXNE	IDLE	ORE	NF	FE	PE
r	r	-	r	r	r	r	r	r	r	r	r	r	r	r	r

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

Table 34. USARTx_ICR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	WUCF	Res	Res	CMCF	Res
-	-	-	-	-	-	-	-	-	-	-	w	-	-	w	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	EOBCF	RTOCF	Res	CTSCF	LBDCF	TCBGTCF	TCCF	Res	IDLECF	ORECF	NCF	FECF	PECF
-	-	-	w	w	-	w	w	w	w	-	w	w	w	w	w

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

2.13 RTC peripheral

The power consumption is optimized in the STM32L443xx/433xx versus the STM32L486xx/476xx microcontrollers thanks to the RTC kernel clock and APB clock that can be controlled independently in STM32L443xx/433xx microcontrollers. Please refer to the *Section 2.8* for more details.

2.14 GPIO controller

The VDDIO2 with independent power supply rail (down to 1.08V) that is present for STM32L486xx/476xx microcontrollers, is not available for STM32L443xx/433xx microcontrollers. Hence, the I/O PORT G that is present for STM32L486xx/476xx microcontrollers, is not available for STM32L443xx/433xx microcontrollers.

Beside, there is an additional I/O on the port H (PH3) in the STM32L443xx/433xx microcontrollers. This general purpose I/O is sharing the BOOT0 feature which was a dedicated I/O in the STM32L486xx/476xx microcontrollers. For more details about this additional boot feature, please refer to the *Section 2.4*.

2.15 LCD controller

Table 35 presents the LCD availability depending on the packages and the products.

Table 35. LCD controller availability depending on products

LCD availability	STM32L443xx/433xx	STM32L486xx/476xx
Packages	All packages except for the UFQFN32 package for which the VLCD pin is not present	All packages

2.16 Interconnect matrix

The STM32L443xx/433xx microcontrollers interconnect matrix is a reduced subset of the STM32L486xx/476xx interconnect matrix since the number of peripherals is decreased. Please refer to the *Table 5* to figure out the differences between the products.

2.17 DMA

There are two DMA master interfaces for the STM32L443xx/433xx microcontrollers as well as for the STM32L486xx/476xx microcontrollers. The DMA channels connections corresponding to peripherals that are present only for STM32L486xx/476xx microcontrollers, are left free for STM32L443xx/433xx microcontrollers.

2.18 12-bit ADC

Table 5 shows the number of ADC instances depending on the products.

The STM32L443xx/433xx microcontrollers have a single ADC whereas the STM32L486xx/476xx microcontrollers have 3 ADCs. Some internal connections that are spread over the 3 ADCs for the STM32L486xx/476xx microcontrollers are redirected to other input channels on the STM32L443xx/433xx microcontrollers. The aim is to propose the same internal hardware connections to the ADC whatever the number of instances (DACs, temperature sensor, VBAT/3, VREFINT). They are presented into *Table 36*.

Table 36. ADC analog input channels comparison between STM32L443xx/433xx and STM32L486xx/476xx microcontrollers

-	STM32L443xx/433xx	STM32L486xx/476xx
Analog inputs from the I/O	Channel 1 to 16 - ADC1	Channel 1 to 16 - ADC1 & ADC2 Channel 1 to 4 - ADC3 Channel 6 to 13 - ADC3
VBAT/3	Channel 18 - ADC1	Channel 18 - ADC1 Channel 18 - ADC3
VREBUF	Channel 0 - ADC1	
Temperature sensor	Channel 17 - ADC1	Channel 17 - ADC1 Channel 17 - ADC3
DAC1	Channel 17 - ADC1	Channel 17 - ADC2 Channel 14 - ADC3
DAC2	Channel 18 - ADC1	Channel 18 - ADC2 Channel 15 - ADC3

Table 37 highlights in pink the 2 bit names that are specific to STM32L443xx/433xx microcontrollers. These bits are called VBATEN and TSEN in the STM32L486xx/476xx microcontrollers. They are fully software compatible because for the STM32L443xx/433xx microcontrollers, when the bit CH18SEL or CH17SEL is set, the VBAT channel or temperature sensor channel are enabled respectively like for the STM32L486xx/476xx microcontrollers. When these bits are kept cleared, DAC2 and DAC1 are connected to the ADC input channel 18 and 17 for the STM32L443xx/433xx microcontrollers whereas nothing is connected for the STM32L486xx/476xx microcontrollers.

Table 37. ADC1_CCR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	CH18SEL	CH17SEL	VREFEN	PRESC[3:0]				CKMODE[1:0]	
-	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDMA[1:0]		DMA_CFG	Res	DELAY[3:0]				Res	Res	Res	DUAL[4:0]				
rw	rw	rw	-	rw	rw	rw	rw	-	-	-	rw	rw	rw	rw	rw

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

2.19 Comparators

For STM32L443xx/433xx microcontrollers with low pin count packages (down to 32-pins), some comparator inputs and or outputs have more remapping capabilities than for STM32L486xx/476xx microcontrollers. STM32L443/433xx microcontrollers are fully compatible with STM32L486xx/476xx microcontrollers.

To cover the new remapping capabilities present in the STM32L443xx/433xx microcontrollers, the bits INMSEL in the COMPx_CSR register must be extended. Extension is supported thanks to the bits INMESEL in the COMPx_CSR register as

described in *Table 38* (pink text).

Table 38. COMPx_CSR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LOCK	VALUE	Res	Res	Res	INMESEL		Res	SCALEN	BRGEN	Res	BLANKING			HSYT	
rw	rw	-	-	-	rw	rw	-	rw	rw	-	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
POLARITY	Res	Res	Res	Res	Res	Res	INPSEL		INMSEL			PWRMODE		Res	EN
rw	-	-	-	-	-	-	rw	rw	rw	rw	rw	rw	rw	-	rw

1. Pink color highlights information that is available only for STM32L443xx/433xx microcontrollers.

2.20 Debug

For the debug module, the green text in *Table 39* and *Table 40* highlights the bits that are available only in the STM32L486xx/476xx microcontrollers. These bits correspond to timers that are not present in the STM32L443xx/433xx microcontrollers.

Table 39. DBGMCU_APB1FZR1 register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LPTIM1_STOP	Res	Res	Res	Res	Res	DBG_CAN_STOP	Res	DBG_I2C3_STOP	DBG_I2C2_STOP	DBG_I2C1_STOP	Res	Res	Res	Res	Res
rw	-	-	-	-	-	rw	-	rw	rw	rw	-	-	-	-	-
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	DBG_IWDG_STOP	DBG_WWDG_STOP	DBG_RTC_STOP	Res	Res	Res	Res	DBG_TIM7_STOP	DBG_TIM6_STOP	DBG_TIM5_STOP	DBG_TIM4_STOP	DBG_TIM3_STOP	DBG_TIM2_STOP
-	-	-	rw	rw	rw	-	-	-	-	rw	rw	rw	rw	rw	rw

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

Table 40. DBGMCU_APB2FZR register(1)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	DBG_TIM17_STOP	DBG_TIM16_STOP	DBG_TIM15_STOP
-	-	-	-	-	-	-	-	-	-	-	-	-	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	DBG_TIM8_STOP	Res	DBG_TIM1_STOP	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
-	-	rw	-	rw	-	-	-	-	-	-	-	-	-	-	-

1. Green color highlights information that is available only for STM32L486xx/476xx microcontrollers.

3 Revision history

Table 41. Document revision history

Date	Revision	Changes
10-May-2016	1	Initial release.