AN4807
Application note

Migrating between STM32F303 and STM32F302 line products

Introduction

For the designers of the STM32 microcontroller applications, being able to replace easily one microcontroller type by another in the same product family is an important asset. Migrating an application between the STM32F303 and STM32F302 line products is often needed, when the product requirements grow, putting extra demands on the memory size or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to another product with less memory and peripherals.

This application note analyzes the steps required to migrate from an existing STM32F302 or STM32F303 based design to any other STM32 device in the same line. It compares the STM32F302 and STM32F303 line products and highlights the differences between all the devices within the same line (STM32F303 or STM32F302).

The STM32F302 and STM32F303 line products are compatible, but few differences exist that could have an impact on the migration. All the most important information is in this application note.

To fully benefit from this application note, the user should be familiar with the STM32F3 microcontroller documentation available on *www.st.com*:

- STM32F302 reference manual (RM0365)
- STM32F303 reference manual (RM0316)
- STM32F302x6/8 datasheet
- STM32F302xB/C datasheet
- STM32F302xD/E datasheet
- STM32F303x6/8 datasheet
- STM32F303xB/C datasheet
- STM32F303xD/E datasheet

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1 STM32F302 line product differences

1.1 STM32F302 line product overview

Table 1 provides an overview of the STM32F302x6/8/B/C/D/E peripherals.

Table 1. STM32F302x6/8/B/C/D/E peripherals(1)

STM32F302 device		STM32F302x6/8	STM32F302xB/C	STM32F302xD/E
System				
Embedded SRAM size		Up to 16 Kbytes	Up to 40 Kbytes	Up to 64 Kbytes
SRAM parity check		N/A	Implemented only on the first 16 Kbytes	Implemented only on the first 32 Kbytes
MPU		N/A	✓	✓
Flash memory size		Up to 64 Kbytes	Up to 256 Kbytes	Up to 512 Kbytes
Direct memory access (DMA)	-	7-channel DMA controller	12-channel DMA controller	12-channel DMA controller
	GP-DMA1	✓	✓	✓
	GP-DMA2	N/A	✓	✓
FMC		N/A	N/A	✓
GPIO		Up to 51 fast I/Os	Up to 87 fast I/Os	Up to 115 fast I/Os
Analog				
Analog to digital converter (ADC) 5MSPS	-	1	2	2
	Number of channels	Up to 15 channels	Up to 17 channels	Up to 18 channels
	ADC1	✓	✓	✓
	ADC2	-	✓	✓
Available operational amplifiers (OPAMP)	-	1	2	2
	OPAMP1	-	✓	✓
	OPAMP2	✓	✓	✓
Digital to analog converter (DAC)	-	1 x 12-bit DAC channel	1 x 12-bit DAC channel	1 x 12-bit DAC channel
Comparators (COMP)	-	3 x ultra-fast comparators	4 x fast comparators	4 x ultra-fast comparators
	COMP1	-	✓	✓
	COMP2	✓	✓	✓
	COMP4	✓	✓	✓
	COMP6	✓	✓	✓

Table 1. STM32F302x6/8/B/C/D/E peripherals(1) (continued)

STM32F302 device		STM32F302x6/8	STM32F302xB/C	STM32F302xD/E
Touch Sensing		Up to 18 capacitive sensing channels supporting touch key, linear and rotary sensors	Up to 24 capacitive sensing channels supporting touch key, linear and rotary touch sensors	Up to 24 capacitive sensing channels supporting touch key, linear and rotary touch sensors
Communication				
I2C Available	-	3 x I^2Cs	2 x I^2Cs	3 x I^2Cs
	I2C1	✓	✓	✓
	I2C2	✓	✓	✓
	I2C3	✓	-	✓
USART/UART Available	-	3 x U(S)ARTs	5 x U(S)ARTs	5 x U(S)ARTs
	USART1	✓	✓	✓
	USART2	✓	✓	✓
	USART3	✓	✓	✓
	UART4	-	✓	✓
	UART5	-	✓	✓
SPI Available	-	2 x SPIs/2 x I2Ss	3 x SPIs/2 x I2Ss	4 x SPIs/2 x I2Ss
	SPI1	-	✓	✓
	SPI2/I2S2	✓	✓	✓
	SPI3/I2S3	✓	✓	✓
	SPI4	-	-	✓
USB 2.0 full-speed interface		✓with LPM support	✓	✓with LPM support
CAN 2.0B		✓	✓	✓
Infrared transmitter		✓	✓	✓
Timers				
General purpose/motor control/basic timer	-	Up to 9 timers	Up to 11 timers	Up to 11 timers
	TIMER1	✓	✓	✓
	TIMER2	✓	✓	✓
	TIMER3	-	✓	✓
	TIMER4	-	✓	✓
	TIMER6	✓	✓	✓
	TIMER15	✓	✓	✓

Table 1. STM32F302x6/8/B/C/D/E peripherals(1) (continued)

STM32F302 device		STM32F302x6/8	STM32F302xB/C	STM32F302xD/E
General purpose/motor control/basic timer	TIMER16	✓	✓	✓
	TIMER17	✓	✓	✓
	SysTick timer 24-bit down-counter	✓	✓	✓
	Watchdog timers	2 x watchdog timers (independent, window)	2 x watchdog timers (independent, window)	2 x watchdog timers (independent, window)
RTC	-	✓	✓	✓
Packages				
Available packages		WLCSP49 UFQFPN32 LQFP 64/48	LQFP 100/64/48 WLCSP100	LQFP 144/100/64 UFBGA100 WLCSP100

1. ✓= supported.

1.2 STM32F302 line product differences

1.2.1 Clock tree

When the HSI is selected as the PLL clock source, the maximum CPU clock can be reached:

- On the STM32F302x6/8/B/C devices, there is one bit PLLSRC (bit 16 in the RCC_CFGR register) dedicated to select the PLL clock source; and when the HSI is selected as the PLL clock source, the maximum CPU frequency that can be reached is 64 MHz.
- On the STM32F302xD/E devices, two bits (bit 15 and 16 in the RCC_CFGR register) are used in order to select the PLL clock source. The purpose is to add a configuration where the HSI is selected as the PLL clock source and 72 MHz CPU clock is reached.

Table 2. PLL clock source selection

Bit 15	Bit 16	Description
0	0	HSI/2 used as PREDIV1 entry and PREDIV1 forced to div by 2
0	1	HSI used as PREDIV1 entry (only on STM32F302xD/E)
1	0	HSE used as PREDIV1 entry
1	1	Reserved

1.2.2 Clock out capability

Compared to the STM32F302xB/C devices, on the STM32F302x6/8/D/E devices:

- One PLLNODIV bit in the RCC_CFGR register is added, its purpose is to control the divider bypass for a PLL clock input to the MCO.
- The MCO frequency can be reduced by a configurable divider, controlled by the MCOPRE [2..0] bits in the RCC_CFGR register.

Figure 1. STM32F302xB/C clock out capability

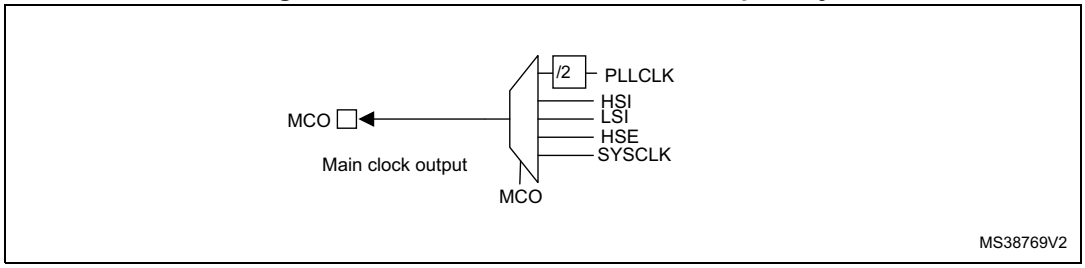
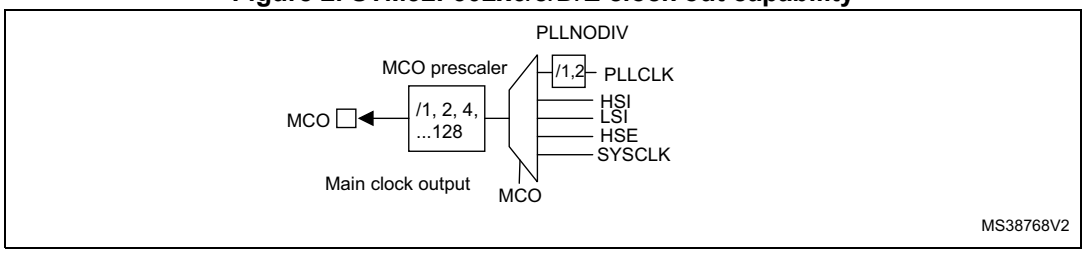


Figure 2. STM32F302x6/8/D/E clock out capability



1.2.3 Embedded SRAM

The SRAM in the STM32F302x6/8 devices does not support the hardware parity check; however the SRAM in the STM32F302xB/C/D/E devices supports the hardware parity check which is implemented on the first 16 Kbytes in the STM32F302xB/C devices and implemented on the first 32 Kbytes on the STM32F302xD/E devices.

1.2.4 SYSCFG

In the SYSCFG configuration register2 (SYSCFG_CFGR2): PVD_LOCK, SRAM_PARITY_LOCK and LOCKUP_LOCK bits are reset only by system reset on the STM32F302x6/8/D/E devices.

However on the STM32F302xB/C devices, these bits can be reset also by a reset coming from RCC (using the SYSCFGRST bit).

1.2.5 I/O and pinout

The STM32F302x6/8/B/C/D/E devices are pinout compatible except for the fact that PF4 in the STM32F302xB/C devices, is VSS in the STM32F302x6/8/D/E devices. Refer to *Figure 3* and *Figure 4*:

Figure 3. STM32F302xx LQFP64 pinout discrepancies

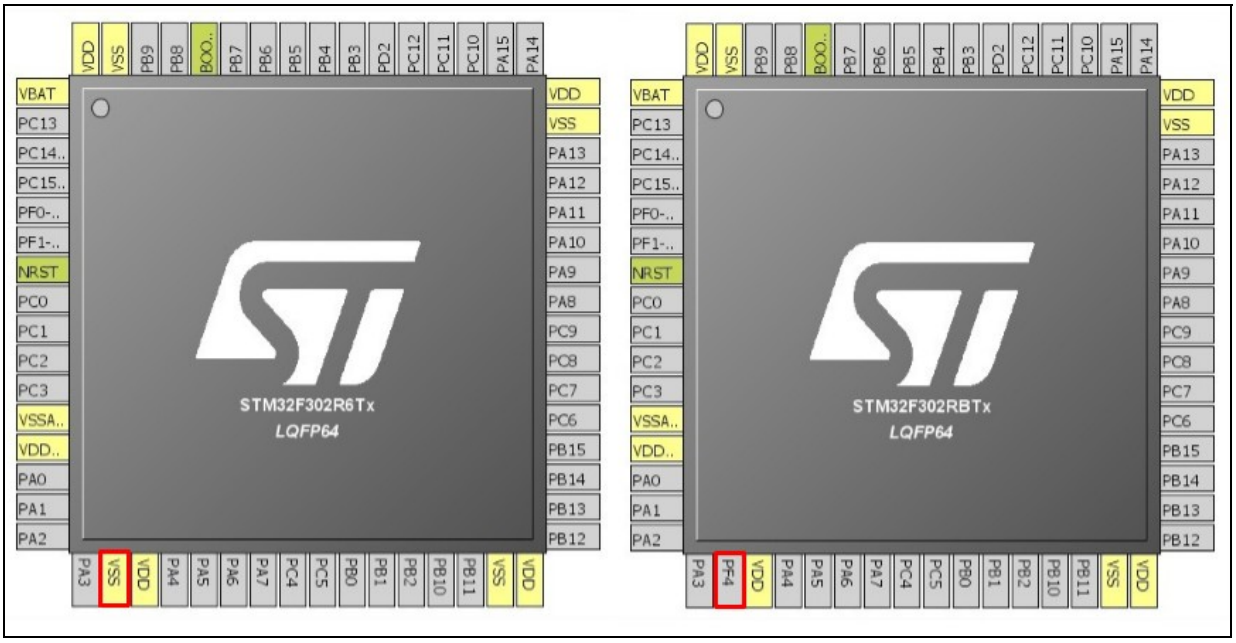
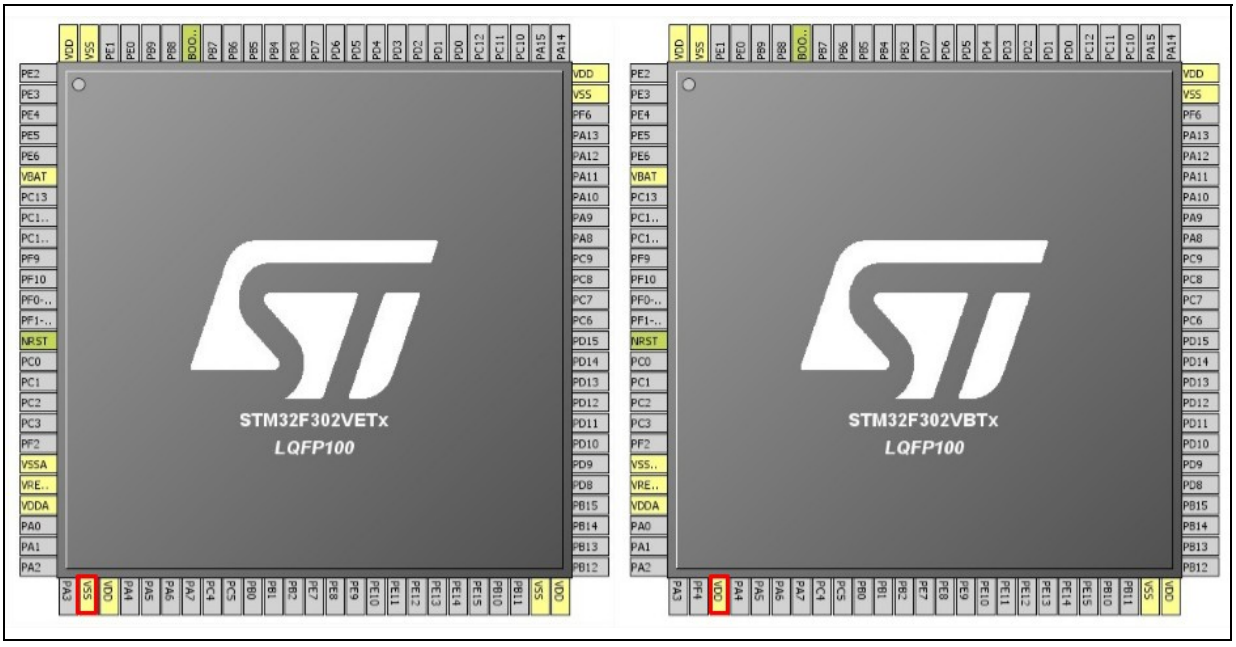


Figure 4. STM32F302xx LQFP100 pinout discrepancies



The GPIO LOCK feature is only available on Port A, B and D for the STM32F302xB/C devices. This feature is implemented for all GPIOs on the STM32F302x6/8/D/E devices.

Table 3 summarizes all added alternate functions in the STM32F302x6/8/D/E devices compared to the STM32F302xB/C devices.

Table 3. Alternate functions added

I/O and alternate function	Added function
PB8 (AF7)	USART3_Rx
PB9 (AF7)	USART3_Tx
PC0 (AF2)	TIM1_CH1
PC1 (AF2)	TIM1_CH2
PC2 (AF2)	TIM1_CH3
PC3 (AF2)	TIM1_CH4
PC4 (AF2)	TIM1_ETR
PC5 (AF2)	TIM15_BKIN
PA12 (AF5)	I2S_CKIN
PF0 (AF5)	SPI2_NSS/I2S2_WS
PF1 (AF5)	SPI2_SCK/I2S2_CK
PA10 (AF5)	SPI2_MISO/I2S2ext_SD
PA11 (AF5)	SPI2_MOSI/I2S2_SD
PB5 (AF8)	I2C3_SDA
PA8 (AF3)	I2C3_SCL
PC9 (AF3)	I2C3_SDA
PA9 (AF2)	I2C3_SMBAL

Note: The FMC is available only on the STM32F302xD/E devices. The corresponding alternate functions are not mentioned in Table 3.

1.2.6 Analog to Digital Converter (ADC)

Table 4 shows the mapping differences of ADC channels on the STM32F302 line products.

Table 4. ADC channel mapping differences

I/O	STM32F302x6/8	STM32F302xB/C	STM32F302xD/E
PA4	ADC1_IN5	ADC2_IN1	ADC2_IN1
PA5	-	ADC2_IN2	ADC2_IN2
PC4	-	ADC2_IN5	ADC2_IN5
PC5	-	ADC2_IN11	ADC2_IN11
PA6	ADC1_IN10	ADC2_IN3	ADC2_IN3
PB0	ADC1_IN11	-	-
PB1	ADC1_IN12	-	-
PB2	-	ADC2_IN12	ADC2_IN12

Table 4. ADC channel mapping differences (continued)

I/O	STM32F302x6/8	STM32F302xB/C	STM32F302xD/E
PB11	ADC1_IN14	-	ADC12_IN14
PB13	ADC1_IN13	-	-
PA7	ADC1_IN15	ADC2_IN4	ADC2_IN4

1.2.7 Digital to Analog Converter (DAC)

Table 5 lists the DAC external triggers.

Table 5. DAC external triggers

TSEL control bits			Devices	
2	1	0	STM32F302xB/C/D/E	STM32F302x6/8
0	0	0	TIM6_TRGO	
0	0	1	TIM3_TRGO (1)	Reserved
0	1	0	Reserved	
0	1	1	TIM15_TRGO	
1	0	0	TIM2_TRGO	
1	0	1	TIM4_TRGO	Reserved
1	1	0	EXTI_9	
1	1	1	SWTRIGx	

1. The DAC1_TRIG_RMP bit in the SYSCFG_CFGR1 register needs to be set by software.

1.2.8 Comparators

The STM32F302x6/8/D/E devices embed ultra-fast comparators while the STM32F302xB/C devices embed fast comparators.

Compared to the STM32F302xB/C devices, the comparators on the STM32F302x6/8/D/E devices:

- Do not support programmable speed/consumption mode: High speed mode only
- Do not support the hysteresis feature
- Have only one VINP input:
  - COMP2_INP: PA7
  - COMP4_INP: PB0
  - COMP6_INP: PB11
- Do not have COMP2_OUT on PA7
- Do not support the window mode

On the STM32F302x6/8/D/E devices, the comparators registers are reset only by system reset. However, on the STM32F302xB/C devices, they can be reset also by a reset from the RCC (using the SYSCFGRST bit).

1.2.9 Operational amplifier

The OPAMP register is reset only by system reset for both STM32F302x6/8/D/E and STM32F302xB/C devices. However, on the STM32F302xB/C devices, this register can be reset also by a reset from the RCC (using the SYSCFGRST bit).

1.2.10 Timer

Table 6 lists all the timers that can be clocked at 144 MHz in each device of the STM32F302 line.

Table 6. Timers available for STM32F302 line

Timers can be clocked at 144MHz(1)			
	STM32F302x6/8	**STM32F302xB/C**	**STM32F302xD/E**
TIMER1	✓	✓	✓
TIMER2	-	-	✓
TIMER3	-	-	✓
TIMER4	-	-	✓
TIMER6	-	-	-
TIMER15	✓	-	✓
TIMER16	✓	-	✓
TIMER17	✓	-	✓

1. ✓=supported.

Table 7 summarizes the interconnection of timer triggers.

Table 7. Interconnection of timer triggers

Slave timer	Product	ITR0	ITR1	ITR2	ITR3
1	STM32F302xB/C/D/E	15	2	3	4 or 17
	STM32F302x6/8	15	2	Reserved	17(1)
2	STM32F302xB/C/D/E	1	8	3	4
	STM32F302x6/8	1	Reserved	Reserved	Reserved
3	STM32F302xB/C/D/E	1	2	15	4
4	STM32F302xB/C/D/E	1	2	3	8
15	STM32F302xB/C/D/E	2	3	16	17
	STM32F302x6/8	2	Reserved	16	17

1. The TIM1_ITR3_RMP bit in the SYSCFG_CFGR1 register needs to be set by software.

1.2.11 USART/UART

Table 8 highlights the differences between the USART/UART available on the STM32F302 line.

Table 8. USART/UART discrepancies(1)

USART modes/ features	STM32F302x6/8		STM32F302xB/C			STM32F302xD/E		
	USART1	USART2/ USART3	USART1/ USART2/ USART3	UART4	UART5	USART1/ USART2/ USART3	UART4	UART5
Hardware flow control for modem	✓	✓	✓	-	-	✓	-	-
Continuous communication using DMA	✓	✓	✓	✓	-	✓	✓	-
Multiprocessor communication	✓	✓	✓	✓	✓	✓	✓	✓
Synchronous mode	✓	✓	✓	-	-	✓	-	-
Smartcard mode	✓(3)	-	✓(2)(3)	-	-	✓(4)	-	-
Single-wire half-duplex communication	✓	✓	✓	✓	✓	✓	✓	✓
IrDA SIR ENDEC block	✓	-	✓	✓	✓	✓	✓	✓
LIN mode	✓	-	✓	✓	✓	✓	✓	✓
Dual clock domain and wakeup from Stop mode	✓	-	✓	✓	✓	✓	✓	✓
Receiver timeout interrupt	✓	-	✓	✓	✓	✓	✓	✓
Modbus communication	✓	-	✓	✓	✓	✓	✓	✓
Auto baud rate detection	✓	-	✓	-	-	✓	-	-
Driver Enable	✓	✓	✓	-	-	✓	-	-
USART data length	7, 8 and 9 bits		8 and 9 bits			7, 8 and 9 bits		

1. ✓=supported.
2. SCLK output is disabled when UE bit = 0.
3. With the following limitation for the STM32F302xB/C device: If the USART is used in the Smartcard mode and the card cannot use the default communication parameters after Answer to Reset and does not support a clock stop, it is not possible to use SCLK to clock the card. This is due to the fact that the USART and its clock output must be disabled while reprogramming some of the parameters.
4. SCLK is always available when CLKEN = 1, regardless of the UE bit value.

1.2.12 USB

On the STM32F302x6/8/D/E devices, the USB peripheral supports the LPM.

Note that for the STM32F302xB/C devices, the USB_DM and USB_DP are mapped on AF14 of PA11 and PA12, while on the STM32F302x6/8/D/E devices, there is no need to configure AF since those inputs are directly connected to GPIO, when the USB is enabled.

On the STM32F302x6/8/D/E devices, there are 768 bytes dedicated SRAM for the USB plus 256 bytes shared SRAM with the CAN. When the CAN is disabled, the whole 1 Kbyte can be used for the USB.

Consequently, the USB SRAM management is different between the STM32F302xB/C and the STM32F302x6/8/D/E devices.

Table 9. STM32F302 line USB Implementation(1)

USB features	STM32F302x6/8/D/E	STM32F302xB/C
Number of endpoints	8	8
Size of dedicated packet buffer memory SRAM	1024 bytes(2)	512 bytes(3)
Dedicated packet buffer memory SRAM access scheme	2 x 16 bits / word	1 x 16 bits / word
USB 2.0 Link Power management (LPM) support	✓	-

1. ✓= supported.
2. When the CAN peripheral clock is enabled in the RCC_APB1ENR register, only the first 768 bytes are available to the USB while the last bytes are used by the CAN.
3. The 512 bytes are totally available to the USB; nothing is shared with the CAN.

2 STM32F303 line product differences

2.1 STM32F303 line product overview

Table 10 provides an overview of the STM32F303x6/8/B/C/D/E peripherals.

Table 10. Peripheral overview(1)

STM32F303 line				
Device		**STM32F303x6/8**	**STM32F303xB/C**	**STM32F303xD/E**
System				
Embedded SRAM	Size	Up to 12 Kbytes of SRAM	Up to 40 Kbytes	Up to 64 Kbytes
	CCM-SRAM size	4 Kbytes	8 Kbytes	16 Kbytes
	Parity check	Implemented on the whole SRAM and CCM SRAM.	Implemented on the first 16 Kbytes of SRAM and on the whole CCM SRAM.	Implemented on the first 32 Kbytes of SRAM and on the whole CCM SRAM.
MPU	-	N/A	✓	✓
Flash memory size	-	Up to 64 Kbytes	Up to 256 Kbytes	Up to 512 Kbytes
Direct memory access (DMA)	-	7-channel DMA controller	12-channel DMA controller	12-channel DMA controller
	GP-DMA1	✓	✓	✓
	GP-DMA2	N/A	✓	✓
FMC	-	N/A	N/A	✓
GPIO		Up to 51 fast I/Os	Up to 87 fast I/Os	Up to 115 fast I/Os
Analog				
Analog to digital converter (ADC) 5MSPS	-	2	4	4
	Number of channels	Up to 21 channels	Up to 39 channels	Up to 40 channels
	ADC1	✓	✓	✓
	ADC2	✓	✓	✓
	ADC3	N/A	✓	✓
	ADC4	N/A	✓	✓

Table 10. Peripheral overview[1] (continued)

STM32F303 line				
Device		**STM32F303x6/8**	**STM32F303xB/C**	**STM32F303xD/E**
Comparators (COMP)	-	3 x ultra-fast comparators	7 x fast comparators	7 x ultra-fast comparators
	COMP1	N/A	✓	✓
	COMP2	✓	✓	✓
	COMP3	N/A	✓	✓
	COMP4	✓	✓	✓
	COMP5	N/A	✓	✓
	COMP6	✓	✓	✓
	COMP7	N/A	✓	✓
Available operational amplifiers	-	1	4	4
	OPAMP1	N/A	✓	✓
	OPAMP2	✓	✓	✓
	OPAMP3	N/A	✓	✓
	OPAMP4	N/A	✓	✓
Digital to analog converter (DAC)	-	3 x 12-bit DAC channels	2 x 12-bit DAC channels	2 x 12-bit DAC channels
	DAC1_CH1	✓	✓	✓
	DAC1_CH2	✓	✓	✓
	DAC2_CH1	✓	N/A	N/A
Touch Sensing		Up to 18 capacitive sensing channels supporting touch keys, linear and rotary touch sensors	Up to 24 capacitive sensing channels supporting touch key, linear and rotary touch sensors	Up to 24 capacitive sensing channels supporting touch key, linear and rotary touch sensors
Communication				
I2C	-	1 x I²C	2 x I²Cs	3 x I²Cs
	I2C1	✓	✓	✓
	I2C2	N/A	✓	✓
	I2C3	N/A	✓	✓

Table 10. Peripheral overview(1) (continued)

STM32F303 line				
Device		**STM32F303x6/8**	**STM32F303xB/C**	**STM32F303xD/E**
USART/UART	-	3 x U(S)ARTs	5 x U(S)ARTs	5 x U(S)ARTs
	USART1	✓	✓	✓
	USART2	✓	✓	✓
	USART3	✓	✓	✓
	UART4	N/A	✓	✓
	UART5	N/A	✓	✓
SPI available	-	1 x SPI	3 x SPIs/ 2 x I2Ss	4 x SPIs/ 2 x I2Ss
	SPI1	✓	✓	✓
	SPI2/I2S2	N/A	✓	✓
	SPI3/I2S3	N/A	✓	✓
	SPI4	N/A	N/A	✓
USB 2.0 full speed		N/A	✓	✓ with LPM support
CAN interface (2.0 B Active)		✓	✓	✓
Infrared transmitter		✓	✓	✓
Timers				
General purpose/motor control/basic timers	Number	Up to 11 timers	Up to 13 timers	Up to 14 timers
	TIMER1	✓	✓	✓
	TIMER2	✓	✓	✓
	TIMER3	✓	✓	✓
	TIMER4	N/A	✓	✓
	TIMER6	✓	✓	✓
	TIMER7	✓	✓	✓
	TIMER8	N/A	✓	✓
	TIMER15	✓	✓	✓
	TIMER16	✓	✓	✓
	TIMER17	✓	✓	✓
	TIMER20	N/A	N/A	✓
SysTick timer 24-bit down-counter		✓	✓	✓
Watchdog timers		2 (independent, window)	2 (independent, window)	2 (independent, window)

Table 10. Peripheral overview(1) (continued)

STM32F303 line			
Device	**STM32F303x6/8**	**STM32F303xB/C**	**STM32F303xD/E**
RTC	Calendar RTC with alarm, periodic wakeup from Stop	Calendar RTC with alarm, periodic wakeup from Stop/Standby	Calendar RTC with alarm, periodic wakeup from Stop/Standby
Packages			
Packages	LQFP64/48/32	LQFP100/64/48 WLCSP100	LQFP144/100/64 UFBGA100/WLCSP100

1. ✓ = supported.

2.2 STM32F303 line product differences

2.2.1 Clock tree

When the HSI is selected as the PLL clock source, the maximum CPU clock can be reached:

- On the STM32F303x6/8/B/C devices, there is one bit PLLSRC (bit 16 in the RCC_CFGR register) that allows selecting the PLL clock source; and when the HSI is selected as the PLL clock source, the maximum CPU frequency that can be reached is 64 MHz.
- On the STM32F303xD/E devices, two bits (bit 15 and 16 in the RCC_CFGR register) are used in order to select the PLL clock source. The purpose is to add a configuration where the HSI is selected as the PLL clock source and 72 MHz CPU clock is reached.

Table 11. PLL clock source selection

Bit 15	Bit 16	Configuration description
0	0	HSI/2 used as PREDIV1 entry and PREDIV1 forced to div by 2
0	1	HSI used as PREDIV1 entry (only on STM32F303xD/E)
1	0	HSE used as PREDIV1 entry
1	1	Reserved

2.2.2 Clock out capability

Compared to the STM32F303xB/C devices, on the STM32F303x6/8/D/E devices:

- One PLLNODIV bit in the RCC_CFGR register is added, its purpose is to control the divider bypass for a PLL clock input to the MCO.
- The MCO frequency can be reduced by a configurable divider, controlled by the MCOPRE [2..0] bits in the RCC_CFGR register.

Figure 5. STM32F303xB/C clock out capability

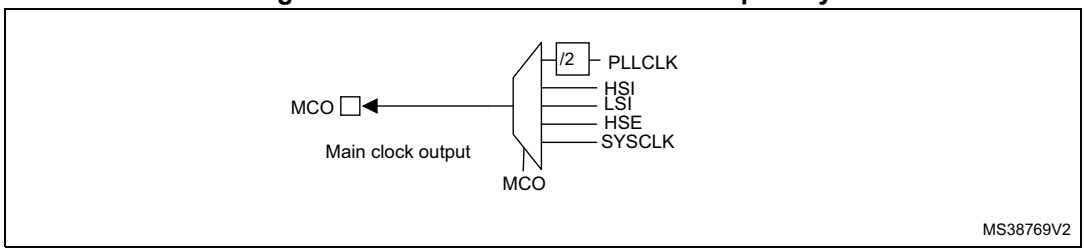
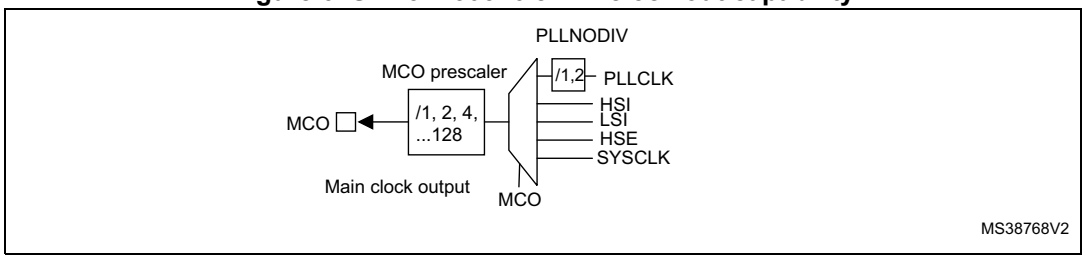


Figure 6. STM32F303x6/8/D/E clock out capability



2.2.3 Embedded SRAM

Table 12. Embedded SRAM for the STM32F303 line

	STM32F303x6/8	STM32F303xB/C	STM32F303xD/E
SRAM	12 Kbytes	40 Kbytes	64 Kbytes
CCM SRAM	4 Kbytes	8 Kbytes	16 Kbytes
Hardware parity check implemented	Whole SRAM and CCM SRAM	First 16 Kbytes of SRAM and whole CCM SRAM	First 32 Kbytes of SRAM and whole CCM SRAM

2.2.4 SYSCFG

In the SYSCFG configuration register2 (SYSCFG_CFGR2): PVD_LOCK, SRAM_PARITY_LOCK and LOCKUP_LOCK bits are reset only by system reset in the STM32F303x6/8/D/E devices.

However on the STM32F303xB/C devices, these bits can be reset also by a reset from RCC (using the SYSCFGRST bit).

The SYSCFG_CFGR3 register is only available on the STM32F303x6/8 devices; this register allows for the remapping of the ADC2, I2C1, SPI1 DMA channels.

The SYSCFG_CFGR4 register is only available on the STM32F303xD/E devices; this register allows for the remapping of the triggers of the ADCs, mainly the new TIM20 events.

2.2.5 I/O and pinout

The STM32F303x6/8/B/C/D/E devices are pinout compatible except for the fact that PF4 in the STM32F303xB/C devices, is VSS in the STM32F303x6/8/D/E devices. Refer to *Figure 7* and *Figure 8*:

Figure 7. STM32F303xx LQFP64 pinout discrepancies

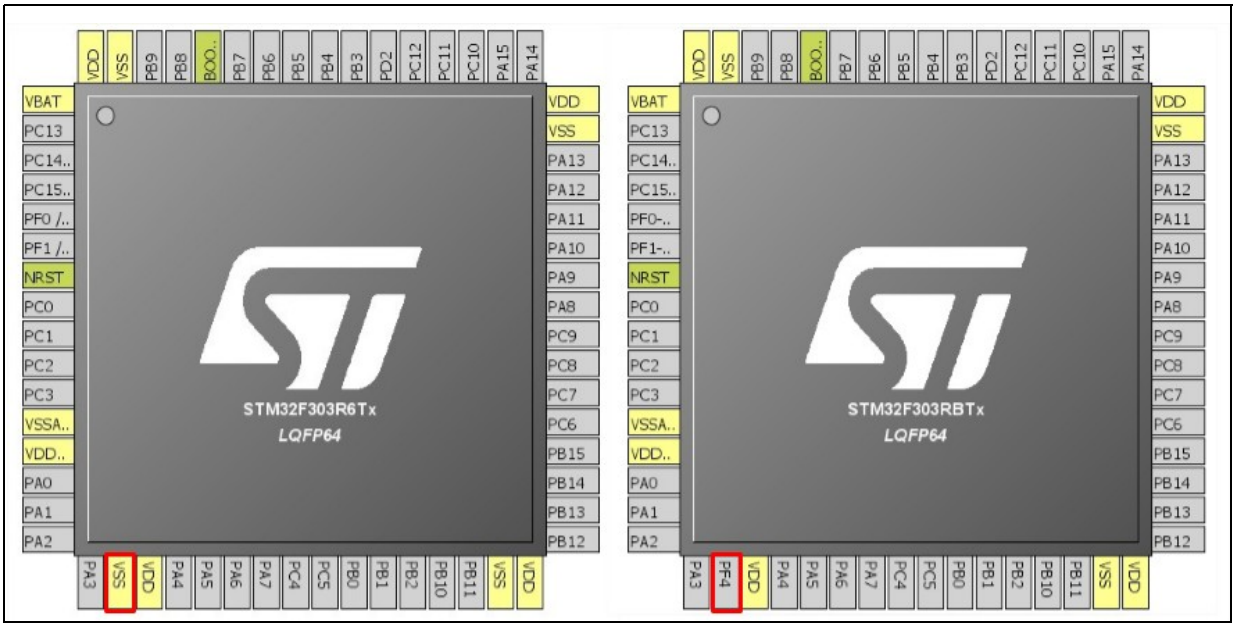
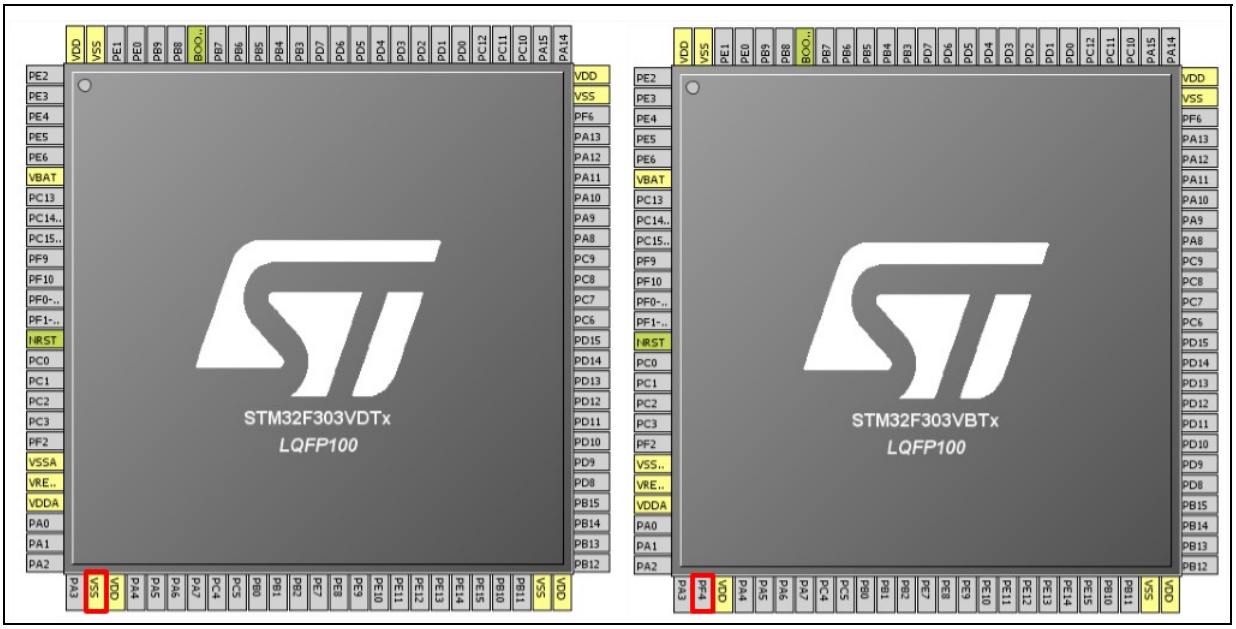


Figure 8. STM32F303xx LQFP100 pinout discrepancies



The GPIO LOCK feature is only available on Port A, B and D on the STM32F303xB/C devices. It is implemented for all the GPIO ports on the STM32F303x6/8/D/E devices.

Table 13 summarizes all added alternate functions in the STM32F303x6/8 and the STM32F303xD/E devices compared to the STM32F303xB/C devices.

Table 13. Alternate functions added

I/O and Alternate function	Added function
PB8 (AF7)	USART3_Rx
PB9 (AF7)	USART3_Tx
PC0 (AF2)	TIM1_CH1
PC1 (AF2)	TIM1_CH2
PC2 (AF2)	TIM1_CH3
PC3 (AF2)	TIM1_CH4
PC4 (AF2)	TIM1_ETR
PC5 (AF2)	TIM15_BKIN
PA12 (AF5)	I2S_CKIN
PF0 (AF5)	SPI2_NSS/I2S2_WS(1)
PF1 (AF5)	SPI2_SCK/I2S2_CK(1)
PA10 (AF5)	SPI2_MISO/I2S2ext_SD(1)
PA11 (AF5)	SPI2_MOSI/I2S2_SD(1)
PB5 (AF8)	I2C3_SDA(1)
PA8 (AF3)	I2C3_SCL(1)
PC9 (AF3)	I2C3_SDA(1)
PA9 (AF2)	I2C3_SMBAL(1)

1. These alternate functions are only available on the STM32F303xD/E devices.

Note: The FMC is available only on the STM32F303xD/E devices. The corresponding alternate functions are not mentioned in Table 13.

2.2.6 Analog to Digital Converter (ADC)

Table 14 shows the mapping differences of ADC channels on the STM32F303 line products.

Table 14. ADC channel mapping differences

GPIO	STM32F303x6/8	STM32F303xB/C	STM32F303xD/E
PB0	ADC1_IN11	ADC3_IN12	ADC3_IN12
PB1	ADC1_IN12	ADC3_IN1	ADC3_IN1
PB11	-	-	ADC12_IN14
PB12	ADC2_IN13	ADC4_IN3	ADC4_IN3
PB13	ADC1_IN13	ADC3_IN5	ADC3_IN5
PB14	ADC2_IN14	ADC4_IN4	ADC4_IN4
PB15	ADC2_IN15	ADC4_IN5	ADC4_IN5

2.2.7 Digital to Analog Converter (DAC)

The STM32F303xB/C/D/E devices embed two DAC channels with output buffers.

The STM32F303x6/8 devices embed 3 DAC channels: DAC1 channel1 is coming with an output buffer whereas DAC1 channel 2 and DAC2 channel 1 are coming without output buffers.

Table 15 lists DAC external triggers:

Table 15. DAC external triggers

TSEL control bits			Devices	
2	1	0	**STM32F303xB/C/D/E**	**STM32F303x6/8**
0	0	0	TIM6_TRGO	
0	0	1	TIM8_TRGO or TIM3_TRGO	TIM3_TRGO(1)
0	1	0	Reserved	
0	1	1	TIM15_TRGO	
1	0	0	TIM2_TRGO	
1	0	1	TIM4_TRGO	Reserved
1	1	0	EXTI_9	
1	1	1	SWTRIGx	

1. DAC1_TRIG_RMP bit in SYSCFG_CFGR1 register needs to be set by software.

2.2.8 Comparators

The STM32F303x6/8/D/E devices embed ultra-fast comparators while the STM32F303xB/C devices embed fast comparators.

Compared to the STM32F303xB/C devices, the comparators on the STM32F303x6/8/D/E devices:

- Do not support programmable speed/consumption mode: High speed mode only
- Do not support the hysteresis feature
- Have only one VINP input:
  - COMP2_INP: PA7
  - COMP3_INP: PB14
  - COMP4_INP: PB0
  - COMP5_INP: PB13
  - COMP6_INP: PB11
  - COMP7_INP: PC1
- Do not have COMP2_OUT on PA7
- Do not support the window mode

On the STM32F303x6/8/D/E devices, the comparators registers are reset only by system reset. However, on the STM32F303xB/C devices, they can be reset also by a reset from the RCC (using the SYSCFGRST bit).

2.2.9 Operational amplifier

On the STM32F303x6/8/D/E devices, the OPAMP register is reset only by system reset. However, on the STM32F303xB/C devices, this register can be reset also by a reset from the RCC (using the SYSCFGRST bit).

2.2.10 Timer

Table 16 lists all the timers that can be clocked at 144 MHz in each device of the STM32F303 line.

Table 16. Timers that can be clocked at 144 MHz(1)

	STM32F303x6/8	STM32F303xB/C	STM32F303xD/E
TIMER1	✓	✓	✓
TIMER2	-	-	✓
TIMER3	-	-	✓
TIMER4	-	-	✓
TIMER8	-	✓	✓
TIMER15	-	-	✓
TIMER16	-	-	✓
TIMER17	-	-	✓
TIMER20	-	-	✓

1. ✓= supported.

Table 17 summarizes the interconnection of timer triggers

Table 17. Interconnection of timer triggers

Slave timer	Product	ITR0	ITR1	ITR2	ITR3
1	STM32F303xB/C/D/E	15	2	3	4 or 17
	STM32F303x6/8	15	2	3	17(1)
2	STM32F303xB/C/D/E	1	8	3	4
	STM32F303x6/8	1	Reserved	3	Reserved
3	STM32F303xB/C/D/E	1	2	15	4
	STM32F303x6/8	1	2	15	Reserved
4	STM32F303xB/C/D/E	1	2	3	8
8	STM32F303xB/C/D/E	1	2	4	3
15	STM32F303xB/C/D/E	2	3	16	17
	STM32F303x6/8	2	3	16	17
20	STM32F303xD/E	1	8	4	15

1. TIM1_ITR3_RMP bit in SYSCFG_CFGR1 register needs to be set by software.

2.2.11 USART/UART

Table 18 highlights the differences between the USART/UART available on the STM32F303 line.

Table 18. USART/UART discrepancies(1)

USART modes/ features	STM32F303x6/8		STM32F303xB/C			STM32F303xD/E		
	USART1	USART2/ USART3	USART1/ USART2/ USART3	UART4	UART5	USART1/ USART2/ USART3	UART4	UART5
Hardware flow control for modem	✓	✓	✓	-	-	✓	-	-
Continuous communication using DMA	✓	✓	✓	✓	-	✓	✓	-
Multiprocessor communication	✓	✓	✓	✓	✓	✓	✓	✓
Synchronous mode	✓	✓	✓	-	-	✓	-	-
Smartcard mode	✓(2)	-	✓(3)(4)	-	-	✓(3)	-	-
Single-wire half-duplex communication	✓	✓	✓	✓	✓	✓	✓	✓
IrDA SIR ENDEC block	✓	-	✓	✓	✓	✓	✓	✓
LIN mode	✓	-	✓	✓	✓	✓	✓	✓
Dual clock domain and wakeup from Stop mode	✓	-	✓	✓	✓	✓	✓	✓
Receiver timeout interrupt	✓	-	✓	✓	✓	✓	✓	✓
Modbus communication	✓	-	✓	✓	✓	✓	✓	✓
Auto baud rate detection	✓	-	✓	-	-	✓	-	-
Driver Enable	✓	✓	✓	-	-	✓	-	-
USART data length	7, 8 and 9 bits		8 and 9 bits			7, 8 and 9 bits		

1. ✓ = supported.
2. SCLK is always available when CLKEN = 1, regardless of the UE bit value.
3. SCLK output is disabled when UE bit = 0.
4. With the following limitation for the STM32F303xB/C device: If the USART is used in the Smartcard mode and the card cannot use the default communication parameters after Answer to Reset and does not support clock stop, it is not possible to use SCLK to clock the card. This is due to the fact that the USART and its clock output must be disabled during the reprogramming of some of the parameters.

2.2.12 USB

On the STM32F303x6/8 devices, there is no USB.

The USB peripheral contained on the STM32F303D/E devices supports the LPM.

Note that for the STM32F303xB/C devices, the USB_DM and USB_DP are mapped on AF14 of PA11 and PA12, while on the STM32F303xD/E devices, there is no need to configure AF since those inputs are directly connected to GPIO, when the USB is enabled.

On the STM32F303xD/E devices, there are 768 bytes dedicated SRAM for USB plus 256 bytes shared SRAM with the CAN. When the CAN is disabled, the whole 1 Kbyte can be used for the USB.

Consequently, the USB SRAM management is different between the STM32F303xB/C devices and the STM32F303xD/E devices.

Table 19. USB RAM management

Device	STM32F303x6/8	STM32F303xB/C	STM32F303xD/E
Number of endpoints	N/A	8	8
Size of dedicated packet buffer memory SRAM	N/A	512 bytes	1024 bytes
Dedicated packet buffer memory SRAM access scheme	N/A	1 x 16 bits / word	2 x16 bits / word
USB 2.0 Link Power Management (LPM) support	N/A	N/A	✓(supported)

3 Revision history

Table 20. Document revision history

Date	Revision	Changes
20-Apr-2016	1	Initial release.
13-Oct-2016	2	Updated *Section 1.2.8: Comparators* and *Section 2.2.8: Comparators* not supporting the window mode.