AN4809
Application note

Migrating between STM32L0 Series and STM32L4 Series / STM32L4+ Series microcontrollers

Introduction

For the designers of STM32 microcontroller applications, being able to easily replace one microcontroller type by another between different product families is an important asset. Migrating an application to a different microcontroller is often needed when the product requirements grow putting extra demands on the memory size or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and to shrink the PCB area.

This application note analyzes the required steps to migrate an existing design between STM32L0 Series and STM32L4 Series / STM32L4+ Series microcontrollers. Three aspects need to be considered for the migration: the hardware migration, the peripheral migration and the firmware migration.

This document lists the “full set” of features available for the STM32L0 Series and the STM32L4 Series / STM32L4+ Series (some products may have less features depending on their part number). It groups together the most important information and lists the key aspects that need to be addressed.

To fully benefit from this application note, the user should be familiar with the STM32 microcontrollers documentation available on *www.st.com*, with a particular focus on:

- STM32L0 Series reference manuals:
  - RM0377 (STM32L0x1xx)
  - RM0376 (STM32L0x2xx)
  - RM0367 (STM32L0x3xx)
- STM32L0 Series datasheets.
- STM32L4 Series reference manuals:
  - RM0351 (STM32L4x6xx, STM32L4x5xx)
  - RM0394 (STM32L41xxx, STM32L42xxx, STM32L43xxx, STM32L44xxx, STM32L45xxx, STM32L46xxx)
  - RM0392 (STM32L471xx)
- STM32L4 Series datasheets
- STM32L4+ Series reference manual:
  - RM0432 (STM32L4Rxxx, STM32L4Sxxx)
- STM32L4+ Series datasheets

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1 STM32L0 Series and STM32L4 Series / STM32L4+ Series overview

STM32L0 Series and STM32L4 Series / STM32L4+ Series have in common the achievement of an outstanding low-power consumption level. They are all genuine ultra-low-power MCUs with record breaking.

STM32L0 Series target the very low-power applications while STM32L4 Series / STM32L4+ Series bring additional processing performances and new peripherals.

The detailed list of available features and packages for each product is available in the respective product's datasheet. As reminded in *Table 1* the STM32L0 Series products have been organized in categories to ease the referencing.

Table 1. STM32L0 Series product category overview

Type(1)	Part number
Category 1	STM32L01xxx, STM32L02xxx
Category 2	STM32L03xxx, STM32L04xxx
Category 3	STM32L05xxx, STM32L06xxx
Category 5	STM32L07xxx, STM32L08xxx

1. Category X devices are referred as "Cat. X" devices within this document.

This document applies to Arm®(a)-based devices.

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1.1 STM32L0 Series: ultra-low-power MCU

The exclusive combination of an ARM® Cortex®-M0+ core (max speed 32 MHz) and STM32 ultra-low-power features, makes STM32L0 Series the best fit for applications operating on battery or supplied by energy harvesting and the world's lowest power consumption MCU at 125°C.

STM32L0 Series offer a dynamic voltage scaling, an ultra-low-power clock oscillator, LCD interface, comparators, DAC and hardware encryption. Autonomous peripherals (including USART, I2C, touch sense controller) reduce the load of the ARM® Cortex®-M0+ core leading to fewer CPU wakeups and contribute to decrease the processing time and the power consumption.

Other value-added features such as the 16-bit ADC (HW oversampling), the crystal-less USB, short wakeup time and communication peripherals capable of operating in Ultra-low-power mode, make up for an unrivaled tradeoff between the feature integration, the performance and ultra-low-energy consumption.

The STM32L0 Series devices are available with up to 192 Kbytes of Flash memory, 20 Kbytes of RAM and up to 6 Kbytes of embedded EEPROM (no emulation needed) in 14- to 100-pin packages. Three feature levels and four categories cover a wide range of customer needs. *Table 2* and *Table 3* summarize the feature levels and memory availability of the STM32L0 Series products.

Table 2. STM32L0 Series feature levels

Feature level	Additional features
1	– Access Line
2	– Crystal-less USB 2.0 FS (BCD, LPM compliant) 16 capacitive touch keys – True random number generator (TRNG)
3	– Crystal-less USB 2.0 FS – 16 capacitive touch keys – True random number generator (TRNG) – LCD driver (8x48)

Table 3. STM32L0 memory amount availability and feature levels

Category	Part number	Flash size (Kbytes)	EEPROM size (Kbytes)(1)	Ram size (Kbytes)	Feature level
Cat. 1	STM32L01xxx	8/16	0,5	2	1
	STM32L02xxx				1 + AES
Cat. 2	STM32L03xxx	16/32	1	8	1,2
	STM32L04xxx				1
Cat. 3	STM32L05xxx	32/64	2	8	1,2,3
	STM32L06xxx				2,3 + AES
Cat. 5	STM32L07xxx	64/128/192	3/6	20	1,2,3
	STM32L08xxx				1,2,3 + AES

1. Not available for all part numbers.

1.2 STM32L4 Series / STM32L4+ Series: ultra-low-power and performances

The STM32L4 Series / STM32L4+ Series devices extend the ultra-low-power portfolio and performance with the ARM® Cortex®-M4 core with DSP, floating-point unit (FPU) and START Accelerator™ at up to 120 MHz.

The STM32L4 Series / STM32L4+ Series devices have scored 153 (world record) in the standardized EEMBC™ ULPBench® tests that compare the efficiency of ultra-low-power microcontrollers.

The STM32L4 Series / STM32L4+ Series devices offer from 256 Kbytes to 2 Mbytes of Flash memory and from 32- to 169-pin packages. Their memory range can easily be extended using SDIO, Quad-SPI, Octo-SPI and FSMC interfaces.

Table 4 and *Table 5* summarize the feature levels and memory availability of STM32L4 Series / STM32L4+ Series.

Table 4. STM32L4 Series / STM32L4+ Series feature levels

Feature level	Additional features
1	Access line
2	1 + USB specification version 2.0 full-speed
3	2 + liquid crystal display controller
4	1 + USB FS OTG
5	4 + LCD
7	5 + LTDC
9	7 + DSI

Table 5. STM32L4 Series / STM32L4+ Series memory availability

Part number	Flash size		RAM size			Feature level
	Size	Bank	SRAM1	SRAM2	SRAM3	
STM32L4S9xx	2 Mbytes	Dual	192 Kbytes	64 Kbytes	384 Kbytes	9+crypto
STM32L4R9xx						9
STM32L4S7xx						7+crypto
STM32L4R7xx						7
STM32L4S5xx						5+crypto
STM32L4R5xx						5
STM32L496xx	1 Mbyte	Dual	256 Kbytes	64 Kbytes	NA	6
STM32L4A6xx						6+crypto
STM32L471xx			96 Kbytes	32 Kbytes		1
STM32L475xx						5
STM32L476xx						6
STM32L486xx						6+crypto
STM32L451xx	512 Kbytes	Single	128 Kbytes	32 Kbytes		1
STM32L452xx						2
STM32L462xx						2+crypto
STM32L431xx	256 Kbytes	Single	48 Kbytes	16 Kbytes		1
STM32L432xx						2
STM32L442xx						2+crypto
STM32L433xx						3
STM32L443xx						3+crypto
STM32L412xx	128 Kbytes	Single	32 Kbytes	8 Kbytes		2
STM32L422xx						2+crypto

2 Hardware migration

2.1 Packages availability

STM32L0 Series and STM32L4 Series / STM32L4+ Series have a wide selection of packages. The STM32L0 Series devices offer starts with small 14-pin packages and goes up to 100-pin packaged. The STM32L4 Series / STM32L4+ Series devices offer spreads from 32- to 169-pin packages.

The available packages in STM32L4 Series / STM32L4+ Series are listed in *Table 6*.

Table 6. Packages available on STM32L4 Series and STM32L4+ Series

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
UFQFPN32	-	-	-	-	X	X	(5 x 5)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L432xx, STM32L442xx
LQFP32	-	-	-	-	-	X	(5 x 5)	STM32L412xx, STM32L422xx
LQFP48	-	-	-	-	X	X	(7 x 7)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx
UFQFPN48	-	-	-	X	X	X	(7 x 7)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx
WLCSP36	-	-	-	-	-	X	(2.85 x 3.07)	STM32L412xx, STM32L422xx
WLCSP49	-	-	-	-	X	-	(3.141 x 3.127)	STM32L431xx, STM32L433xx, STM32L443xx
WLCSP64	-	-	-	-	X	-	(3.141 x 3.127)	STM32L431xx, STM32L433xx, STM32L443xx

Table 6. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
LQFP64	-	X	X	X	X	X	(10 x 10)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx
UFBGA64	-	-	-	X	X	X	(5 x 5)	STM32L412xx, STM32L422xx, STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx
WLCSP64	-	-	-	X	-	-	(3.357 x 3.657)	STM32L451xx, STM32L452xx, STM32L462xx
WLCSP72	-	-	X	-	-	-	(4.4084 x 3.7594)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx
WLCSP81	-	-	X	-	-	-	(4.4084 x 3.7594)	STM32L476xx
WLCSP100	-	X	-	-	-	-	(4.618 x 4.142)	STM32L496xx, STM32L4A6xx

Table 6. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
LQFP100	X	X	X	X	X	-	(14 x 14)	STM32L431xx, STM32L433xx, STM32L443xx, STM32L451xx, STM32L452xx, STM32L462xx, STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx
UFBGA100	-	-	X	X	X	-	(7 x 7)	STM32L431xx, STM32L433xx, STM32L443xx
UFBGA132	X	X	X	-	-	-	(7 x 7)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4S5xx
UFBGA144	X	-	-	-	-	-	(10 x 10)	STM32L4R9xx, STM32L4S9xx
LQFP144	X	X	X	-	-	-	(20 x 20)	STM32L471xx, STM32L475xx, STM32L476xx, STM32L486xx, STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx

Table 6. Packages available on STM32L4 Series and STM32L4+ Series (continued)

Package[1]	STM32L4+ Series	STM32L4 Series					Size (mm x mm)	Applicable part numbers
		STM32L 49xxx/ 4Axxx	STM32L 47xxx/ 48xxx	STM32L 45xxx/ 46xxx	STM32L 43xxx/ 44xxx	STM32L 41xxx/ 42xxx		
WLCSP144	X	-	-	-	-	-	(5.24 x 5.24)	STM32L4R5xx, STM32L4R7xx, STM32L4R9xx, STM32L4S5xx, STM32L4S7xx, STM32L4S9xx
UFBGA169	X	X	-	-	-	-	(7 x 7)	STM32L496xx, STM32L4A6xx, STM32L4R5xx, STM32L4R9xx, STM32L4S5xx, STM32L4S9xx

1. X = supported.

The available packages in STM32L0 Series are listed in *Table 7*.

Table 7. Packages available on STM32L0 Series

Package[1]	STM32L0 Series			
	Cat. 1	Cat. 2	Cat. 3	Cat. 5
TSSOP14	X	-	-	-
TSSOP20	X	X	-	-
UFQFPN20	X	-	-	-
UFQFPN28	X	X	-	-
UFQFPN32	X	X	X	X
UFQFPN48	-	-	-	-
WLCSP25	X	X	-	-
WLCSP36	-	-	X	-
WLCSP49	-	-	-	X
WLCSP64	-	-	-	-
WLCSP72	-	-	-	-
WLCSP81	-	-	-	-
LQFP32	X	X	X	X
LQFP48	-	X	X	X
LQFP64	-	-	X	X
LQFP100	-	-	-	X
LQFP144	-	-	-	-
TFBGA64	-	-	X	X
UFBGA64	-	-	-	X
UFBGA100	-	-	-	X
UFBGA132	-	-	-	-

1. X = supported.

For a detailed availability and a package selection, refer to the STM32L0 Series and STM32L4 Series / STM32L4+ Series web pages and available datasheets.

SMPS packages

Some STM32L4 Series / STM32L4+ Series devices offer a package option allowing the connection of an external SMPS. This is done through two VDD12 pins that are replacing two existing pins in the package baseline.

The compatibility is kept between the STM32L4 Series / STM32L4+ Series derivatives regarding those two pins (the pins replaced are different across the package types but are the same for all the derivatives on similar packages). Refer to the product datasheet for details.

2.2 Pinout comparison

STM32L0 Series and STM32L4 Series / STM32L4+ Series share a high level of pin compatibility. Most of the peripherals share the same pins in the two families hence the transition between the two series is simple as only few pins are impacted.

The next tables (from *Table 8* to *Table 12*) compare the pinout for 32-, 48-, 64- and 100-pin packages.

Table 8. Pinout differences on LQFP32 package(1)

Pin Nb	Pin name		Comment
	STM32L0 Series	STM32L4 Series / STM32L4+ Series	
5	VDDA	VDDA/VREF+	No pin is dedicated to VREF+ in this package, VREF+=VDDA

1. The pinout of STM32L0 Cat. 5 UFQFPN32 devices are not compatible with other STM32L0 devices. Refer to the dedicated datasheet.

Table 9. Pinout differences on UFQFPN32 package(1)

Pin Nb	Pin name		Comment
	STM32L0 Series	STM32L4 Series / STM32L4+ Series	
5	VDDA	VDDA/VREF+	No pin is dedicated to VREF+ in this package, VREF+=VDDA
16	PB2	VSS	PB2 and PB8 IOs do not exist in STM32L4 Series / STM32L4+ Series on this package
32	PB8	VSS	

1. The pinout of STM32L0 Cat. 5 UFQFPN32 devices are not compatible with other STM32L0 devices. Refer to the dedicated datasheet.

Table 10. Pinout differences on LQFP48 package

Pin Nb	Pin name		Comment
	STM32L0 Series	STM32L4 Series / STM32L4+ Series	
1	VLCD	VBAT	VLCD is an alternate function of PB2 pins on STM32L4 Series / STM32L4+ Series VBAT does not exist in STM32L0
8	VSSA	VSSA/VREF-	PB2 and PB8 IOs do not exist in STM32L4 on this package
9	VDDA	VDDA/VREF+	

Table 11. Pinout differences on LQFP64 package

Pin Nb	Pin name		Comment
	STM32L0 Series	STM32L4 Series / STM32L4+ Series	
1	VLCD	VBAT	VLCD is an alternate function of PC3 pins on STM32L4 Series / STM32L4+ Series VBAT does not exist in STM32L0
12	VSSA	VSSA/VREF-	No pins are dedicated to VREF- and VREF+ in this package: VREF-=VSSA VREF+=VDDA
13	VDDA	VDDA/VREF+	

Table 12. Pinout differences on LQFP100 package

Pin Nb	Pin name		Comment
	STM32L0 Series	STM32L4 Series / STM32L4+ Series	
6	VLCD	VBAT	VLCD is an alternate function of PC3 pins on STM32L4 Series / STM32L4+ Series VBAT does not exist in STM32L0 Series
10	PH9	VSS	PH9 and PH10 IOs do not exist in STM32L4 Series / STM32L4+ Series
11	PH10	VDD	
73	VDD	VDDUSB	-
75	VDD_USB	VDD	-

Table 13. Pinout differences on BGA64 package

Pin Nb	Pin name		Comment
	STM32L0 Series	STM32L4 Series / STM32L4+ Series	
B2	VDD	VBAT	-
B4	BOOT0	BOOT0/PH3	-
E5	VDD	VDDUSB	VDDUSB is available only in STM32L433/L443/L452/L462
E6	VDDIO2	VDD	-
F1	VSSA	VSSA/VREF-	-
G1	VREF+	PC3	-
H1	VDDA	VDDA/VREF+	-

Table 14. Pinout differences on UFBGA100 package

Pin Nb	Pin name		Comment
	STM32L0 Series	STM32L4 Series / STM32L4+ Series	
A4	BOOT0	BOOT0/PH3	-
C11	VDD	VDDUSB	VDDUSB is available only STM32L443/L433/L452/L462
E2	VDD	VBAT	-
F2	PH9	VSS	-
G2	PH10	VDD	-
G11	VDDIO2	VDD	-

Note: STM32L4R9xx/4S9xx are not compatible with STM32L4 Series, for more details please refer to application note Migration between STM32L476xx/486xx and STM32L4Rxxx/4Sxxx microcontrollers (AN5017).

3 Boot mode compatibility

3.1 Boot modes selection

The boot modes selection (main Flash memory, system Flash memory or embedded SRAM) are very close between both series of products. The selection is done through the BOOT0 pin and other option bits.

In small packages, the BOOT0 pin is shared with a GPIO. However, the BOOT0 logic can be controlled by an option bit. This option is available for the STM32L0 Cat. 1 and the STM32L47xxx/L48xxx devices.

STM32L0 Cat. 2, 3, 5 and STM32L47xxx/L48xxx devices

Table 15 shows the boot mode selected function of BOOT0 pin and BOOT1 option bit.

Table 15. Boot mode selection for STM32L0 Cat. 2, 3, 5 and STM32L47xxx/L48xxx devices

BOOT1 bit(1)	BOOT0 pin	Boot
X	0	Main Flash memory
0	1	System memory
1	1	Embedded SRAM

1. X = equivalent to 0 or 1.

STM32L0 Cat. 1 and STM32L41xxx/42xxx, STM32L43xxx/L44xxx, STM32L45xxx/L46xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx devices

Table 16 shows the boot mode selection for the STM32L0 Cat. 1 devices.

Table 16. Boot mode selection for STM32L0 Cat. 1 access line(1)

nBOOT1 bit(2)	BOOT0 pin	nBOOT_SEL bit	nBOOT0 pin	Main Flash memory empty(3)	Boot memory space
X	0	0 (BOOT0 pin)	X	0	Main Flash memory
				1	System memory
1	1		X	X	System memory
0	1		X	X	Embedded SRAM
X	X	1 (BOOT0 bit)	1	X	Main Flash memory
1	X		0	X	System memory
0	X		0	X	Embedded SRAM

1. The cells highlighted in gray concern only the STM32L011xx and the STM32L021xx devices.
2. X = equivalent to 0 or 1.
3. A Flash empty check mechanism is implemented to force the boot from system Flash, if the first Flash memory location is not programmed (0xFFFF FFFF) and if the boot selection is configured to boot from the main Flash memory.

The STM32L0 Cat. 1 devices share the BOOT0 pin with a GPIO pin. The selection of BOOT0 as a pin or an option bit is done by the BOOT_SEL option bit. If the boot target is the main Flash memory and the Flash memory is empty, the boot is automatically redirected on the system memory.

In the STM32L41xxx/42xxx, STM32L43xxx/L44xxx, STM32L45xxx/L46xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx devices, the boot mode is selected with the nBOOT1 option bit and the pin BOOT0 or the nBOOT0 option bit depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register as shown in *Table 17*.

Table 17. Boot modes for STM32L41xxx/L42xxx, STM32L43xxx/L44xxx, STM32L45xxx/L46xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx devices

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main Flash empty(1)	Boot Memory Space Alias
X	X	0	1	0	Main Flash memory is selected as boot area
X	X	0	1	1	System memory is selected as boot area
X	1	X	0	X	Main Flash memory is selected as boot area
0	X	1	1	X	Embedded SRAM1 is selected as boot area
0	0	X	0	X	Embedded SRAM1 is selected as boot area
1	X	1	1	X	System memory is selected as boot area
1	0	X	0	X	System memory is selected as boot area

1. Only for the STM32L45xxx/L46xxx, STM32L43xxx/L44xxx and STM32L41xxx/42xxx devices: a Flash empty check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed (0xFFFF FFFF) and if the boot selection is configured to boot from the main Flash memory.

3.2 Embedded bootloader

The embedded bootloader is located in the system memory, programmed by ST during the production. It is used to reprogram the Flash memory using one of the following serial interfaces.

STM32L4 Series / STM32L4+ Series offer a wider range of interfaces compared to STM32L0 Series. *Table 18* lists all the interface possibilities.

Table 18. Boot serial interfaces

Interfaces (1)	STM32L 02xxx STM32L 01xxx	STM32L 04xxx STM32L 03xxx	STM32L 06xxx STM32L 05xxx	STM32L 081xx STM32L 071xx	STM32L 082xx STM32L 072xx STM32L 083xx STM32L 073xx	STM32L4 Series
DFU	-	-	-	-	X	X
USART1	-	-	X	X	X	X
USART2	X	X	X	X	X	X
USART3	-	-	-	-	-	X
I2C1	-	-	-	X	-	X
I2C2	-	-	-	X	-	X
I2C3	-	-	-	-	-	X
I2C4	-	-	-	-	-	X(2)
SPI1	X	X	X	X	-	X
SPI2	-	-	X	X	-	X
SPI3	-	-	-	-	-	-
CAN1	-	-	-	-	-	X(3)
CAN2	-	-	-	-	-	X(4)

1. “X”: interface available.
2. Only for STM32L45xxx/L46xxx devices.
3. Not available on STM32L41xxx/L42xxx devices.
4. Only for STM32L49xxx/L4Axxx devices.

For details concerning the bootloader serial interface corresponding I/O, refer to the device datasheets. For other details concerning the bootloader on all STM32 devices, refer to application note *STM32 microcontroller system memory boot mode* (AN2606).

4 Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. Several low-power modes are available to save power when the CPU does not need to be kept running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between a low-power consumption, a short startup time and available wakeup sources.

STM32L0 Series and STM32L4 Series / STM32L4+ Series share the same main low-power modes (Low-power run, Stop, Sleep, Low-power sleep and Standby) with voltage ranges specifics to each series. STM32L4 Series / STM32L4+ Series offer in addition three stop modes (Stop 0 and Stop 1 with USB capabilities and Stop 2) and a new shutdown mode.

Details on the low-power modes configuration in each series can be found in the device reference manual. The consumption figures are given in the device datasheets.

4.1 Low-power modes in STM32L0 Series

Low-power modes

The STM32L0 Series devices have the five following low-power modes:

- **Low-power run** mode: regulator in low-power mode, limited clock frequency, limited number of peripherals running.
- **Sleep** mode: CPU stopped, peripherals kept running.
- **Low-power sleep** mode: CPU stopped, limited clock frequency, limited number of peripherals running, regulator in low-power mode, Flash memory stopped
- **Stop** mode: SRAM and all registers content are retained. All clocks in the VCORE domain are stopped, the PLL, the MSI, the HSI16 and the HSE are disabled. LSI and LSE can be kept running.
- **Standby** mode: VCORE domain powered off.

Dynamic voltage scaling

The ultra-low-power STM32L0 Series devices support the dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply. There are three power consumption ranges:

- Range 1 (VCore= 1.8V), with the CPU running at up to 32 MHz.
- Range 2 (VCore= 1.5V), with a maximum CPU frequency of 16 MHz.
- Range 3 (VCore= 1.2V), with a maximum CPU frequency limited to 4.2 MHz.

The global power consumption is reduced by using clock gating on unused peripherals.

Table 19 presents the STM32L0 Series low-power modes summary.

Table 19. STM32L0 Series low-power modes summary

Mode	Reg.	CPU	Flash (1)	SRAM	Clocks	Peripherals(2)	Consum-ption (µA/MHz)	Wakeup time (µs)
Run	Range1	ON	ON	ON	Any	All peripherals available	200	NA
	Range2						160	
	Range3						130	
LPRun	LPR	ON	ON	ON	MSI 131 KHz max	No USB, no ADC, no TSC. Other peripherals available	200	3
Sleep	Range1 Range2 Range3	OFF	ON	ON	Any	All peripherals available	Down to 30	0.36
LPSleep	LPR	OFF	ON	ON	MSI 131 KHz max	No USB, no ADC, no TSC. Other peripherals available	200	3.2
Stop	LPR	OFF	OFF	ON	LSI/LSE	RTC available	-	3.5
Standby	OFF	DOWN	OFF	OFF	LSI/LSE	RTC and IWDG available	-	50

1. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
2. Can be clock gated when unused.

Wakeup sources

The STM32L0 Series devices can get out of the low-power modes on the following events:

Sleep mode

- Any peripheral interrupt/wakeup event

Stop modes

- Any EXTI line event
- BOR, PVD, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, LPTIM

Standby mode

- WKUP pins rising or falling edge
- RTC alarm
- RTC wakeup
- RTC tamper event
- RTC timestamp event
- External reset in NRST pin
- IWDG reset

4.2 Low-power modes in STM32L4 Series / STM32L4+ Series

Low-power modes

The STM32L4 Series / STM32L4+ Series devices offer more flexibility to reduce the global consumption, in addition to the low-power modes from the STM32L0 Series devices. It offers these new modes:

- **Stop 0, Stop 1 and Stop 2 modes**: SRAMs and all the register content are retained. All the clocks in the VCORE domain are stopped, PLL, MSI, HSI16 and HSE are disabled. LSI and LSE can be kept running.
- **Shutdown mode**: the VCORE domain is powered off. All the clocks in the VCORE domain are stopped, PLL, MSI, HSI16, LSI and HSE are disabled. LSE can be kept running.

In the main Run mode, the power consumption can be reduced by one of the following means:

- Slowing down the system clocks
- Gating the clocks to APB and AHB peripherals when they are unused.

Dynamic voltage scaling

The main regulator (MR) has two voltage ranges for dynamic voltage scaling (R1 and R2) used in the Run and Sleep modes.

- Range 1 (VCore = 1.2 V) with the CPU running at up to 80 MHz
- Range 2 (VCore = 1.0 V) with a maximum CPU frequency of 26 MHz. All the peripheral clocks are also limited to 26 MHz.

For STM32L4Rxxx/4Sxxx devices, R1 can be configured in Normal mode or in Boost mode following the R1MODE bit in the PWR_CR5 register:

- Range 1 boost mode (Vcore = 1.28 V) with the CPU running at up to 120 MHz
- Range 1 normal mode (Vcore = 1.2 V) with the CPU running at up to 80 MHz
- Range 2 (Vcore = 1.0 V) with a maximum CPU frequency of 26 MHz. All the peripheral clocks are also limited to 26 MHz.

The low-power regulator (LPR) is for low-power run, low-power sleep, Stop 1, and Stop 2 modes as well as for the RAM retention in the Standby mode.

Table 20 summarizes the different low-power modes of STM32L4 Series / STM32L4+ Series. The consumption figures are given for the STM32L476xx devices as indication. For the power consumption figures of other references, refer to the dedicated datasheets.

Table 20. STM32L4 Series / STM32L4+ Series low-power modes summary

Mode	Reg.	CPU	Flash (1)	SRAM	Clocks	DMA & Peripherals(2)	Consum-ption (µA/MHz) (3)	Wakeup time (µs)
Run	Range 1	ON	ON	ON	Any	All peripherals available	112	NA
	Range 2					All except USB, RNG	100	

Table 20. STM32L4 Series / STM32L4+ Series low-power modes summary (continued)

Mode	Reg.	CPU	Flash (1)	SRAM	Clocks	DMA & Peripherals(2)	Consum-ption (µA/MHz) (3)	Wakeup time (µs)
LPRun	LPR	ON	ON	ON	Any except PLL	All except USB, RNG	136	Range1: 4 µs to range2: 64 µs
Sleep	Range 1	OFF	ON	ON	Any	All peripherals available	37	6 cycles
	Range 2					All except USB, RNG	35	6 cycles
LPSleep	LPR	OFF	ON	ON	Any except PLL	All except USB, RNG	40	6 cycles
Stop 0	MR	OFF	OFF	ON	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	NC	NC
Stop 1	LPR	OFF	OFF	ON	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	– 6.6 w/o RTC – 6.9 w RTC	– 4 µs in SRAM – 6 µs in Flash
Stop 2	LPR	OFF	OFF	ON	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	– 1.1 w/o RTC – 1.4 w RTC	– 5 µs in SRAM – 7 µs in Flash
Standby	LPR	OFF	OFF	SRAM2 ON	LSI/LSE	BOR, RTC, IWDG All other peripherals are powered off I/O configuration can be floating, pull-up or pull-down	– 0.35 w/o RTC – 0.65 w RTC	14
	OFF			OFF			– 0.12w/o RTC – 0.42w RTC	
Shutdown	OFF	OFF	OFF	OFF	LSE	RTC All other peripherals are powered off I/O configuration can be floating, pull-up or pull-down	– 0.03 w/o RTC – 0.33w RTC	256

1. The Flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
2. All peripherals can be active or clock gated to save power consumption.
3. Typical current at VDD=1.8V, 25°C. The consumption values are provided when running from the SRAM, Flash memory off, 80 MHz in the range 1.26 MHz in range 2.2 MHz in Low-power run / Low-power sleep modes. The values differ for different products, refer to product datasheet for exact values.

Wakeup sources

The device can get out of the low-power modes on the following events:

Sleep mode

- Any peripheral interrupt/wakeup event

Stop modes

- Any EXTI line event
- BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD

Standby mode

- WKUP pins rising or falling edge
- RTC event
- External reset in NRST pin
- IWDG reset

Shutdown mode

- WKUP pins rising or falling edge
- RTC event
- External reset in NRST pin

5 Peripheral migration

5.1 STM32Lx product cross-compatibility

STM32L4 Series / STM32L4+ Series embed more peripherals than STM32L0 Series and more instances of the same type or new peripherals. Both series often embed the same versions or very close versions of the same peripherals, allowing an easy migration.

The migration from STM32L0 Series to STM32L4 Series / STM32L4+ Series is easy since its peripherals can be considered as a subset of those of STM32L4 Series / STM32L4+ Series. Inversely, the migration from STM32L4 Series / STM32L4+ Series to STM32L0 Series may need resource sharing to compensate the peripheral instance numbers (DMA, ADC …).

The migration between the series focuses on common peripherals to all the products. With very close peripheral versions, the software does not need significant development efforts.

The common peripherals may be split in two classes:

1. The peripherals strictly identical between the series. They share the same architecture, the same registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
2. The new peripheral versions. In general, it implies an upgraded version for STM32L4 Series / STM32L4+ Series. These peripherals require minor changes to support the new features.

Table 21 gives a global view of the peripherals available as well as the differences between both series. Note that the availability and the number of instances may vary inside each series depending on the devices. Refer to the product datasheets for details.

Table 21. Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series

Peripherals[1]		STM32L0 Series	STM32L4 Series / STM32L4+ Series	Comments
Core	Cortex®-M	M0+	M4	-
	Nested vectored interrupt controller (NVIC)	39 interrupt channels	Up to 94 interrupt channels	-
	Extended interrupts and events controller (EXTI)	Up to 30 event/ interrupt	Up to 40 event/ interrupt	-

Table 21. Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

Peripherals[1]		STM32L0 Series	STM32L4 Series / STM32L4+ Series	Comments
System	Firewall (FW)	✓	✓	Same IP
	Cycle redundancy check calculation unit (CRC)	✓	✓	Same IP
	Power control (PWR)	✓	✓	See *Section 5.5*
	Reset and clock control (RCC)	✓	✓	See *Section 5.4*
	General-purpose I/Os (GPIO)	Up to 84	Up to 140 (STM32L4Rxxx/4Sxxx)	Refer to component packages
	Clock recovery system (CRS)	✓	✓	Same IP Used for USB XTAL less support
	General purpose DMA (DMA)	✓	✓	Same IP See *Section 5.3*
	Chrom-Art Accelerator™ controller (DMA2D)	-	DMA2D	Only in STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx
	Flexible static memory controller (FSMC)	-	FSMC	Only in STM32L47xxx/L48xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx
	Quad-SPI Interface (QUADSPI)	-	QUADSPI	Not available in STM32L4Rxxx/4Sxxx
	OCTOSPI	-	✓ (x2)	Only in STM32L4Rxxx/4Sxxx
	OCTOSPIM	-	✓	Only in STM32L4Rxxx/4Sxxx
	DMAMUX	-	✓	Only in STM32L4Rxxx/4Sxxx
	GFXMMU	-	✓	Only in STM32L4Rxxx/4Sxxx
	DSI	-	✓	Only in STM32L4Rxxx/4Sxxx

Table 21. Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

	Peripherals[1]	STM32L0 Series	STM32L4 Series / STM32L4+ Series	Comments
Analog	Voltage reference buffer (VREFBUF)	-	VREFBUF	Voltage reference for ADCs, DACs and external components, available externally on packages with at least 100 pins
	Analog-to-digital converters (ADC)	✓(x1)	– ✓ x3 for STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx – x2 for STM32L41xxx/L42xxx – x1 for STM32L45xxx/L46xxx, STM32L43xxx/L44xxx and STM32L4Rxxx/4Sxxx	See *Section 5.9*
	Digital-to-analog converter (DAC)	✓	✓	See *Section 5.10* Not available on STM32L41xx/L42xxx
	Comparator (COMP)	✓(x2)	✓(x2)	See *Section 5.11*
	Operational amplifiers (OPAMP)	-	✓	-
	Digital filter for sigma delta modulators (DFSDM)	-	✓	Not available in STM32L43xxx/L44xxx nor STM32L41xxx/L42xxx
	Liquid crystal display controller (LCD)	✓	✓	– Same IP – Up to 52 segments for STM32L0 Series – Up to 44 segments for STM32L4 Series Not available in STM32L4+ Series nor in STM32L4x1xx/4x2xx
	Touch sensing controller (TSC)	✓	✓	Same IP
	Random number generator (RNG)	✓	✓	Same IP
	Advanced encryption standard hardware accelerator (AES)	✓	✓	Only on specific part numbers (reference to *Table 5*)
	Hash processor (HASH)	-	HASH	Only in STM32L4A6xx and STM32L4Sxxx
	Device electronic signature	✓	✓	Package ID added in STM32L4 Series / STM32L4+ Series

Table 21. Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

Peripherals[1]		STM32L0 Series	STM32L4 Series / STM32L4+ Series	Comments
Clock and Timers	Advanced-control timers	-	TIM1/TIM8	– GP-Timer with advanced PWM/Motor Control capabilities – TIM8 only in STM32L47xxx/ L48xxx/L49xxx/ L4Axxx/4Rxxx/ 4Sxxx
	General-purpose timers 4 channels	TIM2/TIM3 (16 bits)	TIM2/TIM5 (32 bits) TIM3/TIM4 (16 bits)	– Updated for STM32L4 – TIM5 and TIM4 only in STM32L47xxx/ L48xxx/L49xxx/ L4Axxx/4Rxxx/ 4Sxxx
	General-purpose timers 16bits with 1 or 2 channels	TIM21/ TIM22	TIM15/16/17	– Updated for STM32L4 – TIM17 only in STM32L47xxx/ L48xxx/L49xxx/ L4Axxx/4Rxxx/ 4Sxxx
	Basic timers	TIM6/TIM7	TIM6/TIM7	– Updated for STM32L4 Series / STM32L4+ Series – TIM7 not available on STM32L41xxx/L42xxx nor STM32L45xxx/L46xxx devices
	Low-power timer (LPTIM)	✓	✓	Same IP
	Independent watchdog (IWDG)	✓	✓	Same IP
	System window watchdog (WWDG)	✓	✓	Same IP
	Real-time clock (RTC)	✓	✓	Same IP

Table 21. Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

Peripherals[1]		STM32L0 Series	STM32L4 Series / STM32L4+ Series	Comments
Connectivity	I2C	✓	✓	– Same IP – Up to 4 per Series
	USART	✓ (up to 4)	✓ (up to 5)	Same IP
	LPUART	✓	✓	Same IP
	Serial peripheral interface (SPI)	✓ (x2)	✓ (x3)	– Upgraded version in STM32L4 Series / STM32L4+ Series – I2S no longer supported by SPI but by SAI interface instead – See *Section 5.7*
	Serial audio interface (SAI)	-	✓	– Also used to support I2S interface – Refer to *Section 5.7* – x2 in STM32L49xxx/ L4Axxx, STM32L47xxx/ L48xxx and STM32L4Rxxx/ 4Sxxx – x1 in STM32L45xxx/ L46xxx and STM32L44xxx/ L43xxx
	Inter-IC sound (I2S)	✓	✓	– I2S by SPI in STM32L0 Series – I2S by SAI in STM32L4 Series / STM32L4+ Series
	Digital camera Interface (DCMI)	-	✓	Only in STM32L496xx/ L4A6xx and STM32L4Rxxx/4Sxxx
	USB 2.0 OTG full-speed	-	✓	– Only in STM32L49xxx/ L4Axxx, STM32L47xxx/ L48xxx and STM32L4Rxxx/ 4Sxxx – Refer to *Section 5.8*.
	USB 2.0 device full speed Xtal less	✓	✓	Refer to *Section 5.8*.
	Single wire protocol master interface (SWPMI)	-	✓	Not available in STM32L4Rxxx/4Sxxx
	SD/SDIO/MMC card host interface (SDMMC)	-	✓	-

Table 21. Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

Peripherals[1]		STM32L0 Series	STM32L4 Series / STM32L4+ Series	Comments
Connectivity (continued)	Controller area network (bxCAN)	-	✓	– x2 for STM32L47xxx/ L48xxx and STM32L49xxx/ L4Axxx – x1for STM32L42xxx/ L43xxx, STM32L44xxx/ L45xxx and STM32L4Rxxx/ 4Sxxx
	LTDC	-	✓	Only in STM32L4R7xx/ 4S7xx/4R9xx/4S9xx

Color key:

= same peripheral in both series

= peripheral only on STM32L4 Series / STM32L4+ Series

= different versions of peripheral

1. "✓": supported.

5.2 Memory mapping

5.2.1 Global memory map

Figure 1 and *Figure 2* give the global memory map of each series. New areas in STM32L4 Series / STM32L4+ Series concern the external memory map (FMC, QUADSPI and SRAM2). In the Flash memory address map, there are additional system memory and option bytes areas for dual-banks devices.

Figure 1. STM32L0 Series memory map

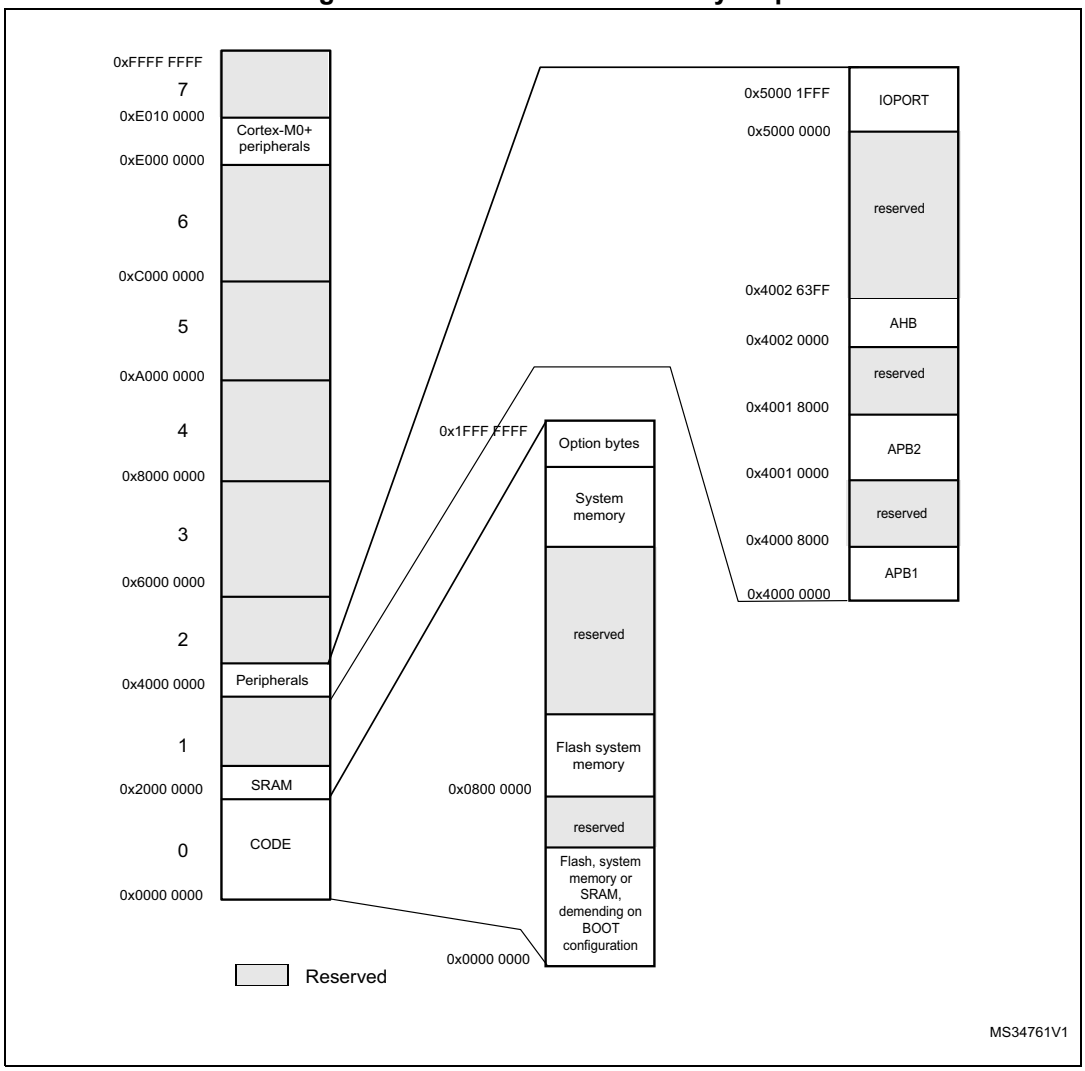
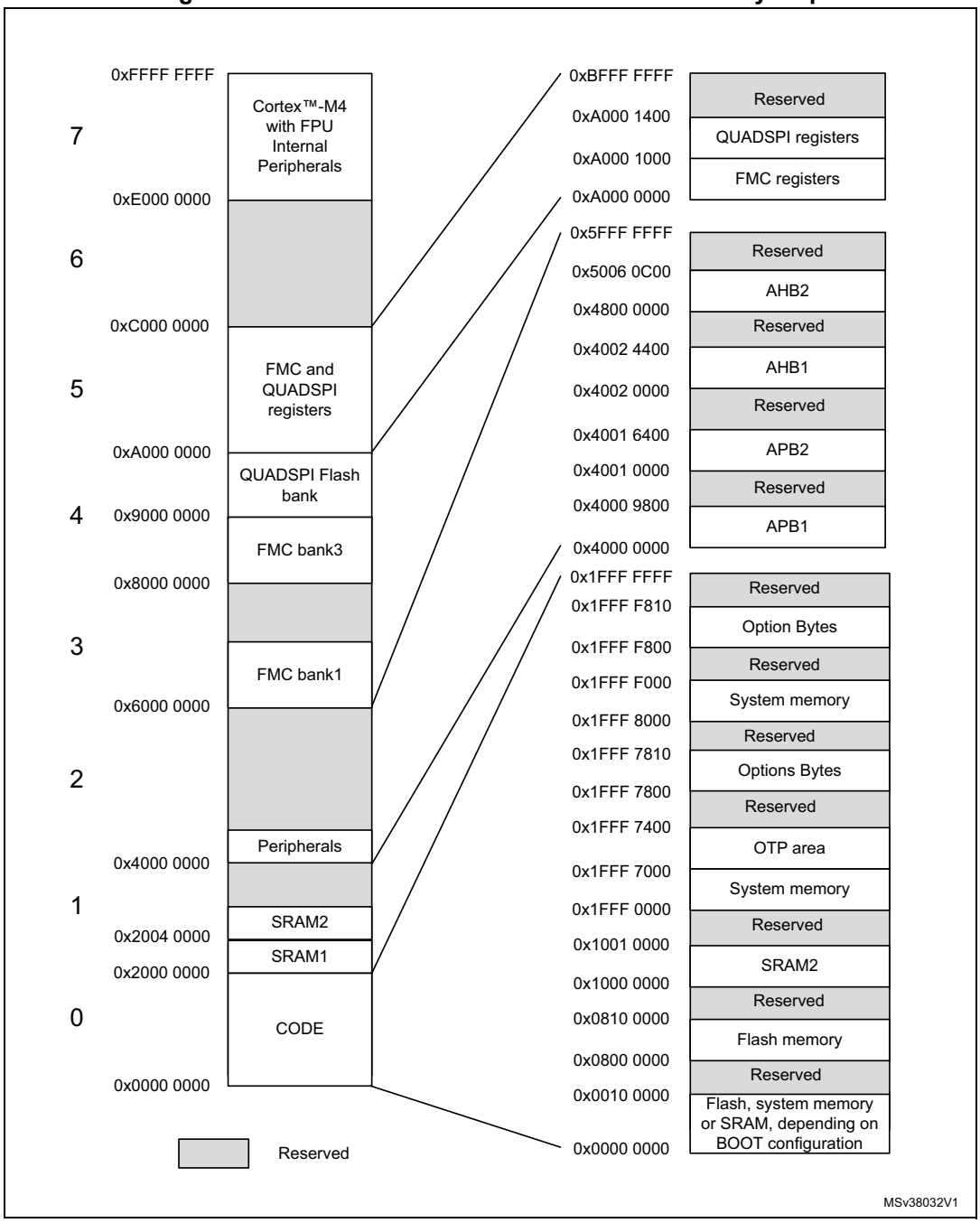


Figure 2. STM32L4 Series / STM32L4+ Series memory map



1. External memory address range may vary for different part numbers.
2. This figure is not applicable on STM32L4Rxxx/4Sxxx.

5.2.2 Peripherals memory map

There are some differences between the peripheral base address for both series. *Table 22* provides the peripheral address mapping correspondence between STM32L0 Series and STM32L4 Series / STM32L4+ Series. Note that not all the IPs are available in both series depending on the category and feature level of the devices. In case the IP is not present, the associated memory map is reserved.

Table 22. Peripherals memory map

Peripheral	STM32L0 Series		STM32L4 Series / STM32L4+ Series	
	Bus	Base address	Bus	Base address
GPIOH	IOPORT	0X5000 1C00 - 0X5000 1FFF	AHB2	0x4800 1C00 - 0x4800 1FFF
GPIOE		0X5000 1000 - 0X5000 13FF		0x4800 1000 - 0x4800 13FF
GPIOD		0X5000 0C00 - 0X5000 0FFF		0x4800 0C00 - 0x4800 0FFF
GPIO C		0X5000 0800 - 0X5000 0BFF		0x4800 0800 - 0x4800 0BFF
GPIOB		0X5000 0400 - 0X5000 07FF		0x4800 0400 - 0x4800 07FF
GPIOA		0X5000 0000 - 0X5000 03FF		0x4800 0000 - 0x4800 03FF
AES	AHB	0X4002 6000 - 0X4002 63FF		0x5006 0000 - 0x5006 03FF
RNG		0X4002 5000 - 0X4002 53FF		0x5006 0800 - 0x5006 0BFF
TSC		0X4002 4000 - 0X4002 43FF	AHB1	0x4002 4000 - 0x4002 43FF
CRC		0X4002 3000 - 0X4002 33FF		0x4002 3000 - 0x4002 33FF
FLASH		0X4002 2000 - 0X4002 23FF		0x4002 2000 - 0x4002 23FF
RCC		0X4002 1000 - 0X4002 13FF		0x4002 1000 - 0x4002 13FF
DMA1		0X4002 0000 - 0X4002 03FF		0x4002 0000 - 0x4002 03FF
USART1	APB2	0X4001 3800 - 0X4001 3BFF	APB2	0x4001 3800 - 0x4001 3BFF
SPI1		0X4001 3000 - 0X4001 33FF		0x4001 3000 - 0x4001 33FF
ADC1		0X4001 2400 - 0X4001 27FF	AHB2	0x5004 0000 - 0x5004 03FF
Firewall		0X4001 1C00 - 0X4001 1FFF	APB2	0x4001 1C00 - 0x4001 1FFF
EXTI		0X4001 0400 - 0X4001 07FF		0x4001 0400 - 0x4001 07FF
COMP(1)		0X4001 0000 - 0X4001 03FF		0x4001 0200 - 0x4001 03FF
SYSCFG				0x4001 0000 - 0x4001 002F

Table 22. Peripherals memory map (continued)

Peripheral	STM32L0 Series		STM32L4 Series / STM32L4+ Series	
	Bus	Base address	Bus	Base address
LPTIM1	APB1	0X4000 7C00 - 0X4000 7FFF	APB1	0x4000 7C00 - 0x4000 7FFF
I2C3		0X4000 7800 - 0X4000 7BFF		0x4000 5C00- 0x4000 5FFF
DAC1/2		0X4000 7400 - 0X4000 77FF		0x4000 7400 - 0x4000 77FF
PWR		0X4000 7000 - 0X4000 73FF		0x4000 7000 - 0x4000 73FF
CRS		0X4000 6C00 - 0X4000 6FFF		0x4000 6000 - 0x4000 63FF
USB SRAM		0X4000 6000 - 0X4000 67FF		0x4000 6C00 - 0x4000 6FFF
USB FS		0X4000 5C00 - 0X4000 5FFF		0x4000 6800 - 0x4000 6BFF
I2C2		0X4000 5800 - 0X4000 5BFF		0x4000 5800 - 0x4000 5BFF
I2C1		0X4000 5400 - 0X4000 57FF		0x4000 5400 - 0x4000 57FF
USART5		0X4000 5000 - 0X4000 53FF		0x4000 5000 - 0x4000 53FF
USART4		0X4000 4C00 - 0X4000 4FFF		0x4000 4C00 - 0x4000 4FFF
LPUART1		0X4000 4800 - 0X4000 4BFF		0x4000 8000 - 0x4000 83FF
USART2		0X4000 4400 - 0X4000 47FF		0x4000 4400 - 0x4000 47FF
SPI2		0X4000 3800 - 0X4000 3BFF		0x4000 3800 - 0x4000 3BFF
IWDG		0X4000 3000 - 0X4000 33FF		0x4000 3000 - 0x4000 33FF
WWDG		0X4000 2C00 - 0X4000 2FFF		0x4000 2C00 - 0x4000 2FFF
RTC + BKP_REG		0X4000 2800 - 0X4000 2BFF		0x4000 2800 - 0x4000 2BFF
LCD		0X4000 2400 - 0X4000 27FF		0x4000 2400 - 0x4000 27FF
TIMER7		0X4000 1400 - 0X4000 17FF		0x4000 1400 - 0x4000 17FF
TIMER6		0X4000 1000 - 0X4000 13FF		0x4000 1000 - 0x4000 13FF
TIMER3		0X4000 0400 - 0X4000 07FF		0x4000 0400 - 0x4000 07FF
TIMER2		0X4000 0000 - 0X4000 03FF		0x4000 0000 - 0x4000 03FF
OCTOSPI2	NA	NA	AHB3	0xA000 14000 - 0xA000 17FF
OCTOSPI1				0xA000 1000 - 0xA000 13FF
FSMC				0xA000 000 - 0xA000 03FF
SDMMC				0x5006 2400 - 0x5006 27FF (for STM32L4Rxxx/4Sxxx) (AHB2)

Table 22. Peripherals memory map (continued)

Peripheral	STM32L0 Series		STM32L4 Series / STM32L4+ Series	
	Bus	Base address	Bus	Base address
OCTOSPIM	NA	NA	AHB2	0x5006 1C00 - 0x5006 1FFF
HASH				0x5006 0400 - 0x5000 07FF
DCMI				0x5005 0000 - 0x5005 03FF
OTG_FS				0x5000 0000 - 0x5003 FFFF
GPIOI				0x4800 2000 - 0x4800 23FF
GPIOG				0x4800 1800 - 0x4800 1BFF
GPIOF				0x4800 1400 - 0x4800 17FF
GFXMMU			AHB1	0x4002 C000 - 0x4002 EFFF
DMA2D				0x4002 B000 - 0x4002 BBFF
DMA2				0x4002 0400 - 0x4002 07FF
DMAMUX				0x4002 0800 - 0x4002 0BFF
DSIHOST			APB2	0x4001 6C00 - 0x4001 73FF
LCD-TFT				0x4001 6800 - 0x4001 6BFF
DFSDM				0x4001 6000 - 0x4001 67FF
SAI2				0x4001 5800 - 0x4001 5BFF
SAI1				0x4001 5400 - 0x4001 57FF
TIM17				0x4001 4800 - 0x4001 4BFF
TIM16				0x4001 4400 - 0x4001 47FF
TIM15				0x4001 4000 - 0x4001 43FF
TIM8				0x4001 3400 - 0x4001 37FF
TIM1				0x4001 2C00 - 0x4001 2FFF
VREFBUF				0x4001 0030 - 0x4001 01FF
LPTIM2			APB1	0x4000 94000 - 0x4000 97FF
I2C4				0x4000 84000 - 0x4000 87FF
OPAMP				0x4000 7800 - 0x4000 7BFF
CAN1				0x4000 6400 - 0x4000 67FF
USART3				0x4000 4800 - 0x4000 4BFF
SPI3				0x4000 3C00 - 0x4000 3FFF
TIM5				0x4000 0C00 - 0x4000 0FFF
TIM4				0x4000 0800 - 0x4000 0BFF

Color key:

= same address in both series

= different base address in both series

1. COMP and SYSCFG share the same base address in the STM32L0 Series.

Refer to the reference manual or the datasheet for more details.

Note: An additional SRAM (SRAM2) is available in STM32L4 Series / STM32L4+ Series (64 Kbytes on STM32L4Rxxx/4Sxxx and STM32L49xxx/L4Axxx, 32 Kbytes on STM32L47xxx/L48xxx and STM32L45xxx/L46xxx, 16 Kbytes on STM32L43xxx/L44xxx, 8 Kbytes on STM32L41xxx/L42xxx) and an additional SRAM (SRAM3) of 384 Kbytes is available only in STM32L4Rxxx/4Sxxx.

The SRAM2 includes additional features listed below:

- Maximum performance through ICode bus access without physical remap
- Parity check option (32 bits + 4 bits parity check)
- Write protection with 1 Kbyte granularity
- Read protection (RDP)
- Erase by system reset (option byte) or by software
- Content is preserved in low-power run, low-power sleep, Stop 0, Stop 1 and Stop 2 modes
- Content can be preserved (RRS bit set in the PWR_CR3 register) in Standby mode (not the case for SRAM1)

5.3 Direct memory access controller (DMA)

STM32L0 Series and STM32L4 Series / STM32L4+ Series use the same DMA controller block. STM32L0 Series have one instance of this block with seven independent channels. STM32L4 Series / STM32L4+ Series have two instances of the same block bringing to 14 the number of independent channels.

For STM32L4Rxxx/4Sxxx, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer. In the rest of the STM32L4 Series / STM32L4+ Series, the DMA request line is connected directly to the peripherals.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routine function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

Table 23 presents the correspondence between the DMA requests of the peripherals in STM32L0 Series and STM32L4 Series / STM32L4+ Series.

Table 23. DMA request differences migrating STM32L0 Series to STM32L4 Series / STM32L4+ Series

Peripheral	DMA request	STM32L0 Series	STM32L4 Series / STM32L4+ Series
ADC	ADC	Channel1 Channel2	DMA1_Channel1 DMA2_Channel3
DAC	DAC1	Channel2	DMA1_Channel3 DMA2_Channel4
	DAC2	Channel4	DMA1_Channel4 DMA2_Channel5

Table 23. DMA request differences migrating STM32L0 Series to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32L0 Series	STM32L4 Series / STM32L4+ Series
SPI1	SPI1_Rx	Channel2	DMA1_Channel2 DMA2_Channel3
	SPI1_Tx	Channel3	DMA1_Channel3 DMA2_Channel4
SPI2	SPI2_Rx	Channel4 Channel6	DMA1_Channel4
	SPI2_Tx	Channel5 Channel7	DMA1_Channel5
USART1	USART1_Rx	Channel3 Channel5	DMA1_Channel5 DMA2_Channel7
	USART1_Tx	Channel2 Channel4	DMA1_Channel4 DMA2_Channel6
USART2	USART2_Rx	Channel5 Channel6	DMA1_Channel6
	USART2_Tx	Channel4 Channel7	DMA1_Channel7
LPUART	LPUART_Rx	Channel3 Channel6	DMA2_Channel7
	LPUART_Tx	Channel2 Channel7	DMA2_Channel6
UART4	UART4_Rx	Channel2 Channel6	DMA2_Channel5
	UART4_Tx	Channel3 Channel7	DMA2_Channel3
UART5	UART5_Rx	Channel2 Channel6	DMA2_Channel2
	UART5_Tx	Channel3 Channel7	DMA2_Channel1
I2C1	I2C1_Rx	Channel3 Channel7	DMA1_Channel7 DMA2_Channel6
	I2C1_Tx	Channel2 Channel6	DMA1_Channel6 DMA2_Channel7
I2C2	I2C2_Rx	Channel5	DMA1_Channel5
	I2C2_Tx	Channel4	DMA1_Channel4
I2C3	I2C3_Rx	Channel3 Channel5	DMA1_Channel3
	I2C3_Tx	Channel3 Channel5	DMA1_Channel2

Table 23. DMA request differences migrating STM32L0 Series to STM32L4 Series / STM32L4+ Series (continued)

Peripheral	DMA request	STM32L0 Series	STM32L4 Series / STM32L4+ Series
TIM2	TIM2_UP	Channel2	DMA1_Channel2
	TIM2_CH1	Channel5	DMA1_Channel5
	TIM2_CH2	Channel7 Channel3	DMA1_Channel7
	TIM2_CH3	Channel1	DMA1_Channel1
	TIM2_CH4	Channel4	DMA1_Channel7
TIM3	TIM3_UP	Channel3	DMA1_Channel3
	TIM3_CH1	Channel5	DMA1_Channel6
	TIM3_TRIG	Channel6	DMA1_Channel6
	TIM3_CH3	Channel2	DMA1_Channel2
	TIM3_CH4	Channel3	DMA1_Channel3
TIM6	TIM6_UP	Channel2	DMA1_Channel3 DMA2_Channel4
TIM7	TIM7_UP	Channel4	DMA1_Channel4 DMA2_Channel5
AES	AES_OUT	Channel2 Channel3	DMA2_Channel3 DMA2_Channel2
	AES_IN	Channel1 Channel5	DMA2_Channel1 DMA2_Channel5

5.4 Reset and clock control (RCC)

Figure 3, *Figure 4* and *Figure 5* represent the clock-trees of high-end devices of STM32L0 Series and STM32L4 Series / STM32L4+ Series. Their architecture are very similar. Both series share the same clock sources: three internal (LSI, HSI and MSI) and two external oscillators (LSE and HSE).

There is a dedicated RC system @ 48 MHz for USB and RNG on some part numbers. They embed a PLL and prescalers to adjust frequencies for the targeted devices. STM32L4 Series / STM32L4+ Series embed additional PLLs (x1 in STM32L45xxx/L46xxx and STM32L43xxx/L44xxx, x2 in STM32L4Rxxx/4Sxxx, STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx) dedicated to the audio interfaces (SAIx), ADC, RNG, SDMMC and OTG FS clock (STM32L4Rxxx/4Sxxx, STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx only).

Figure 3. STM32L0 Series clock tree

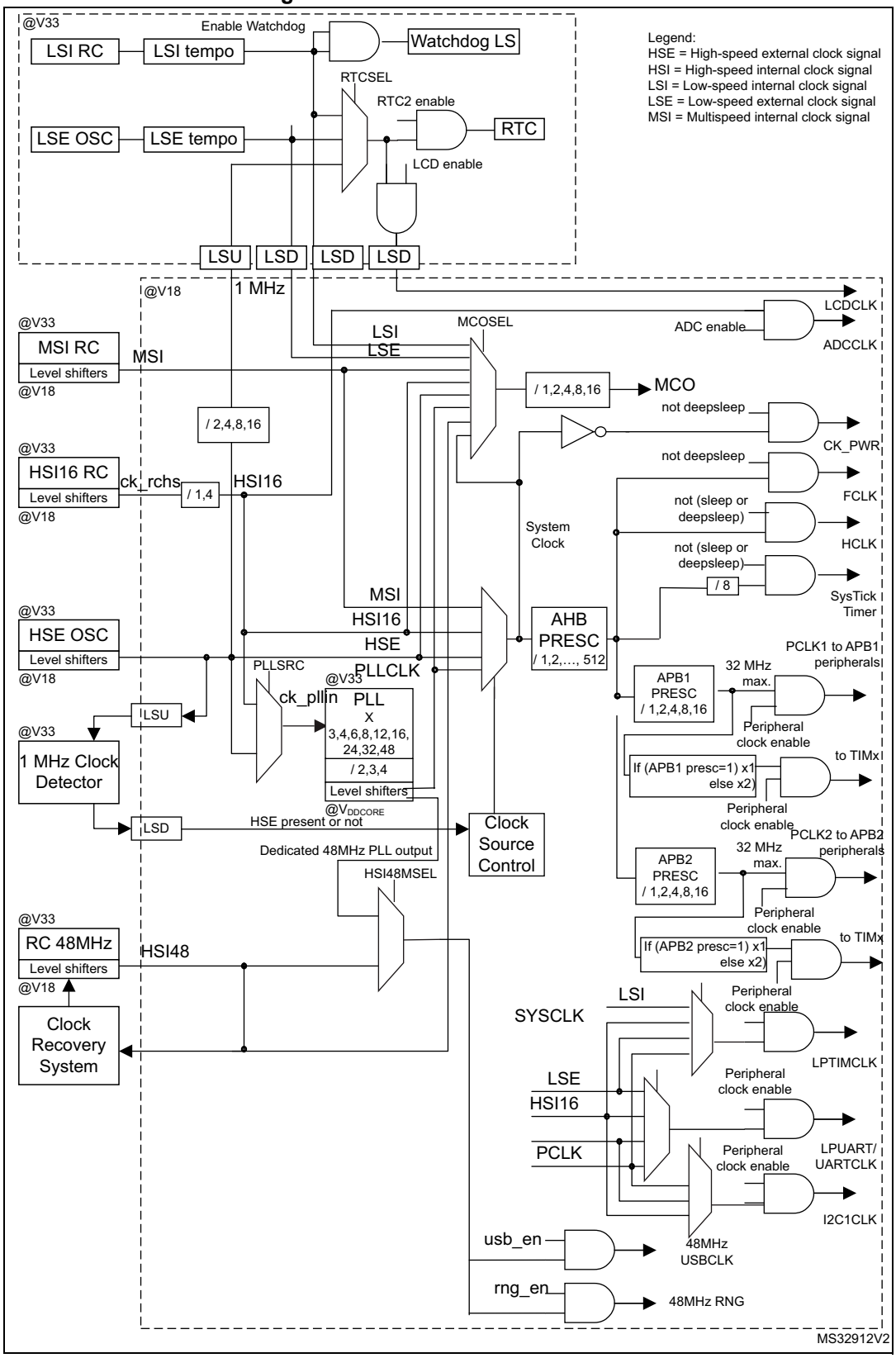


Figure 4. STM32L49xxx/L4Axxx clock tree

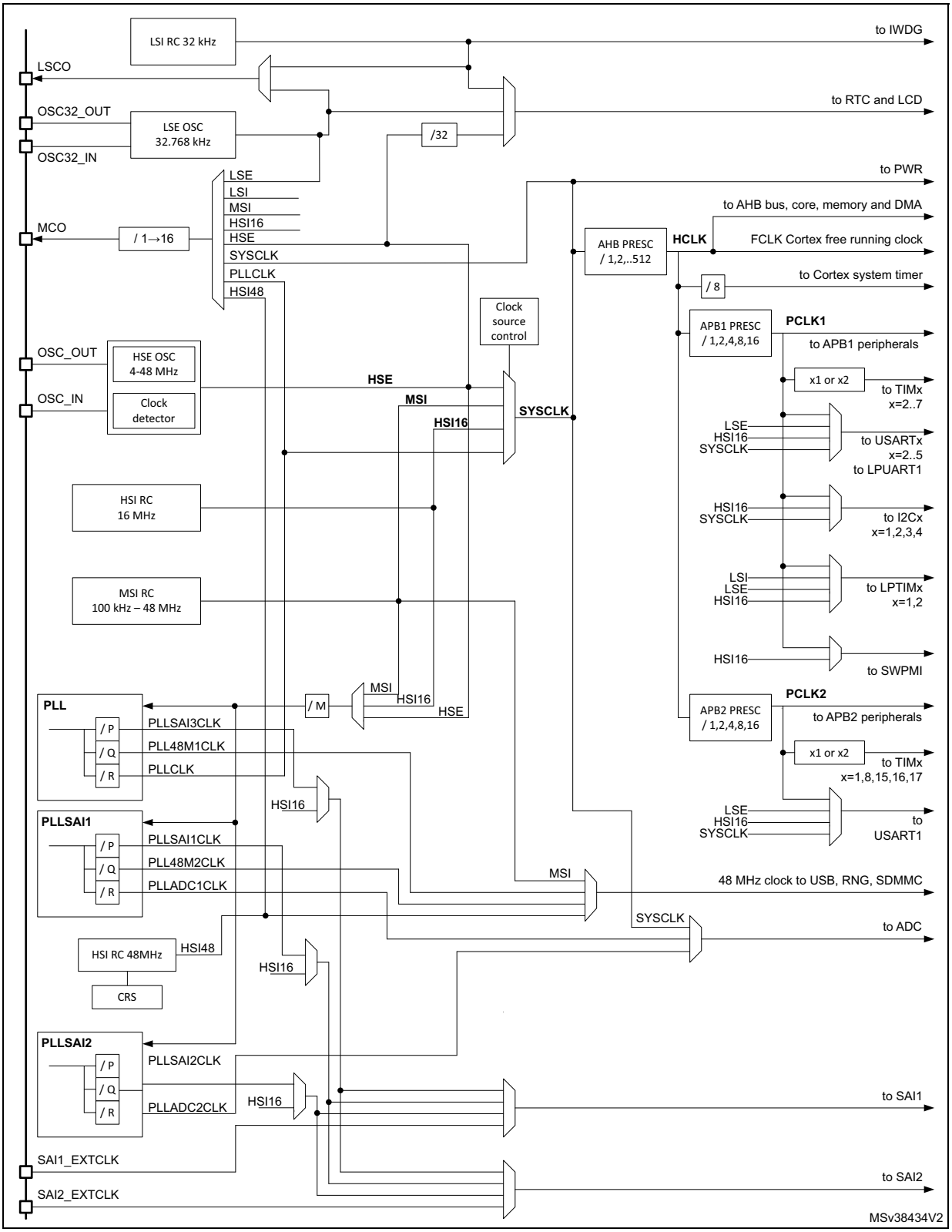
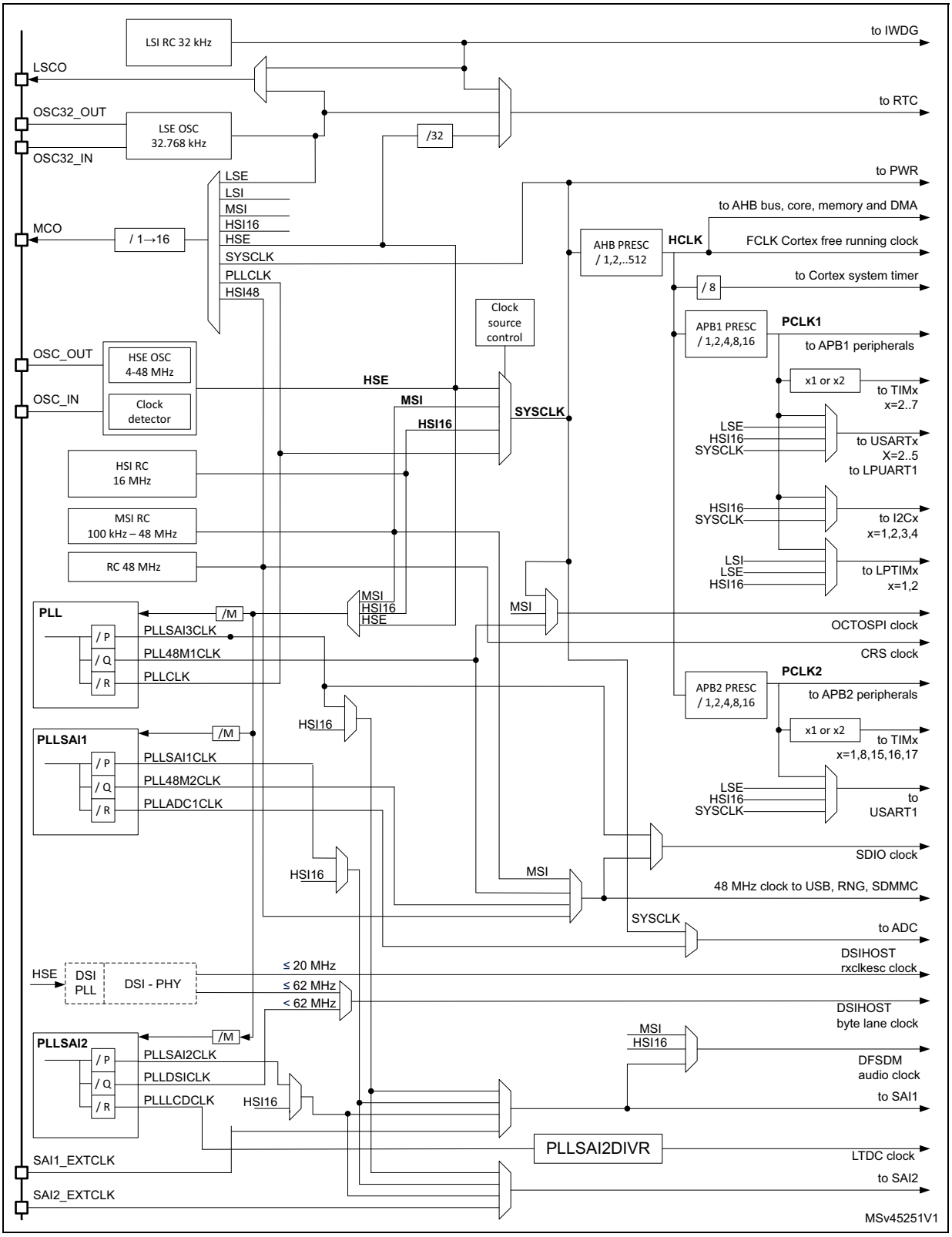


Figure 5. STM32L4Rxx/4Sxxx clock tree



The main RCC differences in STM32L4 Series / STM32L4+ Series compared to STM32L0 Series are presented in *Table 24*.

Table 24. RCC comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series

RCC		STM32L0 Series	STM32L4 Series / STM32L4+ Series
Clock sources	MSI	– Multi speed internal RC oscillator – Frequency ranges: 65.536 kHz, 131.072 kHz, 262.144 kHz, 524.288 kHz, 1.048 MHz, 2.097 MHz (default value) and 4.194 MHz – Factory and user calibration	– Multi speed internal RC oscillator – 12 frequency ranges: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz – Factory and user calibration – Auto calibration from LSE
	HSI16	– High speed internal 16 MHz RC oscillator – Factory and user trimmed	
	HSI48	– High speed internal 48 MHz RC oscillator – High precision clock for USB (CRS)	– High speed internal 48 MHz RC oscillator (only for STM32L4+ Series, STM32L49xxx/4Axxx, STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx) – High precision clock for USB (CRS) (not available in STM32L47xxx/L48xxx)
	LSI	– Low speed Internal clock – 32 Hz RC oscillator – Low-power clock	
	HSE	– High speed external clock – 1 to 24 MHz – From external clock or external crystal/ceramic resonator	– High speed external clock – 4 to 48 MHz – From external clock or external crystal/ceramic resonator
	LSE	– Low speed external clock – Low-power – Configurable drive/consumption – High accuracy 32.768 KHz	– Low speed external clock – 32.768 kHz – Configurable drive/consumption – Available in backup domain (VBAT)

Table 24. RCC comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

RCC		STM32L0 Series	STM32L4 Series / STM32L4+ Series
PLL	Input frequency	2 MHz to 24 MHz	4 MHz to 16 MHz
	Max output Frequency	48 MHz	80 MHz (and 120 MHz only in STM32L4Rxxx/4Sxxx)
	Sources	HSI16, HSE	HSI16, HSE, MSI
	Features	– One PLL with single output – PLL multiplication/division factors are different from STM32 L4 Series	– PLL embedded depending on devices – Main PLL for system PLL x1 for STM32L45xxx/L46xxx and STM32L43xxx/L44xxx x2 for STM32L4Rxxx/4Sxxx, STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx for SAI, ADC, RNG, SDMMC and OTG FS clock – Each PLL can provide up to 3 independent outputs – PLL multiplication/division factors are different from STM32L0 Series
System Clock	Sources	MSI, HSI, HSE or PLL	
	Frequency (see *Table 25*)	– Up to 32 MHz – 2.1 MHz after reset using MSI	– Up to 80 MHz (or 120MHz for STM32L4Rxxx/4Sxxx) – 4 MHz after reset using MSI
RTC clock source		LSI, LSE or HSE/32	
MCU clock outputs		MCO: SYSCLK, HSI16, HSI48, MSI, HSE, PLL, LSI, LSE	– MCO: SYSCLK, HSI16, MSI, HSE, PLL, LSI, LSE – HSI48 for STM32L45xxx/L46xxx, STM32L43xxx/L44xxx, STM32L41xxx/L42xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx – LSCO: LSI, LSE
Clock Security System (CSS)		Available on LSE and HSE	
TIMERS for clock measurement		TIM21	TIM15/16/17

Clock source frequency versus voltage scaling

The maximum system clock frequency and the Flash memory wait state depends on the selected voltage range VCORE and also on VDD for STM32L0 Series. *Table 25* gives the different clock source frequencies depending on the product voltage range.

Table 25. Performance versus V_{CORE} ranges(1)

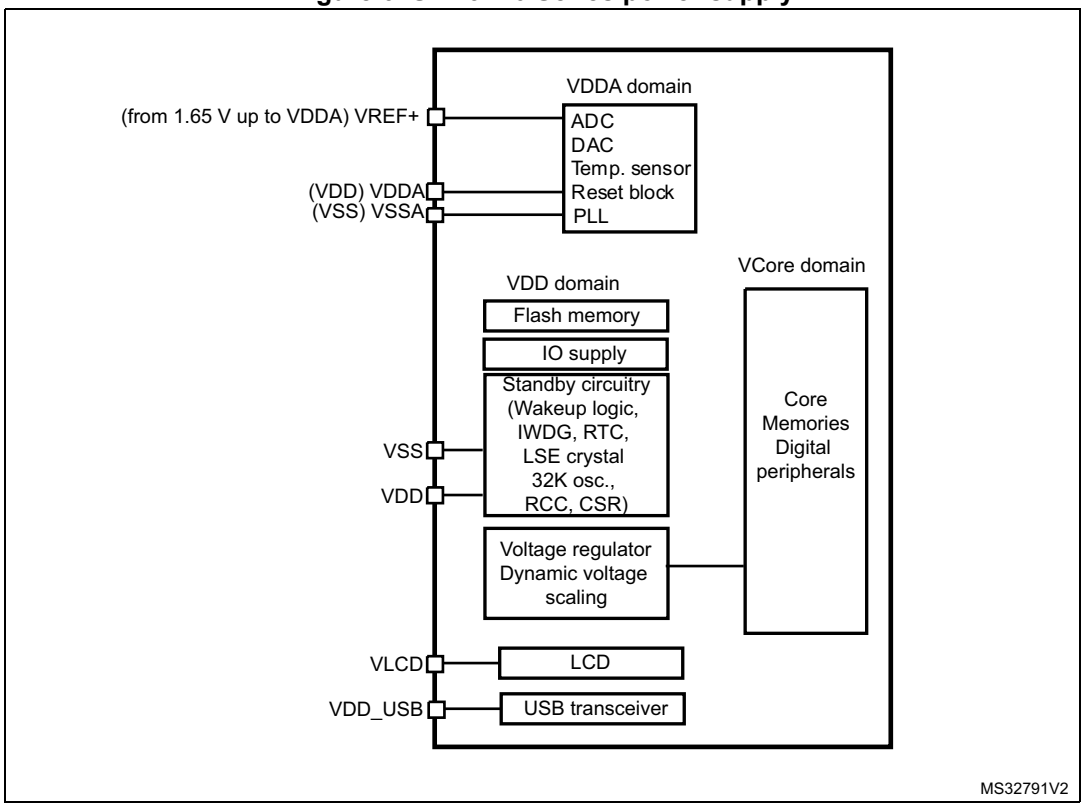
CPU performance	Power performance	VCORE range	Typical value (V)	Max frequency (MHz)						V_{DD} range
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS	
STM32L0 Series										
High	Low	1	1.8	-	-	-	-	32	16	1.71 - 3.6
Medium	Medium	2	1.5	-	-	-	-	16	8	1.65 - 3.6
Low	High	3	1.2	-	-	-	-	4.2	4.2	
STM32L4 Series										
High	Medium	1	1.2	-	80	64	48	32	16	NA
Medium	High	2	1.0	-	26	26	18	12	6	NA
STM32L4+ Series										
High	Medium	1 (boost mode)	1.28	120	100	80	60	40	20	NA
		1 (normal mode)	1.2	-	-	80	60	40	20	NA
Medium	High	2	1.0	-	-	-	26	16	8	NA

1. WS = wait state.

5.5 Power control (PWR)

Figure 6 and *Figure 7* present the power supply for both series. The differences are summarized in *Table 26*. For the low-power mode comparison, refer to *Section 4*.

Figure 6. STM32L0 Series power supply



1. This figure is not applicable on STM32L4Rxxx/4Sxxx.

Figure 7. STM32L4 Series power supply

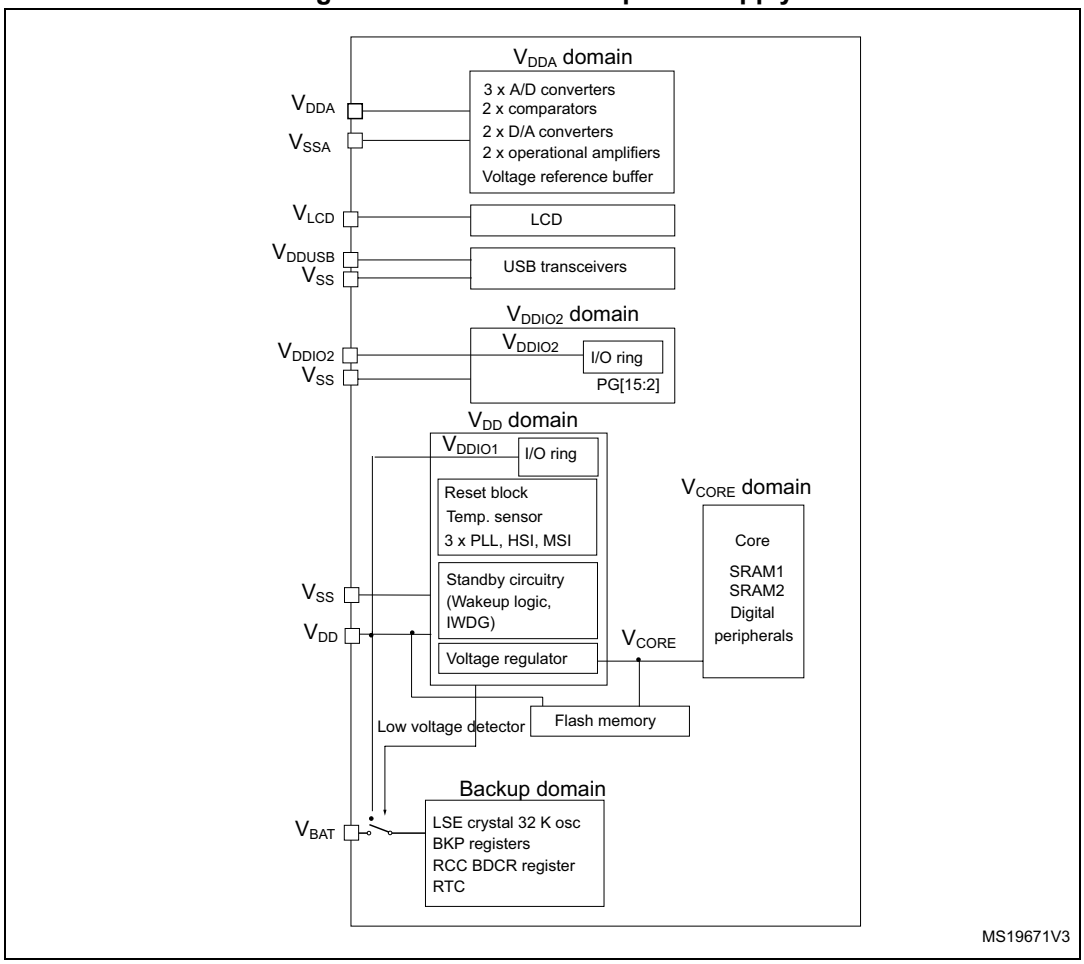


Figure 8. STM32L4+ Series power supply overview

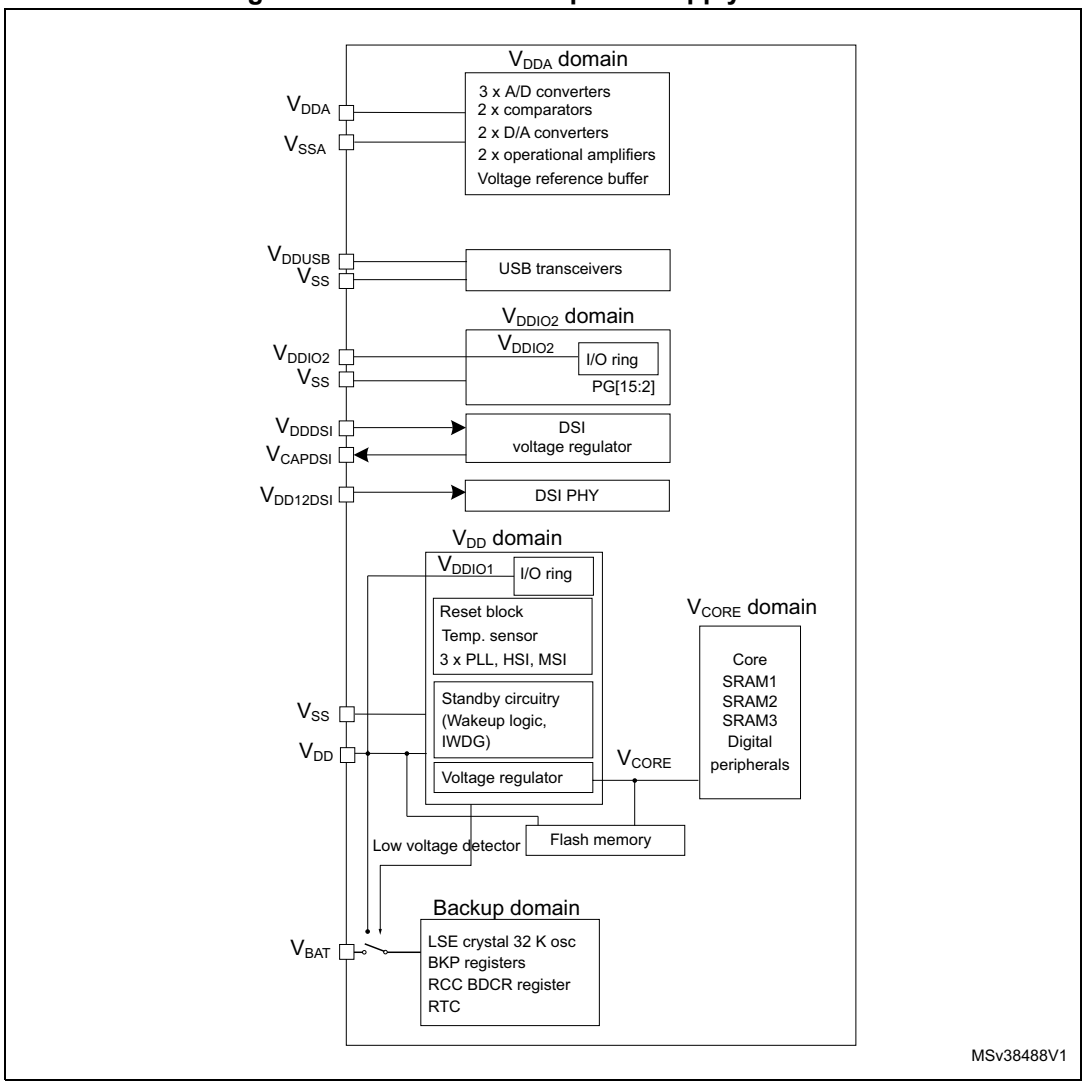


Table 26 compares the power features for both series.

Table 26. PWR comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series

PWR		STM32L0 Series	STM32L4 Series / STM32L4+ Series
Power supplies	**VDD**	– VDD is the external power supply for I/Os and internal regulator – It is provided externally through VDD pins	
		– 1.8 V at power-on or 1.65 V at power-down to 3.6 V when the BOR is available – VDD = 1.65 V to 3.6 V when BOR is not available	1.71 to 3.6 V
	VDDIO2	-	– 1.08 V to 3.6 V – VDDIO2 is the external power supply for 14 I/Os (Port G[15:2]) – The VDDIO2 voltage level is independent from the VDD voltage and can be tied to ground when PG[15:2] are not used
	VCore	– VCORE is the power supply for digital peripherals, SRAM and Flash memory – It is generated by an internal voltage regulator – Three VCORE ranges can be selected by software depending on target frequency	
		1.2 to 1.8 V	1.0 to 1.28 V
	VSSA, VDDA	VDDA is the external analog power supply for ADC, DAC, voltage reference buffer, operational amplifiers and comparators.	
		– 1.8 V at power-on or 1.65 V at power-down to 3.6 V when BOR is available – VSSA, VDDA = 1.65 to 3.6 V when BOR is not available – For DAC min VDDA = 1.8 V	From – 1.62 V (ADCs/COMPs) – 1.8 V (DACs/OPAMPs) – 2.4 V (VREFBUF) to 3.6 V
	VREF-, VREF+	– VREF+ is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled – VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA, respectively	
	V_{BAT}	NA	– 1.55 to 3.6 V – VBAT is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present – When VDD is present, it is possible to charge the external battery on VBAT through an internal resistance – It is automatically disabled in VBAT mode

Table 26. PWR comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

PWR		STM32L0 Series	STM32L4 Series / STM32L4+ Series
Power supply (continued)	**V_{LCD}**	– 2.5 to 3.6 V – The LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter	
	VDD_USB	– 3.0 to 3.6V – VDDUSB is the external independent power supply for USB transceivers – The VDDUSB voltage level is independent from the VDD voltage and should preferably be connected to VDD when the USB is not used	
	VDDDSI	NA	– Available only on SM32L4R9xx/4S9xx – Independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY – This supply must be connected to the global VDD
	VCAPDSI	NA	– Available only on SM32L4R9xx/4S9xx – Output of the DSI regulator (1.2 V) which must be connected externally to VDD12DSI
	VDD12DSI	NA	– Available only on SM32L4R9xx/4S9xx – It is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins – An external capacitor of 2.2 µF must be connected on the VDD12DSI pin
Battery backup domain		NA	– To retain the content of the Backup registers and supply the RTC function when VDD is turned off, the VBAT pin can be connected to an optional backup voltage supplied by a battery or by another source
Voltage regulator		– Range 1 (VCore 1.8V); HCLK up to 32 MHz – Range 2 (VCore 1.5V); HCLK @ 16 MHz – Range 3 (VCore 1.2V); HCLK @ 4.2 MHz	– Range 1 boost mode (Vcore = 1.28 V); HCLK up to 120 MHz (applicable only on STM32L4Rxxx/4Sxxx) – Range 1 normal mode (default) (VCore= 1.2 V); HCLK up to 80 MHz – Range 2 (VCore = 1.0 V); HCLK @ 26 MHz

Table 26. PWR comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

PWR	STM32L0 Series	STM32L4 Series / STM32L4+ Series
Power supply supervisor	Integrated POR / PDR circuitry @ 1.5 V	Integrated POR / PDR circuitry
	Brownout reset (BOR)	Brownout reset (BOR)
	PVD monitors VDDA/VDD	– 4 peripheral voltage monitoring (PVM) – PVM1 for V_{DDUSB} – PVM2 for V_{DDIO2} – PVM3/PVM4 for V_{DDA} (~1.65V/ ~2.2V)
Low-power modes	– Sleep mode – Low-power Run mode up to 131 KHz – Low-power Sleep mode up to 131 KHz – Stop mode – Standby mode (V_{CORE} domain powered off) – Refer to *Section 4.1*	– Sleep mode – Low-power Run mode up to 2 MHz – Low-power Sleep mode up to 2 MHz – Stop 0, Stop 1 and Stop 2 modes – Standby mode (V_{CORE} domain powered off) – Shutdown mode (V_{CORE} domain powered off and power monitoring off) – Refer to *Section 4.2*
External SMPS	NA	– Support for external SMPS for high-power efficiency. Refer to AN4978.

5.6 Flash memory

Table 27 presents the difference between the Flash memory interface of STM32L0 Series and STM32L4 Series / STM32L4+ Series.

The STM32L4 Series / STM32L4+ Series devices instantiate a different Flash module both in terms of architecture, technology and interface. Consequently the STM32L4 Flash memory programming procedures and registers are different from the ones in STM32L0 Series. Any code written for the Flash interface in STM32L0 Series needs to be rewritten to run on STM32L4 Series / STM32L4+ Series.

For more information on programming, erasing and protection of the STM32L4 Flash memory, refer to STM32L4 Series / STM32L4+ Series reference manuals (RM0351, RM0394, RM0392 and RM0432).

Table 27. FLASH differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series

FLASH	STM32L0 Series	STM32L4 Series / STM32L4+ Series
Main/ Program memory	– Up to 192 Kbytes in one or two banks (only in STM32L07/8x devices) – Word: 32 bits – Page: 128 bytes (316 bytes) – Sector: 32 pages (4 Kbytes)	– Up to 1 Mbyte Split in 2 Banks – Word: 64 bits – Page: 2 Kbytes (8 rows of 256 bytes) – Bank: up to 256 pages of 2 Kbytes (512 Kbytes) – For STM32L4Rxxx/4Sxxx: Up to 2 Mbytes Split in 2 Banks Single-bank mode: word = 64 bits Up to 256 pages of 8 Kbytes Dual-bank mode: word = 128 bits Up to 256 page of 4 Kbytes
Flash empty check	In Cat. 1 only	– ECC – Flash empty check (only for STM32L45xxx/46xxx, STM32L43xxx/44xxx, STM32L41xxx/L42xxx, STM32L49xxx/4Axxx and STM32L4Rxxx/4Sxxx)
ECC	– 6 bits/word (32bits) – One error correction – Two errors detection	– 8 bits for 64-bit double word – One error correction – Two errors detection
Wait State	0 or 1	Up to 5 (depending on the Core voltage and frequency)
ART Accelerator™	NA	– Prefetch on ICODE – Instruction Cache: 32 cache lines of 4 x 64 bits on ICode (1 Kbyte RAM) – Data Cache: 8 cache lines of 4 x 64 bits on DCode (256 bytes RAM)

Table 27. FLASH differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

FLASH	STM32L0 Series	STM32L4 Series / STM32L4+ Series
Data EEPROM memory	– Up to 6 Kbytes in one or two banks – Write Access byte, half word, word	NA (can be emulated by SW)
System memory	Up to 8 Kbytes	28 Kbytes per bank
One time programmable (OTP)	-	1 KByte (Bank1 only)
Option bytes	96 bytes (factory) + 32 bytes (user)	32 bytes per bank
Erase granularity	Page erase: 128 bytes	Page erase (2 Kbytes), Bank erase and Mass erase (both banks)
Readout protection (RDP)	– Level 0 no protection – RDP = 0xAA	
	– Level 1 memory protection – RDP!= (Level 2 & Level 0)	
	Level 2 RDP = 0xCC (1)	
Proprietary code readout protection (PCROP)	Protection set by sector (4 Kbytes)	– One protected area per bank – Granularity: 64 bit – PCROP_RDP option: PCROP area preserved when RDP level decreased – For STM32L4Rxxx/4Sxxx: Dual bank: 1 PCROP area per bank Single bank: 2 PCROP area
Write protection (WRP)	– Single protected area – Protection set by sector (4 Kbytes)	– 2 Write protection areas per bank – Granularity: 2 Kbytes – For STM32L4Rxxx/4Sxxx: Dual bank: 2 areas per bank Single bank: 4 areas
Option bytes	Global options: – RDP protection – User option bytes – Write/PCROP sectors number	Global options: – RDP protection – User option bytes Bank options: – PCROP start@ – PCROP end@ – Write Protection Area 1 @ – Write Protection Area 2 @ – DBANK (only for STM32L4Rxxx/4Sxxx) – DB1M (only for STM32L4Rxxx/4Sxxx)

1. Memory read protection Level 2 is an irreversible operation. When the Level 2 is activated, the level of protection cannot be decreased to Level 0 or Level 1.

5.7 Serial peripheral interface (SPI)/ IC to IC sound (I2S) serial audio interface (SAI)

STM32L4 Series / STM32L4+ Series and STM32L0 Series implement a very close version of the SPI peripheral. STM32L4 Series / STM32L4+ Series have an upgraded version of the IP without the support of the I2S interface. In STM32L4 Series / STM32L4+ Series, the I2S is supported by the SAI interface (see *Section 5.7*).

The SPI peripherals in both series share the following features:

- Master or slave operation
- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- Multimaster mode capability
- 8 master mode baud rate prescalers up to fPCLK/2.
- Slave mode frequency up to fPCLK/2.
- NSS management by hardware or software for both master and slave: dynamic change of master/slave operations
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Dedicated transmission and reception flags with interrupt capability
- SPI bus busy status flag
- SPI Motorola support
- Hardware CRC feature for reliable communication:
  - CRC value can be transmitted as last byte in Tx mode
  - Automatic CRC error checking for last received byte
- Master mode fault, overrun flags with interrupt capability
- CRC Error flag
- SPI TI mode support

The differences between both series are listed in *Table 28*.

Table 28. SPI differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series

SPI	STM32L0 Series	STM32L4 Series / STM32L4+ Series
Instances	– SPI1 w/o I2S support – SPI2 with I2S support	SPI1, SPI2, SPI3. All without I2S support
Features	I2S support	– I2S feature is not supported by SPI2 – SAI interfaces are available instead
Data size	8-bits or 16 bits	– Programmable from 4 to 16 bits – Data packing
Data buffer	NA	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	NA	– YES – 8-bit, 16-bit or 32-bit data access, programmable FIFOs data thresholds
Speed	Up to 16 Mbits/s slave and master modes	– Up to 40 Mbits/s in master mode – Up to 24 Mbits/s in slave mode

The I2S protocol is supported by the SPI peripheral in STM32L0 Series. STM32L4 Series / STM32L4+ Series embed a new SAI peripheral instead. The SAI peripheral brings more flexibility and improves the robustness of communication in the Slave mode compared to the I2S peripheral (in case of the data clock glitch for example). *Table 29* presents the main differences between both implementations.

Table 29. Audio interface support in STM32L0 Series and STM32L4 Series / STM32L4+ Series

I2S	STM32L0 Series (SPI)	STM32L4 Series / STM32L4+ Series (SAI)
Instances	1 (with SPI2 peripheral)	– x2 in STM324Rxxx/4Sxx, STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx (SAI1 and SAI2) – x1 in STM32L45xxx/L46xxx and STM32L43xxx/L44xxx (SAI1)
Architecture	– I2S supported by SPI peripheral. – Support Master and slave modes	– Two independent audio sub-blocks (per SAI) which can be transmitters or receivers with their respective FIFO – Master/Slave configuration independent for both audio sub-blocks (2 sub-blocks per SAI peripherals) – Synchronous or asynchronous mode between the audio sub-blocks. Possible synchronization between multiple SAIs – Frame synchronization active level configurable (offset, bit length, level) – Stereo/Mono audio frame capability – Mute mode – PDM interface for STM32L4Rxxx/L4Sxxx
Pins mapping	– SD (serial data) => on MOSI pin – WS (word select) => on NSS pin – CK (serial clock) => on SCK pin – MCLK	SD, SCK, FS, MCLK
Data formats	– 16-bit data packed in a 16-bit frame – 16-bit data packed in a 32-bit frame – 24-bit data packed in a 32-bit frame – 32-bit data packed in a 32-bit frame	– 8-bit, 10-bit, 16-bit, 20-bit, 24-bit, 32-bit – LSB or MSB first
Standards	– I2S Philips – I2S MSB justified – I2S LSB justified – PCM	– I2S Philips – I2S MSB justified – IS2 LSB justified – PCM/DSP – TDM (Time Division Multiplexing) up to 16 channels) – AC’97 (Intel)

5.8 USB

STM32L45xxx/L46xxx, STM32L43xxx/L44xxx, STM32L41xxx/L42xxx and STM32L0 Cat.3 and Cat.5 implement the same USB 2.0 device full-speed controller. This version supports a crystal-less device by using a clock recovery system (CRS) peripheral. The CRS provides a precise clock to the USB peripheral. The synchronization signal is derived from the start-of-frame (SOF) packet signalization on the USB bus, which is sent by a USB host at precise 1 ms intervals.

STM32L4Rxxx/4Sxxx, STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx devices embed a new 2.0 USB-OTG full speed version with integrated PHY.

The key differences between both USB peripherals are listed in *Table 30*.

Table 30. USB peripheral comparison

USB	STM32L0 Cat. 3 and Cat. 5 STM32L45xxx/L46xxx, STM32L43xxx/L44xxx and STM32L41xxx/L42xxx	STM32L4Rxxx/4Sxxx, STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx
Features	– Universal Serial Bus Revision 2.0, including Link Power Management (LPM) support – Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps)	
	NA	– Full support for the USB On-The-Go (USB OTG) – Up to 12 host channels
	Embedded FS USB Device PHY	Embedded FS OTG PHY
	FS mode: – 1 bidirectional control endpoint – 7 IN endpoints (Bulk, Interrupt, Isochronous) – 7 OUT endpoints (Bulk, Interrupt, Isochronous)	FS mode: – 1 bidirectional control endpoint – 5 IN endpoints (Bulk, Interrupt, Isochronous) – 5 OUT endpoints (Bulk, Interrupt, Isochronous)
	Battery charging detection (BCD)	– Attach detection protocol (ADP) – Battery charging detection (BCD)
	Independent VDDUSB power supply allowing lower VDD while using USB	
Buffer memory	1024 bytes (endpoint buffers and buffer descriptors structure)	Device mode: 1.25 Kbyte data FIFOs
Low-power modes	– USB suspend and resume – Link power management (for STM32L0 Series only)	– USB suspend and resume – Link power management (LPM)

5.9 Analog-to-digital converters (ADC)

The ADC converters embedded in both series share advanced options such as:

- Several resolutions
- Auto-calibration
- Analog watchdogs
- Over-sampler up to 256x
- Efficient low-power mode

STM32L0 Series embed one ADC instance while STM32L4 Series / STM32L4+ Series embed three of them. The two instances (ADC1 and ADC2) can be coupled to allow dual mode operation.

Table 31 presents the differences between the ADC peripheral of the STM32L0 Series and the STM32L4 Series.

Table 31. ADC differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series

ADC	STM32L0 Series	STM32L4 Series / STM32L4+ Series
ADC Type	SAR structure	SAR structure
Instances	ADC1	– x3 for STM32L49xxx/L4Axxx and STM32L47xxx/L48xxx – x2 for STM32L41xxx/L42xxx – x1 for STM32L4Rxxx/4Sxxx, STM32L45xxx/L46xxx and STM32L43xxx/L44xxx
Max Sampling freq @12bits	1.14 MSPS	– 5.33 MSPS (Fast channels) – 4.21 MSPS (Slow channels)
Max Sampling freq @10bits	1.23 MSPS	6.25 MSPS
Number of external channels	16 external analog inputs	For each ADC: – Up to 5 fast external channels – Up to 11 slow external channels
Number of internal channels	– Temperature sensor – Reference voltage – VLCD power supply	– Temperature sensor – Reference voltage – Power supply – DAC1, DAC2 output
Resolution	12,10,8 or 6 bits configurable resolution	12,10,8 or 6 its configurable resolution
Conversion modes	Single / continuous / scan / discontinuous/ dual mode	Single / continuous / scan / discontinuous/ dual mode
Dual ADC mode	NA	ADC1+ADC2
DFSDM redirection	NA	Available for STM32L45xxx/L46xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx
DMA	Yes	Yes

Table 31. ADC differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series (continued)

ADC	STM32L0 Series	STM32L4 Series / STM32L4+ Series
SW trigger	Yes	Yes
HW trigger	– Internal timers (TIM2, TIM3, TIM6, TIM21, TIM22) – GPIO input events	– Internal timers (TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15) – GPIO input events
Supply requirement	1.65 V to 3.6 V	– 1.62 V to 3.6 V – Independent power supply (VDDA)
Reference Voltage	External	External or Internal (2.048 V or 2.5 V)
Input range	V_{SSA} <= V_{IN} <= V_{DDA} (analog ground and power supply)	V_{REF-} <= V_{IN} <= V_{REF+} (V_{REF-} = V_{SSA} and 1.62 V ≤ V_{REF+} ≤ V_{DDA})

5.10 Digital-to-analog converter (DAC)

The DAC of both series shares the following features:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave and Triangular-wave generation
- Dual DAC channel for independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- External triggers for conversion
- Input voltage reference
- V_{REF+}

STM32L4 Series / STM32L4+ Series implement an enhanced DAC version compared to the STM32L0 Series one. *Table 32* shows these differences.

Table 32. DAC differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series

DAC	STM32L0 Series	STM32L4 Series / STM32L4+ Series
Instances	– x1 on STM32L05xxx and STM32L06xxx – x2 on STM32L07xxx and STM32L08xxx – No DAC for other devices	– x2 on STM32L4Rxxx/4Sxxx, STM32L49xxx/L4Axxx, STM32L47xxx/L48xxx and STM32L43xxx/L44xxx – x1 on STM32L45xxx/L46xxx devices
Resolution	12-bit	12-bit
Features	– Left or right data alignment in 12-bit mode – Noise-wave and Triangular-wave generation – Dual DAC channel for independent or simultaneous conversions	
	NA	– Auto-calibration – DAC_OUTx can be disconnected from output pin – Sample and Hold mode for low-power operation in STOP mode
External trigger	– TIM6 TRGO – TIM3 TRGO – TIM3 CH3 – TIM21 TRGO – TIM2 TRGO – TIM7 TRGO – EXTI line9 – SW TRIG	– TIM6 TRGO – TIM8 TRGO(1) – TIM7 TRGO – TIM5 TRGO(1) – TIM2 TRGO – TIM4 TRGO(1) – EXTI line9 – SW TRIG Additional trigger for STM32L4Rxxx/4Sxxx: – TIM1_TRGO – TIM15_TRGO – LPTIM1_OUT – LPTMI2_OUT

1. Except on STM32L43xxx/L44xxx devices.

5.11 Comparator (COMP)

Both series embed two comparators that can be used for a variety of functions including:

- Wake up from the low-power mode triggered by an analog signal
- Analog signal conditioning
- Cycle-by-cycle current control loop when combined with a PWM output from a timer.

Table 33 presents the differences between the COMP interface of STM32L0 Series and STM32L4 Series / STM32L4+ Series.

Table 33. COMP differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series

COMP	STM32L0 Series	STM32L4 Series / STM32L4+ Series
Type	– COMP1 ultra-low-power – COMP2 Rail to rail	– COMP1 – COMP2 Rail to rail
Inputs +	– COMP1 & COMP2 – PA3/PB4/PA5(DAC2)/PB6/PB7 – COMP1 – PA1	– PC5/PB2 (COMP1) – PB4/PB6 (COMP2)
Inputs -	– COMP1: V_{REFINT} PA0 DAC Channel1 (PA4) DAC Channel2 (PA5) – COMP2: ¼ V_{REFINT} ½ V_{REFINT} ¾ V_{REFINT} V_{REFINT} PA2 DAC Channel1 (PA4) DAC Channel2 (PA5) PB3	– COMP1& COMP2: ¼ V_{REFINT} ½ V_{REFINT} ¾ V_{REFINT} V_{REFINT} DAC Channel1 DAC Channel2 PB1/PC4 (COMP1) PB3/ PB7(COMP2)
Outputs	– EXTI line – GPIOx – Timers input	
Features	Window comparator	Window comparator
	NA	Hysteresis
	NA	– Output with Blanking Source – Programmable hysteresis
	COMP2 only: – High speed/ full power – Low speed / low-power	Power/speed modes: – High speed/ full power – Medium speed/ medium power – Low speed/ ultra-low-power

6 Firmware migration

The STM32L0 Series and STM32L4 Series / STM32L4+ Series libraries have the same architecture and are CMSIS compliant, they use the same driver naming and the same APIs for all compatible peripherals.

The HAL libraries has been built in order to reduce the migration needs between products through the usage of high level functions usable by all products.

Only a few peripheral drivers need to be updated to migrate the application from one series to another.

As examples, the next sections focus on the most sensible features: FLASH, PWR and RCC settings/ activation.

6.1 HAL FLASH

STM32L0 Series and STM32L4 Series / STM32L4+ Series are based on the different Flash memory technology with different controllers. Refer to *Section 5.6* for detailed description of these differences. The impacts on software concern the option bytes access, the data access and the protections settings:

- Different option byte structures
- PCROP settings
- Word length
- EEPROM for the STM32L0 Series only

Table 34 gives the option byte structures in both series. On STM32L0 Series the PCROP protection is managed by setting a bit for each sector to protect, while on STM32L4 Series / STM32L4+ Series the user defines the start and end protection address into the dedicated PCROP address registers (FLASH_PCROP1SR, FLASH_PCROP1ER, FLASH_PCROP2SR, FLASH_PCROP2ER).

On STM32L0 Series, the SPRMOD bit sets the protection mode from WRP to PCROP while, on STM32L4 Series / STM32L4+ Series, the protection modes can be set separately.

Table 34. Option byte structure comparison

Structure	STM32L0 Series	STM32L4 Series / STM32L4+ Series
FLASH_OBProgramInitTypeDef	uint32_t OptionType uint32_t WRPState uint32_t WRPSector uint32_t WRPSector2 uint8_t RDPLevel uint8_t BORLevel uint8_t USERConfig uint8_t BOOTBit1Config	uint32_t OptionType uint32_t WRPArea uint32_t WRPStartOffset uint32_t WRPEndOffset uint32_t RDPLevel uint32_t USERType uint32_t USERConfig uint32_t PCROPConfig uint32_t PCROPStartAddr uint32_t PCROPEndAddr
FLASH_AdvOBProgramInitTypeDef	uint32_t OptionType uint8_t PCROPState uint32_t PCROPSector uint32_t PCROPSector2 uint8_t BootConfig	NA

Generic API

Both series share the same generic API. The only difference is the Flash memory word size: 32 bits in STM32L0 Series and 64 bits in STM32L4 Series / STM32L4+ Series (*Table 35*).

Table 35. FLASH generic API

FLASH Generic API	STM32L0 Series	STM32L4 Series / STM32L4+ Series
HAL_FLASH_Program	Uint32_t data	Uint64_t data
HAL_FLASH_Program_IT	Uint32_t data	Uint64_t data
HAL_FLASH_IRQHandler	Same prototype	
HAL_FLASH_EndOfOperationCallback		
HAL_FLASH_OperationErrorCallback		
HAL_FLASH_Unlock		
HAL_FLASH_Lock		
HAL_FLASH_OB_Unlock		
HAL_FLASH_OB_Lock		
HAL_FLASH_OB_Launch		
HAL_FLASH_GetError		

Extended API

The extended HAL functions are dedicated to the option bytes programming and the EEPROM management.

Table 36. FLASH extended API

FLASH Extended API	STM32L0 Series	STM32L4 Series / STM32L4+ Series
HAL_FLASHEx_Erase	Same prototype	
HAL_FLASHEx_Erase_IT		
HAL_FLASHEx_OBProgram		
HAL_FLASHEx_OBGetConfig		
HAL_FLASHEx_AdvOBProgram	Used for PCROP configuration	NA All OB programmed in HAL_FLASHEx_OBProgram
HAL_FLASHEx_AdvOBGetConfig		
HAL_FLASHEx_OB_SelectPCROP		
HAL_FLASHEx_OB_DeSelectPCROP		
HAL_FLASHEx_DATAEEPROM_Unlock	EEPROM configuration	NA No EEPROM
HAL_FLASHEx_DATAEEPROM_Lock		
HAL_FLASHEx_DATAEEPROM_Erase		
HAL_FLASHEx_DATAEEPROM_Program		
HAL_FLASHEx_DATAEEPROM_EnableFixedTimeProgram		
HAL_FLASHEx_DATAEEPROM_DisableFixedTimeProgram		

6.2 HAL_PWR

The HAL_PWR functions are used to configure the power management strategy: the low-power mode selection, the wakeup management and the power voltage monitoring. *Table 37* presents the main power API. It is dedicated to the special power management features available (mostly) in STM32L4 Series / STM32L4+ Series.

There are five low-power modes in STM32L0 Series (low-power run, sleep, low-power sleep, stop and standby) and nine in STM32L4 Series / STM32L4+ Series (low-power run, sleep, low-power sleep, Stop 0, Stop 1, Stop 2, standby with or without SRAM2 retention and shutdown).

Generic API

Table 37. HAL_PWR

Power management API	STM32L0 Series	STM32L4 Series / STM32L4+ Series
HAL_PWR_DeInit	Same prototype	
HAL_PWR_EnableBkUpAccess	Backup registers Same prototypes	
HAL_PWR_DisableBkUpAccess		
HAL_PWR_ConfigPVD	Programmable voltage detector Same prototypes	
HAL_PWR_EnablePVD		
HAL_PWR_DisablePVD		
HAL_PWR_PVDCallback		
HAL_PWR_EnableWakeUpPin	Same prototypes	
HAL_PWR_DisableWakeUpPin		
HAL_PWR_EnterSLEEPMode	Sleep and Low-power sleep modes (depending on regulator status)	
HAL_PWR_EnterSTOPMode	Stop mode	For legacy only. See HAL_PWREx_EnterSTOP1Mode and HAL_PWREx_EnterSTOP2Mode
HAL_PWR_EnterSTANDBYMode	Standby mode	
HAL_PWR_EnableSleepOnExit	Same prototypes	
HAL_PWR_DisableSleepOnExit		
HAL_PWR_EnableSEVOnPend		
HAL_PWR_DisableSEVOnPend		

The power extension API is for management of the new power features available in STM32L4 Series / STM32L4+ Series. The STM32L0 API extension concerns the low-power and ultra-low-power (ULP) modes.

Extended API

Table 38. HAL_PWREx

Extended Power API	STM32L0 Series	STM32L4 Series / STM32L4+ Series
HAL_PWREx_GetVoltageRange	NA	Main regulator range (1 or 2)
HAL_PWREx_ControlVoltageScaling		
HAL_PWREx_EnableBatteryCharging		Battery charging
HAL_PWREx_DisableBatteryCharging		
HAL_PWREx_EnableVddUSB		USB supply
HAL_PWREx_DisableVddUSB		
HAL_PWREx_EnableVddIO2		IO2 supply
HAL_PWREx_DisableVddIO2		
HAL_PWREx_EnableInternalWakeUpLine		Internal Wakeup line
HAL_PWREx_DisableInternalWakeUpLine		
HAL_PWREx_EnableGPIOPullUp		Manage GPIO state in Standby and Shutdown modes
HAL_PWREx_DisableGPIOPullUp		
HAL_PWREx_EnableGPIOPullDown		
HAL_PWREx_DisableGPIOPullDown		
HAL_PWREx_EnablePullUpPullDownConfig		
HAL_PWREx_DisablePullUpPullDownConfig		
HAL_PWREx_EnableSRAM2ContentRetention		Retention configuration in Standby mode
HAL_PWREx_DisableSRAM2ContentRetention		
HAL_PWREx_EnablePVM1		VDDUSB versus 1.2V
HAL_PWREx_DisablePVM1		
HAL_PWREx_EnablePVM2		VDDUSB versus 0.9V
HAL_PWREx_DisablePVM2		
HAL_PWREx_EnablePVM3		VDDUSB versus 1.62V
HAL_PWREx_DisablePVM3		
HAL_PWREx_EnablePVM4		VDDA versus 2.2V
HAL_PWREx_DisablePVM4		
HAL_PWREx_ConfigPVM		PVM management
HAL_PWREx_PVM1Callback		
HAL_PWREx_PVM2Callback		
HAL_PWREx_PVM3Callback		
HAL_PWREx_PVM4Callback		
HAL_PWREx_PVD_PVM_IRQHandler		
HAL_PWREx_EnterSTOP0Mode		Stop 0 mode

Table 38. HAL_PWREx (continued)

Extended Power API	STM32L0 Series	STM32L4 Series / STM32L4+ Series
HAL_PWREx_EnterSTOP1Mode	NA	Stop 1 mode
HAL_PWREx_EnterSTOP2Mode		Stop 2 mode
HAL_PWREx_EnterSHUTDOWNMode		Shutdown mode
HAL_PWREx_EnableLowPowerRunMode	Low-power run mode Entry/Exit	
HAL_PWREx_DisableLowPowerRunMode		
HAL_PWREx_EnableUltraLowPower	ULP = Low-power mode with VREFINT OFF	NA
HAL_PWREx_DisableUltraLowPower		
HAL_PWREx_EnableFastWakeUp	Wakeup config. in ULP	
HAL_PWREx_DisableFastWakeUp		

6.3 HAL RCC

There are few differences in HAL_RCC between STM32L0 Series and STM32L4 Series / STM32L4+ Series. The PLL has specific configurations (see *Table 39*) and there is a wider range of peripherals supported by RCC_PeriphCLKInitTypeDef in STM32L4 Series / STM32L4+ Series.

Table 39. PLL configuration

STM32L0 Series	STM32L4 Series / STM32L4+ Series	
Main PLL	**Main PLL**	**SAIx PLL**
uint32_t PLLState	uint32_t PLLState	uint32_t PLLSAIxN
uint32_t PLLSource	uint32_t PLLSource	uint32_t PLLSAIxP
uint32_t PLLMUL	uint32_t PLLM	uint32_t PLLSAIxQ
uint32_t PLLDIV	uint32_t PLLN	uint32_t PLLSAIxR
-	uint32_t PLLP	uint32_t PLLSAIxClockOut
-	uint32_t PLLQ	uint32_t PLLSAIxM (only for STM32L4Rxxx/4Sxxx)
-	uint32_t PLLR	-

Generic API

All the following functions have the same prototype in both series.

- HAL_RCC_DeInit
- HAL_RCC_OscConfig
- HAL_RCC_ClockConfig
- HAL_RCC_MCOConfig
- HAL_RCC_EnableCSS
- HAL_RCC_GetSysClockFreq
- HAL_RCC_GetHCLKFreq
- HAL_RCC_GetPCLK1Freq
- HAL_RCC_GetPCLK2Freq
- HAL_RCC_GetOscConfig
- HAL_RCC_GetClockConfig
- HAL_RCC_NMI_IRQHandler
- HAL_RCC_CSSCallback

Extended API

The main differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series are on specific blocks: the CRS for STM32L0 Series devices and the SAI PLLs in STM32L4 Series / STM32L4+ Series devices. *Table 40* compares the HAL_RCCEx API for both series.

Table 40. RCC extended peripheral control functions

RCC Extension API	STM32L0 Series	STM32L4 Series / STM32L4+ Series
HAL_RCC_DeInit	Reset Default RCC settings	
HAL_RCCEx_PeriphCLKConfig	Manage peripherals clocks	
HAL_RCCEx_GetPeriphCLKConfig		
HAL_RCCEx_GetPeriphCLKFreq		
HAL_RCCEx_EnableLSECSS	Manage LSE clock Security system	
HAL_RCCEx_DisableLSECSS		
HAL_RCCEx_EnableLSECSS_IT		
HAL_RCCEx_LSECSS_IRQHandler		
HAL_RCCEx_LSECSS_Callback		
HAL_RCCEx_CRSConfig	NA	Manage Clock Recovery System
HAL_RCCEx_CRSSoftwareSynchronizationGenerate		
HAL_RCCEx_CRSGetSynchronizationInfo		
HAL_RCCEx_CRSWaitSynchronization		
HAL_RCCEx_EnableHSI48_VREFINT	VREFINT for HSI48	NA
HAL_RCCEx_DisableHSI48_VREFINT		

Table 40. RCC extended peripheral control functions (continued)

RCC Extension API	STM32L0 Series	STM32L4 Series / STM32L4+ Series
HAL_RCCEx_EnableLSCO	NA	Low Speed clock source to output on LSCO pin (PA2)
HAL_RCCEx_DisableLSCO		
HAL_RCCEx_EnableMSIPLLMode		PLL mode for MSI (calibration LSE)
HAL_RCCEx_DisableMSIPLLMode		
HAL_RCCEx_EnablePLLSAI1		Enable/Disable PLLs for SAI1 and SAI2 interfaces
HAL_RCCEx_DisablePLLSAI1		
HAL_RCCEx_EnablePLLSAI2		
HAL_RCCEx_DisablePLLSAI2		
HAL_RCCEx_WakeUpStopCLKConfig		Stop mode wakeup or CSS backup clock (HSI/MSI)
HAL_RCCEx_StandbyMSIRangeConfig		Configure the MSI range after Standby mode (default 4 MHz)

7 Revision history

Table 41. Document revision history

Date	Revision	Changes
08-Jul-2016	1	Initial release.
14-Feb-2017	2	Updated the whole document with reference to: – STM32L49xxx/L4Axxx devices – STM32L47xxx/L48xxx devices – STM32L45xxx/L46xxx devices – STM32L43xxx/L44xxx devices Updated STM32L4 Series and STM32L0 Series reference manual list in cover. Removed STM32L4 Series product category overview table. Added *Table 4: STM32L4 Series / STM32L4+ Series feature levels*. Updated *Table 5: STM32L4 Series / STM32L4+ Series memory availability*. Updated *Section 2.1: Packages availability*: – Added *Table 6: Packages available on STM32L4 Series and STM32L4+ Series*. – Updated *Table 7: Packages available on STM32L0 Series*. – Added *Section : SMPS packages*. Updated *Table 17: Boot modes for STM32L41xxx/L42xxx, STM32L43xxx/L44xxx, STM32L45xxx/L46xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx devices*. Added I2C4, CAN2 in *Table 18: Boot serial interfaces*. Updated *Table 20: STM32L4 Series / STM32L4+ Series low-power modes summary*. Added DCMI in *Table 21: Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series*.
31-Aug-2017	3	Updated the whole document to add STM32L4+ Series information.

Table 41. Document revision history

Date	Revision	Changes
22-Nov-2017	4	Added: – *Table 13: Pinout differences on BGA64 package* – *Table 14: Pinout differences on UFBGA100 package*
20-Sep-2018	5	Added: – Information related to STM32L41xxx/42xxx to the whole document – *Table 8: Pinout differences on LQFP32 package* Updated: – Cover page – *STM32L0 Cat. 2, 3, 5 and STM32L47xxx/L48xxx devices on page 19* – *Note: on page 39* – *Table 5: STM32L4 Series / STM32L4+ Series memory availability* – *Table 6: Packages available on STM32L4 Series and STM32L4+ Series* – *Table 17: Boot modes for STM32L41xxx/L42xxx, STM32L43xxx/L44xxx, STM32L45xxx/L46xxx, STM32L49xxx/L4Axxx and STM32L4Rxxx/4Sxxx devices* – *Table 18: Boot serial interfaces* – Footnote *3.* on *Table 20: STM32L4 Series / STM32L4+ Series low-power modes summary* – *Table 21: Peripherals comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series* – *Table 24: RCC comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series* – *Table 26: PWR comparison between STM32L0 Series and STM32L4 Series / STM32L4+ Series* – *Table 27: FLASH differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series* – *Table 30: USB peripheral comparison* – *Table 31: ADC differences between STM32L0 Series and STM32L4 Series / STM32L4+ Series*