AN4828
Application note

STEVAL-IFP017V3 evaluation board based on the L6362A transceiver for IO-Link and SIO mode communication

Introduction

The STEVAL-IFP017V3 is an evaluation board for the features of the L6362A, including fast demagnetization, reverse polarity, overload, overtemperature, ground and supply open wire protections.

The highly robust design of the L6362A allows the STEVAL-IFP017V3 to meet IEC 61000-4-4 (burst), IEC 61000-4-2 (ESD) and EN60947-5-2/IEC 61000-4-5 (surge) without additional external components.

The STEVAL-IFP017V3 offers dedicated input and output screw connectors to facilitate easy and flexible connections for user requirements. The on-board red and green LEDs signal the IC status.

On the STEVAL-IFP017V3, the exposed pad of the L6362A is connected to an electrically floating copper area which acts as a heatsink.

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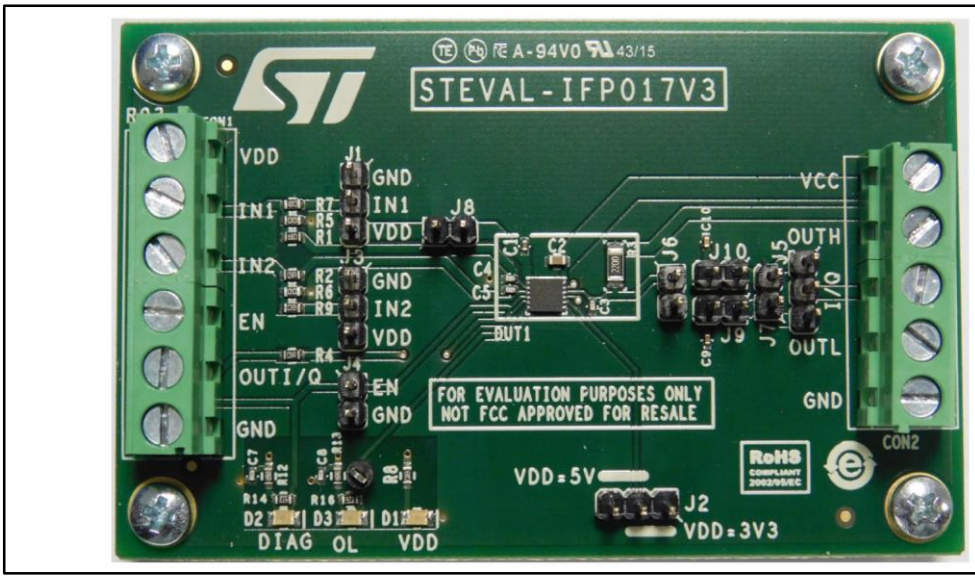
1 STEVAL-IFP017V3 features

- Operating voltage from 7 to 36 V
- Operating current up to 240 mA
- Configurable as push-pull, high side or low side
- Overcurrent protection with cutoff function
- Overtemperature protection
- Suitable to drive R, L and C loads
- Delayed cutoff for quick charging of capacitive loads
- Able to handle up to 500 mJ inductive loads
- Full reverse polarity protection on V_{CC}, GND, OUTH, OUTL and I/Q pins
- Green device status LED (ON or OFF)
- Red diagnostic LEDs for:
  - cutoff and overtemperature events
  - overload
- Supports COM1, COM2 and COM3
- Meets IEC 61000-4-4 (burst), IEC 61000-4-2 (ESD) and EN60947-5-2/IEC 61000-4-5 (surge) requirements

Figure 1: STEVAL-IFP017V3 evaluation board



2 Board description

Table 1: STEVAL-IFP017V3 Connectors and jumpers description

Name	Type	Description / Function		Note
CON1	Low voltage connector	PIN1	V_{DD}	Low voltage supply (3.3 V / 5 V)
		PIN2	IN1	Drives output in HS or LS configurations. Sets the driving polarity in PP configuration
		PIN3	IN2	Drives output in push-pull configuration. Sets the driving polarity in HS or LS configurations
		PIN4	EN/DIAG	Disable output if forced to GND. Forced down by L6362A in case of: UVLO on V_{CC}, overtemperature or cutoff events
		PIN5	OUT I/Q	Report the status on I/Q pin, swinging between V_{DD} and GND
		PIN6	GND	Board ground.
CON2	High voltage connector	PIN1	V_{CC}	Supply voltage (≤ 36 V)
		PIN2	OUTH	In HS configuration, connect the LOAD between this pin and GND. In case of PP (OUTH=OUTL=OUT) the LOAD can be connected between OUT and GND or between OUT and V_{CC}
		PIN3	I/Q	High voltage receiver input.
		PIN4	OUTL	In LS configuration, connect the LOAD between this pin and V_{CC}. In case of PP (OUTH=OUTL=OUT) the LOAD can be connected between OUT and GND or between OUT and V_{CC}
		PIN5	GND	Board ground
J1	3 ways switch	OPEN	IN1 driven by PIN2 of CON1	IN1 can be driven with signals swinging between 0 V and V_{DD} (see J2)
		CLOSE 1-2	IN1 = GND	OUTH and/or OUTL driven by IN2 or EN in non-inverted mode
		CLOSE 2-3	IN1= V_{DD}	OUTH and/or OUTL driven by IN2 or EN in inverted mode
J3	3 ways switch	OPEN	IN2 driven by PIN3 of CON1	IN2 can be driven with signals swinging between 0V and V_{DD} (see J2)
		CLOSE 1-2	IN2 = GND	OUTH and/or OUTL driven by IN1 or EN in non-inverted mode
		CLOSE 2-3	IN2= V_{DD}	OUTH and/or OUTL driven by IN1 or EN in inverted mode
J2	3 ways switch	OPEN	Not Allowed	-
		CLOSE 1-2	SEL = GND	V_{DD} supplies 3.3 V
		CLOSE 2-3	SEL = V_{DD}	V_{DD} supplies 5 V

Name	Type	Description / Function		Note
J4	2 ways jumper	A-B OPEN	EN/DIAG driven by PIN4 of CON1	OUTH and OUTL driven by IN1, IN2 or EN/DIAG. J4 can be used as EN/DIAG test point: if J4 is OPEN and PIN4 of CON1 is floating, then EN/DIAG is forced low by L6362A in case of fault event (overtemperature or cutoff. In case of UVLO of V_{CC} EN/DIAG is forced low only if an external low voltage supply the system)
		A-B CLOSED	EN/DIAG = GND	OUTH and OUTL disabled
J5	3 ways switch	CLOSE 1-2	I/Q = OUTH	I/Q and OUTH driven by PIN2 or PIN3 of CON2
		CLOSE 2-3	I/Q = OUTL	I/Q and OUTL driven by PIN3 or PIN4 of CON2
J6	2 ways jumper	A-B OPEN	I/Q driven by PIN3 of CON2	I/Q can be driven with signals swinging between 0 V and V_{CC}
		A-B CLOSED	I/Q = GND	
J7	2 ways jumper	A-B OPEN	OUTH connected to PIN2 and OUTL connected to PIN4 of CON2	High side and/or low side configuration
		A-B CLOSED	OUTH = OUTL	Push-pull configuration
J8	2 ways jumper	A-B OPEN	V_{DD} disconnected from PIN1 of CON1	If J8 is OPEN the integrated linear voltage regulator doesn't supply the system (it just supply the green led D1) that can be supplied by an external regulator from the PIN1 of CON1
		A-B CLOSED	V_{DD} connected to PIN1 of CON1	If J8 is CLOSED the integrated linear voltage regulator supply the system (3.3 V / 5 V)
J9	2 ways jumper	A-B OPEN	Disconnect C9 between OUTL and GND	Connecting C9 to OUTL makes the board more robust despite EMC tests: ESD, standard 61000-4-2 and Surge, standard EN60947-5-2/IEC 61000-4-5
		A-B CLOSED	Connect C9 between OUTL and GND	
J10	2 ways jumper	A-B OPEN	Disconnect C10 between OUTH and GND	Connecting C10 to OUTH makes the board more robust despite EMC tests: ESD, standard 61000-4-2 and Surge, standard EN60947-5-2/IEC 61000-4-5
		A-B CLOSED	Connect C10 between OUTH and GND	
OL	Test Point	OL (overload) Status Pin		OL pin is forced low by L6362A if an overload event is triggered

Figure 2: STEVAL-IFP017V3 circuit schematic

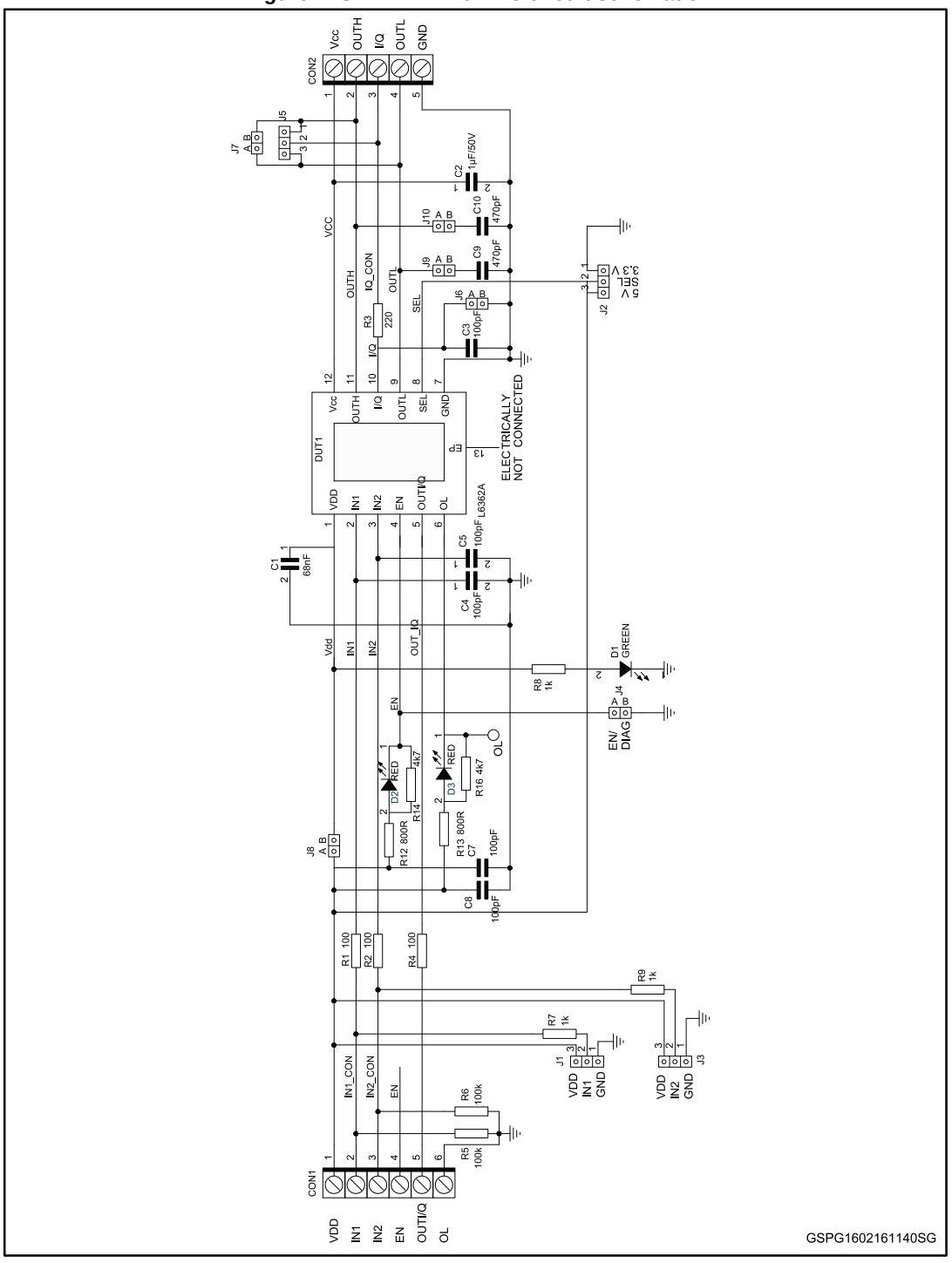


Table 2: Bill of material

Item	Qty	Reference	Value	Description	Package	Part number	Manufacturer
1	1	CON1	6 ways screw connector	LOW Voltage Signals (IN_X, V_{DD} and $OUT_{I/Q}$)	TH	691216510003	WURTH
2	1	CON2	5 ways screw connector	HIGH Voltage Signals (V_{CC}, OUT_X, I/Q)	TH	691216510003/2	WURTH
3	1	C1	68 nF	V_{DD} capacitor	0402	885012205036	WURTH
4	1	C2	1 µF	V_{CC} capacitor	0603	UMK107AB7105KA-T	TAIYO YUDEN
5	5	C3, C4, C5, C7, C8	100 pF	Noise Filter Capacitors	0402	885012205055	WURTH
10	2	C9, C10	470 pF	Capacitors for high voltage EMC	0603	885012205059	WURTH
12	3	R1, R2, R4	100 Ω	Protection resistors of low voltage pins	0603	CRG0603F100R	TECONNECTIVITY
15	1	R3	220 Ω	Protection resistor for I/Q pin	1206	ERJB2AF221V	PANASONIC
16	2	R5, R6	100 kΩ	IN_X pull down resistors	0603	CR0603-FX-1003ELF	BOURNS
18	3	R7, R8, R9	1 kΩ	IN_X pull up resistors	0603	CRCW06031K00FKEA	VISHAY
21	2	R12, R13	806 Ω	Polarization resistors for D2 and D3	0603	CRCW0603806RFKEA	VISHAY
23	2	R14, R16	4.7 kΩ	Pull-up resistors for EN/DIAG and OL pins	0603	CRCW06034K70FKEA	VISHAY
25	1	D1	Green Led	V_{DD} activation LED	0805	LG R971	OSRAM
26	2	D2, D3	Red Led	FAULT LED for EN/DIAG and OL pins	0805	LH R974	OSRAM
28	5	J1, J2, J3, J5	3 pins (2 ways) switch	IN_X, SEL and OUT_X configuration	TH		
33	6	J4, J6, J7, J8, J9, J10	2 pins jumper	Configuration and set-up	TH		
39	1	TP(OL)	Ring Test Point	Test point	TH	20-2137	Vero Technologies
40	1	DUT1	L6362A	SIO and I/O Link controller	L6362A		ST

2.1 Supply voltage section

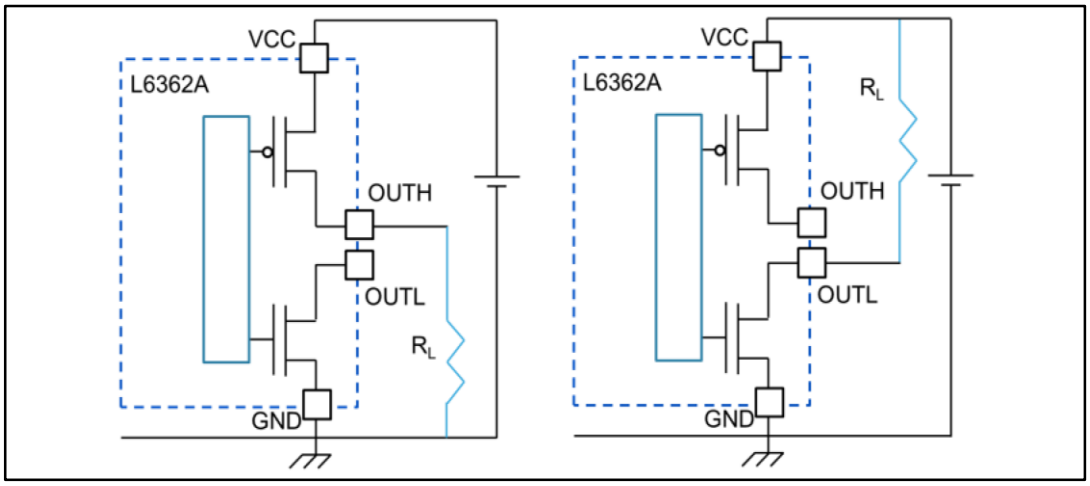
For correct use of this evaluation board, the V_{CC} supply voltage must remain between 7 and 36 V.

2.2 Configuration and load connection

The L6362A can be configured as high side driver, low side driver and push-pull. Whatever the configuration selected, the outputs can be driven in COM1, COM2 or COM3 modes.

In high side configuration, the load is connected between OUTH and GND (PIN2 and PIN5 of CON2). In low side configuration the load is connected between OUTL and V_{CC} (PIN4 and PIN1 of CON2).

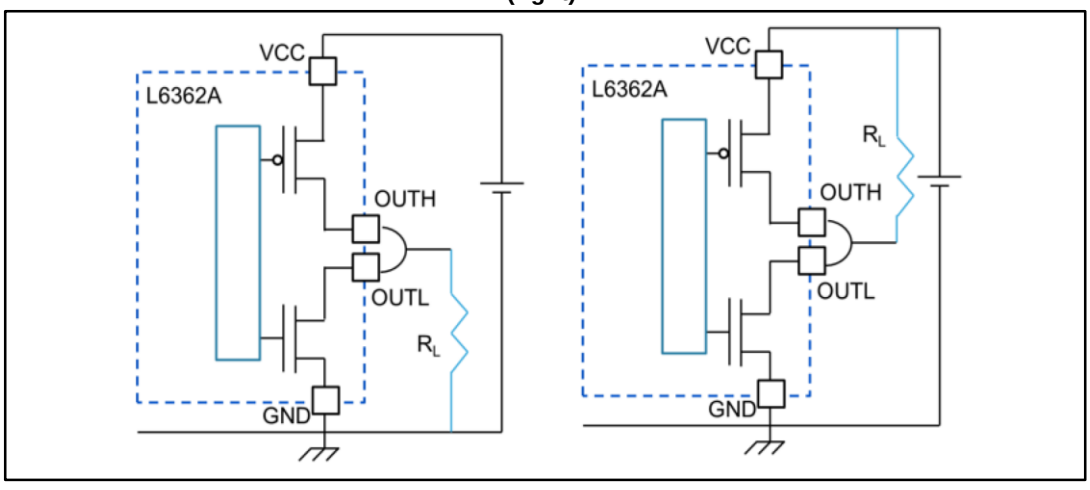
Figure 3: L6362A high side configuration (left) and low side configuration (right)



For HS or LS configuration, the output stage must be driven by IN1, while IN2 must be connected to V_{DD} or GND, depending on the desired driving (inverted or non-inverted); refer to *Table 1: "STEVAL-IFP017V3 Connectors and jumpers description"* and to the datasheet for details.

In push-pull configuration, OUTH and OUTL are shorted (OUTH=OUTL=OUT) and the load can be connected between OUT and V_{CC} (low side load configuration) or between OUT and GND (high side load configuration). The push-pull configuration with I/Q pin connected to the OUT is the typical I/O link configuration.

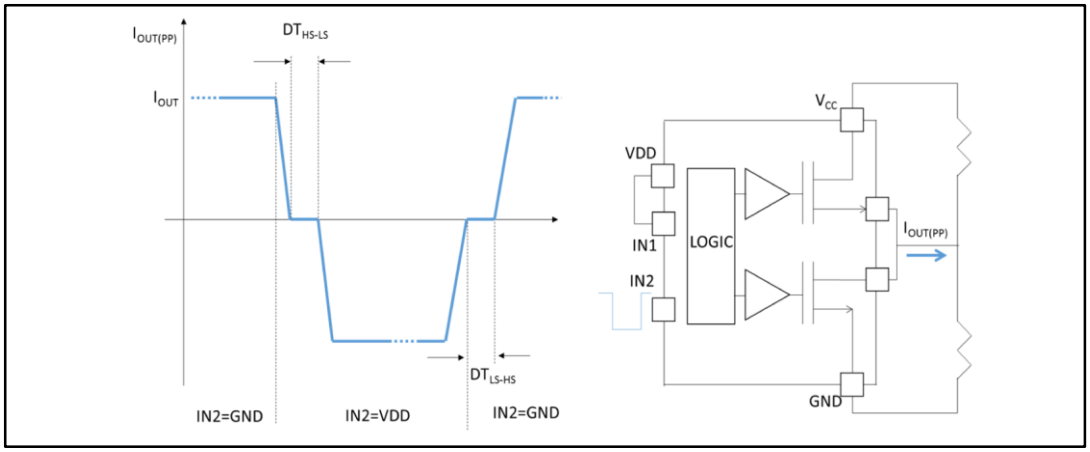
Figure 4: L6362A push-pull configuration with load on low side (left) and load on high side (right)



For the push-pull configuration, the outputs must be driven by the IN2 pin. In fact, by driving from IN2, the dead time delay integrated by the L6362A will avoid any undesired shorts.

The figure below shows the effect of the dead time on the output current (same load on high side and low side switches):

Figure 5: Effect of Dead Time (DT) on output current



For push-pull and capacitive loads, the output stage can be driven from the EN/DIAG pin: this driving method avoids the undesired discharge of the load through the integrated high side switch (when load is connected between OUT and V_{CC}) or through the integrated low side switch (when load is connected between OUT and GND).

2.3 Operating current, overload and cutoff

The L6362A mounted on the STEVAL-IFP017V3 is designed to supply any kind of load whereby nominal currents do not exceed the overcurrent limitation threshold.

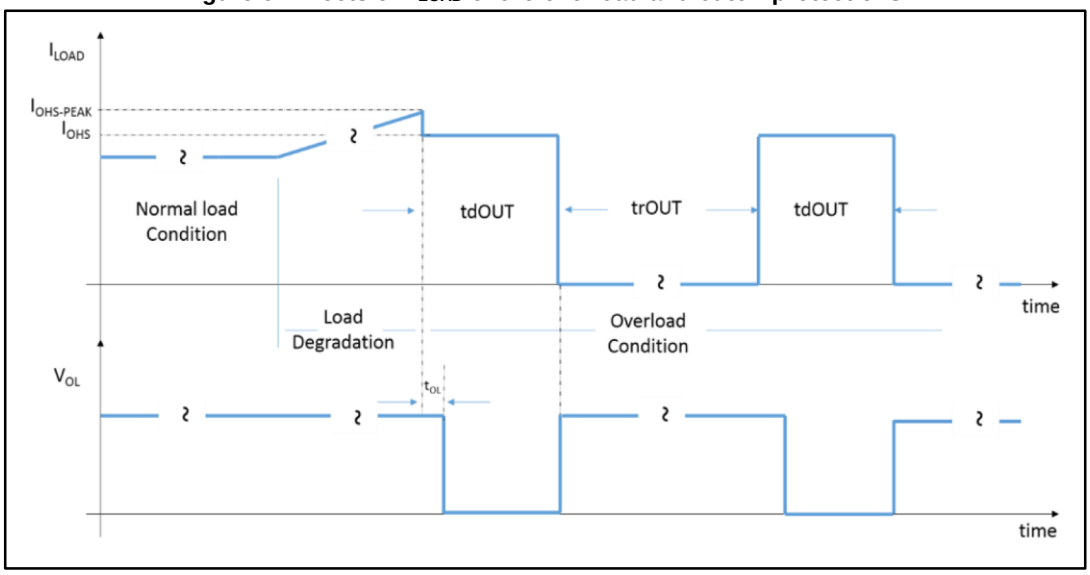
In fact, in case of overload (due to load degradation or accidental short circuit), the integrated overload protection will guarantee the IC is not damaged. The integrated current sense circuits monitor the current flowing between pins V_{CC} and OUTH (through the high side switch) and between the OUTL and GND pin (through the low side switch).

When the sensed current triggers the internal safety threshold ($I_{OLS-PEAK}$ for the low side switch; $I_{OHS-PEAK}$ for the high side switch) the IC automatically regulates the internal resistance of the switches to limit the current limitation value (I_{OLS} for low side switch, I_{OHS} for high side switch).

The triggering of the overload threshold is reported on OL pin which is forced low: on the STEVAL-IFP017V3, this event leads to the D3 red LED to be turned ON.

The figure below shows the expected waveform in case of overload on the high side switch (I_{LOAD} is considered positive when exiting from OUTH pin towards the load).

Figure 6: Effects on I_{LOAD} of the overload and cutoff protections



If the overload condition persists, the cutoff protection is activated as well. In fact, once the limitation threshold is triggered, the related switch is maintained ON until t_{dOUT} has elapsed and then OFF until t_{rOUT} has elapsed.

the overtemperature protection is always a higher priority than the other protections.

The delay of the cutoff intervention (t_{dOUT}) is designed to accelerate the charging of capacitive loads. For an R/C load in the push-pull configuration:

- the output has to be driven from EN/DIAG pin (instead of IN1 or IN2), to avoid the undesired discharge of the load through the integrated switches;
- the activation pulses on EN/DIAG pins may be reset before t_{dOUT} is triggered (EN/DIAG remains high less than $t_{dOUT(MIN)}$) in order to avoid/postpone the intervention of the cutoff function. In case of overheating (see *Section 2.4: "Overheating and thermal protection"*), the device is protected.

If the cutoff function is activated, the EN/DIAG pin is forced low: on the STEVAL-IFP017V3, this event turns D2 red LED ON.

the integrated open drain on the EN/DIAG pin is a shared diagnostic output with UVLO on V_{CC}, cutoff and overtemperature.

2.4 Overheating and thermal protection

The L6362A is protected from overheating by the integrated thermal protection: once its junction temperature triggers the T_{JSD} threshold (150 °C, minimum) the outputs are forced OFF until the temperature decreases by T_{JHYST} (25 °C typ.).

If the overtemperature event is triggered, then the EN/DIAG pin is forced low: on the STEVAL-IFP017V3, this event turns D2 red LED ON.

the integrated open drain on the EN/DIAG pin is a shared diagnostic output with UVLO on V_{CC}, cutoff and overtemperature.

2.5 V_{DD} output regulated voltage

The L6362A provides a regulated output voltage on V_{DD} supporting up to 8 mA load ($I_{scr(MIN)}$). It is possible to select V_{DD} = 3.3 V or V_{DD} = 5 V according to the setup of the SEL pin through J2 (see *Table 1: "STEVAL-IFP017V3 Connectors and jumpers description"*).

On the STEVAL-IFP017V3, the V_{DD} pin supplies:

- Green LED D1, which turns on once the V_{CC} rises above V_{UVON} and remains higher than V_{UVOFF}
- Red LED D2, which turns on in case of cutoff or overtemperature events. The UVLO event on V_{CC} will be not visible because D2 is supplied by V_{DD} (which is not active when V_{CC} goes lower than V_{UVOFF}). In order to verify the UVLO fault event, R12 must be disconnected from V_{DD} by opening J8 and then connected to an external power supply via the PIN1 of CON1.
- Red LED D3, which turns on in an overload event.

2.6 I/Q and OUT I/Q

The I/Q pin is typically used in I/O Link: push-pull configuration (OUTH=OUTL=OUT) and I/Q connected through an RC to the OUT. The STEVAL-IFP017V3 provides an on-board RC network (R3 = 220 W and C3 = 100 pF) and the possibility to connect the I/Q to OUTH or to OUTL through J5 (see *Table 1: "STEVAL-IFP017V3 Connectors and jumpers description"*). The connection OUTH=OUTL is done by closing J7.

According to the L6362A characteristics, the OUT I/Q pin swings between GND and V_{DD}, reflecting the same status (low or high) of the I/Q pin (which swings between GND and V_{CC}).

2.7 Reverse polarity protection

The reverse polarity protection of the STEVAL-IFP017V3 is fully integrated in L6362A and it is related to the pins V_{CC}, OUTH, OUTL, I/Q and GND.

The digital pins (V_{DD}, IN1, IN2, OL, EN/DIAG) are not protected despite reverse polarity.

3 Board layout

The figures below show the top and bottom views of the STEVAL-IFP017V3.

Figure 7: STEVAL-IFP017V3: top and component placement layout view

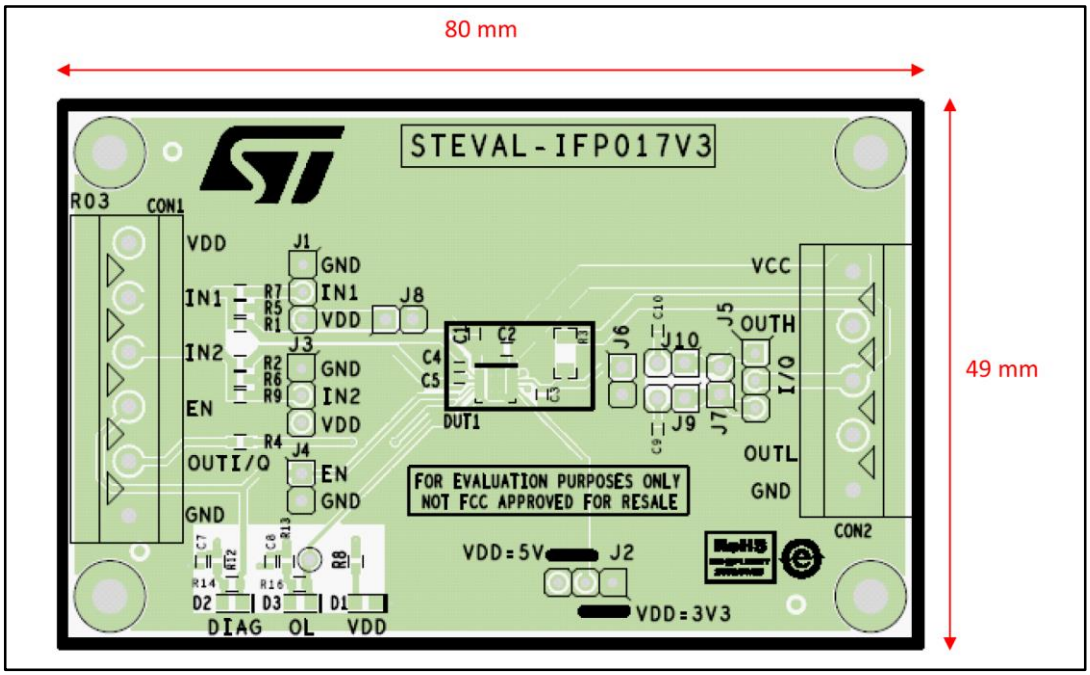
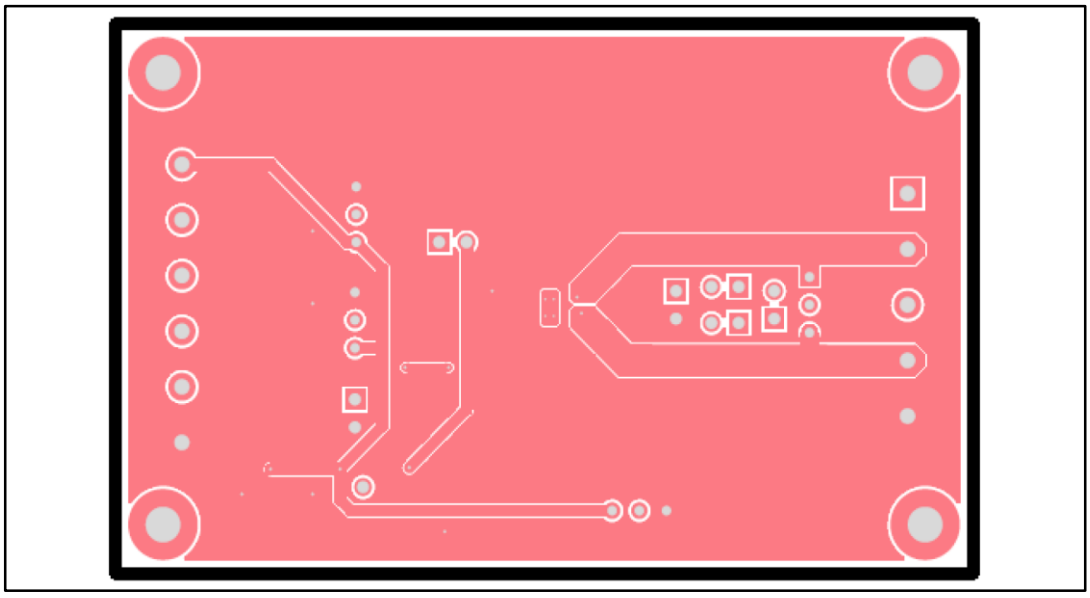


Figure 8: STEVAL-IFP017V3: bottom side layout view



4 Reference documents

- L6362A datasheet
- IEC 61000-4-4, IEC 61000-4-2 and EN60947-5-2/IEC 61000-4-5 documentation

5 Revision history

Table 3: Document revision history

Date	Revision	Changes
18-Apr-2016	1	Initial release.

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