STM32 MCUs spread-spectrum clock generation
principles, properties and implementation

Introduction

The STM32F2 Series, STM32F4 Series and STM32F7 Series embed a SSCG (spread-spectrum clock generation) in their main PLL (phase-locked loop) system. This SSCG offers some advantages regarding electromagnetic compatibility.

The main objectives of this application note are:

- to describe the SSCG principle in a simple way
- to present and explain its properties and features
- to compare the SSCG systems against non-SSCG systems.

This document covers a SSCG technique's overview, an explanation of the SSCG principle in a simple way as well as an overview of the SSCG advantages and disadvantages. This application note also presents a parameters summary of the SSCG inside STM32F2 Series, STM32F4 Series and STM32F7 Series and includes details on how to configure the SSCG parameters in those products.

Table 1. Applicable products

Type	Product series
Microcontrollers	STM32F2 Series, STMF4 Series, STM32F7 Series

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1 Spread-spectrum clock generation

The conventional clock generator provides a very stable clock frequency while the SSCG (spread-spectrum clock generation) provides more jitters compared to the conventional clock generator. Having a SSCG results in lower peak-energy on the central frequency; however, total energy does not change.

1.1 Electromagnetic interference (EMI) problems and the clock generation

Any semiconductor device creates an electromagnetic emission. Most of the times, this radiated emission has peak energy at the operating clock frequency and its associated harmonics of the digital circuitry.

The most modern digital ICs (like microcontrollers) are designed with the synchronous logic techniques where the flip-flop status update is cadenced by a central clock source. This implied current flowing through the chip nodes at the each active clock edge. This current results in an electromagnetic radiation at the operating clock frequency and its associated harmonics.

If the electromagnetic radiation level caused by the digital operating clock frequency is above the requirement level, it is possible to reduce the peak amplitude by using a spread-spectrum technique.

A spread-spectrum technique refers to the addition of an intentional modulation on the clock, so that the energy of the clock in a certain bandwidth is reduced. Then the peak amplitude of the electromagnetic energy level can be reduced.

1.2 Using spread-spectrum technique for EMI reduction

Figure 1 shows an example of the spread-spectrum frequency against amplitude and illustrates a comparison between a clock without spread-spectrum and a clock with spread-spectrum enabled.

The emission peak reduction depends mainly on:
*   the modulation depth
*   the resolution bandwidth used for the EMI measurement (the emission does not change, since the way that it is measured changes, the result also changes)
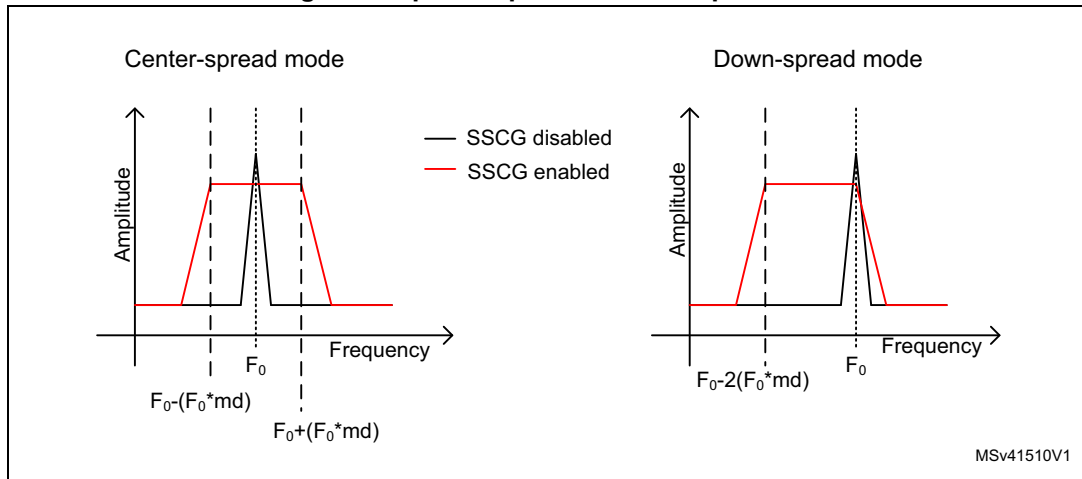
Formula:

EMI $_{Reduction}$ (dB) = 10 log (2md x F_0 / RBW)

where:
*   EMI: electromagnetic interference
*   md: peak-to-peak modulation depth divided by 2
* F_0: nominal output frequency (Hz)
*   RBW: measurement resolution bandwidth (Hz)

Figure 1. Spread-spectrum clock spectrum

1. The **black** curve shows a clock without spread spectrum while the **red** curve shows the spread spectrum enabled.

If one of the harmonics of the main clock has EMI emissions, the effect of the spread spectrum changes.

When the spread-spectrum modulation depth is set as +/-1% on the system frequency of 100M Hz, the modulation depth on this frequency is +/-1 MHz. The second harmonics of the modulation depth will be +/-2 MHz, then the third will be +/-3 MHz and so on.

The result is that the effect of the spread-spectrum will be more efficient on the harmonic frequencies.
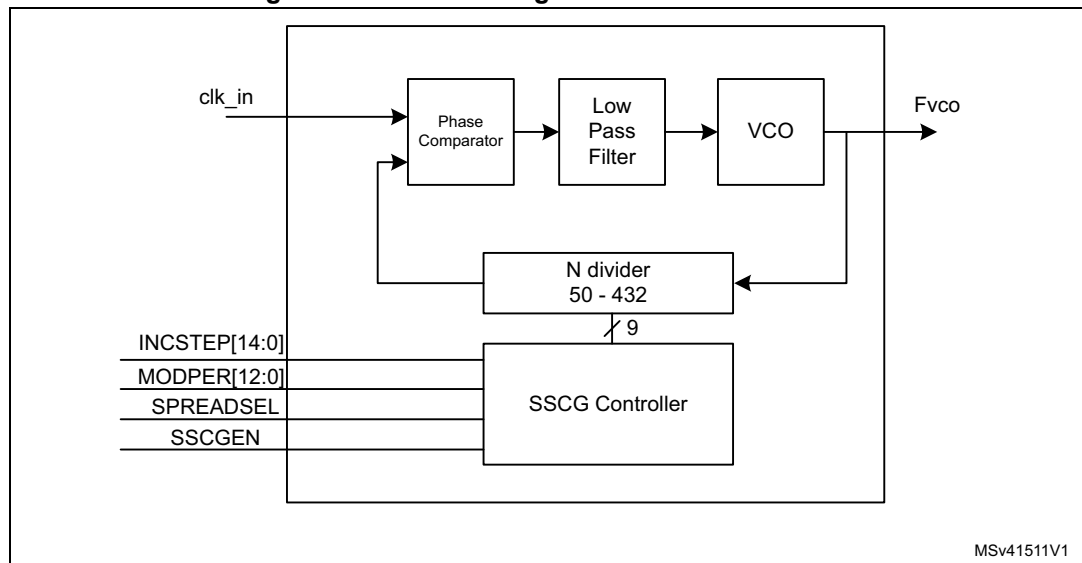
2 SSCG operation overview

2.1 SSCG mechanism

In the STM32F4 Series, the PLL (phase-locked loop) is built-in with the spread-spectrum clock generation feature.

Figure 2 shows the PLL block diagram with SSCG functionality.

Figure 2. PLL block diagram with SSCG function

The SSCG controller controls the divider ratio of the "N divider" block in order for the PLL to generate the clock with a frequency modulated with a triangular profile.

The SSCG controller requires the following parameters to control the "N divider":

- Modulation period (MODPER)
  - define the modulation period / frequency
- Increment step (INCSTEP)
  - define the modulation depth
- Spread-mode select (SPREADSEL)
  - Select center-spread or down-spread mode
- Spread-spectrum clock generation enable (SSCGEN)
  - Enable control of the SSCG

2.2 Implementation of the SSCG controller

The SSCG controller outputs the "N divider" ratio with its internal triangular wave generator and with the oversampled quantizer. The triangular wave generator is the block that generates the linear modulation profile depending on the MODEPER and INCSTEP. After the corresponding modulation profile is created it is passed through the quantizer which represents the same profile in a reduced bit count.

The internal profile generator precision is 16 bits. The positive full scale amplitude is given (2^{15}-1). This full scale corresponds to 20% of the nominal divider value.

Figure 3. N divider modulation

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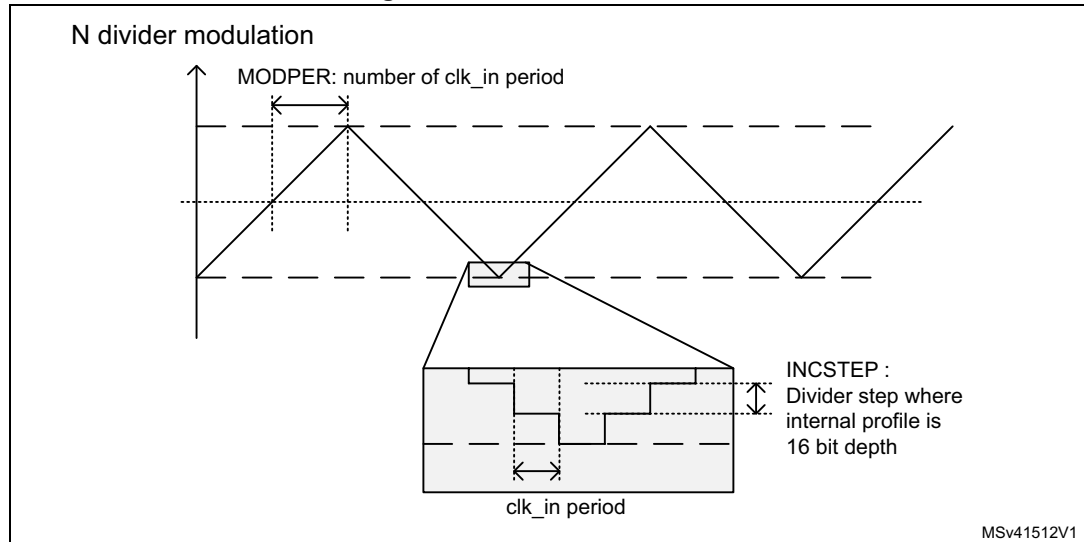
1. MODPER is the parameter to define the 1/4 of the triangular wave period. As this block works on the PLL reference clock (clk_in), the 1/4 of the wave period is MODPER x clik_in(period).

2. INCSTEP is the parameter where each clk_in period, internal profile generator changes its value with up-direction or down-direction.

As the internal profile is 16 bit, an oversampled quantizer reduces the bit count of the modulation profile, then the nominal count is calculated with the nominal divider value to create the 9 bit divider control signal.

The SPREADSEL defines the final stage calculation, to select the center-spread or the down-spread mode.

2.3 SSCG parameter calculation

The first thing to do is to calculate the modulation period parameter, which is calculated from the target frequency of the triangular modulation.

MODPER= round [f_{PLL_IN} / (4 x f_{MOD})]

where:

* f_{PLL_IN} is the PLL input clock frequency in Hz (1~2MHz)
* f_{MOD} is the target modulation frequency in Hz (f_{MOD} =< 10kHz)

The next step, the increment step is calculated form the following formula:

INCSTEP = round [(2^{15} - 1) x md x PLLN) / (100 x 5 x MODPER)

where:

*   md is the modulation depth, which is +/- %. If md =2, it is +/-2% (4% peak to peak)

(0.25% <= md <= 2%)

*   PLLN is the ratio chosen for the N divider.

The user must ensure that the product of INCSTEP and MODPER are not more than (2^{15} - 1). INCSTEP x MODPER < 2^{15}
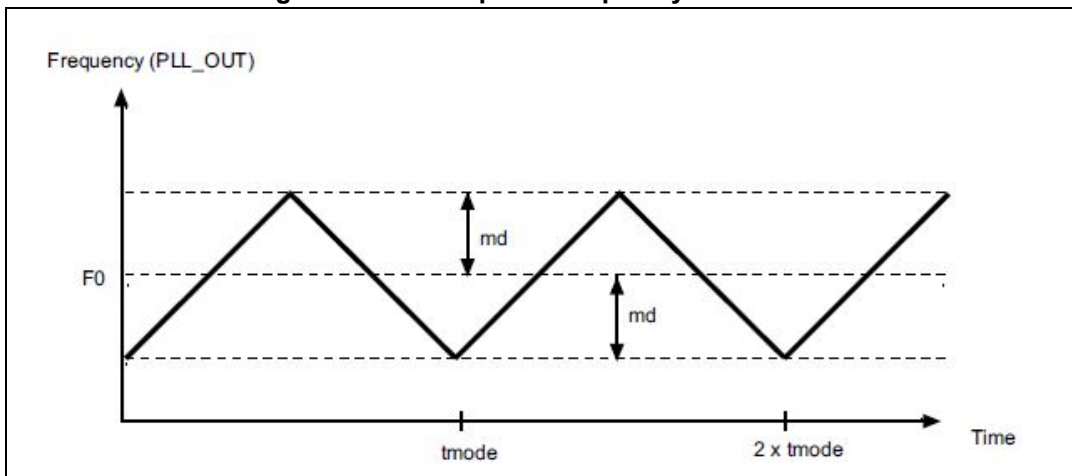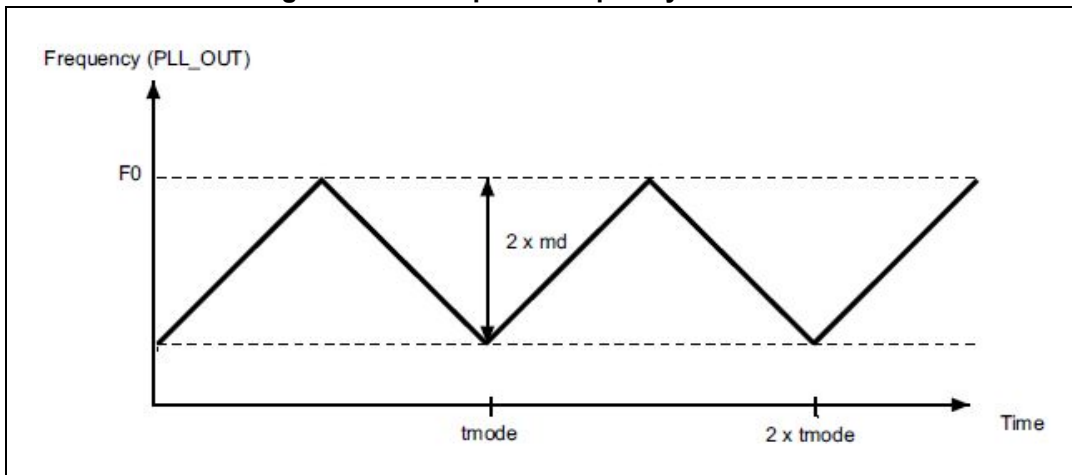
Figure 4. Center-spread frequency modulation

Figure 5. Down-spread frequency modulation

2.3.1 Example of configuration

See below an example of configuration, where:

F_{VCO} = 240MHz

f_{PLL_in} = 1MHz

f_{MOD} = 1kHz

md = 2%

From above parameters, PLLN = F_{VCO} / f_{PLL_in} = 240 x 10^6 / 10^6 = 240

MODEPER = round [f_{PLL_in} / (4 x f_{MOD})] = round [10^6 / (4 x 10^3)] = 250

INCSTEP = round [((2^{15} - 1) x md x PLLN) / (100 x 5 x MODEPER)]

= round [((2^{15} - 1) x 2 x 240) / (100 x 5 x 250)] = round (125.8) = 126

A quantization error may be generated because the linear modulation profile is obtained by taking the quantized value (rounded to the nearest interger) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized.

The percentage of quantized modulation depth is given by the following formula:

md quantized% = (MODEPER x INCSTEP x 100 x 5) / ((2^{15} - 1) x PLLN)

= (250 x 126 x 100 x 5) / ((2^{15} - 1) x 240) = 2.003 %.

2.4   SSCG spectrum measurement

The PLL is configured as follows:

- Clock In:1 MHz
- VCO frequency: 240 MHz (PLLN=240)
- PLL main output frequency: 120 MHz (PLLP=2)
- The output frequency was measured at MCO pad (120 MHz)

Figure 6 shows a spectrum without SSCG enabled as a reference.

Figure 7 shows a spectrum with center-spread mode, modulation frequency = 10 kHz, and modulation depth = +/- 2%.

Figure 8 shows a spectrum with lower-spread mode, modulation frequency = 10 kHz, with 2% modulation depth (total -4%).

The reduction on fundamental frequency is 18 ~ 22 dB.

Under the same conditions, the resolution bandwidth (RBW) was modified from 10 kHz to 100 kHz in *Figure 9*, *Figure 10* and *Figure 11*.

The reduction on fundamental frequency is 15 ~ 19 dB.

Note: *All the measurements were done with video band width at 10 kHz.*

As described in *Section 1.2*, the effect of the SSCG seen by measurement depends on the bandwidth setting on the spectrum analyzer.

The IEC61967 standard specifies both the narrow-band measurement and the broad-band measurement method. For the narrow-band measurement, it defines RBW = 9 kHz at the frequency range of 100 - 1000 MHz, but for the broad-band measurement it defines RBW = 100 kHz at a frequency range of 100 - 1000 MHz and RBW= 1 MHz at a frequency range of 1000 -2000 MHz.

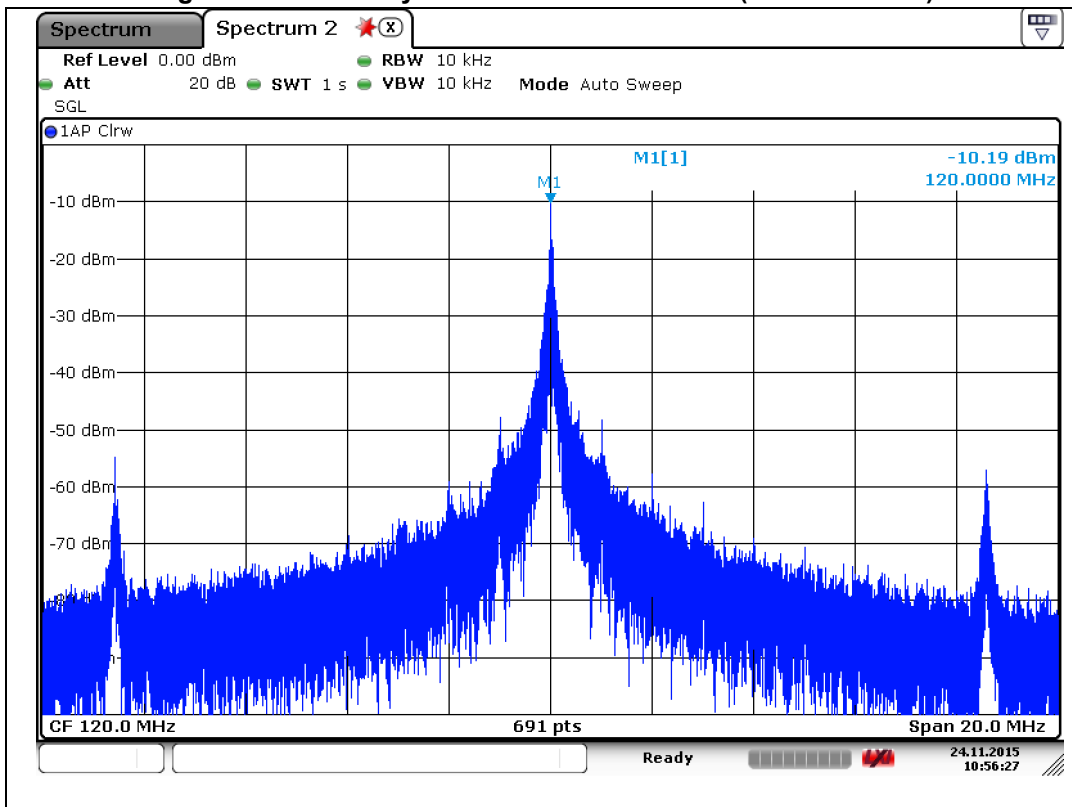**Figure 6. 120 MHz system clock without SSCG(RBW = 10 kHz)**

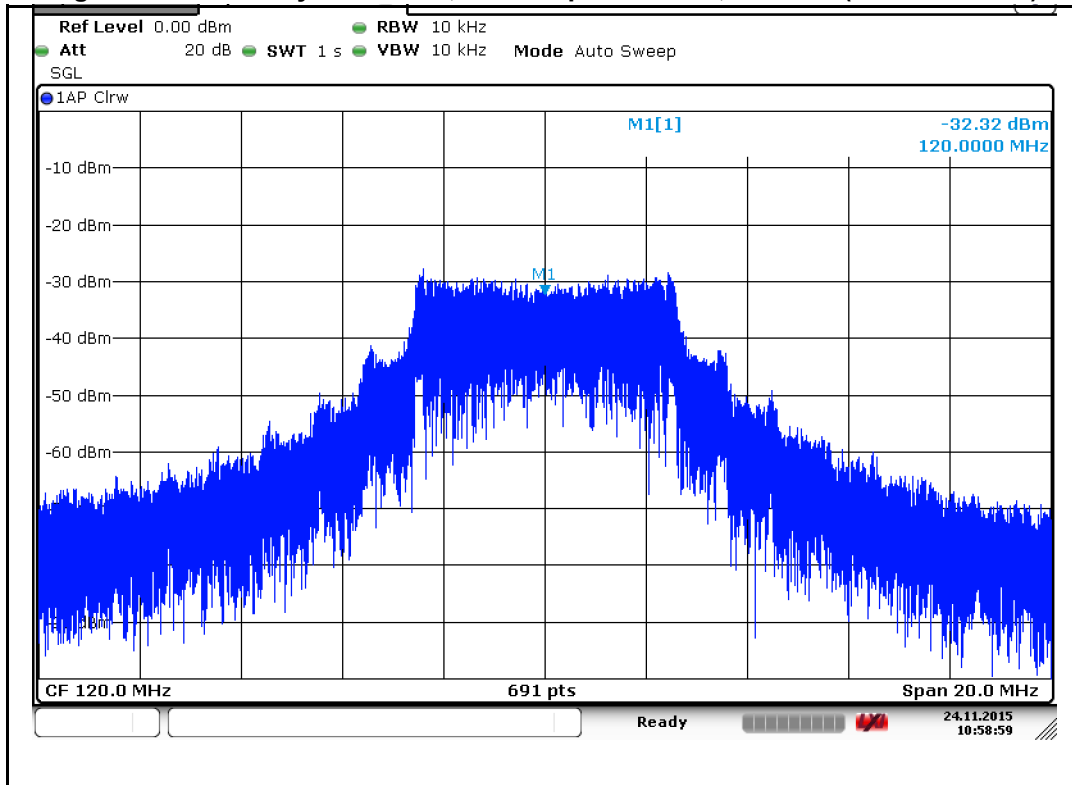**Figure 7. 120 MHz system clock, center-spread mode, md = 2%(RBW = 10 kHz)**

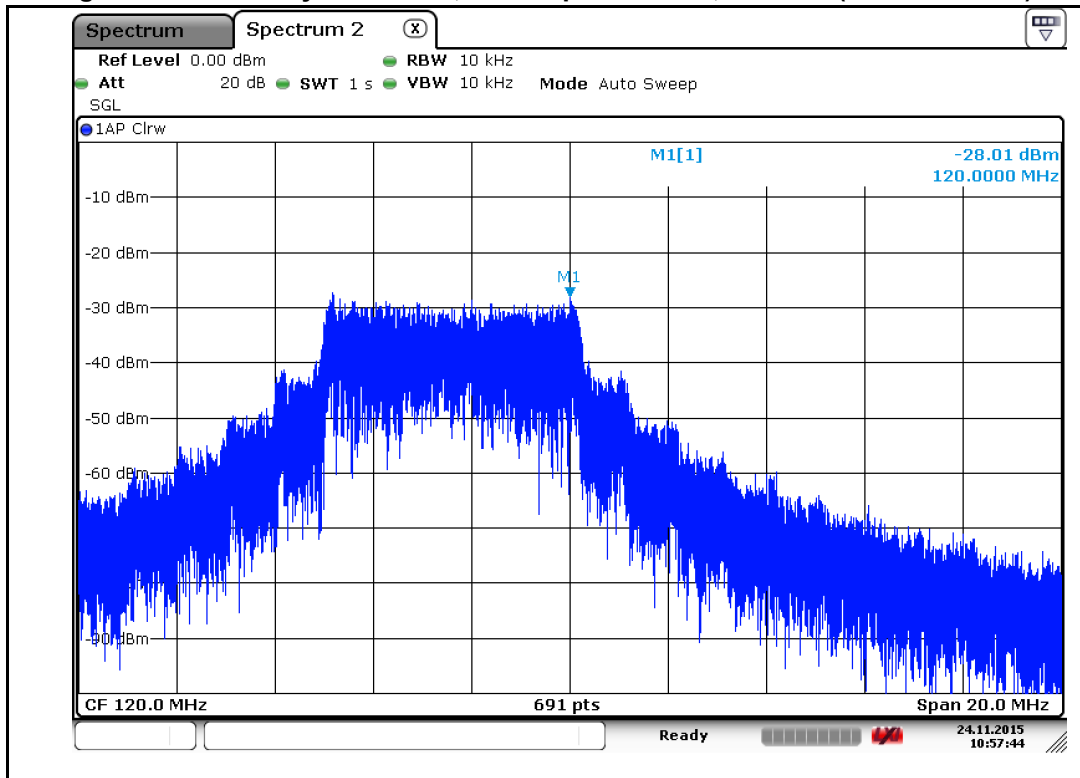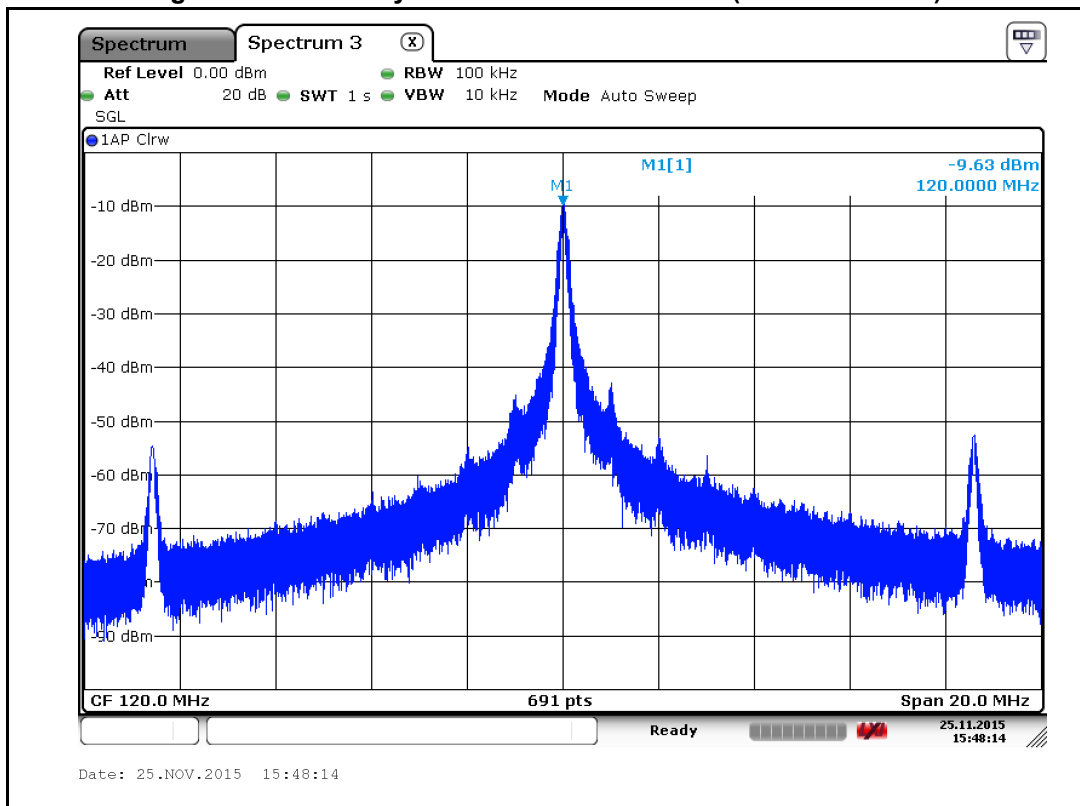**Figure 8. 120 MHz system clock, lower-spread mode, md = 2%(RBW = 10 kHz)**

Figure 9. 120 MHz system clock without SSCG(RBW = 100 kHz)

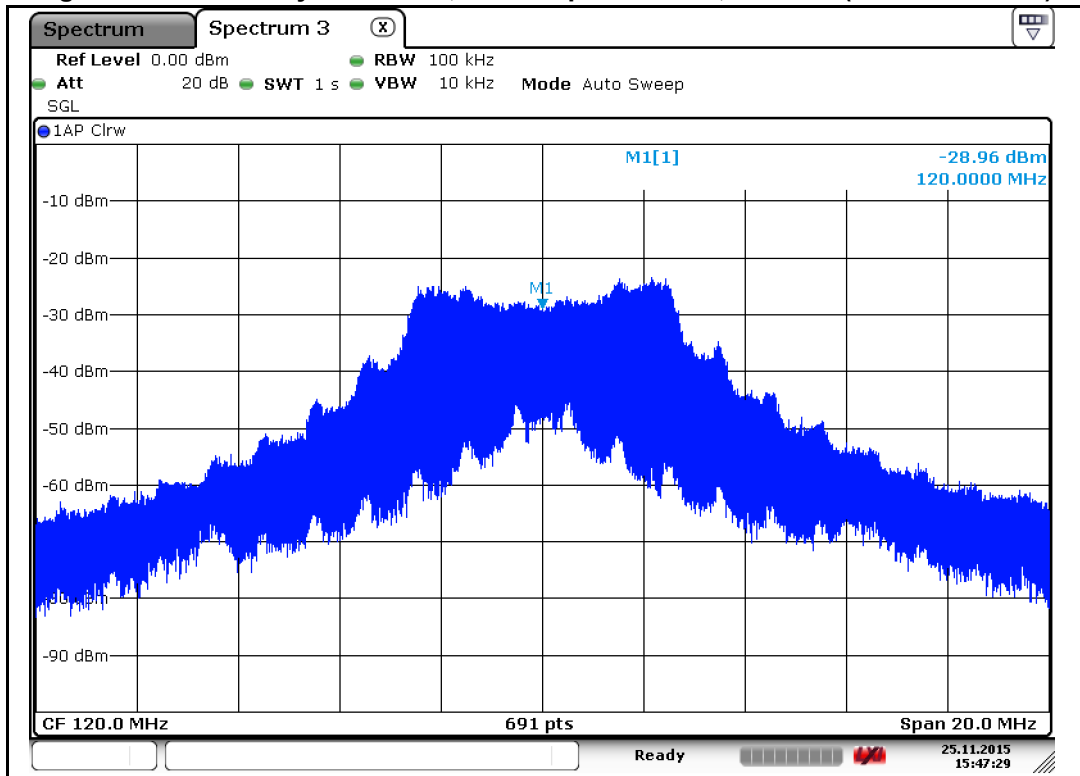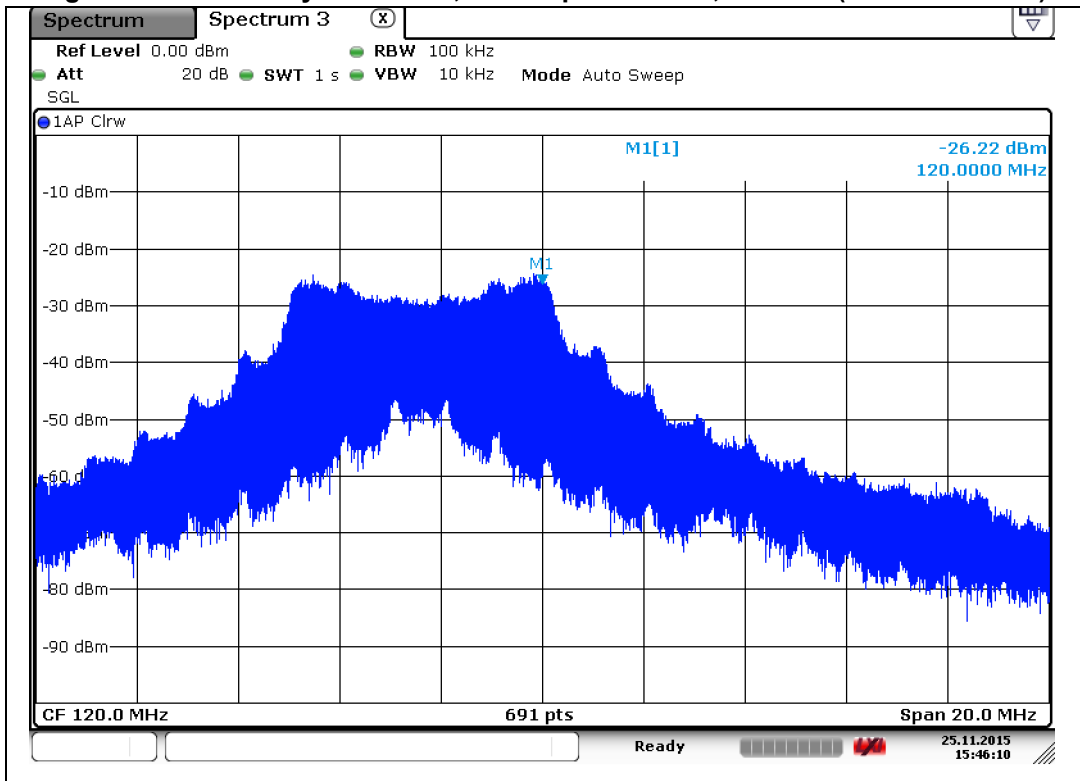**Figure 10. 120 MHz system clock, center-spread mode, md = 2%(RBW = 100 kHz)**

Figure 11. 120 MHz system clock, lower-spread mode, md = 2%(RBW = 100 kHz)

3 SSCG basic properties

3.1 Advantages

- It can reduce the peak energy on the fundamental frequency as well as its harmonic frequencies.

3.2 Disadvantages

- Jitter: essentially spread-spectrum is adding the jitter in the clock on purpose. However, such jitter may not be acceptable for some communication peripherals like the ADC, DAC and timers (used to trigger external components at given precise time).

4   Revision history

Table 2. Document revision history

Date	Revision	Changes
28-Jul-2016	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY