Introduction to LCD-TFT display controller (LTDC) on STM32 MCUs

Introduction

The evolution of the mobile, industrial, and consumer applications lead to a stronger need of graphical user interfaces (GUIs) and to an increase in the required hardware resources. These applications require higher quality graphics, more hardware and software resources (like memory for graphical primitives or framebuffer), and higher processing performances.

To respond to this increasing demand, microprocessor units are often used, which leads to a higher costs and to more complex designs with longer time to market. To face these requirements, the STM32 microcontrollers (MCUs) offer a large graphical portfolio.

Thanks to their embedded LCD-TFT display controller (LTDC), the STM32 MCUs allow high-resolution display panels to be directly driven, without any CPU intervention. In addition, the LTDC can access autonomously to internal memories or external memories to fetch pixel data.

This application note describes the LCD-TFT display controller of the STM32 MCUs listed in Table 1, and demonstrates how to use and configure the LTDC peripheral. It also highlights some hardware, software, and architectural considerations to obtain the best graphical performances.

Table 1. Applicable products

Type	Products
STM32 MCUs	• STM32F429/439 and STM32F469/479 lines • STM32F7x6, STM32F7x7, STM32F7x8, and STM32F7x9 lines • STM32H7A3/B3, STM32H723/733, STM32H725/735, STM32H742, STM32H743/753, STM32H745/755, STM32H747/757 lines • STM32H7B0, STM32H730, STM32H750 value lines • STM32H7R3/7S3 and STM32H7R7/7S7 lines • STM32L4+ series • STM32U595/5A5, STM32U599/5A9, STM32U5F7/5G7, STM32U5F9/5G9 lines • STM32N6 series

1 General information

This document applies to STM32 Arm®-based microcontrollers

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

arm

Reference documents

[1] Application note *TFT LCD interfacing with the high-density STM32F10xxx FSMC* (AN2790)

[2] Application note *QVGA TFT-LCD direct drive using the STM32F10xx FSMC peripheral* (AN3241)

[3] Application note *DSI Host on STM32F469/479, STM32F7x8/x9, and STM32L4R9/S9 MCUs* (AN4860)

[4] Application note *Quad-SPI interface on STM32 microcontrollers and microprocessors* (AN4760)

[5] Application note *Octo-SPI interface on STM32 microcontrollers* (AN5050)

[6] Application note *Managing memory protection unit in STM32 MCUs* (AN4838)

[7] Application note *Level 1 cache on STM32F7 series and STM32H7 series* (AN4839)

[8] Programming manual *STM32F7 series and STM32H7 series Cortex-M7 processor programming manual* (PM0253)

[9] Application note *Quad-SPI (QSPI) interface on STM32 microcontrollers* (AN4760)

[10] Application note *Getting started with STM32F7 series MCU hardware development* (AN4661)

[11] Application note *Getting started with STM32F4xxxx MCU hardware development* (AN4488)

[12] User manual *Discovery kit for STM32F7 series with STM32F746NG MCU* (UM1907)

2 Display and graphics overview

This section describes the basic terms used on the displays and graphics context in order to provide an overview of the general display and graphics environment. This section also summarizes the display interfaces supported by the STM32 Arm-based MCUs.

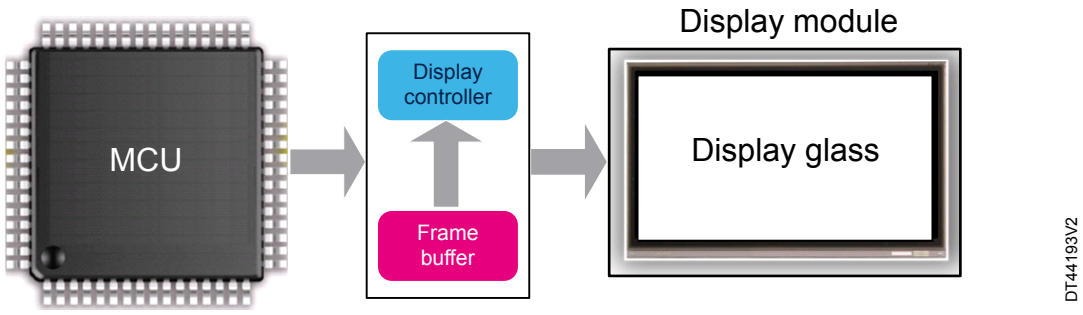
2.1 Basic graphics concepts

This section describes a basic embedded graphic system, the display module categories and the display technologies.

Basic embedded graphic system

A basic embedded graphic system schematic is described in Figure 1.

Figure 1. Basic embedded graphic system



A basic embedded graphic system is composed of a microcontroller, a framebuffer, a display controller and a display glass.

- The MCU computes the image to be displayed in the framebuffer, assembling graphical primitives such as icons or images. The CPU performs this operation by running a graphical library software. This process can be accelerated by a dedicated hardware like the DMA2D Chrom-Art Accelerator, used by the graphical library. The more often the framebuffer is updated, the more fluent the animations are (animation fps).
- The framebuffer is a volatile memory used to store pixel data of the image to be displayed. This memory is usually called the graphic RAM (GRAM). The required size of the framebuffer depends on the resolution and color depth of the display. See Section 5.2.1: Framebuffer memory size requirements and location for more information on the required size of the framebuffer.
  Double buffering is a technique that uses double framebuffers to avoid displaying what is being written to the framebuffer.
- The display controller is continuously “refreshing” the display, transferring the framebuffer content to the display glass 60 times per second (60 Hz). The display controller can be embedded either in the display module or in the MCU.
- The display glass is driven by the display controller and is responsible to display the image that is composed of a matrix of pixels.
  A display is characterized by:
  - Display size (resolution): is defined by the number of pixels of the display that is represented by horizontal (pixels number) x vertical (lines number).
  - Color depth: defines the number of colors in which a pixel can be drawn. It is represented in bits per pixel (bpp). For a color depth of 24 bpp (that can also be represented by RGB888) a pixel can be represented in 16777216 colors.
  - Refresh rate (in Hz): is the number of times per second that the display panel is refreshed. A display must be refreshed 60 times per seconds (60 Hz) since lower refresh rate creates bad visual effects.

Display module categories

The display modules are classified in two main categories, depending on whether they embed or not an internal controller and a GRAM:

- The first category corresponds to the displays with an on-glass display controller and a GRAM (see Figure 2).
- The second category corresponds to the displays with an on-glass display with no main controller and that have only a low-level timing controller.
- To interface with displays without controller nor GRAM, the used framebuffer can be located in the MCU internal SRAM (see Figure 3) or located in an external memory (see Figure 4).

Figure 2. Display module with embedded controller and GRAM

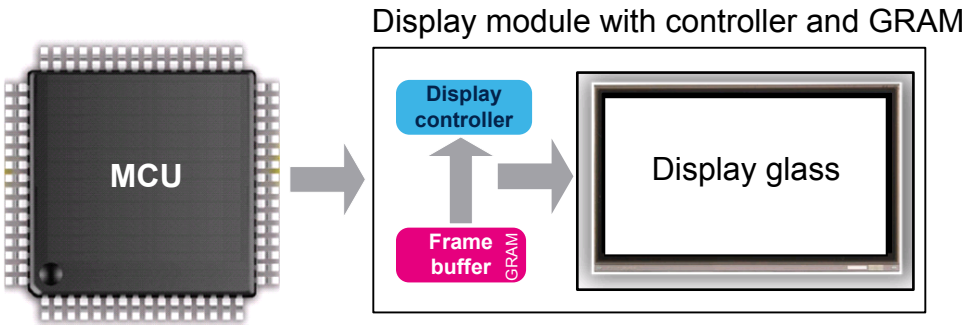


Figure 3. Display module without controller nor GRAM

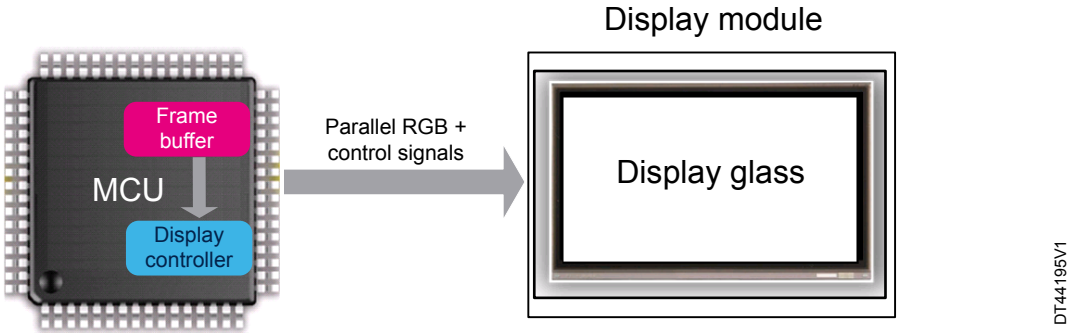
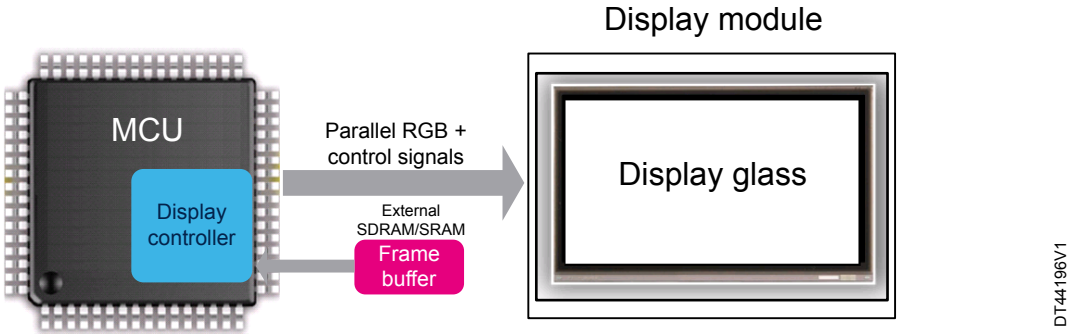


Figure 4. Display module without controller nor GRAM and with external framebuffer



Display technologies

There are many display technologies available on the market. The two main technologies used are described below:

- LCD-TFT displays (liquid crystal display - thin film transistor): variant of LCD that uses the TFT technology to improve the control of each pixel. Thanks to the TFT technology, each pixel can be controlled by a transistor, allowing a fast response time and an accurate color control.
- OLED displays (organic LED): pixels made of organic LEDs emitting directly the light, offering a better contrast and an optimized consumption. The OLED technology enables the possibility to use flexible displays, as no glass nor backlight are required. The response time is very fast and the viewing angle is free as it does not depend on any light polarization.

The way of driving the display module is quite similar in TFT and OLED technologies, the main difference is in the backlight requirement, as the OLED does not require any.

2.2 Display interface standards

The MIPI® (mobile industry processor interface) Alliance is a global, collaborative organization, committed to define and promote interface specifications for mobile devices. The MIPI Alliance develops new standards but also standardizes the existing display interfaces:

MIPI display bus interface (MIPI-DBI)

The MIPI-DBI is one of the first display standards published by the MIPI Alliance to specify the display interfaces. The three types of interfaces defined inside the MIPI-DBI are:

- Type A: based on Motorola 6800 bus
- Type B: based on Intel® 8080 bus
- Type C: based on SPI protocol

The MIPI-DBI is used to interface with a display with an integrated graphic RAM (GRAM). The pixel data is updated in the local GRAM of the display. Figure 5 illustrates a MIPI-DBI type A or B display interfacing example.

Figure 5. MIPI-DBI type A or B interface

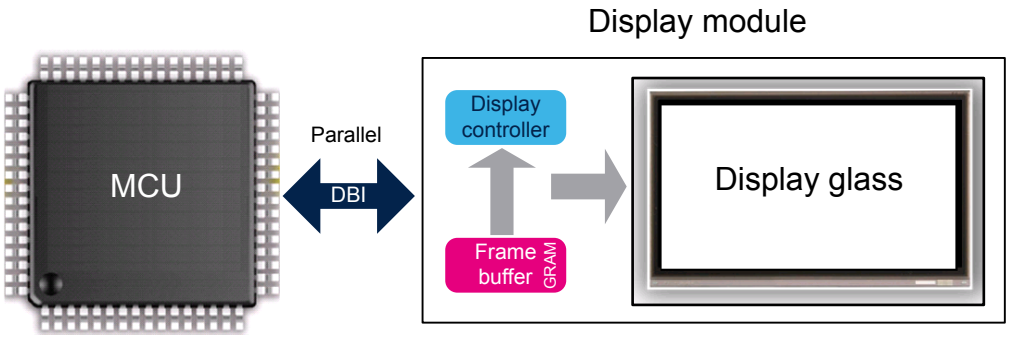
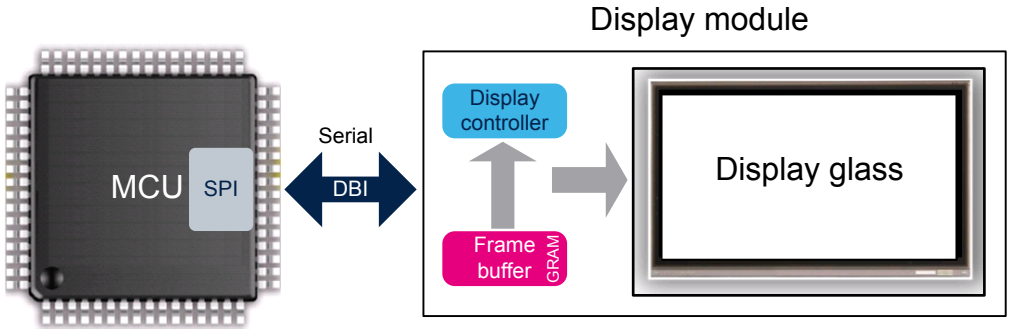


Figure 6 illustrates an MPI-DBI type C display interfacing example.

Figure 6. MIPI-DBI type C interface



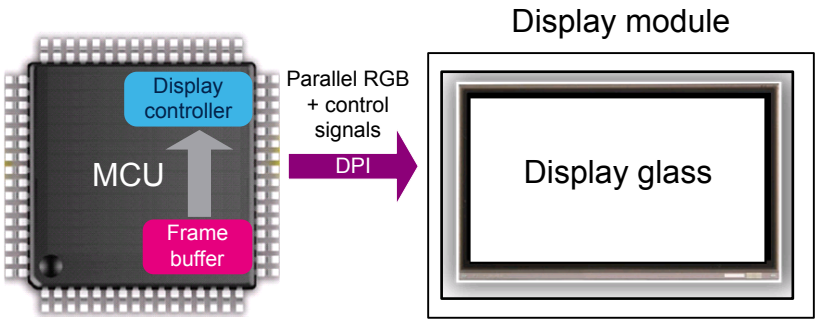
MIPI display parallel interface (MIPI-DPI)

The DPI standardizes the interface through a TFT controller. An example is when using a 16-bit to 24-bit RGB signaling with synchronization signals (HSYNC, VSYNC, EN and LCD_CLK).

The DPI is used to interface with a display without a framebuffer. The pixel data must be streamed real time to the display.

The real-time performance is excellent but requires a high bandwidth in the MCU to feed the display.

Figure 7. **MIPI-DPI interface**

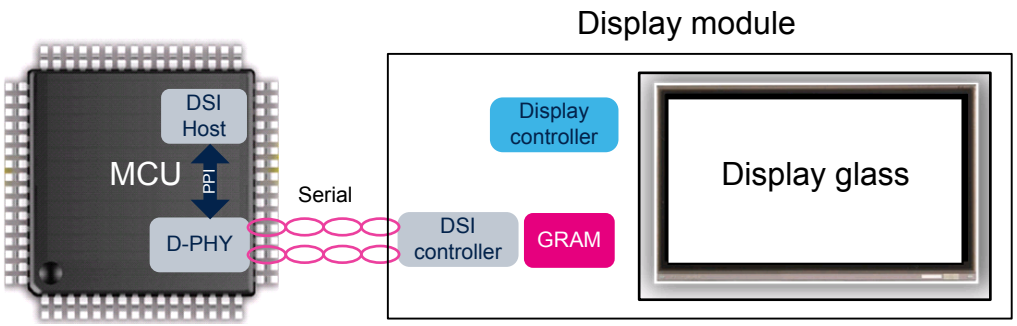


MIPI display serial interface (MIPI-DSI)

In order to decrease the number of lines to interface with a display, the MIPI Alliance has defined the DSI. The DSI is a high bandwidth multilane differential link; it uses standard MIPI D-PHY for the physical link.

The DSI encapsulates either DBI or DPI signals and transmits them to the D-PHY through the PPI protocol.

Figure 8. **MIPI-DSI interface**



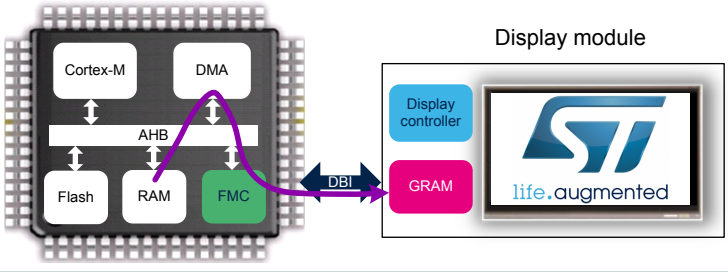
2.3 Display interfaces supported by STM32 MCUs

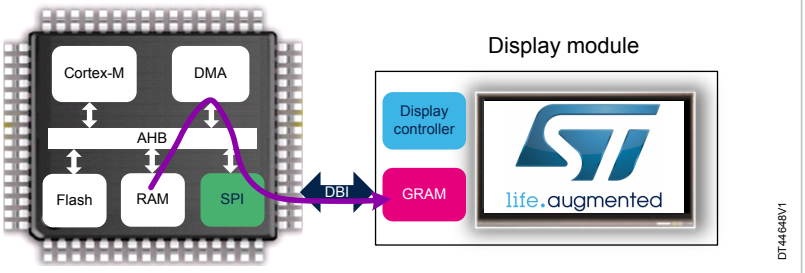
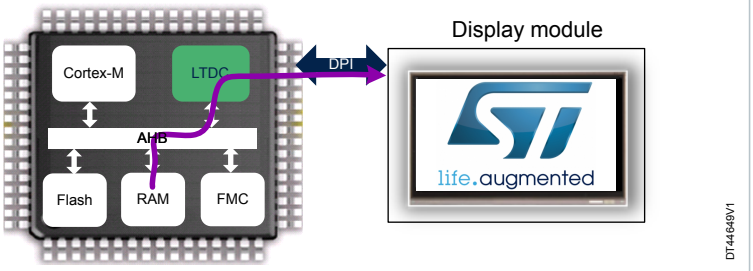
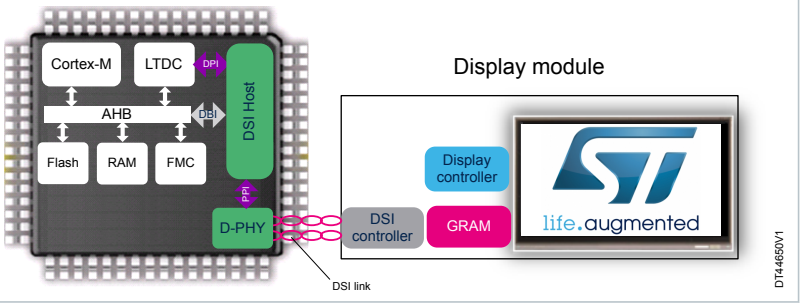
Here below a summary on the MIPI Alliance display interfaces supported by STM32 MCUs:

- All STM32 MCUs support the MIPI-DBI type C (SPI) interface.
- All STM32 MCUs with F(S)MC support the MIPI-DBI type A and B interfaces.
- STM32 MCUs with LTDC support the MIPI-DPI interface.
- STM32 MCUs embedding a DSI Host support the MIPI-DSI interface.

Table 2 illustrates and summarizes the display interfaces supported by the STM32 microcontrollers.

Table 2. . **Display interfaces supported by STM32 MCUs**

Display interface		Connecting display panels to STM32 MCU(1)
DBI(2)	Motorola 6800 DBI Type A	
	Intel 8080 DBI Type B	

Display interface		Connecting display panels to STM32 MCU(1)
DBI(2)	SPI DBI Type C	
DPI parallel RGB using LTDC(3)		
DSI(4)		

1. *Purple arrows show the pixel data path to the display.*
2. *For more information on how to support Motorola 6800 and Intel 8080 with STM32 F(S)MC, refer to the document [1].*
3. *All other STM32 MCUs with no LTDC peripheral can directly drive LCD-TFT panels using FSMC and DMA. Refer to the document [2].*
4. *Only the STM32 MCUs indicated in Table 3 embedding a DSI Host can support the DSI interface. Refer to the document [3] for more information.*

3 Overview of LTDC controller and STM32 MCUs graphical portfolio

This section illustrates the LTDC controller benefits and summarizes the graphical portfolio of the STM32 microcontrollers.

3.1 LCD-TFT display controller on STM32 MCUs

The LTDC on the STM32 microcontrollers is an on-chip LCD display controller that provides up to 24-bit parallel digital RGB signals to interface with various display panels. The LTDC can also drive other display technologies with parallel RGB interface like the AMOLED displays. The LTDC allows interfacing with low-cost display panels that do not embed neither a controller nor a graphic RAM.

3.2 LTDC and graphic portfolio across STM32 MCUs

Table 3 summarizes the STM32 MCUs embedding an LTDC and details the corresponding available graphic portfolio.

Table 3. STM32 MCUs embedding an LTDC and their available graphic portfolio

Device	FLASH (bytes)	On ship SRAM (bytes)	Quad-SPI[1]	Octo-SPI	Hexa-SPI	Max AHB/AXI frequency (MHz)[2]	Max FMC SDRAM frequency (MHz)	Max Octo-SPI frequency (MHz)	Max Hex-SPI frequency (MHz)	Max pixel clock (MHz)[3]	JPEG codec	DMA2D[4]	MIPI-DSI host[5]	Neo-Chrom (GPU2D)	Graphic libraries
STM32F429/439	Up to 2 M	256 K	No	No	No	180	90	-	-	83	No	Yes	No	No	TouchGFX embedded wizard SEGGER STemWin
STM32F469/479	Up to 2 M	384 K	Yes	No	No	180	90	-	-	83	No	Yes	Yes	No	
STM32F7x6	Up to 1 M	320 K	Yes	No	No	216	100	-	-	83	No	Yes	No	No	
STM32F7x7	Up to 2 M	512 K	Yes	No	No	216	100	-	-	83	Yes	Yes	No	No	
STM32F7x8/9	Up to 2 M	512 K	Yes	No	No	216	100	-	-	83	Yes	Yes	Yes	No	
STM32H7A3/B3	Up to 2 M	1.4 M	No	Yes	No	280	110	140	-	140	Yes	Yes	No	No	
STM32H7B0	128 K	1.4 M	No	Yes	No	280	110	140	-	140	Yes	Yes	No	No	
STM32H742/43/45/53/55	Up to 2 M	1 M	Yes	No	No	240	110	-	-	150	Yes	Yes	No	No	
STM32H747/57	Up to 2 M	1 M	Yes	No	No	240	110	-	-	150	Yes	Yes	Yes	No	
STM32H750	128 K	1 M	Yes	No	No	240	110	-	-	150	Yes	Yes	No	No	
STM32H7R7/7S7	Up to 64 K	Up to 488 K	Yes	Yes	Yes	300	100	200	200	90	Yes	Yes	No	Yes	
STM32L4P/Q	Up to 1 M	320 K	No	Yes	No	120	60[6]	92	-	83	No	Yes	No	No	
STM32L4R/S	Up to 2 M	640 K	No	Yes	No	120	60[6]	86	-	83	No	Yes	Yes	No	
STM32H723/33/25/35	Up to 1 M	564 K	No	Yes	275	-	95	150	-	No	Yes	No	No	No	
STM32H730	128 K	564 K	No	Yes	275	-	95	150	-	No	Yes	No	No	No	
STM32U5Fx/5Gx	Up to 4 M	Up to 3 M	No	Yes	Yes	160	80[6]	100	160	116	Yes	Yes	No	Yes	
STM32U59x/5Ax	Up to 4 M	Up to 2.5 M	No	Yes	Yes	160	80[6]	100	160	116	No	Yes	Yes	Yes	
STM32H7R7/7S7	Up to 64 K	Up to 488 K	Yes	Yes	Yes	300	100	200	200	90	Yes	Yes	No	Yes	
STM32N6x7/6x5	-	Up to 4.5 M	Yes	Yes	Yes	400	100	200	200	86	Yes	Yes	No	Yes	

1. *The Quad-SPI and Octo-SPI interfaces allow interfacing with external memories in order to extend the size of the application. Refer to the document [4] and [5] for more details.*
2. *LTDC fetches graphical data at AHB/AXI speed.*
3. *Maximum pixel clock value at I/O level, refer to Table 10 to Table 16 for maximum pixel clock at system level. Pixel clock (LCD_CLK) form relevant STM32 datasheet.*
4. *Chrom-Art Accelerator*
5. *The integrated MIPI-DSI controller allows easier PCB design with fewer pins, lower EMI (electromagnetic interference) and lower power consumption. For more details on STM32 MIPI-DSI host, refer to the document [3].*

6. *Max FMC PSRAM frequency (Mhz)*

3.3 LTDC in a smart architecture

The LTDC is a master on the AHB architecture that performs read access on internal and external memories. The LTDC has two independent layers, each one with its own FIFO enabling more flexibility of the display.

The LTDC controller autonomously fetches graphical data at the speed of the AHB bus from the framebuffer. The graphical data is then stored in one of the FIFO internal layers then driven to the display.

The system architecture allows graphics to be built and plotted to the screen without any CPU intervention. The LTDC retrieves the data belonging to an image from the framebuffer, while the DMA2D prepares the next images.

The LTDC interface is integrated in a smart architecture allowing:

- LTDC autonomously fetches the graphical data from the framebuffer (can be internal memories such as internal flash, internal SRAM or external memories, such as FMC_SDRAM or Quad-SPI) and drives it to the display.
- DMA2D, as an AHB master, can be used to offload the CPU from graphics intensive tasks.
- LTDC is able to continue displaying graphics even in Sleep mode when the CPU does not run.
- The multilayer AHB bus architecture improves memories throughput and leads to higher performance.

System architecture on STM32F429/439 and STM32F469/479 microcontrollers

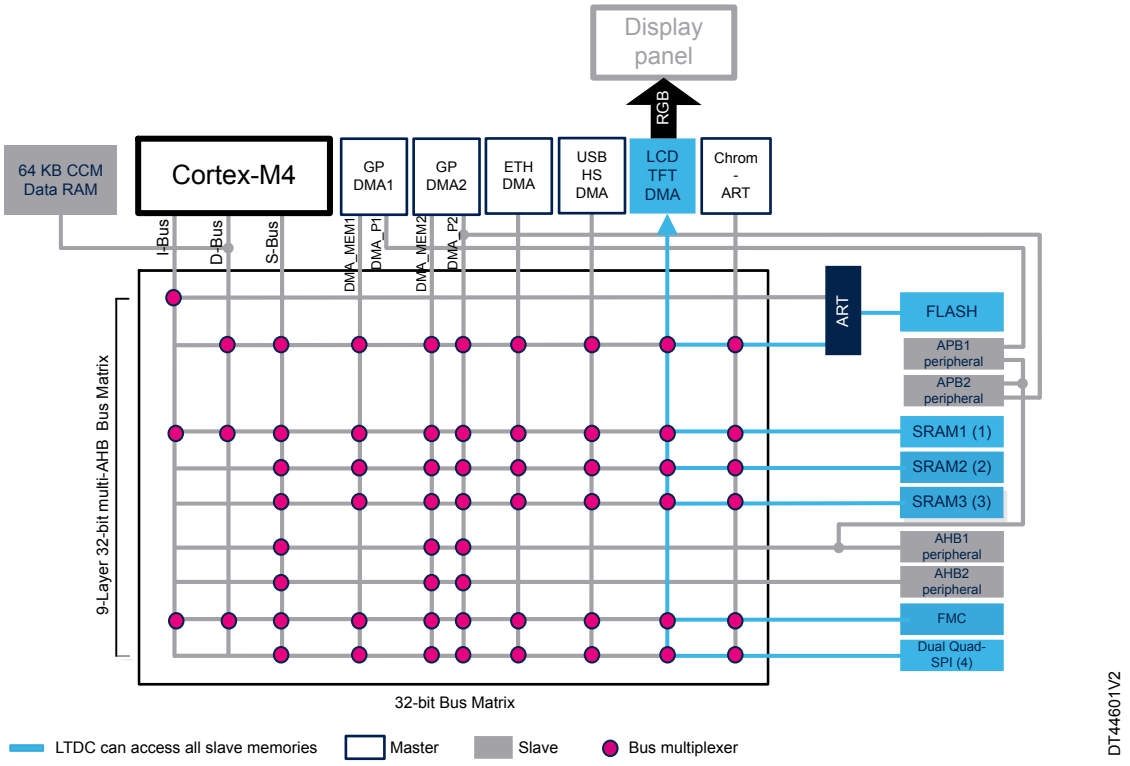
The system architecture of the STM32F429/439 line and the STM32F469/479 line consists mainly of 32-bit multilayer AHB bus matrix that interconnects ten masters and nine slaves (eight slaves for the STM32F429/F439). The LTDC is one of the ten AHB masters on the AHB bus matrix.

The LTDC can autonomously access all the memory slaves on the AHB bus matrix, such as FLASH, SRAM1, SRAM2, SRAM3 FMC or Quad-SPI enabling an efficient data transfer that is ideal for graphical applications.

Figure 9 shows the LTDC interconnection in the STM32F429/439 and STM32F469/479 lines systems.

Figure 9. LTDC AHB master in STM32F429/439 and STM32F469/479 smart architecture

(1) SRAM1 size = 112 Kbytes for STM32F429/439 and 160 Kbytes for STM32F469/479.
(2) SRAM2 size = 16 Kbytes for STM32F429/439 and 32 Kbytes for STM32F469/479.
(3) SRAM3 size = 64 Kbytes for STM32F429/439 and 128 Kbytes for STM32F469/479.
(4) Dual Quad-SPI interface is only available for STM32F469/479.



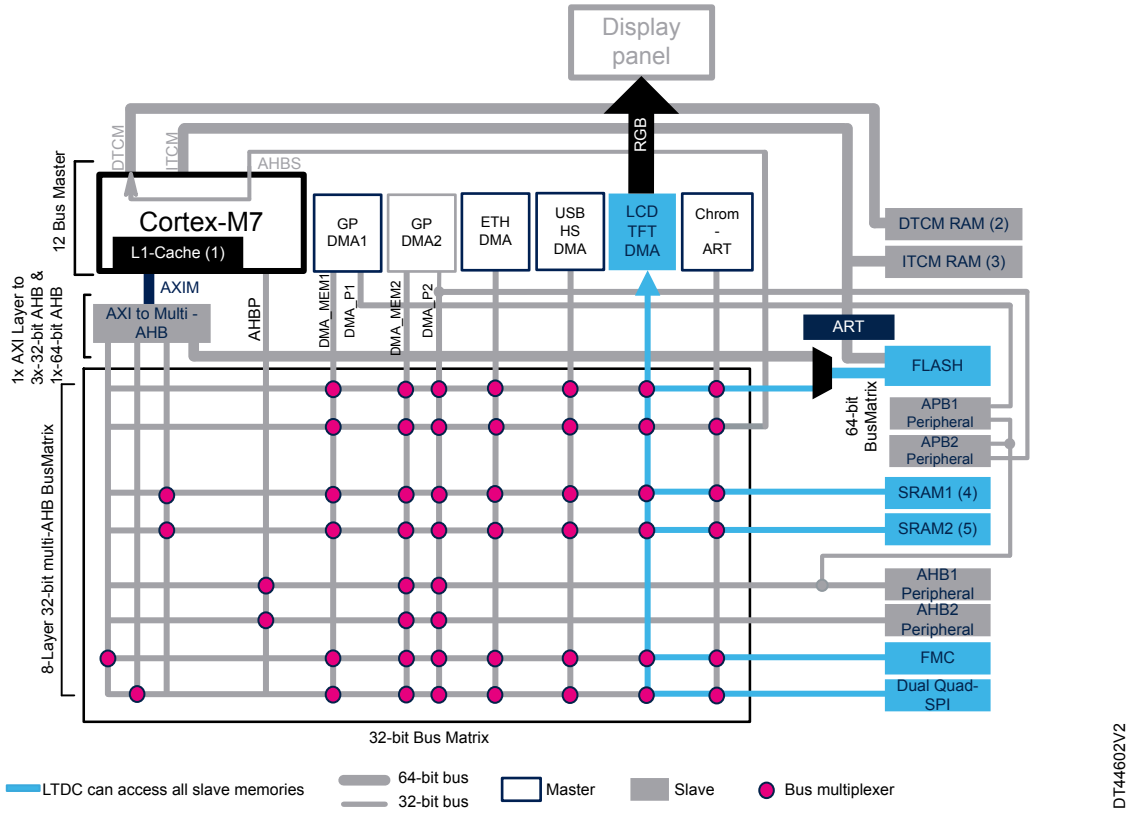
System architecture on STM32F7x6, STM32F7x7, STM32F7x8, and STM32F7x9

The system architecture of the STM32F7x6, STM32F7x7, STM32F7x8, and STM32F7x9 consists mainly of 32-bit multilayer AHB bus matrix that interconnects twelve masters and eight slaves. The LTDC is one of the twelve AHB masters on the AHB bus matrix.

The LTDC can autonomously access all the memory slaves on the AHB bus matrix, such as FLASH, SRAM1, SRAM2, FMC, or Quad-SPI enabling an efficient data transfer that is ideal for graphical applications. Figure 10 shows the LTDC interconnection in the STM32F7x6, STM32F7x7, STM32F7x8, and STM32F7x9 systems.

Figure 10. LTDC AHB master in STM32F7x6, STM32F7x7, STM32F7x8, and STM32F7x9 smart architecture

(1) I/D Cache size = 4 Kbytes for STM32F7x6.
I/D Cache size = 16 Kbytes for STM32F7x7, STM32F7x8, and STM32F7x9.
(2) DTCM RAM size = 64 Kbytes for STM32F7x6.
DTCM RAM size = 128 Kbytes for STM32F7x7, STM32F7x8, and STM32F7x9.
(3) ITCM RAM size = 16 Kbytes for STM32F7x6, STM32F7x7, STM32F7x8, and STM32F7x9.
(4) SRAM1 size = 240 Kbytes for STM32F7x6.
SRAM1 size = 368 Kbytes for STM32F7x7, STM32F7x8, and STM32F7x9.
(5) SRAM2 size = 16 Kbytes for STM32F7x6, STM32F7x7, STM32F7x8, and STM32F7x9.

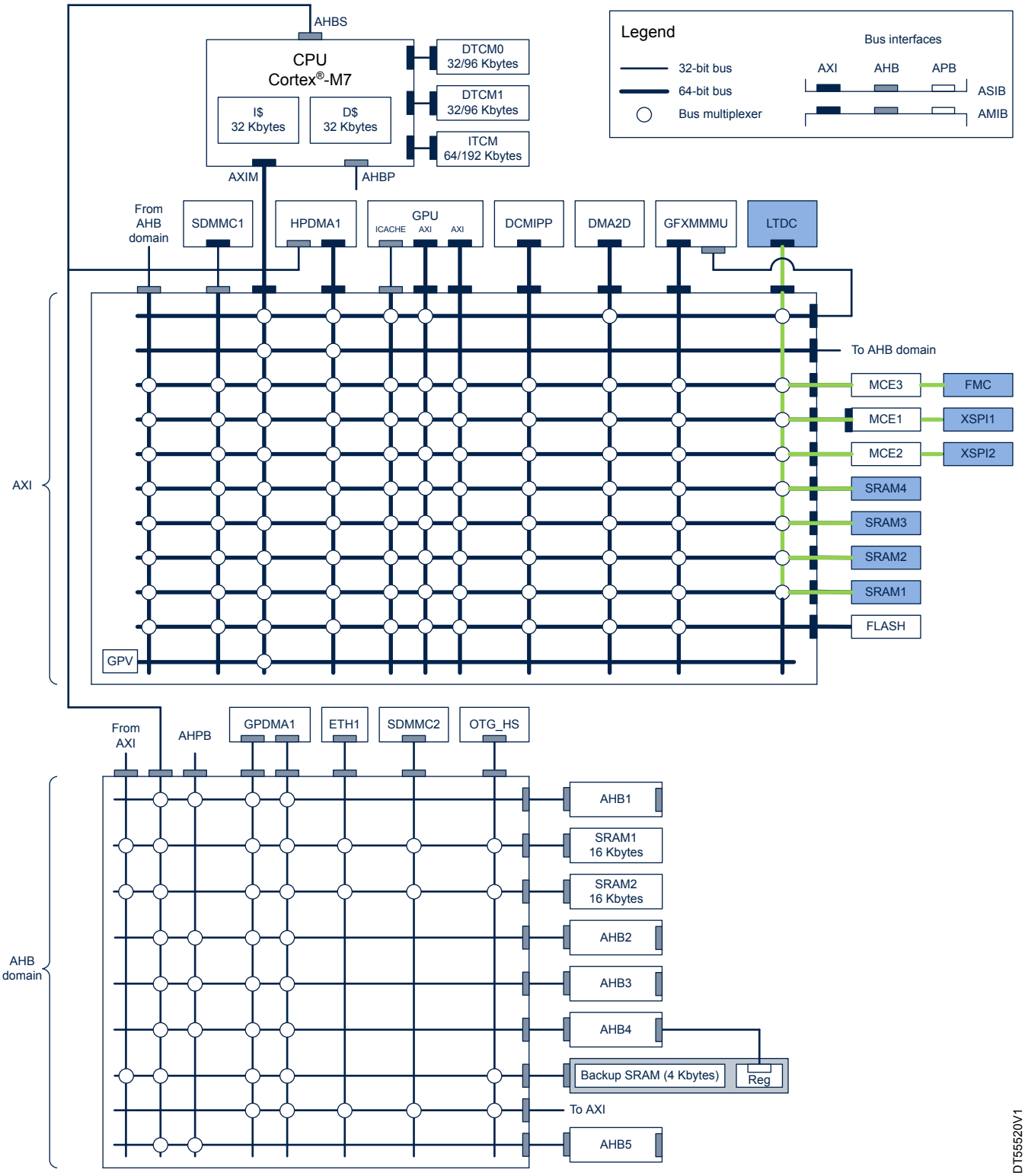


System architecture on STM32H7Rx/7Sx

The system architecture of the STM32H7Rx/7Sx primarily consists of a 64-bit AXI, a 32-bit multilayer AHB bus matrix, and bus bridges that allow interconnection of bus masters with bus slaves. The AXI bus matrix connects 11 masters and 10 slaves. The LTDC is one of the 11 AXI masters on the AXI bus matrix. The LTDC can autonomously access all the memory slaves on the AHB bus matrix, such as FLASH, SRAM1, SRAM2, FMC, or XSPI, enabling efficient data transfer ideal for graphical applications.

- I/D Cache size = 32 Kbytes
- DTCM RAM size = 64 Kbytes
- ITCM RAM size= 64 Kbytes
- SRAM1 size = 16 Kbytes
- SRAM2 size = 16 Kbytes

Figure 11. LTDC AXI master in STM32H7Rx/7Sx



3.4 Advantages of using an STM32 LTDC controller

Table 4 summarizes the major advantages of using the STM32 embedded LTDC interface.

Table 4. Advantages of using STM32 MCUs LTDC controller

Advantage	Comments
Cost savings	Compared to other DBI interfaces (SPI, Motorola 6800 or Intel 8080), the LTDC allows a connection to any low-cost display module with no display controller nor GRAM.
CPU offloaded	The LTDC is an AHB master with its own DMA, that fetches data autonomously from any AHB memory without any CPU intervention.
No need for extra applicative layer	The LTDC hardware fully manages the data fetching, the RGB outputting and the signals control, so no need for extra applicative layer.
Fully programmable resolution supporting custom and standard displays	Fully programmable resolution with total width of up to 4096 pixels and total height of up to 2048 lines and with pixel clock of up to 83 MHz. Support of custom and standard resolutions (QVGA, VGA, SVGA, WVGA, XGA, HD, and others).
Flexible color format	Each LTDC layer can be configured to fetch the framebuffer in the desired pixel format (see Section 4.3.2: Programmable layer: color framebuffer).
Flexible parallel RGB interface	The flexible parallel RGB interface allows to drive 16-bit, 18-bit and 24-bit displays.
Ideal for low-power and mobile applications such as smart watches.	The LTDC is able to continue graphic data fetching and display driving while the CPU is in Sleep mode.

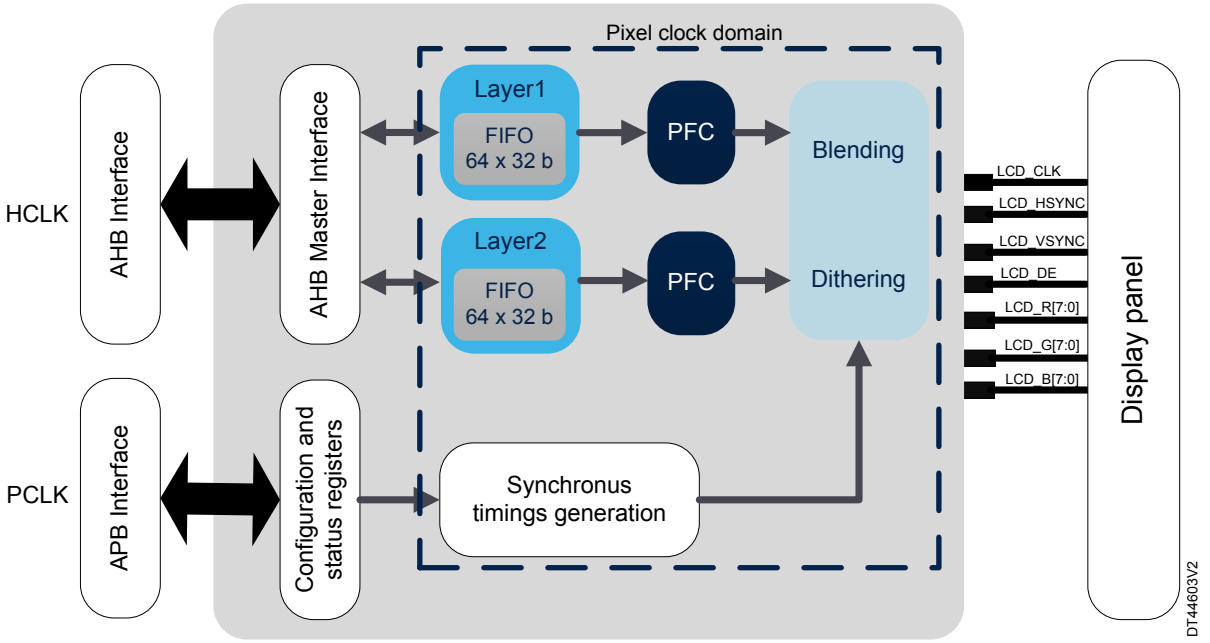
4 LCD-TFT (LTDC) display controller description

The LTDC is a controller that reads the data of images in a line per line fashion. Its memory access mode is 64/128-byte (for AHB/AXI) length, but when the end of a line is reached and less than 64/128 bytes (for AHB/AXI) are left, the LTDC fetches the remaining data.

4.1 Functional description

On every pixel clock-raising edge or clock-falling edge and within the screen active area, the LTDC layer retrieves one pixel data from its FIFO, converts it to the internal ARGB8888 pixel format and blends it with the background and/or with the other layer pixel color. The resulting pixel, coded in the RGB888 format, goes through the dithering unit and is driven into the RGB interface. The pixel is then displayed on the screen.

Figure 12. LTDC block diagram



4.1.1 LTDC clock domains

The LCD-TFT controller peripheral uses three clock domains:

- AHB clock domain (HCLK): used to transfer data from the memories to the FIFO layer and the other way around.
- APB clock domain (PCLK): used to access the configuration and status registers.
- Pixel clock domain (LCD_CLK): used to generate the LCD-TFT interface signals.
  The LCD_CLK output need to be configured following the panel requirements through the PLL.

4.1.2 LTDC reset

The LTDC is reset by setting the LTDCRST bit in the RCC_APB2RSTR register.

4.2 Flexible timings and hardware interface

Thanks to its timings and hardware interface flexibility, the LCD-TFT controller is able to drive several monitors with different resolutions and signal polarities.

4.2.1 LCD-TFT pins and signal interface

To drive LCD-TFT displays, the LTDC provides up to 28 signals using simple 3.3 V signaling including:

- Pixel clock LCD_CLK
- Data enable LCD_DE
- Synchronization signals (LCD_HSYNC and LCD_VSYNC)
- Pixel data RGB888

Note: The LTDC controller may support other display technologies if their interface is compatible.

The LTDC interface output signals are illustrated in Table 5

Table 5. LTDC interface output signals

LCD-TFT signal	Description
LCD_CLK	The LCD_CLK acts as the data valid signal for the LCD-TFT. The data is considered by the display only on the LCD_CLK rising or falling edge.
LCD_HSYNC	The line synchronization signal (LCD_HSYNC) manages horizontal line scanning and acts as line display strobe.
LCD_VSYNC	The frame synchronization signal (LCD_VSYNC) manages vertical scanning and acts as a frame update strobe.
LCD_DE	The DE signal, indicates to the LCD-TFT that the data in the RGB bus is valid and must be latched to be drawn.
Pixel RGB data	The LTDC interface can be configured to output more than one color depth. It can use up to 24 data lines (RGB888) as display interface bus.

Other signals

It is usual that display panel interfaces include other signals that are not part of the LTDC signals described in Table 5. These additional signals are required for a display module to be fully functional. The LTDC controller is able to drive only signals described in Table 5.

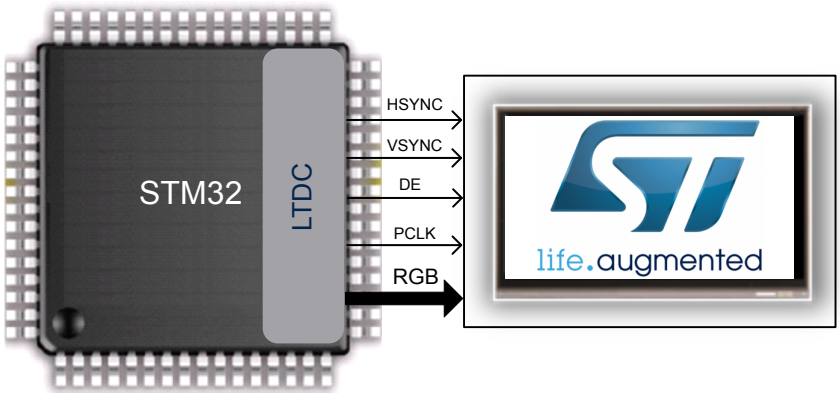
The signals that are not part of the LTDC, may be managed using GPIOs and other peripherals and may need specific circuits.

The display panels usually embed a backlight unit that requires an additional backlight control circuit and a GPIO.

Some display panels need a reset signal and also a serial interface such as I^2C or SPI. These interfaces are used in general for the display initialization commands or for the touch panel control.

Figure 13 shows a display panel connected to an STM32 MCU, using the LTDC interface signals illustrated in Table 5.

Figure 13. LTDC signal interface



The LTDC can output data according to the following parallel formats: RGB565, RGB666, and RGB888. So, 16-bit RGB565, 18-bit RGB666 or 24-bit RGB888 display can be connected.

LTDC signals programmable polarity

The LTDC control signals polarity is programmable allowing the STM32 microcontroller to drive any RGB parallel display. The control signals (HSYNC, VSYNC, and data enable DE) as well as the pixel clock (LCD_CLK) can be defined to be active high or active low through the LTDC_GCR register.

4.2.2 Fully programmable timings for different display sizes

Thanks to its “timings flexibility”, the LTDC peripheral can support any display size that respects the maximal programmable timing parameters in the registers and the maximal supported pixel clock described in Table 3 and Table 11 to Table 16.

The user must consider the timings registers described in Table 6 when programming as the LTDC timings and synchronization signals must be programmed to match the display specification.

Table 6 summarizes the timings registers supported by the LTDC.

Table 6. LTDC timing registers

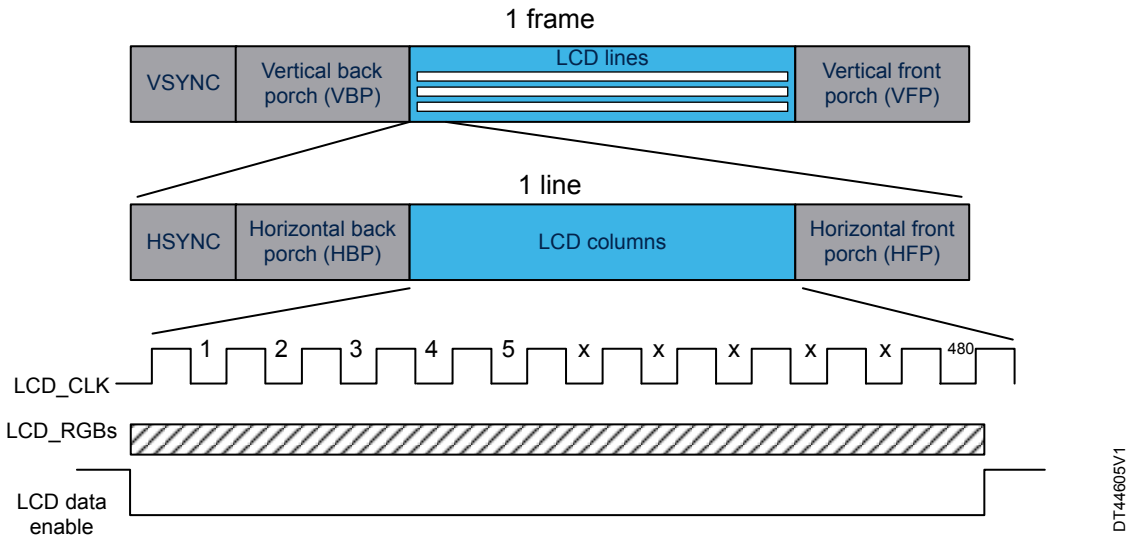
Register		Timing parameter	Value to be programmed
LTDC_SSCR(1)	HSW[11:0]	HSYNC width - 1	From 1 to 4096 pixels
	VSH[11:0]	VSYNC height - 1	From 1 to 2048 lines
LTDC_BPCR	AHBP[11:0]	HSYNC width + HBP - 1	From 1 to 4096 pixels
	AVBP[10:0]	VSYNC height + VBP - 1	From 1 to 2048 lines
LTDC_AWCR	AAW[11:0]	HSYNC width + HBP + active width - 1	From 1 to 4096 pixels
	AAH[10:0]	VSYNC height + BVBP + active height - 1	From 1 to 2048 lines
LTDC_TWCR	TOTALW[11:0]	HSYNC width + HBP + active width + HFP - 1	From 1 to 4096 pixels
	TOTALH[10:0]	VSYNC height + BVBP + active height + VFP - 1	From 1 to 2048 lines

1. *Setting HSYNC to 0 in HSW[11:0] gives one pulse width of one LCD_CLK. Setting VSYNC to 0 in VSW[11:0] gives one total line period.*

Example of a typical LTDC display frame

Figure 14 shows an example of a typical LTDC display frame showing the timing parameters described in Table 6.

Figure 14. Typical LTDC display frame (active width = 480 pixels)

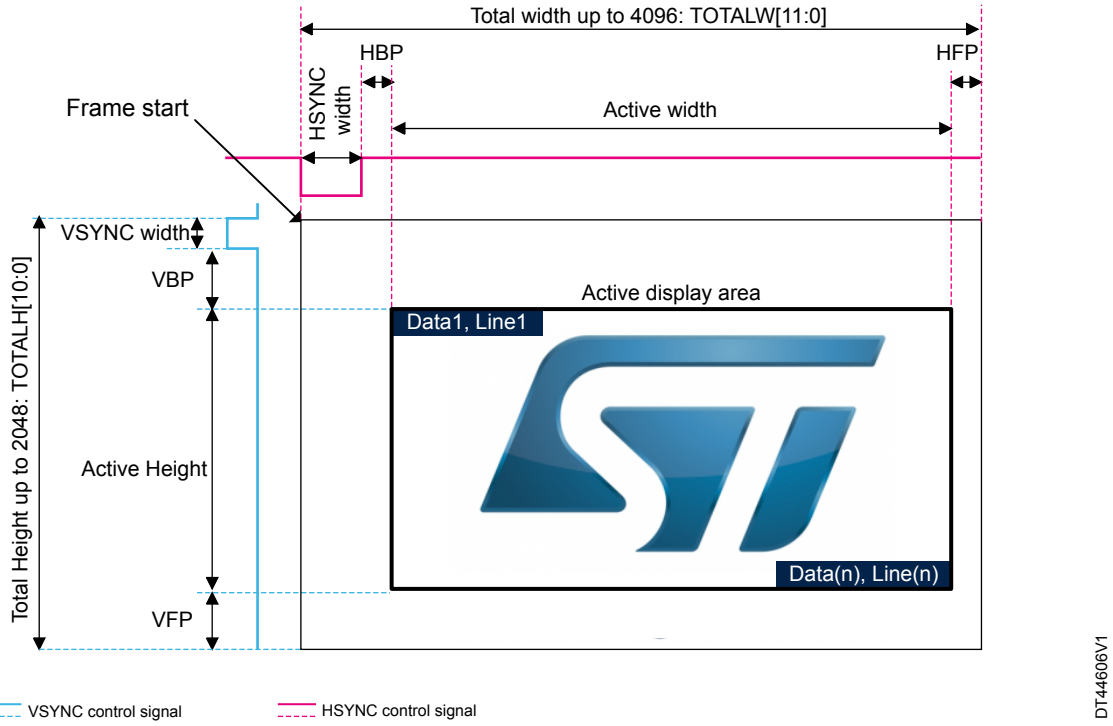


LTDC flexible timings

The LTDC peripheral allows the user to interface with any display size with total width of up to 4096 pixels and total height of up to 2048 lines (refer to Table 6).

Figure 15 illustrates fully programmable timings and resolutions.

Figure 15. Fully programmable timings and resolutions



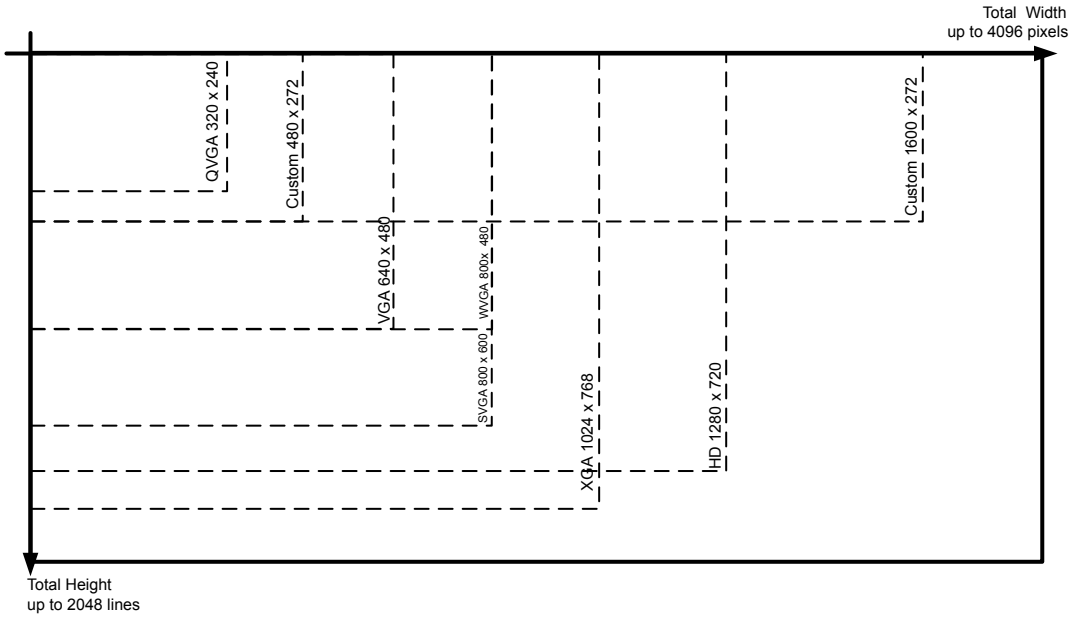
Caution: *Any display resolution belonging to the maximal total area in 4096 x 2048 as described in Figure 15 is supported by the LTDC only if the following conditions are met:*

- *The display panel pixel clock must not exceed the maximal LTDC pixel clock in Table 2.*
- *The display panel pixel clock must not exceed the maximal STM32 pixel clock respecting the framebuffer bandwidth (see Section 5.2: Checking the display size and color depth compatibility with the hardware configuration).*

Figure 16 shows some custom and standard resolutions belonging to the maximal 4096 x 2048 supported by the LTDC.

Figure 16. LTDC fully programmable display resolution with total width up to 4096 pixels and total height up to 2048 lines

Only the active display area is shown in this figure.



4.3 Two programmable LTDC layers

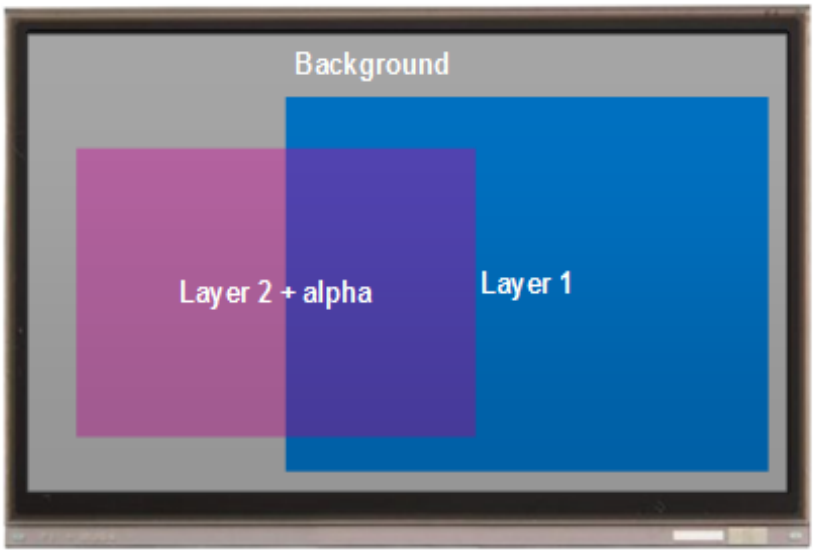
The LTDC features two layers, and each layer can be enabled, disabled, and configured separately. The order of the layer display is fixed, so it is always bottom-up. If two layers are enabled, the Layer2 is the top displayed window.

The LTDC features configurable blending factors. Blending is always active using an alpha value. The blending order is fixed and it is always bottom-up. If two layers are enabled, first the Layer1 is blended with the background color, and then the Layer2 is blended with the result of the blended color of Layer1 and the background.

The background color is programmable through the LTDC_BCCR register. A constant background color can be programmed in the RGB888 format where the BCRED[7:0] field is used for the red value, the BCGREEN[7:0] is used for the green value and the BCBLUE[7:0] is used for the blue value.

Figure 17 illustrates the blending of two layers with a background.

Figure 17. Blending two layers with a background



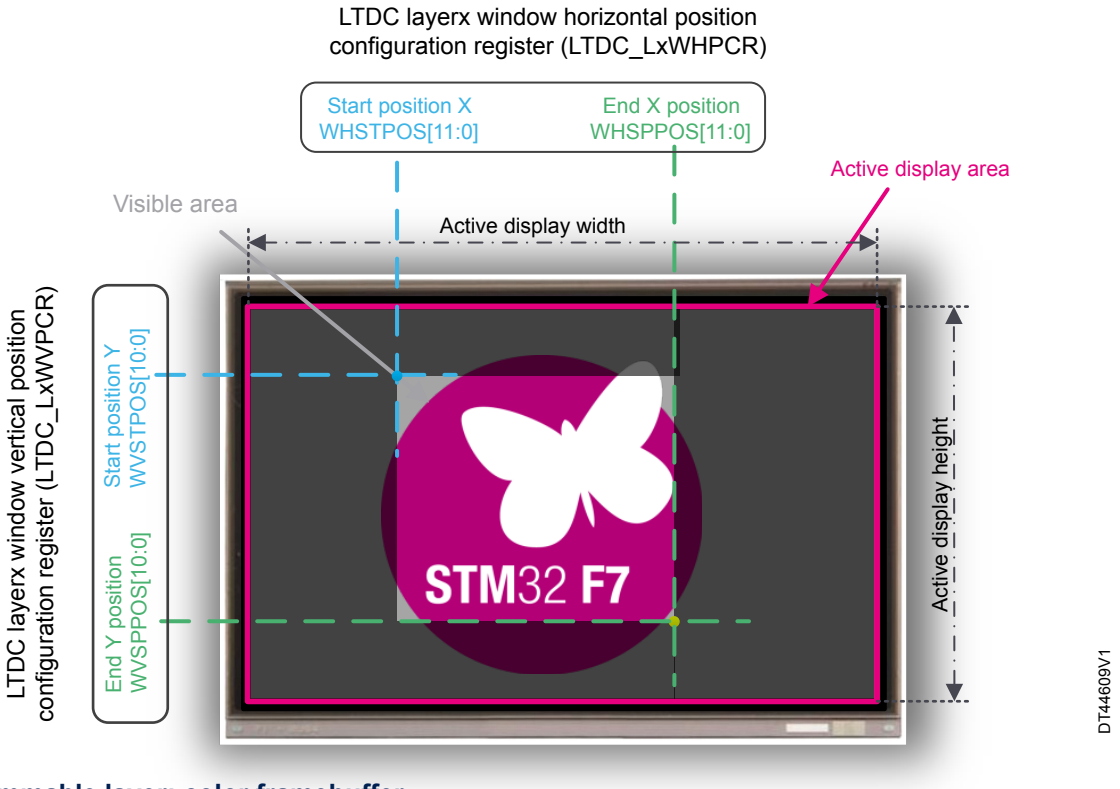
4.3.1 Flexible window position and size configuration

Every layer can be positioned and resized at runtime and it must be inside the active display area. The programmable layer position and size define the first and last visible pixel of a line and the first and last visible line in the window. It allows the display of either the full image (all the active display area) or only a part of the image frame.

Figure 18 shows a small window where only a portion of the image is displayed while the remaining area is not displayed.

Figure 18. Layer window programmable size and position

LTDC_LxWHPCR and LTDC_LxWVPCR are respectively LTDC layer x window horizontal and vertical position configuration registers where “x” can refer to Layer1 or Layer2.



4.3.2 Programmable layer: color framebuffer

Every layer has a dedicated configurable number of lines and line length for the color framebuffer and for the pitch.

Color framebuffer address

Every layer has a start address for the color framebuffer configured through the LTDC_LxCFBAR register.

Color framebuffer length (size)

The line length and the number of lines parameters are used to stop the prefetching of data from the FIFO layer at the end of the framebuffer.

The line length (in bytes) is configurable in the LTDC_LxCFBLR register.

The number of lines (in bytes) is configurable in the LTDC_LxCFBLNR register.

Color framebuffer pitch

The pitch is the distance between the start of one line and the beginning of the next line in bytes. It is configured in the LTDC_LxCFBLR register.

Pixel input format

The programmable pixel format is used in all the data stored in the framebuffer of each LTDC layer.

For each layer, a specific pixel input format can be configured separately. The LTDC can be configured with up to eight programmable input color formats per layer.

Figure 19 illustrates the pixel data mapping versus the selected input color format.

Figure 19. Pixel data mapping versus color format

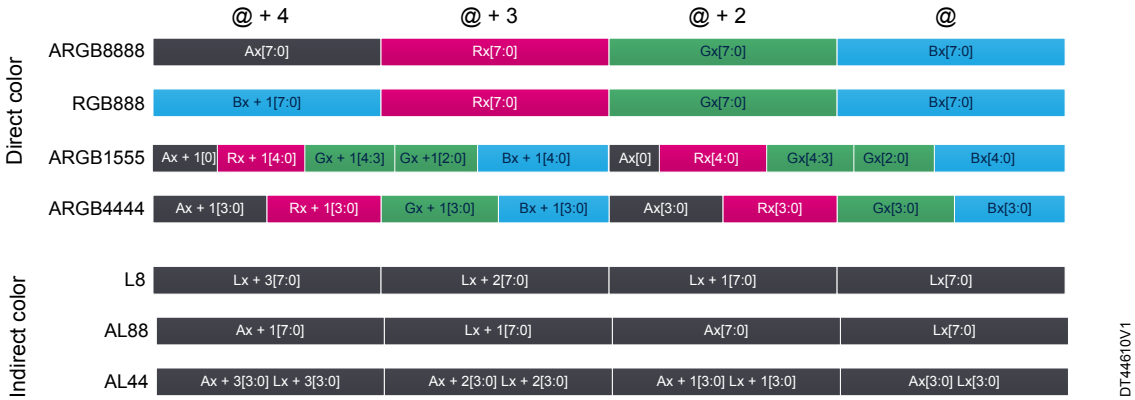
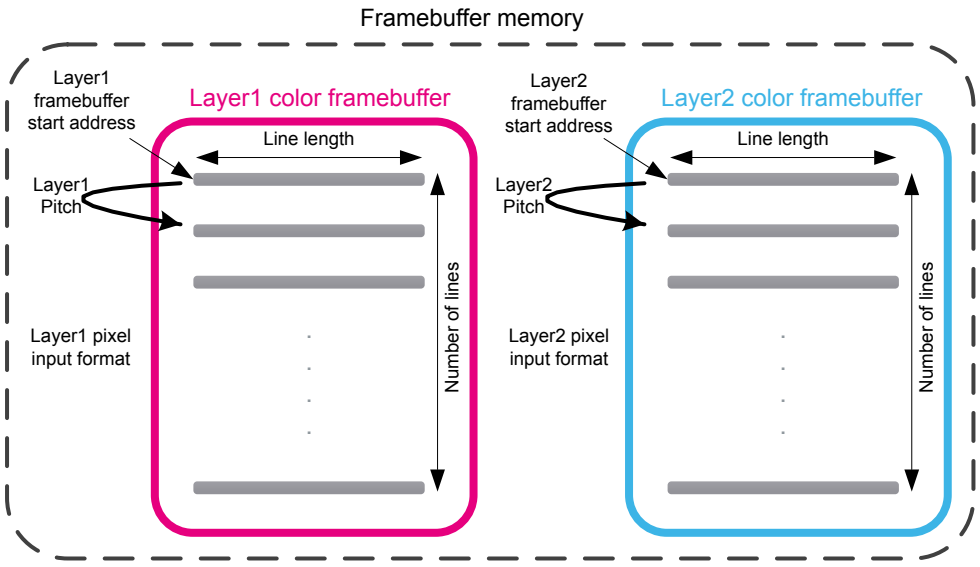


Figure 20 summarizes all layer color framebuffer configurable parameters.

Figure 20. Programmable color layer in framebuffer



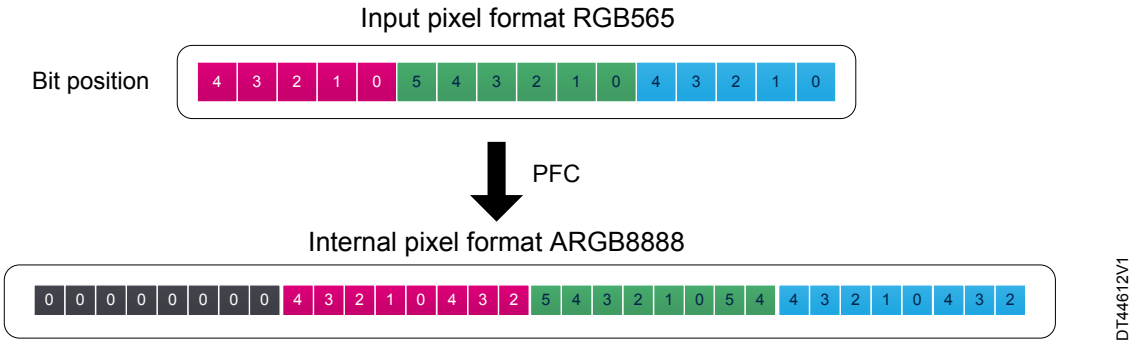
Pixel format conversion (PFC)

After being read from the framebuffer, the pixel data is transformed from the configured pixel input format to the internal ARGB8888 format.

The components that have a width of less than 8 bits, get expanded to 8 bits by bit replication. The 8 MSB bits are chosen.

Figure 21 shows a conversion from RGB565 input pixel format to the internal ARGB8888 format.

Figure 21. Pixel format conversion from RGB565 input pixel format to the internal ARGB8888 format



Note: Using two layers creates bandwidth constraints on the system. It is preferable to use only one layer and to do the composition with the Chrom-Art Accelerator during the framebuffer calculation (see Section 5.2.2: Checking display compatibility considering the memory bandwidth requirements).

4.4 Interrupts

The LTDC peripheral supports two global interrupts:

- LTDC global interrupt
- LTDC global error interrupt

Each global interrupt is connected to two LTDC interrupts (logically disjointed) that can be masked separately through a specific register. Table 7 summarizes all of the related interrupts and all the particular cases when each interrupt is generated.

Table 7. LTDC interrupts summary

Related NVIC interrupt	Interrupt event	Event flag bit (LTDC_ISR register)	Enable bit (LTDC_IER register)	Clear bit (LTDC_ICR register)	Description
LTDC GLOBAL INTERRUPT	Line	LIF	LIE	CLIF	Generated when a defined line on the screen is reached
	Register reload	RRIF	RRIE	CRRIF	Generated when the shadow reload occurs
LTDC GLOBAL ERROR INTERRUPT	FIFO underrun(1)	FUIF	FUIE	CFUIF	Generated when a pixel is requested while the FIFO is empty
	Transfer error	TERRIF	TERRIE	CTERRIF	Generated when bus error occurs

1. *FIFO underrun interrupt is useful for determining the display size compatibility (see Section 5.2.2: Checking display compatibility considering the memory bandwidth requirements).*

4.5 Low-power modes

The STM32 power state has a direct effect on the LTDC peripheral. While in Sleep mode, the LTDC is not affected and keeps driving graphical data to the screen. While in Standby and Stop modes, the LTDC is disabled and no output is driven through its parallel interface. Exiting Standby mode must be followed with the LTDC reconfiguration.

A display panel can be driven in Sleep mode while the CPU is stopped, thanks to the smart architecture embedded in the STM32 MCUs that allows all peripherals to be enabled even in Sleep mode. This feature fits wearable applications where the low-power consumption is a must.

The LTDC, as an AHB master, can continue fetching data from FMC_SDRAM, Quad-SPI or Octo-SPI (when the Memory-mapped mode is used), even after entering the MCU in Sleep mode. A line event or register reload interrupt can be generated to wake up the STM32 when a defined line on the screen is reached or when the shadow reload occurs.

More information on reducing power consumption is available on Section 6.

Table 8 summarizes the LTDC state versus the STM32 low-power modes.

Table 8. LTDC peripheral state versus STM32 low-power modes

Mode	Description
Run	Active
Sleep	Active Peripheral interrupts cause the device to exit Sleep mode.
Stop	Frozen Peripheral registers content is kept.
Standby	Powered-down The peripheral must be reinitialized after exiting Standby mode.

5 Creating a graphical application with LTDC

This section illustrates the different steps required before and during a graphical application development using LTDC. The user must at first determine the graphical application requirements, then check if the desired display size fits the hardware configuration. During the graphical application compatibility check phase, the existing STM32 reference boards described in Table 24 can be used to evaluate his hardware and software configuration.

5.1 Determining graphical application requirements

Determining the graphical application needs is a crucial step to start from. Some of the most important parameters to be defined before starting the creation of the graphical application are display resolution, color depth, as well as the nature of the data to display (static images, text, or animation).

Once the basic parameters mentioned above are defined, the user must determine the graphical hardware architecture of the application, as well as the required hardware resources. The best-fitting STM32 package (see Table 20) must be selected, according to the following parameters:

- If an external memory is needed for the framebuffer.
- The external framebuffer memory bus width
- The LTDC interface: RGB565, RGB666, or RGB888 depending on the display module
- If an external memory is needed to store graphic primitives (QSPI or FMC_NOR).

5.2 Checking the display size and color depth compatibility with the hardware configuration

When starting a graphic application development using an STM32 microcontroller, the user has often a defined desired display size and color depth. A key question that the user must answer before continuing the development is if such display size and color depth match a specific hardware configuration.

The following steps are needed in order to answer this question:

1. Determine the required framebuffer size and its location.
2. Check the compatibility of the display versus the framebuffer memory bandwidth requirements.
3. Check the compatibility of the display panel interface with the LTDC.

5.2.1 Framebuffer memory size requirements and location

Determining the framebuffer memory size and its location is a key parameter for the display compatibility check.

The memory space required in the RAM to support the framebuffer must be contiguous and with a minimum size equal to:

Framebuffer size = number of pixels x bits per pixel

As shown in the formula above, the required framebuffer size depends on the display resolution and on its color depth.

It is not necessary that the framebuffer color depth (bpp) is the same than the display color depth. For instance, an RGB888 display can be driven using an RGB565 framebuffer.

Note: The required framebuffer size is doubled for double-framebuffer configuration. It is common to use a double-buffer configuration where one graphic buffer is used to store the current image, while the second buffer is used to prepare the next image.

Table 9 shows the framebuffer size needed for standard screen resolutions with different pixel formats.

Table 9. Framebuffer size for different screen resolutions

Screen resolution	Number of pixels	Framebuffer size (Kbyte)(1)			
		8 bpp	16 bpp	24 bpp	32 bpp
QVGA (320 x 240)	76800	75	150	225	300
Custom (480 x 272)(2)	130560	128	255	383	510
HVGA(480 x 320)	153600	150	300	450	600
VGA (640 x 480)	307200	300	600	900	1200

Screen resolution	Number of pixels	Framebuffer size (Kbyte)(1)			
		8 bpp	16 bpp	24 bpp	32 bpp
WVGA(800 x 480)	384000	375	750	1125	1500
SVGA (800 x 600)	480000	469	938	1407	1875
XGA (1024 x 768)	786432	768	1536	2304	3072
HD (1280 x 720)	921600	900	1800	2700	3600

1. *The required framebuffer size is doubled for double-framebuffer configuration.*
2. *An example of a custom 480 x 272 display is the ROCKTECH embedded on the STM32F746 discovery kit (32F746GDISCOVERY).*

Framebuffer location

Depending on the required framebuffer size, the framebuffer can be located either in an internal SRAM or in an external SRAM/SDRAM.

If the internal RAM is not enough for the framebuffer, the user must use an external SDRAM/SRAM connected to the FMC.

Consequently, the required framebuffer size determines if the use of an external memory is needed or not. The required framebuffer size depends on the display size and color depth.

Locating the framebuffer in the Internal SRAM

Depending on the framebuffer size, the framebuffer can be placed either in the internal SRAM or the external SRAM or SDRAM.

Using an internal SRAM as a framebuffer allows the maximum performances and avoids any bandwidth limitation issues for the LTDC.

Using the internal SRAM instead of an external SRAM or SDRAM has many advantages:

- higher throughput (0 wait state access)
- reduced number of required pins and PCB design complexity
- reduced BOM, hence cost, since no external memory is needed

The only limitation when using the internal SRAM is its limited size (hundreds of Kbytes). When the framebuffer size exceeds the available memory, the external SDRAM or SRAM (driven by the FMC interface) must be used. However, when dealing with external memories, the user must be careful to avoid bandwidth limitation. For more detailed information, refer to Section 5.5: Graphic performance optimization.

Note: The color look-up table CLUT can be used to decrease the required framebuffer size. (For more details, refer to the STM32 MCU reference manual).

5.2.2 Checking display compatibility considering the memory bandwidth requirements

This section explains how to check a display compatibility considering the framebuffer memory bandwidth. Some important bandwidth aspects are described and this section explains how to determine the required bandwidth for the pixel clock and the LTDC. Finally, a simple method to conclude whether a desired display size is compatible with a specific hardware configuration; is detailed.

Framebuffer memory bandwidth aspects

Once the framebuffer location is fixed (either in internal or external memory), the user must check if its bandwidth can sustain the hardware configuration.

To check if the memory bandwidth can sustain the LTDC required bandwidth, the user must consider any other concurrent accesses to the memory.

In general, a small size framebuffer located in the internal RAM does not require a high bandwidth. This is because a small size framebuffer means low pixel clock, hence low LTDC required bandwidth.

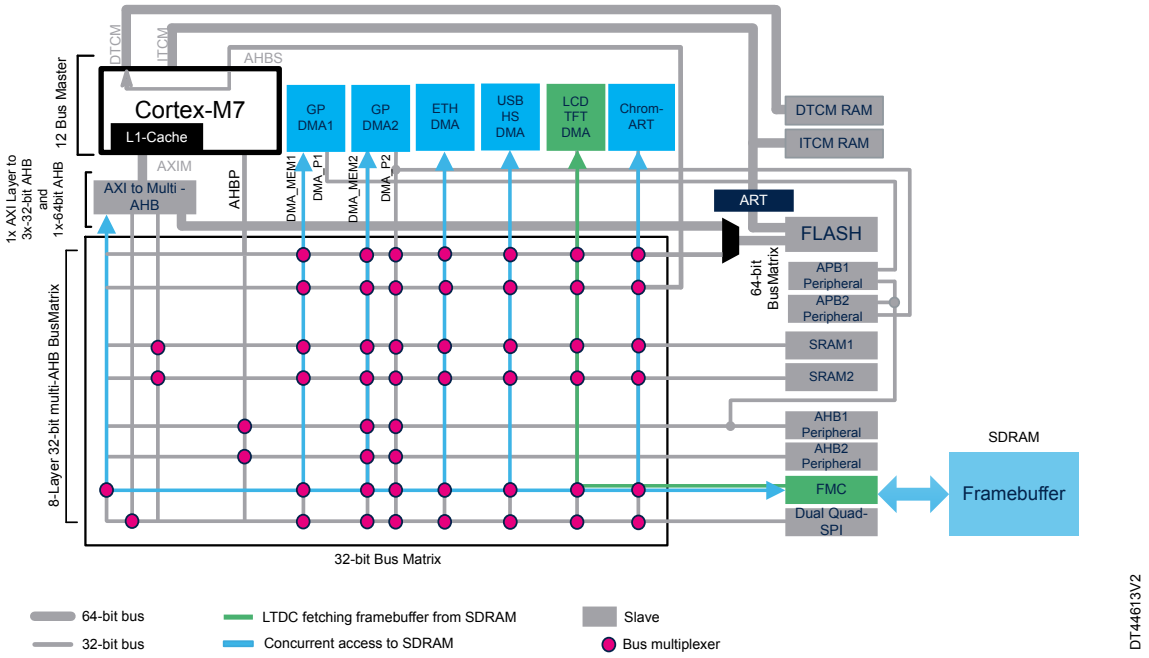
A more complex use case to analyze is when the framebuffer is located in an external memory (SDRAM or SRAM).

Framebuffer memory bus concurrency

- LTDC, DMA2D, and CPU masters.
  In a typical graphic application where an external SDRAM or SRAM memory is used as framebuffer, two or three main AHB masters concurrently use the same memory.
  The DMA2D (or the CPU) updates the next image to be displayed while the LTDC fetches and displays the actual image. The memory bus load depends mainly on the LTDC required bandwidth.
- Other AHB masters.
  It is common that an external SDRAM or SRAM memory is shared by other masters and not only by those used for graphics. This concurrency leads to heavy bus load and may impact the graphic performances.

Figure 22 shows all the AHB masters with concurrent access to the SDRAM.

Figure 22. AHB masters concurrent access to SDRAM



External SDRAM/SRAM memory bus width

When locating the framebuffer in an external SDRAM/SRAM, the user must consider that the external memory running frequency is around half or third of the system frequency. That is the reason why the memory bandwidth must be considered as the bottleneck of the whole graphic system.

One of the needed parameters for checking the display compatibility is the memory bus width. For SDRAM, an 8-bit, 16-bit, or 32-bit configuration can be used.

As previously stated, the most complex to analyze is the use case when the framebuffer is placed in an external memory:

The masters concurrent access on the same external memory leads to more latency and impacts its throughput.

Determining pixel clock and LTDC required bandwidth

Pixel clock computation

The pixel clock is a key parameter for checking display size compatibility with a specific hardware configuration.

To get the typical pixel clock of the display, refer to the display datasheet. The computed pixel clock need to respect the display specifications.

The pixel clock for a specific refresh rate is calculated with the following formula:
LCD_CLK (MHz) = total screen size x refresh rate
Where total screen size = total width x total height.

LTDC required bandwidth

The LTDC required bandwidth depends mainly on three factors:

- Number of used LTDC layers.
- LTDC layer color depth.
- Pixel clock (depends on the resolution of the display panel and on the refresh rate).

The maximum required bandwidth can be calculated as described below:

- If only one LTDC layer is used:
  LTDC required bandwidth = LCD_CLK x BppL1
- If two LTDC layers are used:
  LTDC required bandwidth = LCD_CLK x (BppL1 + BppL2)

Where BppL1 and BppL2 are respectively the color depth for LTDC Layer1 and Layer2. The LTDC required bandwidth must not exceed the memory available bandwidth, otherwise, display problems may occur and the FIFO underrun flag may be set (if the FIFO underrun interrupt was enabled). Note: If the memory used to store the framebuffer is also used for other application purposes, it may impact the graphical performances of the system.

Check if the used display resolution fits the hardware configuration

The general method for checking whether a display size with a particular color depth is compatible with memory bandwidth includes the following steps:

1. Compute the pixel clock according to the display size or extract it from the display datasheet.
2. Check if the display pixel clock does not exceed the maximum system-supported pixel clock described in Table 10 to Table 16. The following parameters must be used to extract from Table 10 or Table 16 the maximum-supported pixel clock corresponding to the used hardware configuration:
   – Number of used LTDC layers.
   – Used system clock speed HCLK and framebuffer memory speed.
   – External framebuffer memory bus width.
   – Number of AHB masters accessing concurrently to external framebuffer memory.
3. The user must perform some tests to confirm the hardware compatibility with the desired display size and color depth. To do it, the user must monitor the LTDC FIFO underrun interrupt flag in the LTDC_ISR register. If the FIFO underrun interrupt flag is always reset, then the user confirms that the desired display size is compatible with the hardware configuration.
   If the FIFO underrun flag is set, the user must check the following points:
   a. Verify if the correct maximum pixel clock is extracted, from Table 10 or Table 16, corresponding to the right hardware (mistake example: 16-bit SDRAM but extracted pixel clock corresponding to a 32-bit SDRAM).
   b. The color framebuffer line width is not 64/128 bytes (for AHB/AXI) aligned (see Section 5.5.2: Optimizing the LTDC framebuffer fetching from external memories (SDRAM or SRAM)).
   c. For the STM32F7 and STM32H7 devices, the MPU is not correctly configured to avoid Cortex®-M7 speculative read accesses to the external memory (see Section 5.6: Special recommendations for Cortex-M7 (STM32F7/H7)).
   d. If the FIFO underrun is still set because there are more than two AHB masters concurrent access to the external memory, the user must relax the memory bandwidth using the below recommendations:
      ◦ Use only one LTDC layer.
      ◦ Use the largest possible memory bus width (32-bit instead of 16- or 8-bit SDRAM/SRAM).
      ◦ Update the framebuffer content during the blanking period when the LTDC is not fetching.
      ◦ Use the highest possible system clock HCLK and the highest memory speed.
      ◦ Decrease the images color depth (bpp).
      For more details on memory bandwidth optimization, see Section 5.5: Graphic performance optimization.

Note: To evaluate the STM32 graphical capability in a specific hardware configuration, the user can use the STM32 boards described in Table 24. STM32 reference boards embedding LTDC and featuring an on-board LCD-TFT panel.

Figure 23 shows a typical graphic hardware configuration where an external SDRAM is connected to the FMC that is used for framebuffer. The SDRAM memory bandwidth depends on the bus width and in the operating clock.

The SDRAM bus width can be 32-bit, 16-bit, or 8-bit, while the operating clock depends on the system clock HCLK and the configured prescaler (HCLK/2 or HCLK/3).

Figure 23. Typical graphic hardware configuration with external SDRAM

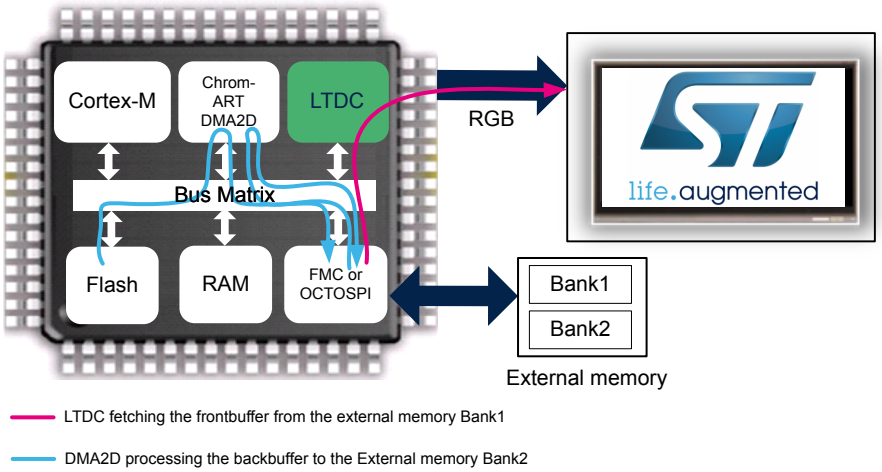


Table 10, Table 11, Table 12, Table 13, Table 14, Table 15, Table 16, and Table 17 list the maximal supported pixel clock at system level for various STM32 MCUs.

Table 10. STM32F4x9 maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock (MHz)(1)			
		LTDC(2)		LTDC + DMA2D(3)	
		FMC			
		SDRAM 16-bit	SDRAM 32-bit	SDRAM 16-bit	SDRAM 32-bit
1 layer	32	38	67	22	35
	24	51	83	30	47
	16	76	83	45	70
	8	83	83	83	83
2 layers	32/32	19	33	NA	18
	32/24	22	38	13	21
	32/16	25	44	15	25
	32/8	30	53	19	30
	24/24	26	44	15	24
	24/16	31	53	18	30
	24/8	38	67	23	38
	16/16	39	67	22	37
	16/8	51	83	31	50
	8/8	78	83	46	74

1. *System clock HCLK = 180 MHz, SDRAM runs at 90 MHz.*
2. *LTDC fetches the front buffer from the external memory. Either only one LTDC layer or two layers are used. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
3. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Table 11. STM32F7x6/7/8/9 maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock (MHz)(1)			
		LTDC(2)		LTDC + DMA2D(3)	
		fmc			
		SDRAM 16-bit	SDRAM 32-bit	SDRAM 16-bit	SDRAM 32-bit
1 layer	32	42	74	25	39
	24	56	83	34	52
	16	83	83	51	78
	8	83	83	83	83
2 layers	32/32	21	37	12	20
	32/24	24	42	14	23
	32/16	28	49	17	28
	32/8	34	59	21	34
	24/24	29	49	17	27
	24/16	34	59	20	33
	24/8	42	74	26	42
	16/16	43	74	25	41
	16/8	57	83	34	56
	8/8	83	83	51	82

1. *System clock HCLK = 200 MHz, SDRAM runs at 100 MHz.*
2. *LTDC fetches the front buffer from the external memory. Either only one LTDC layer or two layers are used. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
3. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Table 12. STM32H742/43/45/47/53/55/57 and STM32H750 maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock(1)			
		LTDC(2)		LTDC + DMA2D(3)	
		FMC			
		SDRAM 16-bit	SDRAM 32-bit	SDRAM 16-bit	SDRAM 32-bit
1 layer	32	49	93	29	48
	24	66	124	38	64
	16	99	150	58	96
	8	150	150	116	150

1. *System clock HCLK = 240 MHz, SDRAM runs at 110 MHz.*
2. *LTDC fetches the front buffer from the external memory. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
3. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Table 13. STM32H7R7/7S7 maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock(1)							
		LTDC(2)				LTDC + DMA2D(3)			
		XSPI		FMC		XSPI		FMC	
		8-bit PSRAM DDR	16-bit PSRAM DDR	SDRAM 16-bit	SDRAM 32-bit	8-bit PSRAM DDR	16-bit PSRAM DDR	SDRAM 16-bit	SDRAM 32-bit
1 layer	32	89	90	48	90	35	61	28	48
	24	90	90	64	90	46	83	36	60
	16	90	90	90	90	69	90	56	90
	8	90	90	90	90	90	90	90	90

1. *System clock HCLK = 300 MHz, PSRAM runs at 200MHz, SDRAM runs at 100 MHz*
2. *LTDC fetches the front buffer from the external memory. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
3. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Table 14. STM32H7A3/B3 and STM32H7B0 maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock(1)					
		LTDC(2)			LTDC + DMA2D(3)		
		OCTOSPI	FMC		OCTOSPI	FMC	
		HyperRAM™ 8-bit DDR	SDRAM 16-bit	SDRAM 32-bit	HyperRAM™ 8-bit DDR	SDRAM 16-bit	SDRAM 32-bit
1 layer	32	52	52	97	22	30	50
	24	70	70	130	29	40	66
	16	105	105	140	44	60	100
	8	140	140	140	89	121	140

1. *System clock HCLK = 280 MHz, SDRAM/HyperRAM run at 110 MHz.*
2. *LTDC fetches the front buffer from the external memory. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
3. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Table 15. STM32L4+ maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock(1)	
		LTDCX(2)	LTDC + DMA2D(3)
		FSMC	
		SRAM 16-bit	
1 layer	32	11	-
	24	15	10
	16	23	15
	8	47	31

1. *System clock HCLK = 120 MHz, SRAM is asynchronous.*
2. *LTDC fetches the front buffer from the external memory. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
3. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Table 16. STM32L4P/Q maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock(1)	
		LTDC(2)	LTDC + DMA2D(3)
		OCTOSPI	
		8-bit PSRAM DDR	
1 layer	32	27	11
	24	37	15
	16	55	23
	8	60	46

1. *System clock HCLK = 120 MHz, PSRAM runs at 60 MHz.*
2. *LTDC fetches the front buffer from the external memory. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
3. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Note: Decreasing the system clock (HCLK then LTDC) leads to a degradation of graphic performances

Table 17. STM32U59/A/F/G maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock(1)(2)	
		LTDC(3)	LTDC + DMA2D(4)
		OCTOSPI	
		16-bit PSRAM DDR	
1 layer	32	116	42
	24	116	48
	16	116	71
	8	116	116

1. *System clock HCLK = 160 MHz, PSRAM memory runs at 160 MHz.*
2. *Limited by LTDC maximum output clock frequency, refer to the relevant product datasheet.*
3. *LTDC fetches the front buffer from the external memory. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*
4. *LTDC fetches the front buffer from the external memory while the DMA2D transfers data from backbuffer to frontbuffer.*

Table 18. STM32N6x5/6x7 maximal supported pixel clock

Used LTDC layers	Color depth (bpp)	Maximum pixel clock(1)	
		LTDC(2)	
		XSPI	
		8-bit PSRAM DDR	16-bit PSRAM DDR
1 layer	32	88	88
	24	88	88
	16	88	88
	8	88	88

1. *System clock HCLK = 400 MHz, PSRAM runs at 200 MHz*
2. *LTDC fetches the front buffer from the external memory. The LTDC layer color depth is 8, 16, 24, or 32 bpp.*

Note: For STM32N6x5/6x7 devices, the AXI QOS is set to maximum for LTDC. As a consequence, the maximal supported pixel clock is the same for both LTDC and LTDC+DMA2D tests. The values are limited by the LTDC Kernel clock at 88 MHz.

Example of supported display resolutions for STM32F4x9 and STM32F7x6/7/8/9

Table 19 lists an example of some standard and custom display sizes supported by the STM32F4x9 and STM32F7x6/7/8/9, in the following conditions:

- For STM32F4x9, the system clock HCLK runs @ 180 MHz and the SDRAM @ 90 MHz.
- For STM32F7x6/7/8/9, the system clock HCLK runs @ 200 MHz and the SDRAM @ 100 MHz.
- Only one LTDC layer is used.
- Two AHB masters concurrent access to the SDRAM (LTDC + DMA2D).

Table 19. Example of supported display resolutions in specific STM32 hardware configurations

<table>
<tr><th colspan="4">Display characteristics</th><th colspan="2">STM32 LTDC configuration</th></tr>
<tr><th rowspan="2">Resolution</th><th rowspan="2">Refresh rate (Hz)</th><th rowspan="2">Pixel clock (MHz)</th><th rowspan="2">Display standard</th><th colspan="2">Color depth</th></tr>
<tr><th>SDRAM 16-bit</th><th>SDRAM 32-bit</th></tr>
<tr><td>320 x 240 (QVGA)</td><td rowspan="7">60</td><td>5.6</td><td rowspan="2">Custom</td><td colspan="2" rowspan="2">Up to 32 bpp</td></tr>
<tr><td>480 x 272</td><td>9.5</td></tr>
<tr><td>640 x 480 (VGA)</td><td>25.175</td><td>Industry standard</td><td>Up to 24 bpp</td><td>Up to 32 bpp</td></tr>
<tr><td>800 x 600 (SVGA)</td><td>40.000</td><td rowspan="2">VESA guidelines(1)</td><td>Up to 16 bpp</td><td>Up to 24 bpp</td></tr>
<tr><td>1024 x 768 (XGA)</td><td>65</td><td rowspan="3">8 bpp</td><td rowspan="2">Up to 16 bpp</td></tr>
<tr><td>1280 x 768</td><td>68.250</td><td>CVT R.B(2)</td></tr>
<tr><td>1280 x 720 (HD)</td><td rowspan="2">74.25</td><td rowspan="2">CEA(3)</td><td rowspan="2">Up to 16 bpp(4)</td></tr>
<tr><td>1920 x1080</td><td>30</td></tr>
</table>

1. *VESA (video electronics standards association) is a technical standards organization for computer display standards providing display monitor timing (DMT) standards.*
2. *CVT R.B: coordinated video timings reduced blanking standard by VESA.*
3. *CEA = consumer electronics association.*
4. *Up to 8 bpp for the STM32F4x9 microcontrollers.*

5.2.3 Check the compatibility of the display panel interface with the LTDC

The user must choose the LCD panel depending on the application needs. The two main factors to consider when choosing the LCD panel are the resolution and the color depth. These two factors have a direct impact on the following parameters:

- required GPIO number
- framebuffer size and location
- pixel clock of the display

When selecting a display panel, the user must:

- Ensure that the display interface is compatible with the LTDC (parallel RGB with control signals).
- Check if the control signals can be controlled by the LTDC (additional GPIOs are sometimes needed).
- Ensure that the display signal levels are matching the LTDC interface signal levels (VDD from 1.8 V to 3.6 V).
- Ensure that the display pixel clock is supported by the LTDC maximum pixel clock defined in the relevant STM32 product datasheet.
- Verify that the display timings parameters are supported by the LTDC timings (see Table 6).
- Check that the display size and color depth are supported by the LTDC (refer to Section 5.2.2: Checking display compatibility considering the memory bandwidth requirements).

5.3 STM32 package selection guide

At this stage of the graphical application development, the user already determined the application requirements in terms of GPIOs:

- whether an external memory is needed and which is the bus width

- which LTDC configuration to use: RGB565, RGB666, or RGB888

When selecting the STM32 package, the user has to consider the RGB interfaces availabilityand the application requirements in terms of GPIOs number. The user must refer to the STM32 product datasheet to get the available packages with GPIOs.

An easy way to check if the STM32 package in which the user is interested matches the application needs in term of GPIO number, is to use STM32CubeMX (the pinout tab).

Table 20 summarizes the available packages and RGB interface of some STM32 MCUs embedding an LTDC.

Table 20. STM32 packages with LTDC peripheral versus RGB interface availability

Cells with “NA” = the package is not available for that specific product.
Cells with "-" = the package is available without RGBXXX outputs options.
Cells with “18” value = only RGB565 and RGB666 parallel outputs are supported.
Cells with “24” value = all of RGB565, RGB666, and RGB888 outputs are supported.

Product	LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176	LQFP176	LQFP208	TFBGA216	WLCSP143	WLCSP168	WLCSP180	WLCSP101	VQN68	UFBGA144	TFBGA225	VFBGA142	VFBGA169	VFBGA178	VFBGA198	VFBGA223
VFBGA264STM32F429/439	18	NA	18	24	24	24	24	24	18	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
STM32F469/479(1)	18	NA	18	24	24	24	24	24	NA	24	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
STM32F7x6	18	18	24	NA	24	24	24	24	24	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
STM32F7x7	18	NA	24	NA	24	24	24	24	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA
STM32F7x8(1)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	24	NA	NA	NA	NA	NA	NA	NA	NA	NA
STM32F7x9(1)	NA	NA	NA	NA	NA	24	24	24	NA	NA	24	NA	NA	NA	NA	NA	NA	NA	NA	NA
STM32H7R7/7S7	-	-	-	-	24	24 (UFBGA176 + 25)	24	NA	NA	NA	NA	-	-	18	24	NA	NA	NA	NA	NA
STM32N647xx	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	24	24	24	24	24	24

1. *The integrated MIPI-DSI controller allows easier PCB design with fewer pins. Refer to the document [3] for more details on STM32 MIPI-DSI host.*

5.4 LTDC synchronization with DMA2D and CPU

5.4.1 DMA2D usage

The DMA2D is a master on the AHB bus matrix performing graphical data transfers inter-memories. It is recommended to use the DMA2D in order to offload the CPU.

The DMA2D implements four basic tasks:

- Fill a rectangular shape with a unique color.
- Copy a frame or a rectangular part of a frame from a memory to another.
- Convert the pixel format of a frame or a rectangular part of a frame while transferring it from one memory to another memory.
- Blend two images with different sizes and pixel format and store the resulting image in one resulting memory.

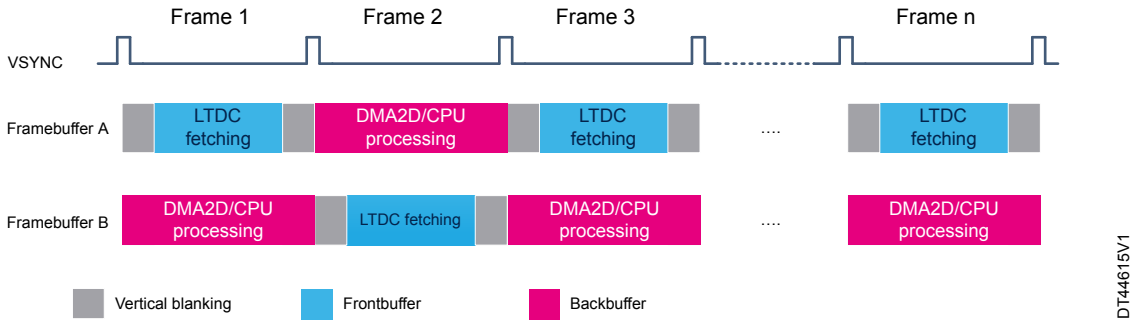
5.4.2 LTDC and DMA2D/CPU synchronization

When only one framebuffer is used, there is a risk that the framebuffer computation is displayed on the screen. Multiple buffering techniques, such as the double buffering, are commonly used to avoid displaying the framebuffer calculation on the screen.

Even when using a double-buffering technique, a tearing effect may appear due to a nonsynchronization between the LTDC and the framebuffer update (either by the CPU or the DMA2D). A way to solve this issue is the use of the VSYNC signal to synchronize the workflow of these two masters (LTDC and either CPU or DMA2D).

The LTDC fetches the graphical data from a buffer (called frontbuffer) while the DMA2D prepares the next frame in another buffer (called backbuffer). The VSYNC period indicates the end of the actual frame display and that the two buffers needs to be flipped.

Figure 24. Double buffering: synchronizing LTDC with DMA2D or CPU



The LTDC provides different options to synchronize this workflow:

- Program the line interruption with the value of the last screen line. The interrupt handler must flip the framebuffers and start the next framebuffer calculation.
- Program the shadow reload register (LTDC_SRCR) to vertical blanking reload to change the LTDC framebuffer address on the VSYNC period, and poll on VSYNC bit of the LTDC_CDSR register to unblock the DMA2D.

5.5 Graphic performance optimization

As previously stated in this document, the framebuffer memory bandwidth is the most important parameter for a graphic application. This section provides some recommendations to optimize the graphic performances based on bandwidth optimizations of the framebuffer memory.

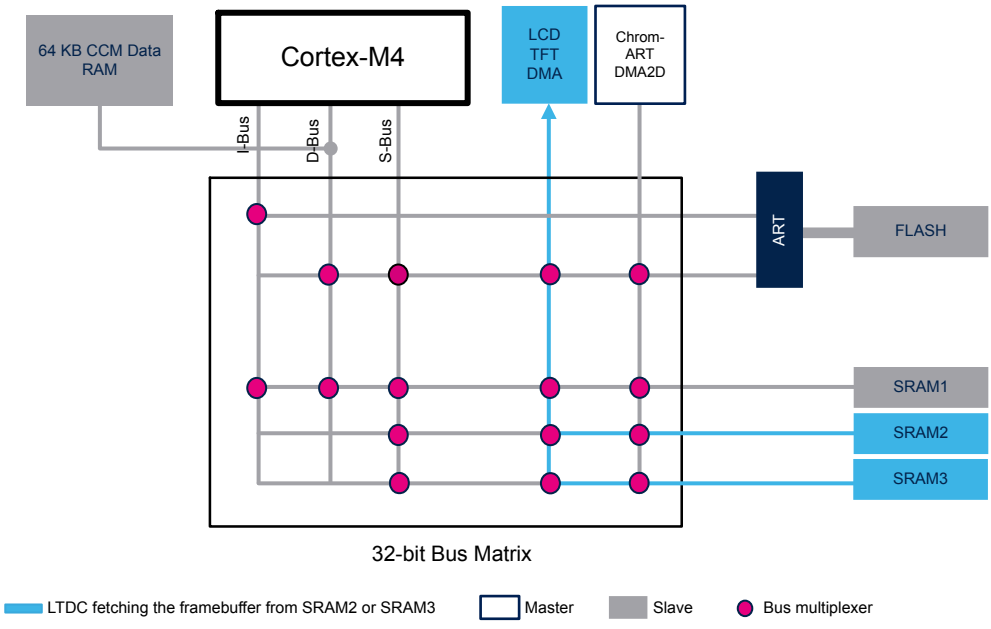
5.5.1 Memory allocation

The smart architecture of the STM32 MCUs enables a significant system performance gain when using the internal SRAM memory, split into two or more slaves.

Splitting up the slaves memories between masters helps to decrease the competition between them when they access simultaneously the same SRAM. This action also creates an additional system bus bandwidth.

As shown in the example described in Figure 25, SRAM2 and SRAM3 are dedicated to graphics for the framebuffer while the SRAM1 is used by the CPU.

Figure 25. Example of taking advantage from memory slaves split on STM32F4x9



5.5.2 Optimizing the LTDC framebuffer fetching from external memories (SDRAM or SRAM)

Another consideration related to the SDRAM/SRAM is the placement of the framebuffer and the line length data size. Since the AHB bus matrix prohibits a memory burst access that crosses the 1-Kbyte boundary, and as the LTDC performs burst read of 64/128 bytes (for AHB/AXI), placing the content of the framebuffer in an address at the edge of 1 Kbyte splits the burst read into single accesses, which can heavily affect the graphical performances.

The same problem can occur when thedata size of one line of pixels is not a multiple of 64/128 bytes (for AHB/AXI). Under these conditions and after a number of accesses, the LTDC read burst crosses the 1-Kbyte boundary that splits the burst read into single accesses.

As a consequence, when the LTDC does not generate a burst, each access is interrupted by a CPU or another master access (such as Chrom-Art Accelerator or Ethernet).

These interruptions highly reduce the LTDC bandwidth on a high-latency memory like the external SDRAM that leads to an underrun.

To solve the issue described above, the user may choose a color depth that does not lead to the described issue, or use one of the two following methods:

- Reduce the layer window and the framebuffer line widths.
- Add a number of dummy bytes at the end of every line of pixels to match the closest frame line width multiple of 64/128 bytes (for AHB/AXI).

Example: 480 x 272 display with 24 bpp

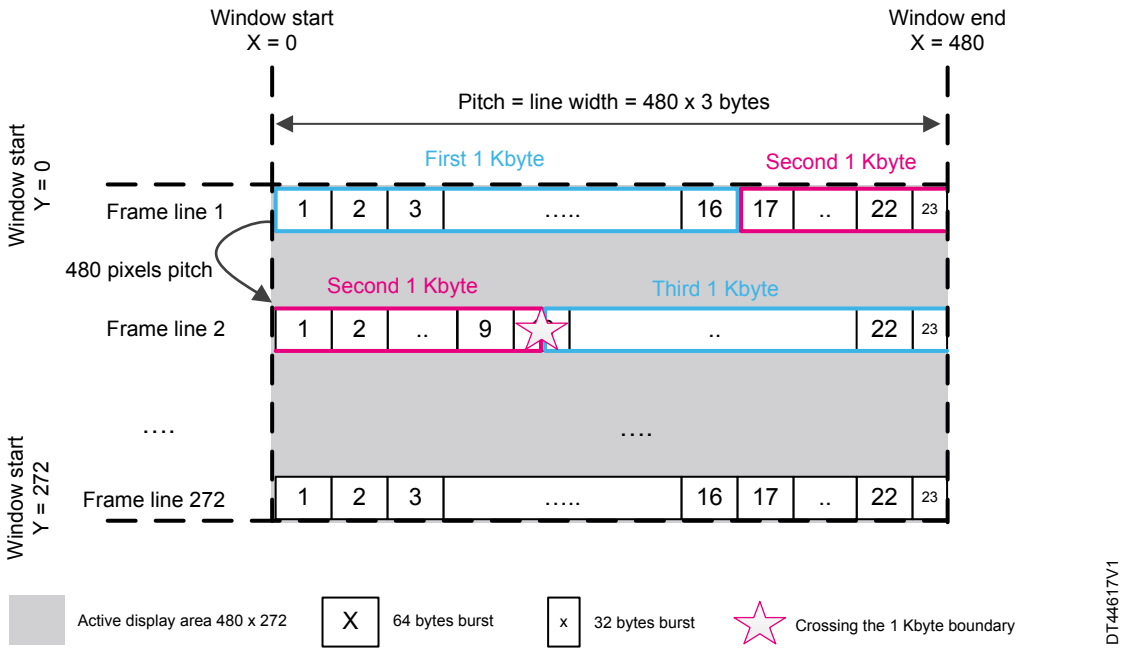
For a 480 x 272 display (the frame line width is 480 pixels) and with a 24 bpp color depth, the line width size is equal to 1440 bytes that is not a multiple of 64/128 bytes (for AHB/AXI).

Note: For that resolution, to have a multiple line width size of 64/128 bytes (for AHB/AXI), the user can use another color depth such as RGB565.

Since the frame line is composed of 22 bursts of 64/128 bytes (for AHB/AXI) and one 32 bytes burst, the 10th burst of the second line of the frame crosses the 1-Kbyte boundary. This leads to the split of the read operation into single accesses.

Figure 26 illustrates the 1-Kbyte boundary cross problem for the given example.

Figure 26. Burst access crossing the 1-Kbyte boundary

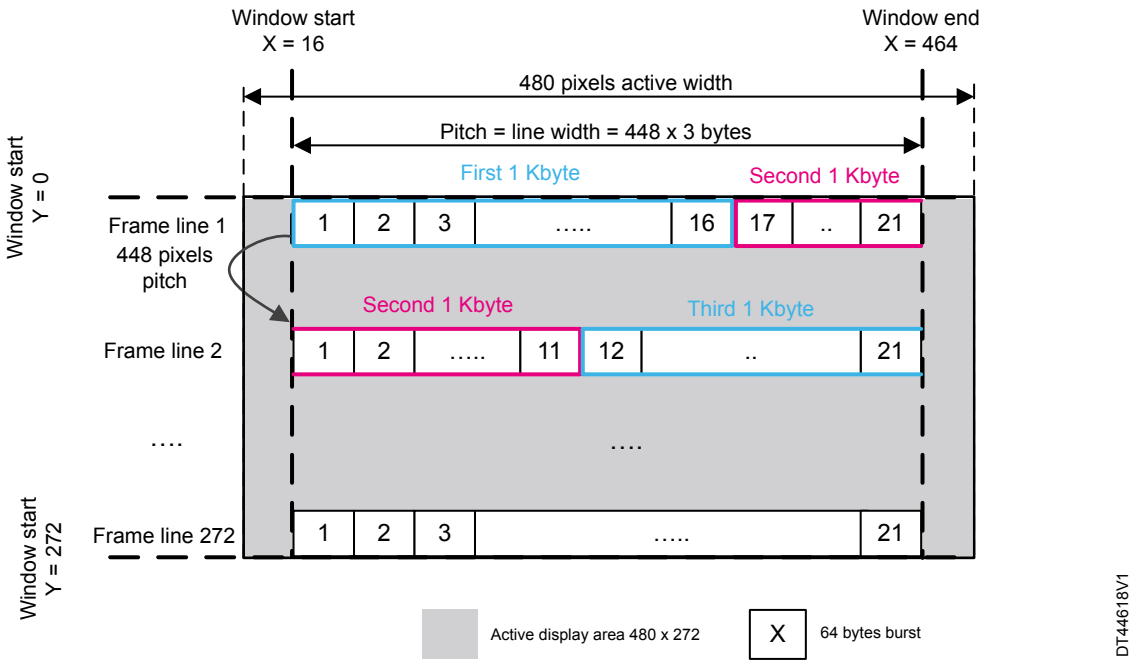


For this example, the two methods to solve the crossing 1-Kbyte boundary issue are detailed below:

- First method
  Reduce the layer window and the framebuffer line widths: use the LTDC layer windowing feature by reducing the window size to match the closest frame line width multiple of 64/128 bytes (for AHB/AXI). Since the window width is reduced, the framebuffer size must also be reduced since the extra 22 and 23 bursts for all frame lines are not fetched nor displayed by LTDC.
  This method solves the 1-Kbyte boundary crossing issue with a slight window width decrease (see Figure 27).
  The code below is based on the HAL drivers and shows an example of setting the pitch as described in Figure 27:

```
/* Setting the Layer1 window to 448x272 at positions X = 16 and Y = 0 */
    pLayerCfg.WindowX0 = 16;
    pLayerCfg.WindowX1 = 464;
    pLayerCfg.WindowY0 = 0;
    pLayerCfg.WindowY1 = 272;
    pLayerCfg.PixelFormat = LTDC_PIXEL_FORMAT_RGB888;
    pLayerCfg.Alpha = 255;
    pLayerCfg.Alpha0 = 0;
    pLayerCfg.BlendingFactor1 = LTDC_BLENDING_FACTOR1_PAxCA;
    pLayerCfg.BlendingFactor2 = LTDC_BLENDING_FACTOR1_PAxCA;
/* Framebuffer start address: LTDC fetches the image directly from internal flash that the re
al image width is 448 pixels. Only the 448 pixels width is displayed*/
    pLayerCfg.FBStartAdress = (uint32_t)&image_data_Image_RGB888_448x272;
    pLayerCfg.ImageWidth = 448;
    pLayerCfg.ImageHeight = 272;
    pLayerCfg.Backcolor.Blue = 0;
    pLayerCfg.Backcolor.Green = 0;
    pLayerCfg.Backcolor.Red = 0;
    if (HAL_LTDC_ConfigLayer(&hltdc, &pLayerCfg, 0) != HAL_OK)
    {
        Error_Handler();
    }
```

Figure 27. Reducing layer window and framebuffer line widths

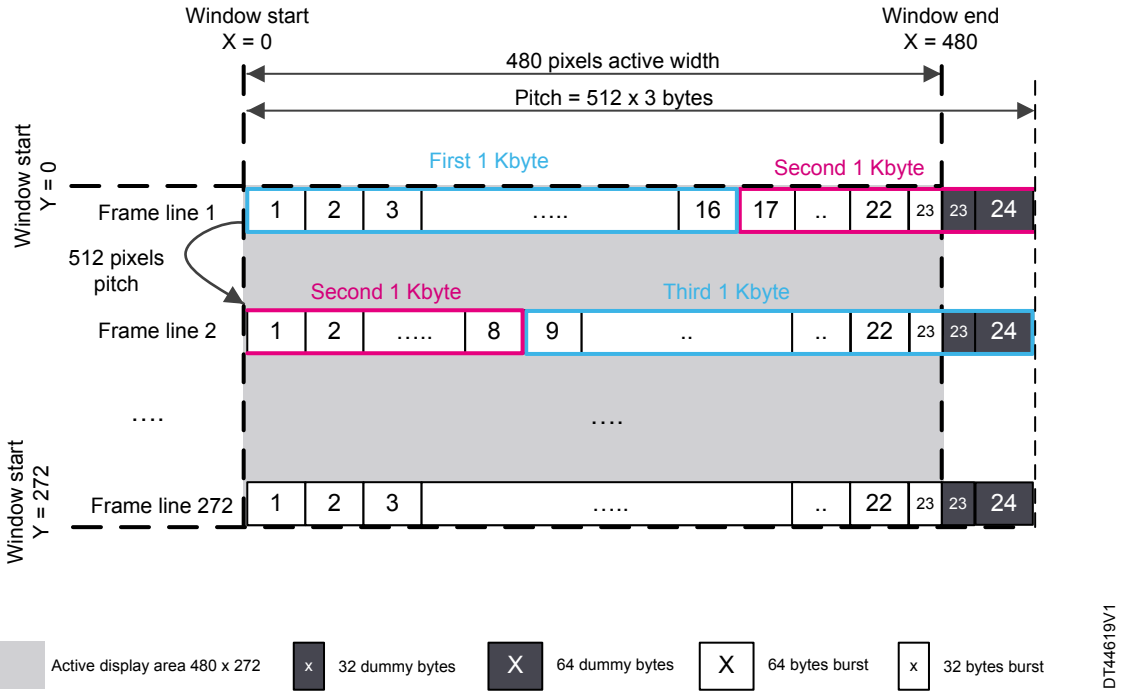


- Second method
  Add a number of dummy bytes at the end of every line of pixels to match the closest frame line width multiple of 64/128 bytes (for AHB/AXI). This can be done using the LTDC layer pitch (see Section 4.3: Two programmable LTDC layers). To do this, the user must consider the two points below:
  – The framebuffer must contain the dummy bytes (as described in Figure 28):when writing data into the framebuffer, it can be done by programming an output offset of the DMA2D equal to the difference between the closest burst multiple and the actual line length data size.
  – The LTDC line length must always be equal to the active data size, but, the LTDC pitch must be programmed with the value of the closest bytes number multiple of 64/128 bytes (for AHB/AXI).

  The `HAL_LTDC_SetPitch` function provided under the hal_ltdc driver can be used to program the desired pitch value in number of pixels. For the previous example, the value of the pitch to pass to this function must be equal to 512 (512 is the number of pixels per line corresponding to a line length size of 1536 bytes that is multiple of 64/128 bytes (for AHB/AXI).
  The code below is based on the HAL drivers and shows an example of setting the pitch as described in Figure 28:

```
/* Setting the Layer1 window to 480x272 at positions X = 0 and Y = 0 */
    pLayerCfg.WindowX0 = 0;
    pLayerCfg.WindowX1 = 480;
    pLayerCfg.WindowY0 = 0;
    pLayerCfg.WindowY1 = 272;
    pLayerCfg.PixelFormat = LTDC_PIXEL_FORMAT_RGB888;
    pLayerCfg.Alpha = 255;
    pLayerCfg.Alpha0 = 0;
    pLayerCfg.BlendingFactor1 = LTDC_BLENDING_FACTOR1_PAxCA;
    pLayerCfg.BlendingFactor2 = LTDC_BLENDING_FACTOR1_PAxCA;
/* Framebuffer start address: LTDC fetches the image directly from internal flash that the re
al image width is 480 pixels but additional 32 pixels are added to each line to get a 512 pix
els pitch.
Only the 480 pixels width is displayed*/
    pLayerCfg.FBStartAdress = (uint32_t)&image_data_Image_RGB888_512x272;
    pLayerCfg.ImageWidth = 480;
    pLayerCfg.ImageHeight = 272;
    pLayerCfg.Backcolor.Blue = 0;
    pLayerCfg.Backcolor.Green = 0;
    pLayerCfg.Backcolor.Red = 0;
    if (HAL_LTDC_ConfigLayer(&hltdc, &pLayerCfg, 0) != HAL_OK)
    {
        Error_Handler();
    }
/* Sets the Layer1 (index 0 refers to Layer1) Pitch to 512 pixels */
    HAL_LTDC_SetPitch(&hltdc, 512, 0);
```

Figure 28. Adding dummy bytes to make the line width multiple of 64 bytes



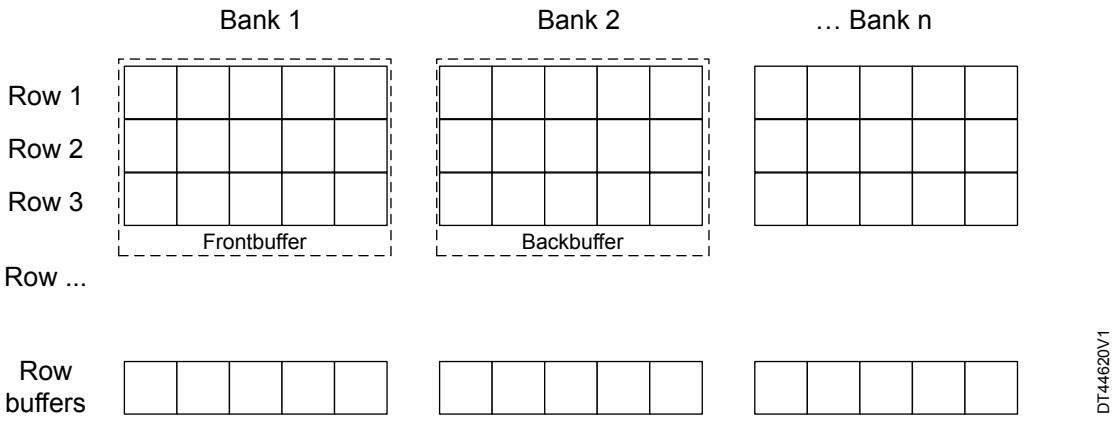
5.5.3 Optimizing the LTDC framebuffer fetching from SDRAM

Making random access into a bank generates some precharge cycles that increase the SDRAM latency seen by the LTDC. As the LTDC performs sequential accesses, it is important that no other masters access the same SDRAM bank.

The external SDRAM is composed of multiple banks. Given that, making random accesses on a bank generates some precharge and activates some cycles. The framebuffer must be placed in an independent bank accessed only by the LTDC. This action reduces the external memory latency and leads to a higher throughput. As a consequence, when the double-framebuffer technique is used, it is recommended to have these buffers in two separate banks.

This can be done by storing the frontbuffer in the first address of the SDRAM and addressing the backbuffer by adding an offset with the size of one bank.

Figure 29. Placing the two buffers in independent SDRAM banks



For instance, when the SDRAM bank size is equal to 4 Mbytes, the following line code can be used:

```
/* Framebuffer addresses within external SDRAM */
/* Frontbuffer in bank 1 of SDRAM memory */
uint32_t FrontBuffer = LCD_FB_START_ADRESS;
/* Backbuffer in the bank 2 of SDRAM memory */
uint32_t BackBuffer = LCD_FB_START_ADRESS + 1024 * 1024 * 4;
```

SDRAMRBURST

Another interesting feature allowing optimization of reading performances from the SDRAM is the use of RBURST.

The SDRAM controller adds a cacheable read FIFO with a depth of six 32-bit lines. The read FIFO is used when the read burst is enabled and allows the next read accesses to be anticipated during CAS latencies.

5.5.4 Framebuffer content update during blanking period

A way to optimize graphic performance (especially when the performance bottleneck is the framebuffer memory bandwidth), is to update the framebuffer content during the blanking period. Since, in this period, the LTDC does not fetch any pixel data from the framebuffer, the bus bandwidth is relaxed and the framebuffer update can be performed.

5.6 Special recommendations for Cortex-M7 (STM32F7/H7)

This section illustrates some recommendations for the STM32F7/H7 devices embedding the Cortex-M7 CPU.

These recommendations are specific to the Cortex-M7 since it has the following particularities compared to the Cortex-M4:

- The Cortex-M7 does some speculative read accesses to normal memory regions.
  These speculative read accesses may cause high latency or system errors when performed on external memories over FMC, Quad-SPI or Octo-SPI. This impacts AHB/AXI masters (such as LTDC) accessing the FMC, Quad-SPI or Octo-SPI, and particularly decreases graphical performances and may lead to system errors (if the LTDC framebuffer is located in external memory and/or if the Quad-SPI memory is used for graphics).
- The Cortex-M7 CPU embeds an L1-Cache (see Figure 10).
  Some graphic issues may be encountered due to unsuitable cache settings. Bad graphic visual effects may occur if cache maintenance is not properly performed. If the suitable cache maintenance method is not used, graphical performances may be impacted.

5.6.1 Disable FMC Bank1 if not used

After reset, the FMC Bank1 is always enabled to allow boot into external memories. Since the CortexM7 does some speculations, it can generate a speculative read access to the first FMC bank.

The default FMC configuration being very slow, this speculative access blocks the access to the FMC by other AHB masters for a very long time, leading to underrun on the LTDC side.

To prevent CPU speculative read accesses on FMC Bank1, it is recommended to disable it when it is not used. This can be done by resetting the MBKEN Bit in FMC_BCR1 register that is, by default, enabled after reset.

To disable the FMC Bank1, the following code can be used in STM32F7 series:

```
/* Disabling FMC Bank1: After reset FMC_BCR1 = 0x000030DB where MBKEN = 1b meaning that FMC_B
ank1 is enabled
and MTYP[1:0]= 10 meaning that memory type is set to NOR Flash/OneNAND Flash*/
FMC_Bank1->BTCR[0] = 0x000030D2;
```

For more details on FMC configuration, refer to the STM32 product reference manual.

5.6.2 Configure the memory protection unit (MPU)

This section defines the STM32F7/H7 system memory attributes and the basic MPU concepts. It also describes how to configure the MPU in order to prevent graphical performance issues related to the Cortex-M7 speculative read accesses and cache maintenance.

Note: This section only describes some necessary basic MPU concepts needed for configuration.

For further details on MPU and cache, refer to the documents [6], [7], [8], and the Arm Cortex-M7 technical reference manual.

MPU attributes configuration

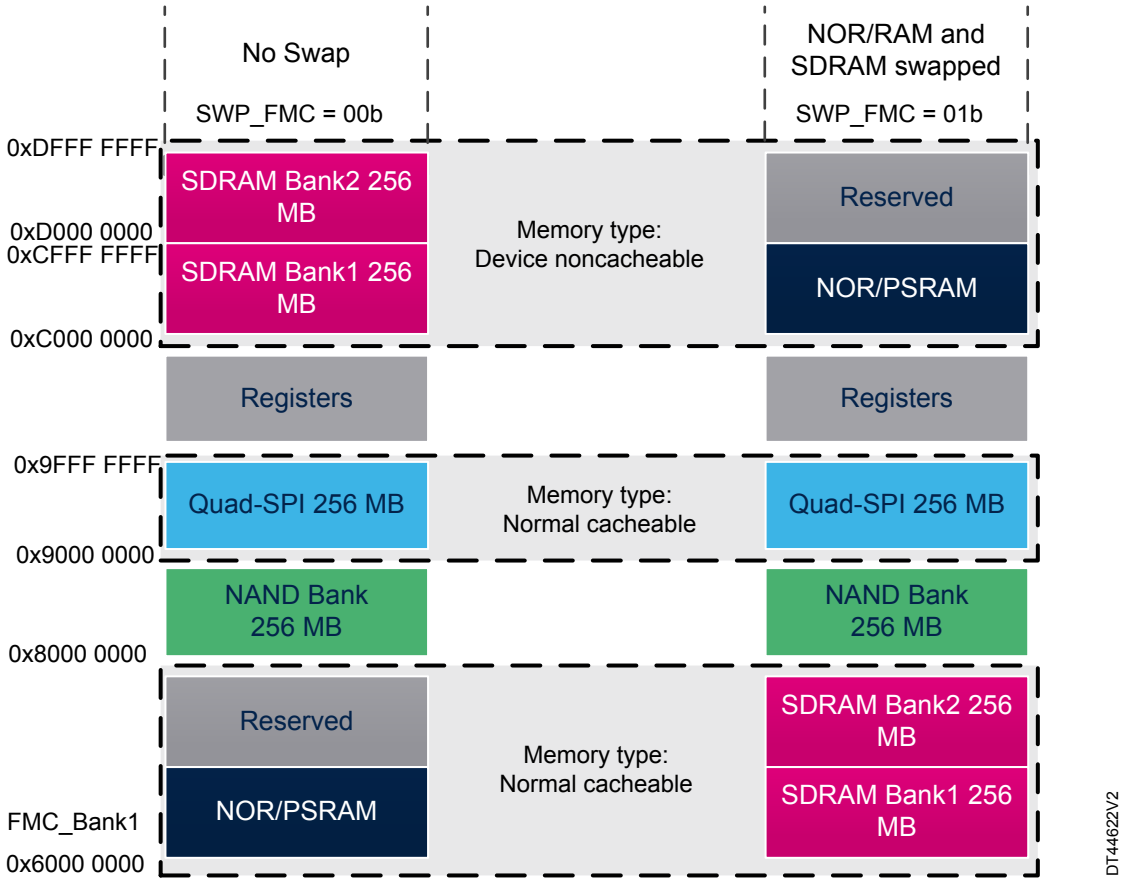
In order to prevent graphic performance issues related to the Cortex-M7 speculative read accesses, the user must review all the memory map of the application and configure the MPU according to the hardware. So, the user has to set the following configurations:

- Define the framebuffer MPU region and the other application MPU regions.
- MPU must be configured according to the size of the memory used by the application.
- The MPU attributes of the unused regions must be configured to strongly ordered execute never (XN). For example, for the Quad-SPI, if an 8-Mbyte memory is connected, the remaining 248-Mbyte unused space (from a total 256-Mbyte addressable space) must be set to strongly ordered XN. See example in Section 7.2.7.
- Prevent the Cortex-M7 speculative read accesses to the external SDRAM/SRAM (if the FMC swap is enabled, see Figure 30). To do it, the SDRAM/SRAM MPU region must be set to execute never (XN).
- If the Cortex-M7 CPU is used for framebuffer processing (writing to SDRAM/SRAM), the framebuffer region MPU attribute must be set to normal cacheable with read and write access permission.

Note: The framebuffer MPU region attribute must be set to execute never since it is only dedicated for graphical content creation.

Figure 30 describes the STM32F7 FMC banks and Quad-SPI MPU memory attributes at default system memory map

Figure 30. FMC SDRAM and NOR/PSRAM memory swap at default system memory map (MPU disabled)



MPU and cache policy configuration

The use of Cortex-M7 cache allows system and graphic performances to be boosted. This performance gain is especially seen when the CPU accesses external memories such as SDRAM or Quad-SPI.

In a graphical application, when the CPU is used for framebuffer processing, it is recommended to use the cache especially if the framebuffer is located in an external memory like SDRAM or SRAM. In that case, the user must consider the following points when using the cache:

- MPU memory region cacheability
  As previously illustrated in Figure 30, in the default system memory region MPU attributes, some system memory regions are normal cacheable while others are device noncacheable.
  When the CPU is used for framebuffer processing, the user must change the framebuffer region MPU attribute to normal cacheable (or do an FMC swap, see Figure 30).
- Cache maintenance and data coherency: visual impact of WBWA without cache maintenance operation
- The data coherency issue is often encountered when performing framebuffer processing using a Cortex-M7 CPU with L1-cache enabled and a WBWA cache policy. This issue occurs when multiple masters such as Cortex-M7 and LTDC share the same region (framebuffer) and the cache maintenance is not performed.
  When the CPU processes the framebuffer (writes to framebuffer), and if the framebuffer region has a write-back cache policy, the processed result (image to be displayed) is not seen on the framebuffer (may be SRAM or SDRAM), and then it is not displayed.
  To avoid this issue, the following methods can be used:
  – Configure the framebuffer region cache attribute to write-through (WT). In that case, each write operation is performed on the cache and on the framebuffer.

Note: For some products, there is a limitation with the write-through policy. Use the write-back policy as stated in the second method. For more details about this limitation, refer to the product related errata sheet.

  – Configure the framebuffer region cache attribute to write back write allocate (WBWA) and perform the cache maintenance by software.

  Write-through is safer for data coherency but may impact graphic performances.
- Cache maintenance may impact graphic performances
  The suitable cache policy matching the application must be used. Each method has its cons and pros, so the user must consider the following particularities for each method:
  – Write-through is very simple to manage (no need to perform cache maintenance by software) and safer for data coherency but it generates a lot of single-write operations to the framebuffer, which may impact LTDC accesses.

Note: The user must also consider that cache maintenance may impact graphic performances even when the CPU is not used for framebuffer processing. Thus, in some applications, the CPU accesses the external SDRAM or SRAM for other purposes than graphics with cache enabled. In that case, cache maintenance may impact the LTDC accesses.

  – Write-back-write allocate: it is more suitable to use WBWA and software routine and to synchronize the cache maintenance operation with the LTDC during blanking. This allows an additional bandwidth creation on the framebuffer memory (SRAM or SDRAM). The cache maintenance operation need to be performed by software after writing data to the framebuffer memory region. This is done by forcing a D-cache clean operation using the CMSIS function `SCB_CleanDCache()`. So, all the dirty lines in the cache are written back to the framebuffer.

MPU configuration example

An example of MPU configuration is described in Section 7.2.7, showing how to set the framebuffer MPU attribute when the CPU is used (with cache enabled) for graphical operations. The described example is created for the STM32F746G-DISCO board hardware configuration, where the external SDRAM is used for framebuffer and the external Quad-SPI flash memory contains the graphic primitives.

5.7 LTDC peripheral configuration

This section describes the steps needed to configure the LTDC peripheral.

Note: It is recommended to reset the LTDC peripheral before starting the configuration and it is alsorecommended to guarantee that the peripheral is in reset state. The LTDC can be reset by setting the corresponding bit in the RCC_APB2RSTR register, which resets the three clock domains.

5.7.1 Display panel connection

The LTDC hardware interface provides eight bits per color bus, and fits perfectly for RGB888 true color panels. The LTDC hardware interface provides also timing signals: LCD_HSYNC, LCD_VSYNC, LCD_DE, and LCD_CLK.

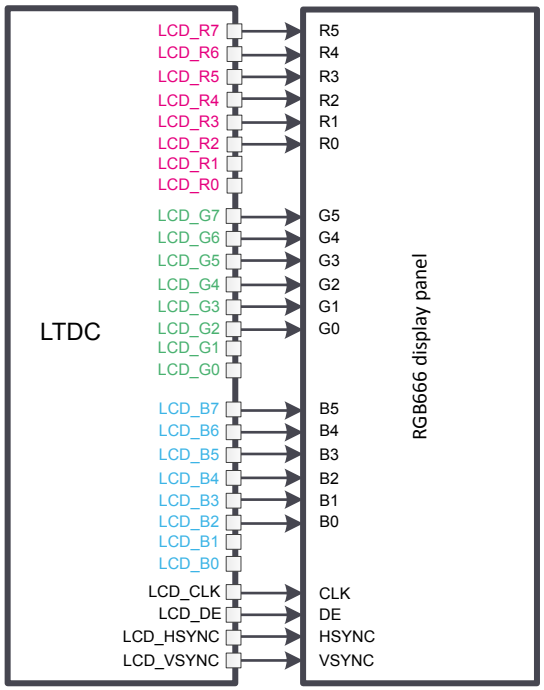
The LTDC GPIOs must be configured to the correspondent alternate function. For more details on LTDC alternate functions availability versus GPIOs, refer to the alternate function mapping table in the product datasheet.

Note: All GPIOs have to be configured in very-high-speed mode.

Connecting lower palette display panels

For display panels with a lower color palette (such as RGB666 and RGB565), the bus connection must be done with the most significant bits of the data signals. Figure 31 shows an example of connecting an RGB666 display panel.

Figure 31. Connecting an RGB666 display panel



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GPIOs configuration using STM32CubeMX tool

To connect a display panel to an STM32 MCU, the user must configure the GPIOs to be used for interfacing.

Using the STM32CubeMX tool is a very simple, easy, and rapid way to configure the LTDC peripheral and its GPIOs, since it allows a project to be generated with a preconfigured LTDC (see Section 7.2.3: LTDC GPIOs configuration).

Configuration of specific pins of a display module

Some display modules may need other signals to be fully functional. GPIOs and some peripherals can be used to control these signals.

An example of using GPIOs to control the *displayenable* pin (LCD_DISP) on a display panel is described in Section 7.2.3: LTDC GPIOs configuration.

Enabling LTDC interrupts

To be able to use the LTDC interrupts, the user must enable the LTDC global interrupts on the NVIC side. Then, each interrupt is enabled separately by enabling its corresponding enable bit. The LTDC interrupt-enable bits are available in the LTDC_IER register described in Table 7. LTDC interrupts summary.

Note: The FIFO underrun and transfer error interrupts are enabled in the hal_ltdc driver `HAL_LTDC_Init()` function

An example of enabling LTDC interrupts using STM32CubeMX is described in Section 7.2.3: LTDC GPIOs configuration

5.7.2 LTDC clocks and timings configuration

This section describes the steps needed to configure the LTDC clock and timings respecting the display specifications. It also provides a configuration example for the ROCKTECH (RK043FN48H) display embedded on the STM32F746G-DISCO board.

System clock configuration

It is recommended to use the highest system clock to get the best graphic performances. This recommendation applies also for the external memory framebuffer. So, if an external memory is used for the framebuffer, the highest allowed clock speed must be used to get the best memory bandwidth.

For instance, for the STM32F4x9, the maximum system speed is 180 MHz. So, if an external SDRAM is connected to the FMC, the maximum SDRAM clock is 90 MHz (HCLK/2).

For the STM32F7, the maximum system speed is 216 MHz but with this speed and HCLK/2 prescaler the SDRAM speed exceeds the maximum allowed speed (see product datasheet for more details). So, to get the maximum SDRAM, it is recommended to configure HCLK to 200 MHz, then the SDRAM speed is set to 100 MHz.

The clock configuration providing the highest performances is:

- STM32F4x9:HCLK @ 180 MHz and SDRAM @ 90 MHz
- STM32F7:HCLK @ 200 MHz and SDRAM @ 100 MHz

An example of LTDC configuration using STM32CubeMX is described in Section 7.2.4: LTDC peripheral configuration.

Pixel clock and timings configuration

At this stage of the graphical application development, the user must have already checked and confirmed that the desired display size and color depth are compatible with the hardware configuration. Therefore, the pixel clock to be configured must be already known, either extracted from the display datasheet or calculated (see Section 5.2.2: Checking display compatibility considering the memory bandwidth requirements).

Example: LTDC timings configuration for ROCKTECH RK043FN48H display embedded on the STM32F746G-DISCO board. At first, the user must extract the timing parameters from the display datasheet (see Table 21). It is recommended to use typical display timings.

Table 21. LCD-TFT timings extracted from ROCKTECH RK043FN48H datasheet

The cells in bold highlight the values used in the example presented below.

Item		Symbol	Min.	Typ.	Max.	Unit
DCLK frequency		Fclk	5	9	12	MHz
DCLK period		Tclk	83	110	200	ns
Hsync	Period time	Th	490	531	605	DCLK
	Display period	Thdisp	-	**480**	-	DCLK
	Back porch	Thbp	8	**43**	-	DCLK
	Front porch	Thfp	2	**8**	-	DCLK
	Pulse width	Thw	**1**	-	-	DCLK
Vsync	Period time	Tv	275	288	335	H
	Display period	Tvdisp	-	**272**	-	H
	Back porch	Tvbp	2	**12**	-	H
	Front porch	Tvfp	1	**4**	-	H
	Pulse width	Tvw	1	**10**	-	H

Based on the above table, the extracted timing parameters are:

- Display period (active width) = 480 pixels

- Back porch HBP = 43 pixels
- Front porch HFP = 8 pixels
- Pulse width HSYNC = 1 pixel (minimum value)
- Display period (active height) = 272 lines
- Vertical back porch VBP = 12 lines
- Front porch VFP = 4 lines
- Pulse width VSYNC = 10 lines

Program timing parameters: once timing parameters are extracted, they are used to program the LTDC timing registers, Table 22 summarizes all the parameters to be programmed.

Timing parameters configuration with STM32CubeMX: it is very easy to program the timing parameters using STM32CubeMX. The user must simply fill the extracted parameters in the LTDC configuration window (see section Section 7.2.4: LTDC peripheral configuration).

Table 22. Programming LTDC timing registers

Register		-	Value to be programmed
LTDC_SSCR	HSW[11:0]	HSYNC Width - 1	0
	VSH[11:0]	VSYNC Height - 1	9
LTDC_BPCR	AHBP[11:0]	HSYNC Width + HBP - 1	43
	AVBP[10:0]	VSYNC Height + VBP - 1	21
LTDC_AWCR	AAW[11:0]	HSYNC Width + HBP + Active Width - 1	523
	AAH[10:0]	VSYNC Height + BVBP + Active Height - 1	293
LTDC_TWCR	TOTALW[11:0]	HSYNC Width + HBP + Active Width + HFP - 1	531
	TOTALH[10:0]	VSYNC Height+ BVBP + Active Height + VFP - 1	297

Pixel clock configuration with STM32CubeMX: the pixel clock is calculated with a 60 Hz refresh rate as shown below:

LCD_CLK = TOTALW x TOTALH x refresh rate

Based on Table 22, *TOTALW= 531 and TOTALH = 297.*

And for this example:

LCD_CLK = 531 x 297 x 60 = 9.5 MHz

Refer to the LTDC pixel clock configuration STM32CubeMX example in Section 7.2.4.

LTDC control signals polarity configuration

The LTDC control signals (HSYNC, VSYNC, DE, and LCD_CLK) polarities must be configured respecting the display specifications.

Note: Only the DE control signal must be inverted versus the DE polarity indicated in the display datasheet. The other control signals must be configured exactly like the display datasheet.

5.7.3 LTDC layers configuration

This section describes the needed steps to configure the LTDC layers, respecting the display size and the color depth.

As previously stated in Section 4.3.2, the LTDC features two independently configurable layers (the user can enable either one or the two layers). By default, both layers are disabled, so only the configured background color is displayed (the default color is black).

The user can display Layer1 + background or display Layer1 + Layer2 + background.

Display only the background

If no layer are enabled, only the background is displayed. If the background color is not configured, the default background black color is displayed (LTDC_BCCR = 0x00000000).

To set a blue background color, the LTDC_BCCR register must be set to 0x000000FF.

Layer parameters configuration

Once LTDC GPIOs, clocks and timings are properly set, the user must configure the following LTDC layer parameters. Each LTDC layer has its own parameters that must be configured separately:

- window size and position
- pixel input format
- framebuffer start address
- framebuffer size (image width and image height) and pitch
- layer default color in ARGB8888 format
- layer constant alpha for blending
- layer blending factor1 and factor2

An example of LTDC layer parameters configuration using STM32CubeMX is described in LTDC Layer parameters configuration.

Note: All layer parameters can be modified on the fly, except for the CLUT. The new configuration has to be either reloaded immediately or during vertical blanking period by configuring the LTDC_SRCR register.

5.7.4 Display panel configuration

Some displays require to be configured using serial communication interfaces such as I^2C or SPI.

For instance, the STM32F429I-DISCO embeds the ILI9341 display module that is initialized through the SPI interface.

A dedicated driver for this display module (ili9341.c), including initialization and configuration commands, is available in the STM32Cube firmware package under:`STM32Cube_FW_F4_Vx.xx.x\Drivers\BSP\Components\ili9341`

An example of display initialization sequence based on the ili9341_Init() function is included in the STM32Cube examples for the STM32F429I-Discovery board under:`STM32Cube_FW_F4_Vx.xx.x\Projects\STM32F429I-Discovery\Examples\LTDC\LTDC_Display_2Layers`

5.8 Storing graphic primitives

Graphic primitives are basic elements (such as images or fonts) that can be combined to build the framebuffer content that is displayed.

Static data must be placed in a nonvolatile memory. When the amount of data to store is relatively low, the internal flash memory can be used. Otherwise, graphical contents must be placed in external memories.

The STM32 MCUs offer parallel (FMC) or serial (Quad-SPI) interface for external NOR Flash memories (see Table 3).

To build the framebuffer content, the DMA2D can directly read graphic primitives from a parallel NOR Flash or a Quad-SPI Flash.

Refer to the document [9] for more details on storing graphic content on QSPI memory.

5.8.1 Converting images to C files

To add graphic primitives to a user project, these primitives must be converted to C or header files. Some specific tools can be used to generate C or *.h files.

Warning: *The user must convert images to C files respecting the configured pixel input format described in Pixel input format. Some tools may generate C or *.h files with Red and Blue colors swapped. To avoid this issue, the LCD image converter tool can be used.*

The LCD image converter is a very customizable free tool used to convert images to C files and to generate the C file in the desired format. An example is described in Section 7.2.5: Display an image from the internal flash.

5.9 Hardware considerations

Two important hardware interfaces must be carefully designed: the LTDC interface and the external memory interface (used for framebuffer) such as FMC_SDRAM or FMC_SRAM.

LTDC parallel interface

When the pixel clock is below 40 MHz (SVGA), a simple 3.3 V signaling can be used.

It is possible to reach 83 MHz with a parallel RGB if the load and the wire length are reduced (for example to interface on the same PCB with on-board an LVDS or HDMI transceiver).

It is recommended to configure the LTDC GPIOs at the maximum operating speed OSPEEDRy[1:0] = 11. Refer to the product reference manual for a description of the GPIOx_SPEEDR register.

FMC SDRAM/SRAM interface

When using an external SRAM or SDRAM memory for a framebuffer, the FMC-SDRAM and the FMC-SRAM interfaces speed depend on many factors including the board layout and the pad speed. A good PCB design enables to reach the maximum pixel clock described in Table 10 to Table 16.

The layout must be as good as possible in order to get the best performances. For more information on PCB routing guidelines, refer to the documents [10] and [11] available on the STMicroelectronics website

6 Saving power consumption

When an application is in idle state and displays only a screen saver, it is important to drive the STM32 product in Sleep mode to reduce the power consumption. In Sleep mode, all peripherals can be enabled (FMC-SDRAM and LTDC for instance) while the CPU is stopped.

External memories, such as SDRAM or Quad-SPI Flash, can be driven in low-power modes whenever it is needed in order to avoid the waste of power.

If the application is in low-power state but requires to display graphics, the LTDC can be kept active, and the SDRAM can be put in self-refresh mode (in order to save power). If the application is set in power-down mode, it saves even more power.

The display can also be disabled or put in low-power mode if it is not needed when running the application.

7 LTDC application examples

This section provides:

- some graphic implementation examples considering the resources requirements
- an example on how to create a basic graphical application
- a summary of STM32 reference boards that embeds LTDC and features an on-board LCD-TFT panel

7.1 Implementation examples and resources requirements

7.1.1 Single-chip MCU

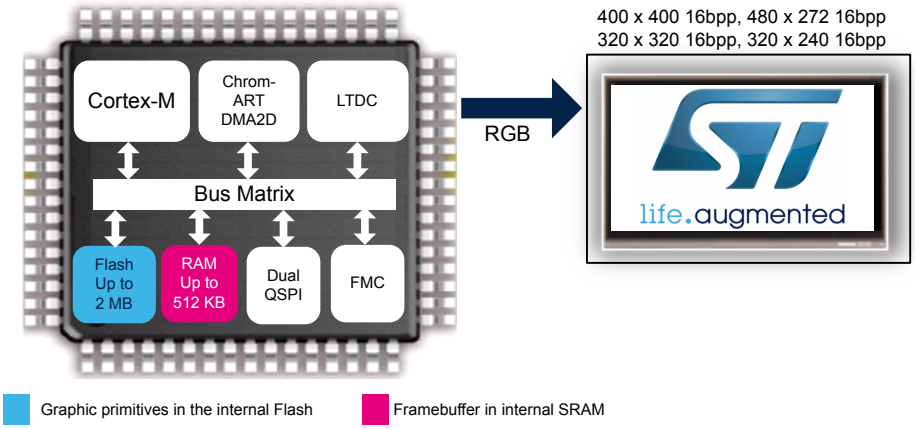
Thanks to their integrated SRAM, the STM32 MCUs can be used for graphic applications, without the need of an external SDRAM/SRAM memory for framebuffer. Also, thanks to their high-size internal flash (up to 2 Mbytes), graphic primitives can be stored in these memories. The use of internal memories allows reduced number of used pins, easy PCB design and cost savings.

In order to use a single-chip MCU for a graphical application, the following hardware configuration can be used:

- internal flash up to 2 Mbytes, storing user application code and graphic primitives
- framebuffer located in the internal SRAM
  Depending on the internal SRAM size for each STM32 MCU, the user can interface with a corresponding display size and color depth as illustrated below:
  - STM32F7x7: use SRAM1 (368 Kbytes) to support resolutions 400 x 400 16 bpp (313 Kbytes) or 480 x 272 16 bpp (255 Kbytes)
  - STM32F7x6: use SRAM1 (240 Kbytes) to support 320 x 320 resolution with 16 bpp (200 Kbytes)
  - STM32F469/F479: use SRAM1 (160 Kbytes) to support 320 x 240 resolution with 16 bpp (154 Kbytes)
  - STM32F429/F439: use SRAM1 (112 Kbytes) to support 320 x 240 resolution with 8 bpp (75 Kbytes).
  - STM32 MCU packages: LQFP 100 or TFBGA100

Figure 32 illustrates a graphic implementation example, with a single chip and no external memories used.

Figure 32. Low-end graphic implementation example



7.1.2 MCU with external memory

In order to interface with higher resolution displays, an external memory connected to the FMC is needed for framebuffer. An external Quad-SPI flash memory can be used to store graphic primitives.

For mid-end or high-end graphical applications, the following hardware configuration example can be used:

- external Quad-SPI flash memory with up to 256 Mbytes addressable memory-mapped, used to store graphic primitives
- external SDRAM 32-bit memory used for framebuffer
- STM32 MCU packages: UFBGA169, UFBGA176, LQFP 176, LQFP 208, TFBGA216, WLCSP168, and WLCSP180.

Figure 33 illustrates a graphic implementation example where two external memories are connected to an STM32 MCU, one for the framebuffer and the other for graphic primitives.

Figure 33. High-end graphic implementation example

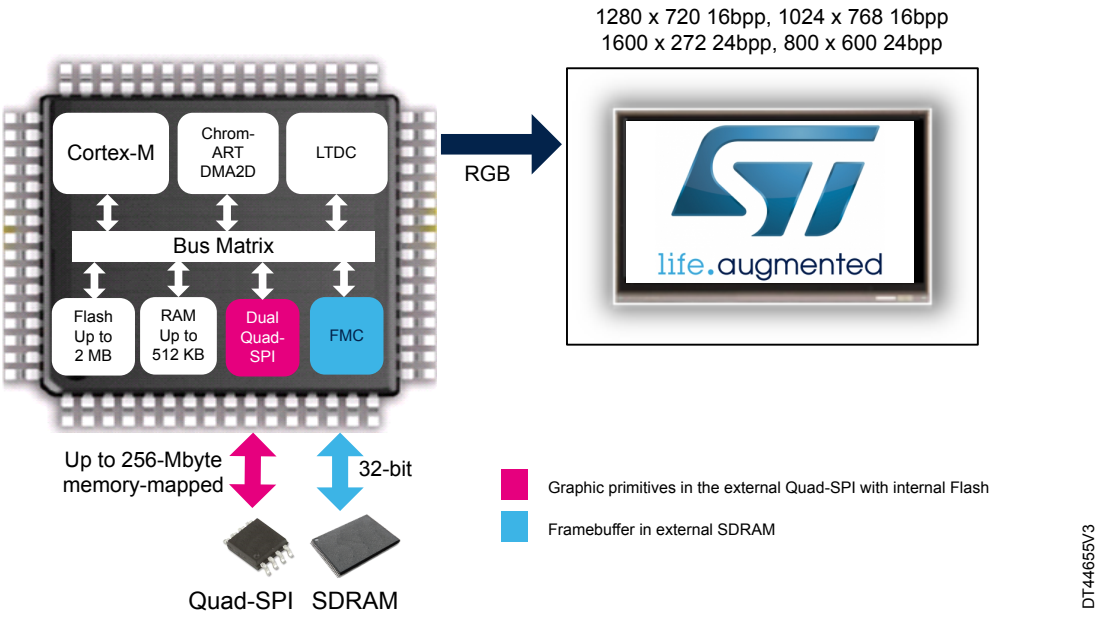


Table 23 summarizes an example of graphic implementations in different STM32 hardware configurations.

Table 23. Example of graphic implantations with STM32 in different hardware configurations

Variant	Display size	Color depth	External memory-SDRAM	Display interface	STM32 package(1)
High-end	1280 x 720	16bpp	32-bit	RGB888	UFBGA176 TFBGA216/ UFBGA169/ LQFP176/ LQFP208 WLCSP180/ WLCSP168/ UFBGA176 + 25/ TFBGA225
	1024 x 768				
	1600 x 272	24bpp			
	800 x 600				
Mid-end	800 x 600	16bpp	16-bit	RGB666	LQFP144/ WLCSP143
	800 x 480	24bpp			
	640 x 480				
	400 x 400(2)				
Low-end	400 x 400	16bpp	No	RGB666	LQFP100/ TFBGA100/ UFBGA144
	480 x 272				
	320 x 320				
	320 x 240				

1. *Package availability of STM32 MCUs embedding LTDC is summarized in Table 20.*
2. *400 x 400 and 320 x 320 are specific display resolutions commonly used for smart watches.*

7.2 Example: creating a basic graphical application

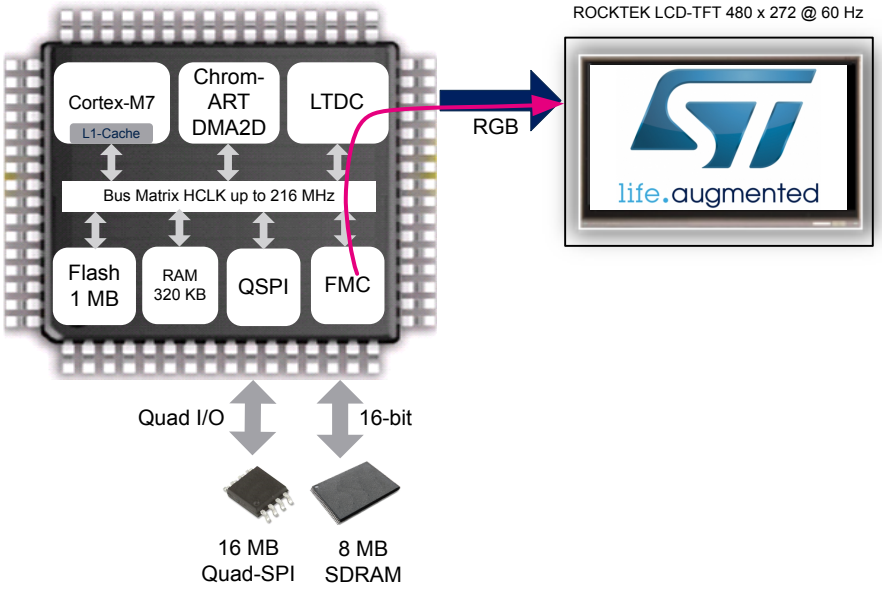
This section provides an example based on the STM32F746G-DISCO board, describing the steps required to create a basic graphic application.

7.2.1 Hardware description

The hardware resources embedded on the STM32F746G-DISCO board are used in this example. Figure 34 describes the graphic hardware resources to be used:

Figure 34. Graphic hardware configuration in the STM32F746G-DISCO

The pink arrow shows the pixel data path to the display.

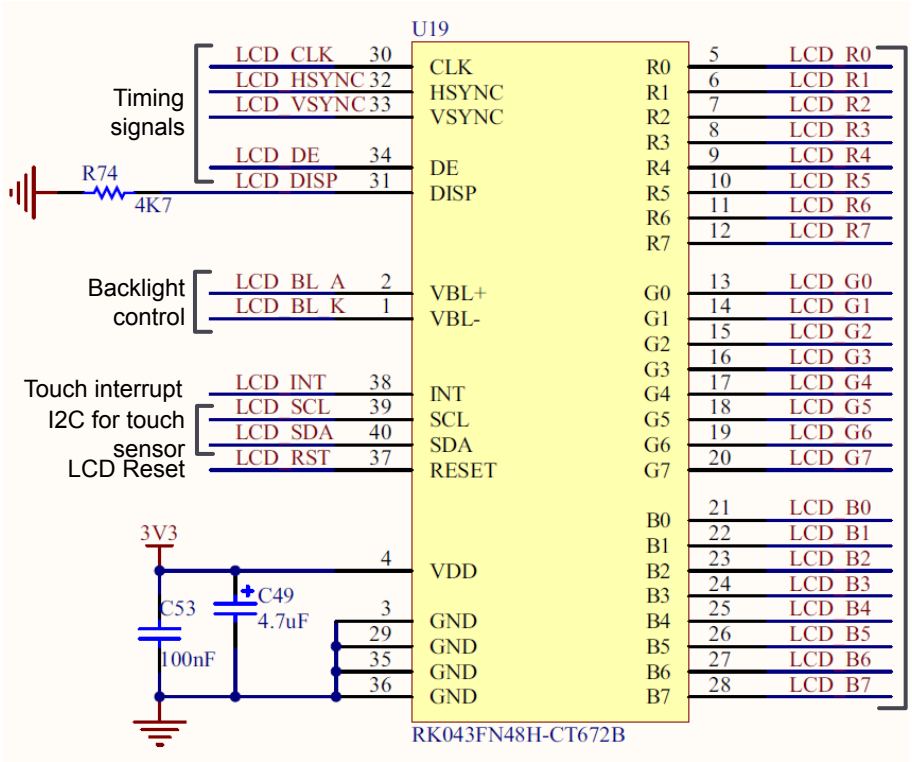


The STM32F746G-DISCO board embeds a parallel true color RGB888 LCD-TFT panel with a 480 x 272 resolution.

For more details on the STM32F746G-DISCO board, refer to the document [12].

Figure 35 shows the ROCKTECH RK043FN48H true color panel (RGB888) connected to the STM32F746 MCU.

Figure 35. LCD-TFT connection in the STM32F746G-DISCO board



As shown in the last figure, the display module is connected to the MCU through two different pin categories:

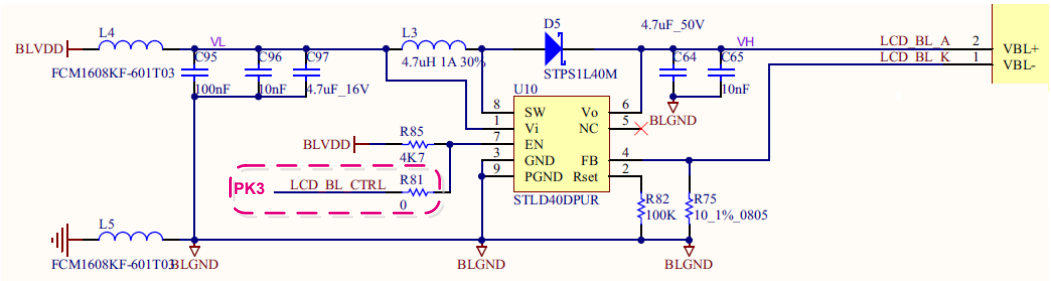
- LTDC interface pins:
  - 24-bit RGB interface
  - Timing signals: LCD_HSYNC, LCD_VSYNC, LCD_DE and LCD_CLK
- Other specific pins:
  - LCD_DISP to enable/disable display Standby mode
  - INT interrupt line: allows the touch sensor to generate interrupts
  - I^2C interface to control the touch sensor
  - LCD_RST reset pin: allows the LCD-TFT reset. This pin is connected to the global MCU reset pin (NRST).
  - LCD_BL_A and LCD_BL_K pins for LED backlight control: the backlight is controlled by the STLD40DPUR circuit.

Backlight controller: the STLD40DPUR circuit described in Figure 36 is a boost converter that operates from 3.0 V to 5.5 V. It can provide an output voltage as high as 37 V and can drive up to ten white LEDs in series. Refer to the STLD40D datasheet for more information on the backlight controller.

The high level on the LCD_BL_CTRL (PK3) signal lights the backlight on, while the low level switches it off.

Note: It is possible to change the display brightness (dim the backlight intensity) by applying a low-frequency(1 to 10 kHz) PWM signal to the EN pin 7 of the STLD40D circuit. This action needs a rework since there is no timer PWM output alternate function available on the PK3 pin. The user must remove the R81 resistance and connect another GPIO pin with the PWM output alternate function.

Figure 36. Backlight controller module



7.2.2 How to check if a specific display size matches the hardware configuration

This section uses a desired display size of 480 x 272 at 60Hz and with a 24 bpp color depth as reference to select the right hardware configuration.

Desired display panel

The desired display is the ROCKTECH RK043FN48H-CT672B display:

- display resolution: 480 x 272 pixels with LED backlight and capacitive touch panel
- display interface: 24-bit RGB888 (in total 28 signals)

Determining framebuffer size and location

Depending on its size and on the internal available SRAM size, the framebuffer can be located either in the internal SRAM or in the external SDRAM. The total embedded SRAM size for the STM32F746NGH6 MCU is 320 Kbytes where SRAM1 (240 Kbytes) can be used (see Figure 10).

The framebuffer size is calculated in the following way:

- for 24 bpp, framebuffer (Kbyte) = 480 x 272 x 3 / 1024 = 382.5
- for 16 bpp, framebuffer (Kbyte) = 480 x 272 x 2 / 1024 = 255
- for 8 bpp, framebuffer (Kbyte) = 480 x 272 / 1024 = 128

Based on these results, the required framebuffer size is about 128 Kbytes for 8 bpp. In that case, the framebuffer can be located in the internal SRAM1 (240 Kbytes). This is not valid for a double-framebuffer case as the size of 128 x 2 Kbytes exceeds the internal SRAM size.

For the 16 bpp color depth and in a double-framebuffer configuration, the required framebuffersize (2 x 255 Kbytes) exceeds the internal SRAM size, so using an external SRAM or SDRAM is a must for this configuration.

For the 24 bpp color depth and in a double-framebuffer configuration, the required framebuffersize exceeds the internal SRAM size (2 x 382.5 Kbytes), so using an external SRAM, or SDRAM is a must for this configuration.

The next step is to check if the SDRAM 16-bit bus width can sustain the desired resolution and color depth.

Check if a 480 x 272 resolution with 24 bpp fits the SDRAM 16-bit configuration

At this stage, the user decided to use an external SDRAM but still has to check if the SDRAM16-bit bus width (actual hardware implementation in the discovery board) matches the 480 x 272 @ 60 Hz display size and 24 bpp color depth.

In order to conclude if such hardware configuration can support the desired display size and color depth or not, the user must first compute the pixel clock.

The computed LCD_CLK is about 9.5 MHz (for computing pixel clock refer to Section 7.2.3: LTDC GPIOs configuration).

Then the user must check, based on the following parameters, if the computed pixel clock is not higher than the maximum LCD_CLK indicated in Table 11:

- number of used LTDC layers: in this example, only one layer used
- system clock speed HCLK and framebuffer memory speed: HCLK @ 200 MHz and SDRAM @ 100 MHz
- external framebuffer memory bus width 16-bit SDRAM
- number of AHB masters accessing concurrently to external SDRAM: two masters (DMA2D and LTDC)

Referring to the pixel clock Table 11 in the “LTDC + DMA2D” column and one layer row, the pixel clock can reach 34 MHz for a 16-bit SDRAM.

So, the 16-bit SDRAM bus width is quite enough to sustain a 480 x 272 @ 60 Hz resolution (LCD_CLK = 9.5 MHz) with 24 bpp color depth.

7.2.3 LTDC GPIOs configuration

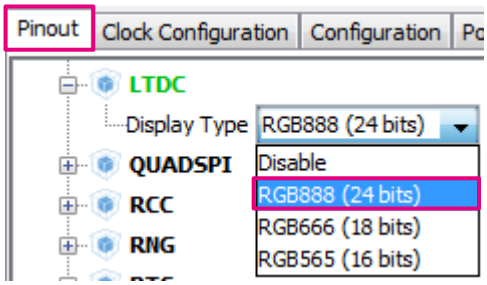
As shown on Figure 35, the ROCKTECH RK043FN48H display is connected to the STM32F746xx using a parallel RGB888 of 24 bits.

LTDCRGB interface pins configuration

Once that the STM32CubeMX project is created, in the *Pinout* tab, choose one from the listed hardware configurations. Figure 37 shows how to select the RGB888 hardware configuration with the STM32CubeMX.

The user can also configure all the GPIOs by setting the right alternate function for each GPIO one by one.

Figure 37. STM32CubeMX: LTDC GPIOs configuration



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If after selecting one hardware configuration (RGB888 as shown in the above figure), the used GPIOs do not match with the display panel connection board, the user can change the desired GPIO and configure the alternate function directly on the pin. Figure 38 shows how to configure manually a PJ7 pin to LTDC_G0 alternate function.

Figure 38. **STM32CubeMX: PJ7 pin configuration to LTDC_G0 alternate function**

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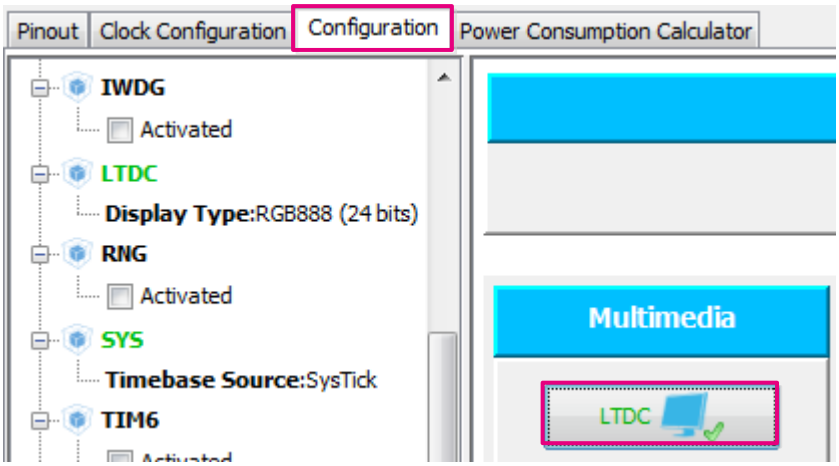
The used pins are highlighted in green once all LTDC interface GPIOs are correctly configured. The user must now set their speed to very high.

To set the GPIOs speed using STM32CubeMX, select the *Configuration* tab then click on the *LTDC* button as shown in Figure 39.

Figure 39. **STM32CubeMX: LTDC configuration**



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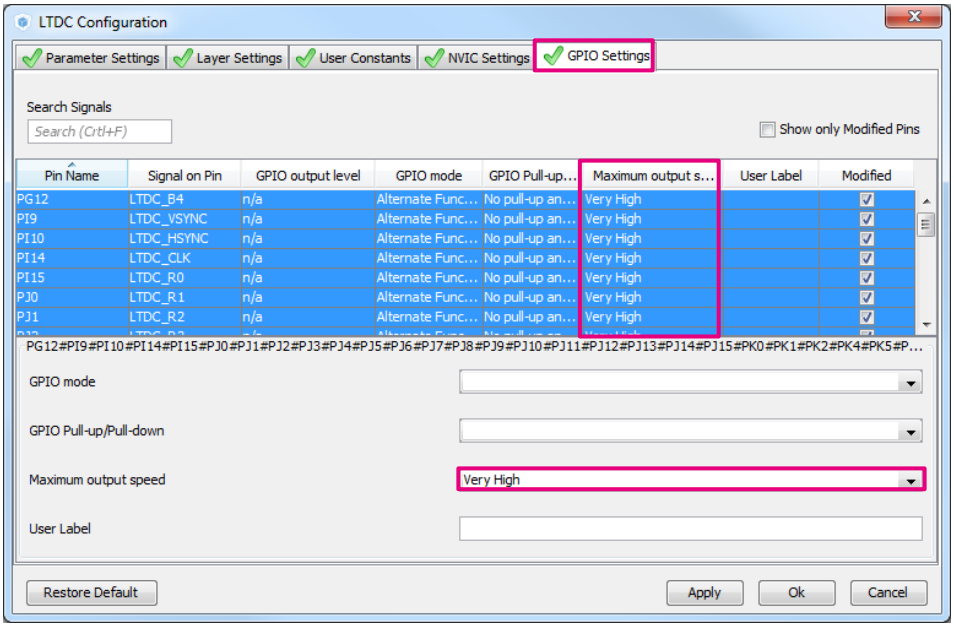
In the *LTDC Configuration* window described in Figure 40, select all the LTDC pins, then set the maximum output speed to *Very High*.

Figure 40. **STM32CubeMX: LTDC GPIOs output speed configuration**



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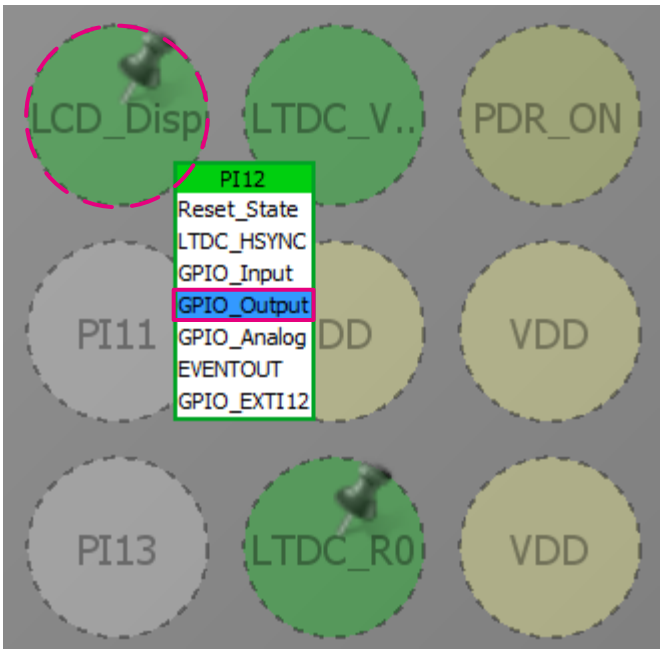
Specific pins configuration of the display module

Once all LTDC interface pins are correctly configured respecting the LCD-TFT panel connection, the user must configure the other specific pins connected to the display (LCD_DISP, INT pin and I^2C interface).

The LCD_DISP pin (PI12 pin) has to be configured as an output push-pull with high level in order to enable the display, otherwise the display stays in Standby mode.

To configure the LCD_DISP pin in output mode with STM32CubeMX, in the pinout tab click on the *PI12* pin then select *GPIO_Output* (see Figure 41).

Figure 41. **STM32CubeMX: display enable pin (LCD_DISP) configuration**



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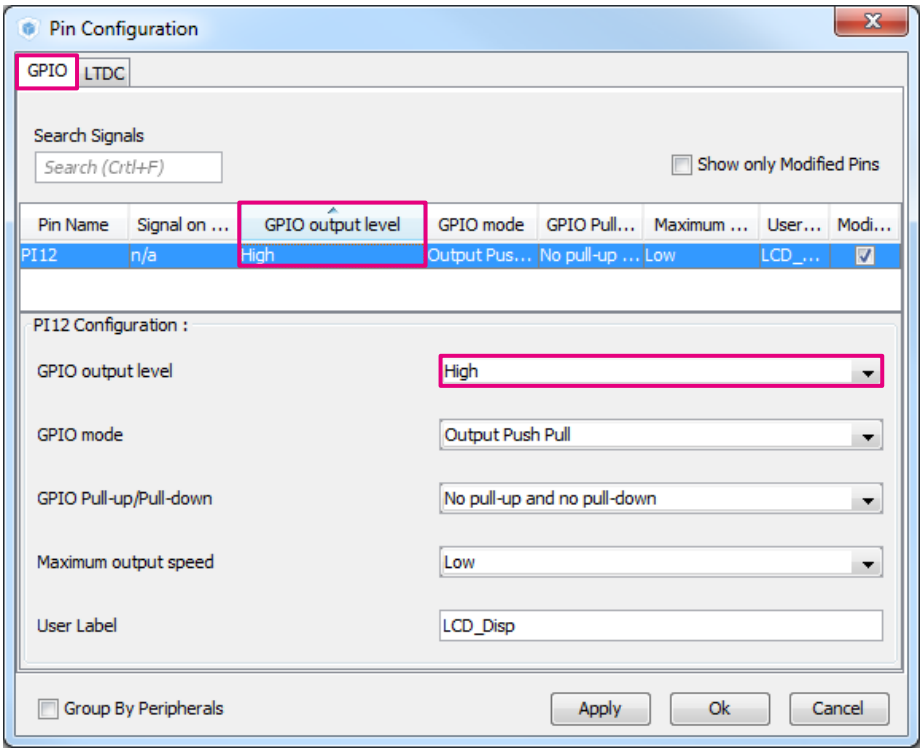
Then, the LDC_DISP (PI12) pin must be configured to high level: in the *Configuration* tab, click on the *GPIO* button. In the *Pin Configuration* window, set the *GPIO output level* to high as described in Figure 42.

Figure 42. **STM32CubeMX: setting LCD_DISP pin output level to high**



Due to the R85 pull-up resistance, the backlight is at its highest level by default if the LCD_BL_CTRL (PK3) pin is kept floating. There is no need to configure this pin.

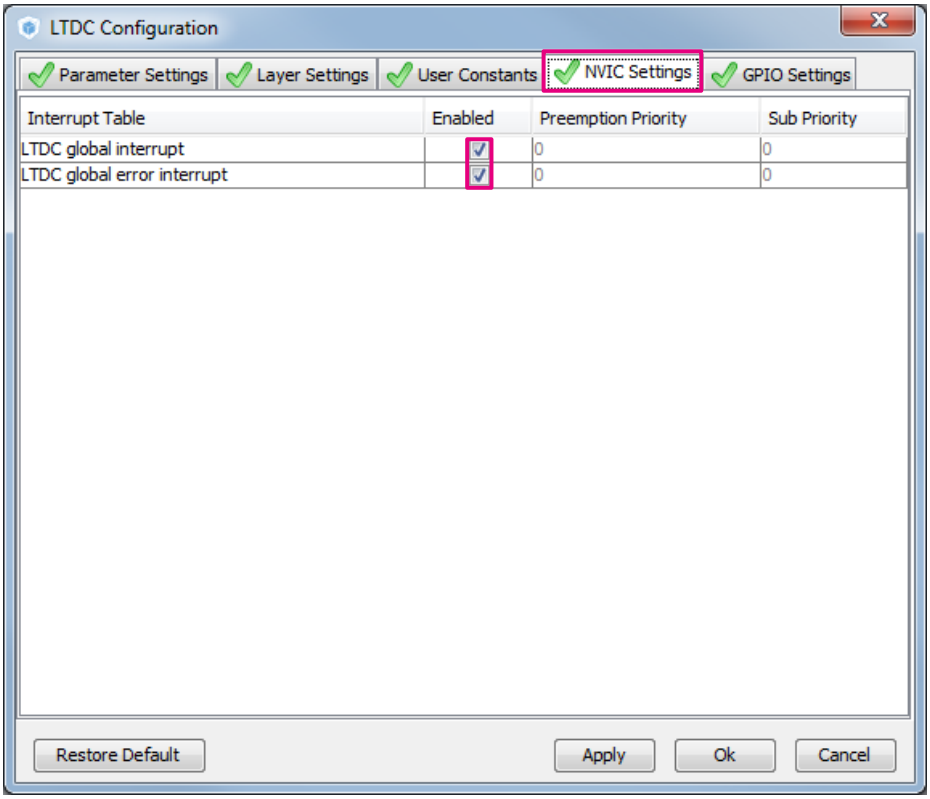
Enabling LTDC interrupts

The FIFO underrun and transfer error interrupts are enabled in the hal_ltdc driver `HAL_LTDC_Init()` function. The user must just enable the LTDC global interrupt on the NVIC side.

To enable the LTDC global interrupts using STM32CubeMX, select the *Configuration* tab then click on the *LTDC* button as shown in Figure 39.

In the *LTDC Configuration* window shown in Figure 43, select the *NVIC settings* tab. Check the *LTDC global interrupts* then click on the *OK* button.

Figure 43. **STM32CubeMX: enabling LTDC global and error interrupts**



7.2.4 LTDC peripheral configuration

This section demonstrates how to configure LTDC clocks, timings, and layer parameters using STM32CubeMX.

LTDC clock and timing configuration

System clock configuration

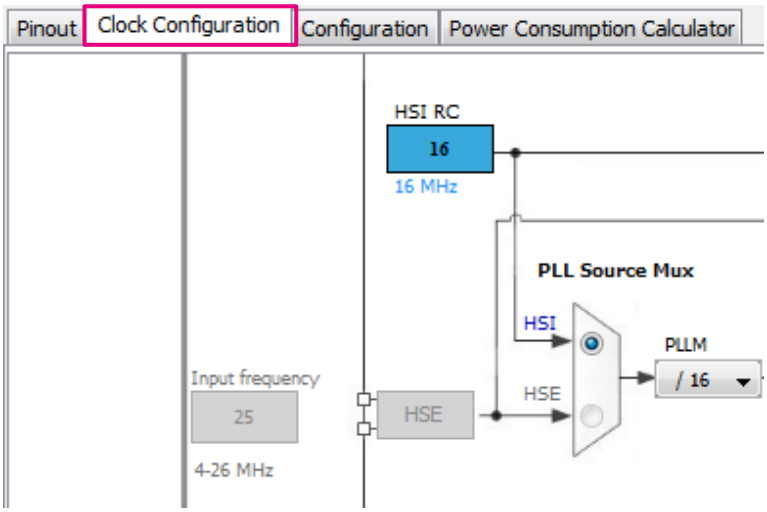
In this example the system clock is configured with the following configuration:

- use of internal HSI RC, where main PLL is used as system source clock
- HCLK @ 200 MHz (Cortex-M7 and LTDC both running @ 200 MHz)

Note: HCLK is set to 200 MHz but not 216 MHz. This is to set the SDRAM_FMC at its maximum speed of 100 MHz with HCLK/2 prescaler.

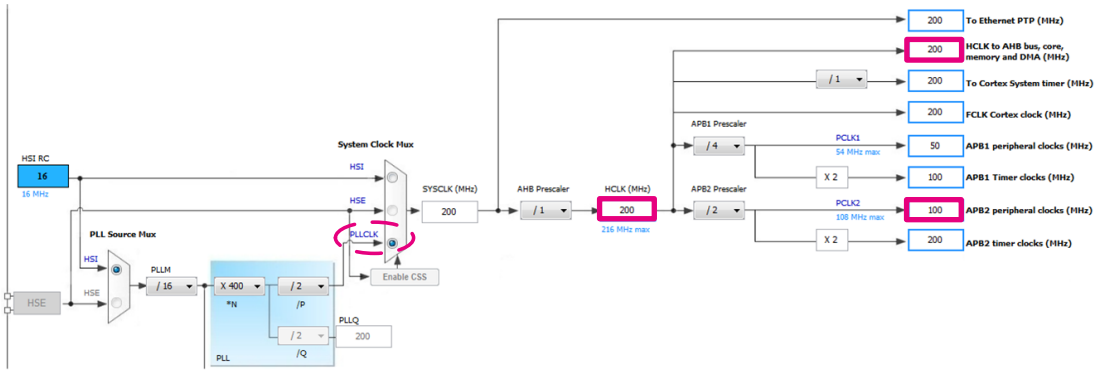
In order to configure the system clock using STM32CubeMX, select the *Clock Configuration* tab as shown in Figure 44.

Figure 44. **STM32CubeMX: clock configuration tab**



To get the system clock HCLK @ 200 MHz, set the PLLs and the prescalers in the *Clock Configuration* tab as shown in Figure 45.

Figure 45. **STM32CubeMX: System clock configuration**



Pixel clock configuration

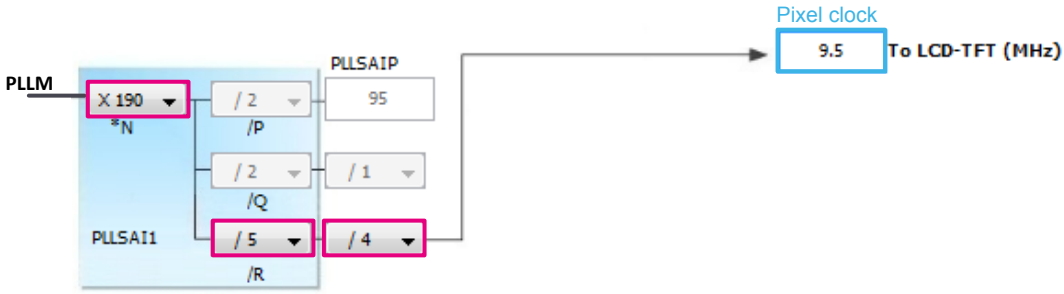
The LCD_CLK must be calculated using the parameters found in the display datasheet. In order to do the calculation, the user must determine the total width and total height. The pixel clock is calculated with a 60 Hz refresh rate as shown below:

LCD_CLK = TOTALW x TOTALH x refresh rate (see extracted display timing parameters in Section 5.7.2)

==> LCD_CLK = 531 x 297 x 60 = 9.5 MHz

To configure the LTDC pixel clock to 9.5 MHz using STM32CubeMX, select the *Clock Configuration* tab, then set the PLLSAI and the prescalers as shown in Figure 46.

Figure 46. **STM32CubeMX: LTDC pixel clock configuration**



Timing parameter configuration

In order to configure the display timings using STM32CubeMX, the user must extract the timing parameters from the device datasheet. For this example, see an extract of ROCKTECH datasheet on Table 21. It is recommended to use the typical display timings.

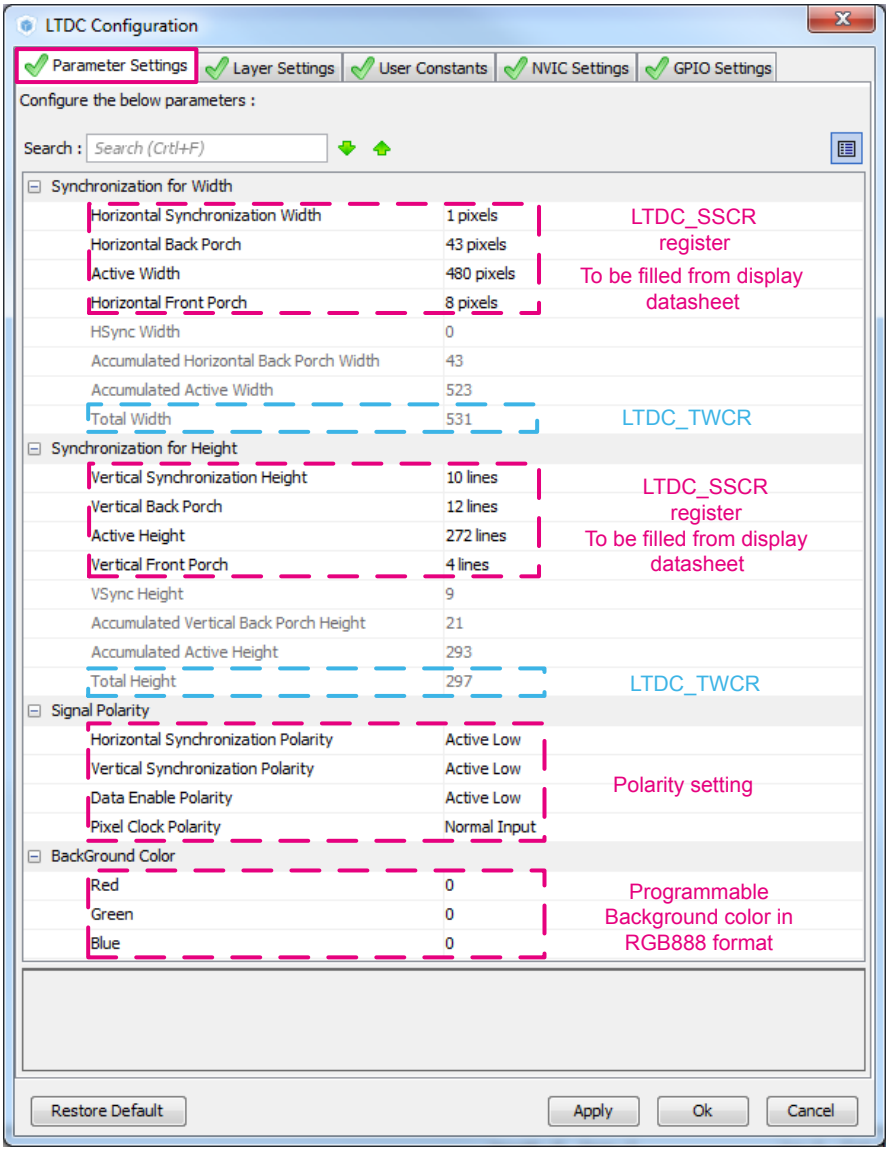
In order to configure the display timing, the user must go to the *Configuration* tab as indicated in Figure 39, and then click on the *LTDC* button. In the LTDC configuration window, the user must select the *Parameter Settings* tab and fill in the timing values (refer to Figure 47).

LTDC control signals polarity configuration

Referring to the display datasheet, HSYNC and VSYNC must be active low and the DE signal must be active high. As the DE signal is inverted in the output, it must be set to active low as well. The LCD_CLK signal must not be inverted.

Figure 47 shows the control signal polarity configuration and the LTDC configuration according to the ROCKTECH display datasheet.

Figure 47. STM32CubeMX: LTDC timing configuration



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LTDC Layer parameters configuration

At this stage, all LTDC clocks and timings have been set in the STM32CubeMX project.

The user must configure the LTDC Layer1 parameters according to the display size and the color depth.

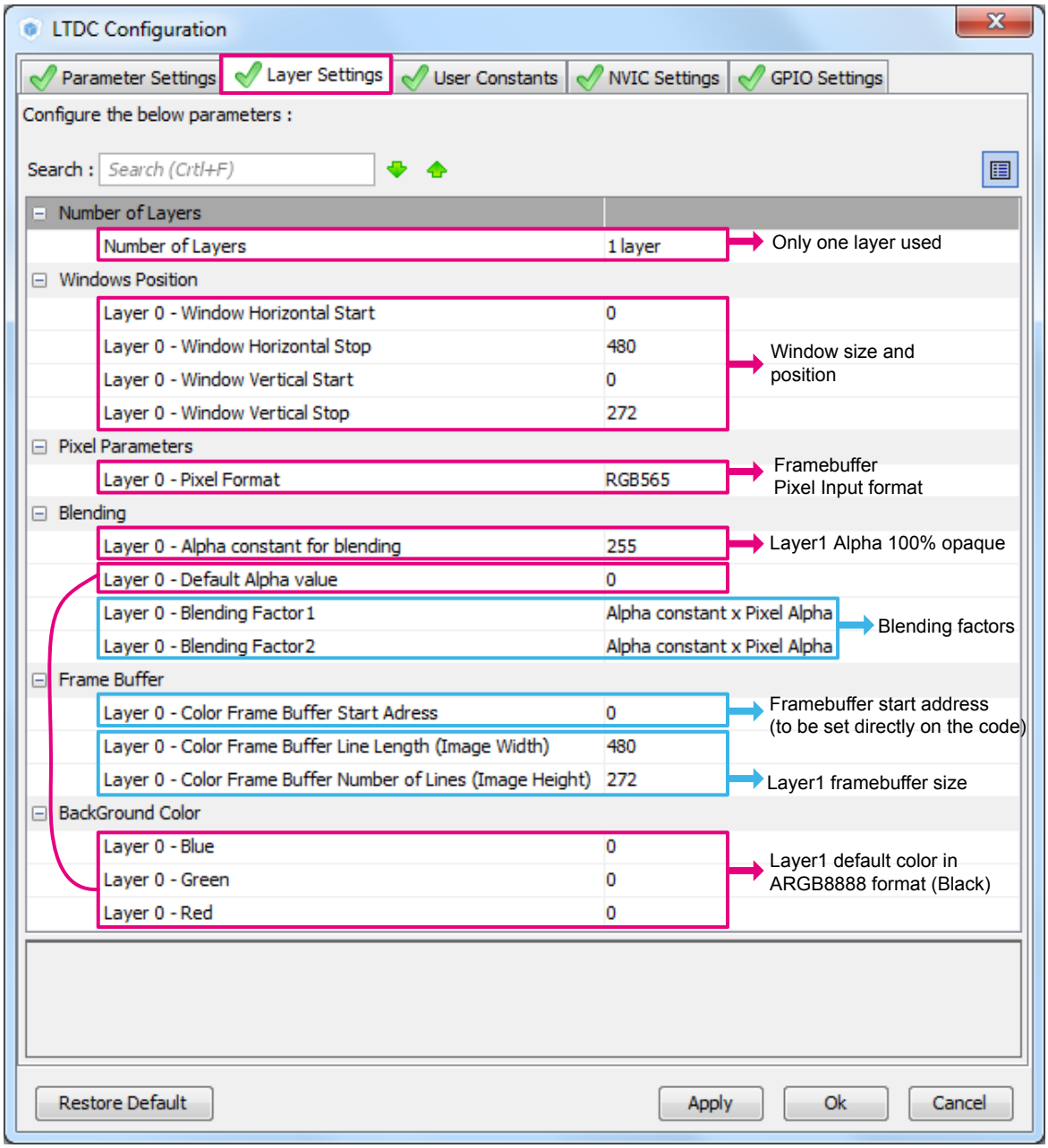
If needed, the user can also enable the Layer2 by setting to *2layers* the *Numberof Layers* field in the LTDC configuration window shown in Figure 48.

To set the LTDC Layer1 parameters using STM32CubeMX, the user must select the *Configuration* tab then click on the *LTDC* button as shown in Figure 38.

In the *LTDCConfiguration* window shown in Figure 48, the user must select the *Layer Settings* tab, set the LTDC layer1 parameters and then click on the *OK* button.

At this step, the user can generate the project with the desired toolchain by clicking on *Project->Generate Code*

Figure 48. STM32CubeMX: LTDC Layer1 parameters setting



7.2.5 Display an image from the internal flash

In order to ensure that the LTDC is properly configured respecting the display panel specifications, it is important to display an image from the internal flash.

To do it, the user must first convert the image to a C or a header file and add it to the project.

Converting the image to a header file using the LCD image converter tool

The user must generate the header file respecting the configured LTDC layer pixel input format RGB565 (see Pixel input format and Section 5.8).

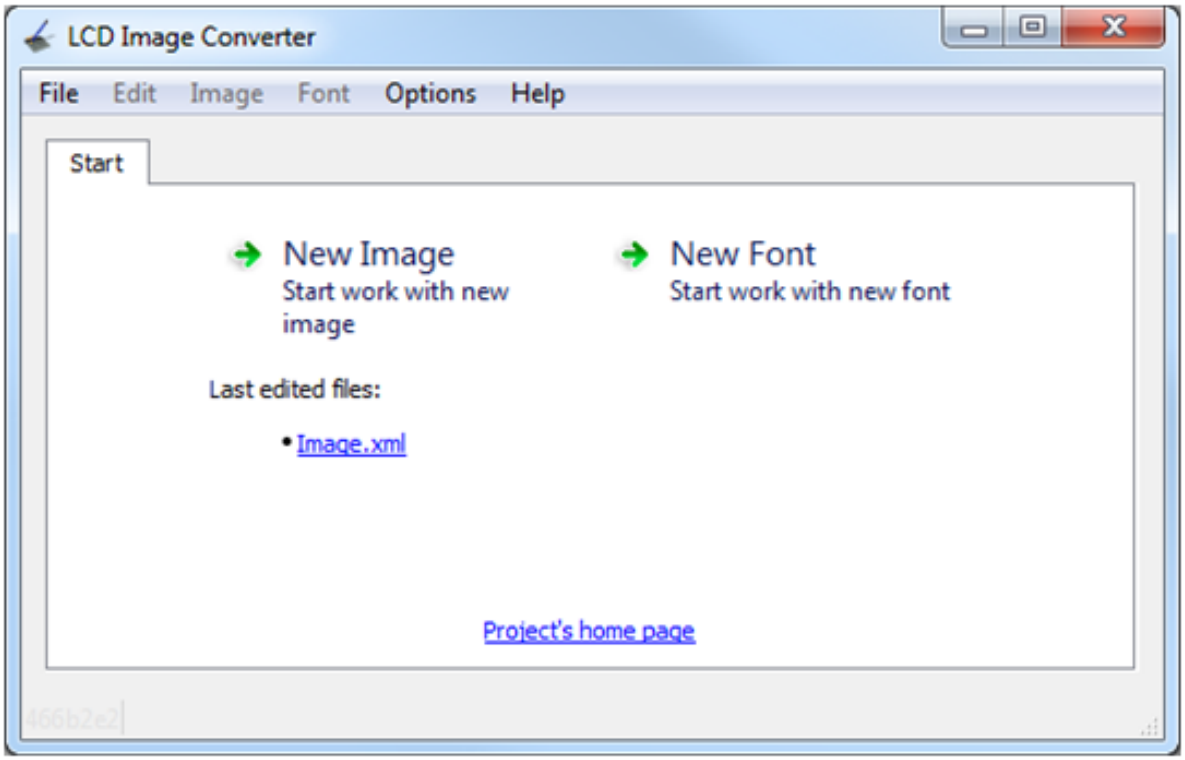
In this example, the LCD-Image-Converter-20161012 tool is used (see Section 5.8 for more details on this tool).

To convert an image, the user must first run the LCD-Image-Converter tool. Then, in the home page shown in Figure 49, click on File->Open and select the image file to be converted.

The used image size must be aligned with the LTDC Layer1 configuration (480 x 272). If the used image size is not aligned with the LTDC Layer1 configuration, the user can resize the image by going to Image->Resize or choose another image with the correct size.

For this example, the used image size is 480 x 272 and shows the STMicroelectronics logo (see Figure 50).

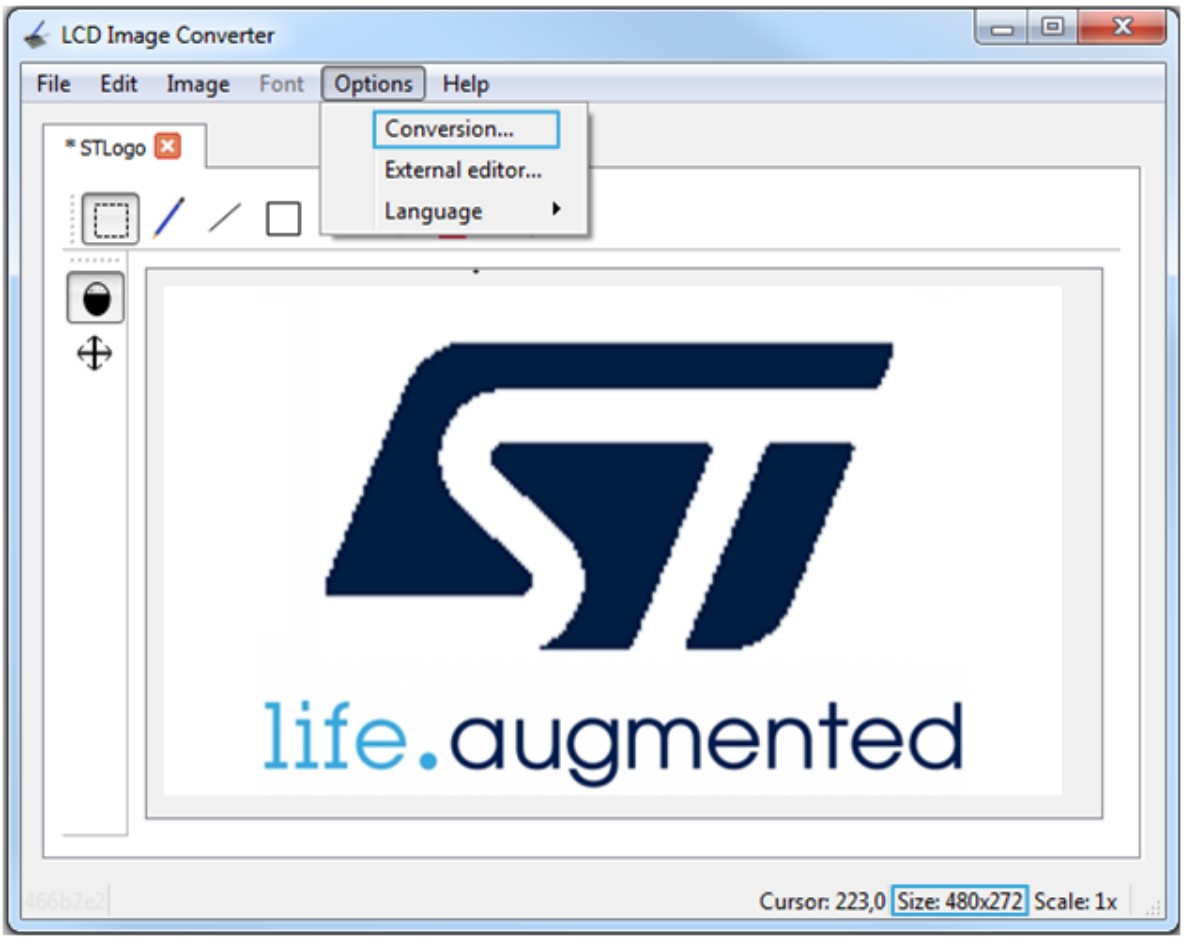
Figure 49. LCD-Image-Converter: home page



The image is then displayed on the LCD-Image-Converter tool home page as described in Figure 50.

To convert the image to a header file avoiding the Red and Blue swap issue explained in Section 5.8, the user must configure the tool to convert the image to a table of 32-bit words. To do it, in the home page menu, click on *Options->Conversion* as shown in Figure 50.

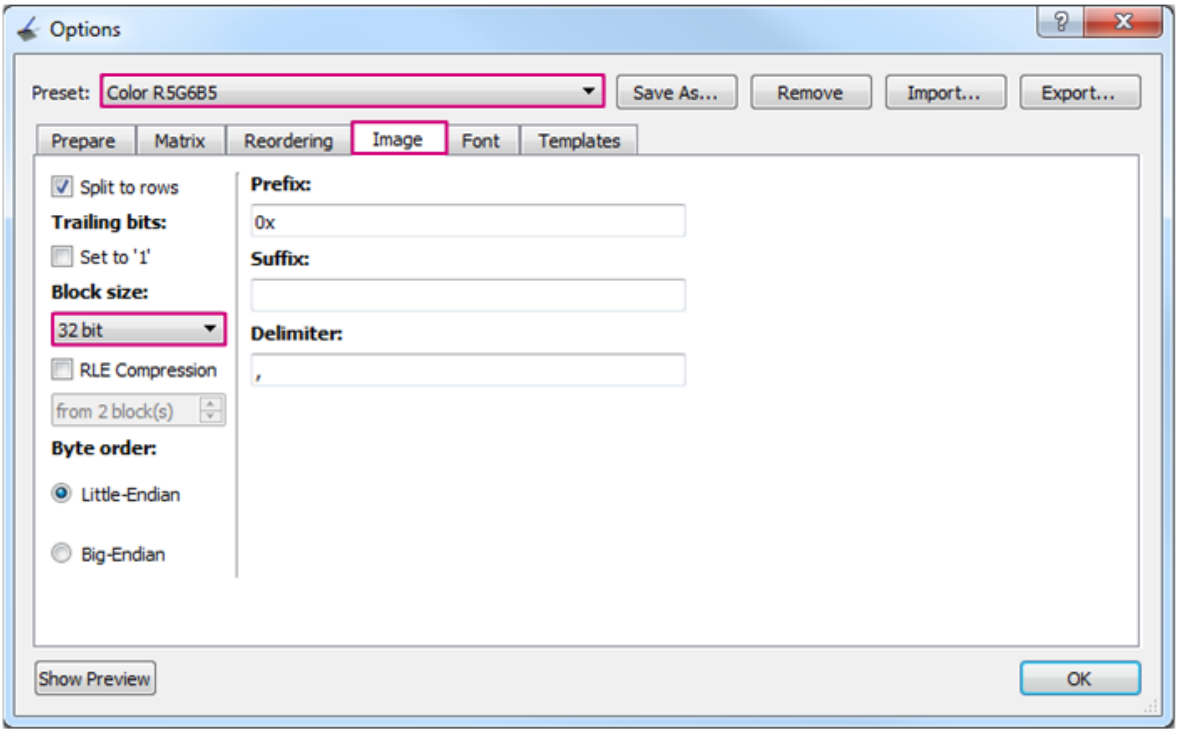
Figure 50. **LCD-Image-Converter: image project**



In the Options window shown in Figure 51, select the Image tab then select the RGB565 color in the Preset field. Set the *Block size* field to 32-bit and click on the *OK* button.

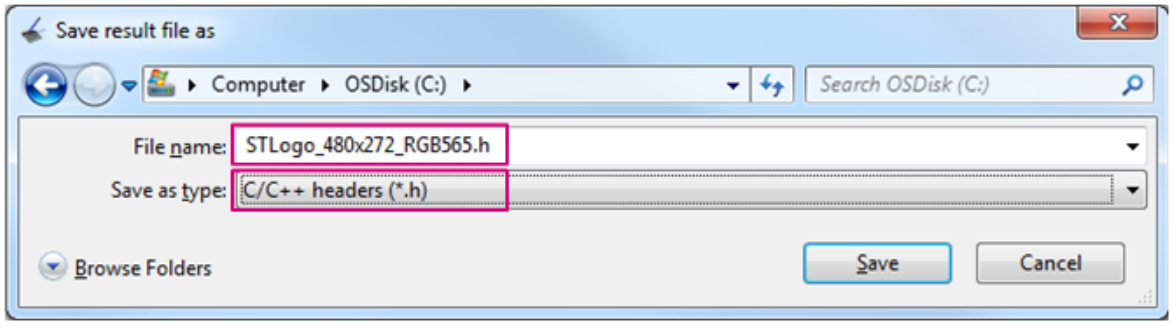
Note: The user can also convert the image to a table of bytes, but in that case he must swap the Red and Blue colors in the Conversion window matrix tab.

Figure 51. **LCD-Image-Converter: setting conversion options**



To generate the header file, click on *File->Convert*. In the displayed window shown in Figure 52, set the file type to *C/C++ headers (*.h)*, then save the *.h file in include \Inc directory (same location as main.h file) by clicking on the *Save* button.

Figure 52. **LCD-Image-Converter: generating the header file**



The generated header file must be included in the main.c file. It includes a table of 32-bit words where each word represents two pixels.

In this header file, the user must comment the structure definition located just after the table and keep only the table definition as shown below:

```
/* Converted image: image_data_STLogo definition */
const uint32_t image_data_STLogo[65280] = {0xffffffff, 0xffffffff, ........};
```

Setting the LTDC framebuffer Layer1 start address to the internal flash (image address in the flash)

The generated project by STM32CubeMX must include in the main.c file the `MX_LTDC_Init()` function that allows the LTDC peripheral configuration.

In order to display the image, the user must set the LTDC Layer1 framebuffer start address to the address of the image in the internal flash.

The `MX_LTDC_Init()` function is presented below with the framebuffer start address setting.

```
/* LTDC configuration function generated by STM32CubeMX tool */
static void MX_LTDC_Init(void)
{

    LTDC_LayerCfgTypeDef pLayerCfg;

    hltdc.Instance = LTDC;
    /* LTDC control signals polarity setting */
    hltdc.Init.HSPolarity = LTDC_HSPOLARITY_AL;
    hltdc.Init.VSPolarity = LTDC_VSPOLARITY_AL;
    hltdc.Init.DEPolarity = LTDC_DEPOLARITY_AL;
    hltdc.Init.PCPolarity = LTDC_PCPOLARITY_IPC;
    /* Timings configuration */
    hltdc.Init.HorizontalSync = 0;
    hltdc.Init.VerticalSync = 9;
    hltdc.Init.AccumulatedHBP = 43;
    hltdc.Init.AccumulatedVBP = 21;
    hltdc.Init.AccumulatedActiveW = 523;
    hltdc.Init.AccumulatedActiveH = 293;
    hltdc.Init.TotalWidth = 531;
    hltdc.Init.TotalHeigh = 297;
    /* Background color */
    hltdc.Init.Backcolor.Blue = 0;
    hltdc.Init.Backcolor.Green = 0;
    hltdc.Init.Backcolor.Red = 0x0;
    if (HAL_LTDC_Init(&hltdc) != HAL_OK)
    {
        Error_Handler();
    }
    /* Layer1 Window size and position setting */
    pLayerCfg.WindowX0 = 0;
    pLayerCfg.WindowX1 = 480;
    pLayerCfg.WindowY0 = 0;
    pLayerCfg.WindowY1 = 272;
    /* Layer1 Pixel Input Format setting */
    pLayerCfg.PixelFormat = LTDC_PIXEL_FORMAT_RGB565;
    /* Layer1 constant Alpha setting 100% opaque */
    pLayerCfg.Alpha = 255;
    /* Layer1 Blending factors setting */
    pLayerCfg.BlendingFactor1 = LTDC_BLENDING_FACTOR1_PAxCA;
    pLayerCfg.BlendingFactor2 = LTDC_BLENDING_FACTOR2_PAxCA;
    /* User should set the framebuffer start address (can be 0xC0000000 if external SDRAM is
used)*/
    pLayerCfg.FBStartAdress = (uint32_t)&image_data_STLogo;
    pLayerCfg.ImageWidth = 480;
    pLayerCfg.ImageHeight = 272;
    /* Layer1 Default color setting */
    pLayerCfg.Alpha0 = 0;
    pLayerCfg.Backcolor.Blue = 0;
    pLayerCfg.Backcolor.Green = 0;
    pLayerCfg.Backcolor.Red = 0;
    if (HAL_LTDC_ConfigLayer(&hltdc, &pLayerCfg, 0) != HAL_OK)
    {
        Error_Handler();
    }
}
```

Once the LTDC is correctly configured in the project, the user must build the project, and then run it.

7.2.6 FMC SDRAM configuration

The external SDRAM must be configured as it contains the LTDC framebuffer. To configure the FMC_SDRAM and the SDRAM memory device mounted on the STM32746G-Discovery board, STM32CubeMX or the existing BSP driver can be used.

To configure the FMC_SDRAM using the BSP driver, follow the steps below:

1. Add the following files to the project: BSP stm32746g_discovery_sdram.c and stm32746g_discovery_sdram.h. Include the stm32f7xx_hal_sdram.h in the main.c file. Add the stm32f7xx_hal_sdram.c and stm32f7xx_ll_fmc.c HAL drivers to the project.

2. Enable the SDRAM module in the stm32f7xx_hal_conf.h file by uncommenting the SDRAM module definition.
3. Call the `BSP_SDRAM_Init()` function in the `main()` function.

7.2.7 MPU and cache configuration

As illustrated in Section 5.6, the MPU attributes must be correctly configured to prevent graphical performance issues related to the Cortex-M7 speculative read accesses and cache maintenance.

This section describes an example of MPU attribute configuration with respect to the STM32F746G-DISCO board hardware configuration.

The MPU memory attributes can be easily configured with STM32CubeMX. A code example of MPU configuration generated using STM32CubeMX is described at the end of this section.

MPU configuration example: FMC_SDRAM

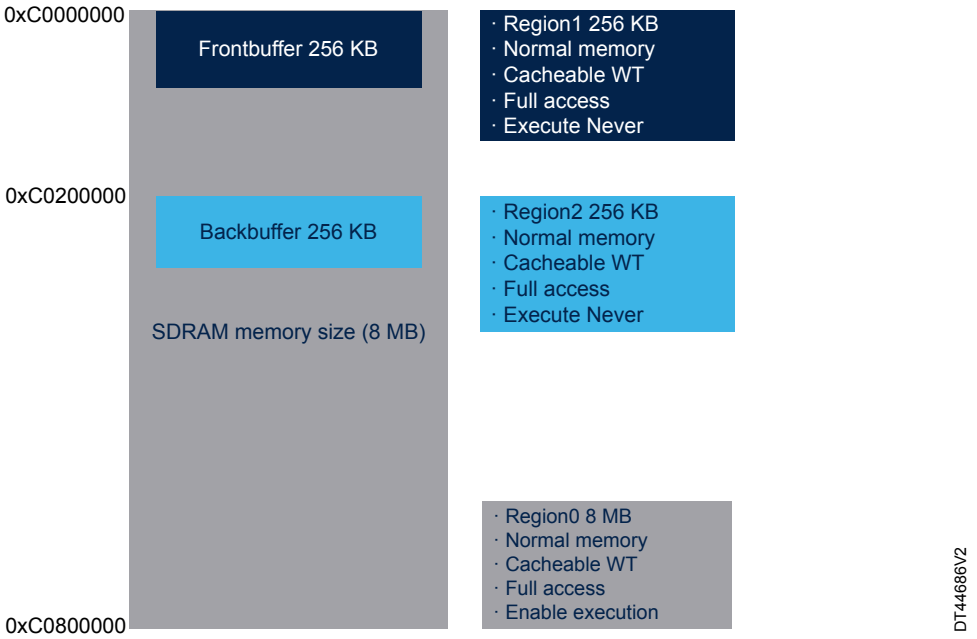
In this configuration example, the double-framebuffer technique is used. The frontbuffer is placed in the SDRAM Bank1 while the backbuffer is placed in the SDRAM Bank2 with respect to the SDRAM bandwidth optimization described in Section 5.5.3.

The following MPU regions are created (FMC without swap):

- Region0: defines the SDRAM memory size 8 Mbytes
- Region1: defines the frontbuffer 256 Kbytes (16 bpp x 480 x 272). It overlaps Region0.
- Region2: defines the backbuffer 256 Kbytes (16 bpp x 480 x 272). It overlaps Region0.

Figure 53 illustrates the MPU configuration of the SDRAM region.

Figure 53. FMC SDRAM MPU configuration example



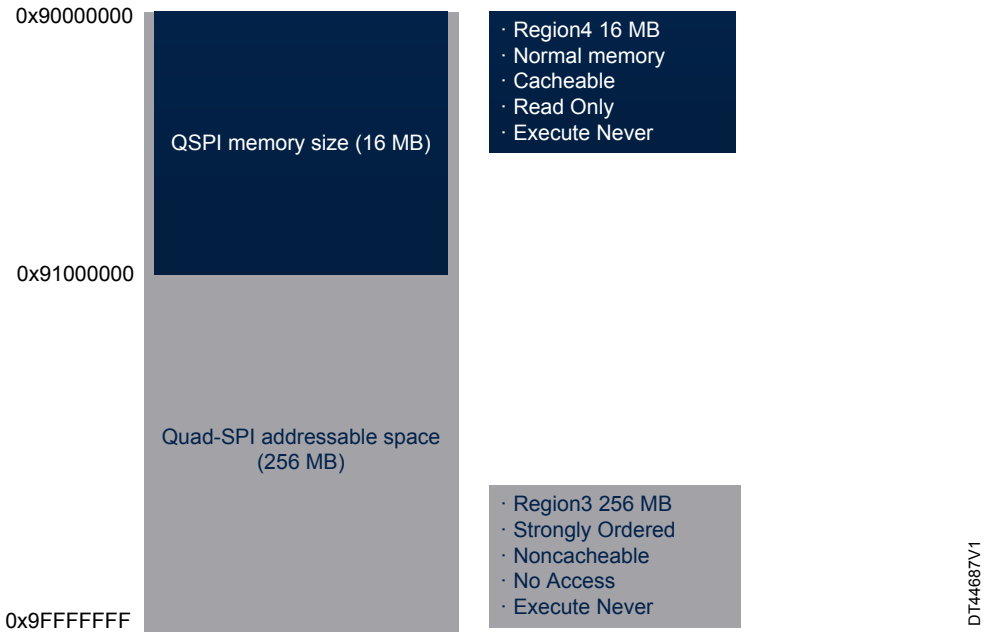
MPU configuration example: Quad-SPI in Memory-mapped mode

This example shows how to configure the MPU for the Quad-SPI interface. The Quad-SPI memory contains graphic primitives and can be accessed by Cortex-M7, DMA2D, or LTDC. For that, the Quad-SPI interface must be set to Memory-mapped mode and the MPU regions must be configured as described below:

- Region3: defines the whole Quad-SPI addressable space. It must be set to strongly ordered to forbid any CPU speculative read access to that region.
- Region4: defines the real Quad-SPI memory space reflecting the size of the memory that can be accessed by any master.

Figure 54 illustrates the MPU configuration of the Quad-SPI region.

Figure 54. **MPU configuration for Quad-SPI region**



SDRAM and Quad-SPI MPU configuration example

The following code (generated by STM32CubeMX) shows how to set the MPU attributes for the FMC_SDRAM and Quad-SPI respecting the previously described configurations.

```
/* MPU Configuration */
void MPU_Config(void)
{
    MPU_Region_InitTypeDef MPU_InitStruct;

    /* Disables the MPU */
    HAL_MPU_Disable();
    /* Configure the MPU attributes for region 0 */
/* Configure the MPU attributes for SDRAM to normal memory*/
    MPU_InitStruct.Enable = MPU_REGION_ENABLE;
    MPU_InitStruct.Number = MPU_REGION_NUMBER0;
    MPU_InitStruct.BaseAddress = 0xC0000000;
    MPU_InitStruct.Size = MPU_REGION_SIZE_8MB;
    MPU_InitStruct.SubRegionDisable = 0x0;
    MPU_InitStruct.TypeExtField = MPU_TEX_LEVEL0;
    MPU_InitStruct.AccessPermission = MPU_REGION_FULL_ACCESS;
    MPU_InitStruct.DisableExec = MPU_INSTRUCTION_ACCESS_ENABLE;
    MPU_InitStruct.IsShareable = MPU_ACCESS_NOT_SHAREABLE;
    MPU_InitStruct.IsCacheable = MPU_ACCESS_CACHEABLE;
    MPU_InitStruct.IsBufferable = MPU_ACCESS_NOT_BUFFERABLE;

    HAL_MPU_ConfigRegion(&MPU_InitStruct);

    /* Configure the MPU attributes for region 1 */
/* Configure the MPU attributes for the frontbuffer to normal memory*/
    MPU_InitStruct.Enable = MPU_REGION_ENABLE;
    MPU_InitStruct.Number = MPU_REGION_NUMBER1;
    MPU_InitStruct.BaseAddress = 0xC0000000;
    MPU_InitStruct.Size = MPU_REGION_SIZE_256KB;
    MPU_InitStruct.SubRegionDisable = 0x0;
    MPU_InitStruct.TypeExtField = MPU_TEX_LEVEL0;
    MPU_InitStruct.AccessPermission = MPU_REGION_FULL_ACCESS;
    MPU_InitStruct.DisableExec = MPU_INSTRUCTION_ACCESS_DISABLE;
    MPU_InitStruct.IsShareable = MPU_ACCESS_NOT_SHAREABLE;
    MPU_InitStruct.IsCacheable = MPU_ACCESS_CACHEABLE;
    MPU_InitStruct.IsBufferable = MPU_ACCESS_NOT_BUFFERABLE;
```

```
    HAL_MPU_ConfigRegion(&MPU_InitStruct);

    /* Configure the MPU attributes for region 2 */
/* Configure the MPU attributes for the backbuffer to normal memory*/
    MPU_InitStruct.Enable = MPU_REGION_ENABLE;
    MPU_InitStruct.Number = MPU_REGION_NUMBER2;
    MPU_InitStruct.BaseAddress = 0xC0200000;
    MPU_InitStruct.Size = MPU_REGION_SIZE_256KB;
    MPU_InitStruct.SubRegionDisable = 0x0;
    MPU_InitStruct.TypeExtField = MPU_TEX_LEVEL0;
    MPU_InitStruct.AccessPermission = MPU_REGION_FULL_ACCESS;
    MPU_InitStruct.DisableExec = MPU_INSTRUCTION_ACCESS_DISABLE;
    MPU_InitStruct.IsShareable = MPU_ACCESS_NOT_SHAREABLE;
    MPU_InitStruct.IsCacheable = MPU_ACCESS_CACHEABLE;
    MPU_InitStruct.IsBufferable = MPU_ACCESS_NOT_BUFFERABLE;

    HAL_MPU_ConfigRegion(&MPU_InitStruct);

/* Configure the MPU attributes for region 3 */
/* Configure the MPU attributes for Quad-SPI area to strongly ordered memory*/
    MPU_InitStruct.Enable = MPU_REGION_ENABLE;
    MPU_InitStruct.Number = MPU_REGION_NUMBER3;
    MPU_InitStruct.BaseAddress = 0x90000000;
    MPU_InitStruct.Size = MPU_REGION_SIZE_256MB;
    MPU_InitStruct.SubRegionDisable = 0x0;
    MPU_InitStruct.TypeExtField = MPU_TEX_LEVEL0;
    MPU_InitStruct.AccessPermission = MPU_REGION_NO_ACCESS;
    MPU_InitStruct.DisableExec = MPU_INSTRUCTION_ACCESS_DISABLE;
    MPU_InitStruct.IsShareable = MPU_ACCESS_NOT_SHAREABLE;
    MPU_InitStruct.IsCacheable = MPU_ACCESS_NOT_CACHEABLE;
    MPU_InitStruct.IsBufferable = MPU_ACCESS_NOT_BUFFERABLE;

    HAL_MPU_ConfigRegion(&MPU_InitStruct);

/* Configure the MPU attributes for region 4 */
/* Configure the MPU attributes for QSPI memory to normal memory*/
    MPU_InitStruct.Enable = MPU_REGION_ENABLE;
    MPU_InitStruct.Number = MPU_REGION_NUMBER4;
    MPU_InitStruct.BaseAddress = 0x90000000;
    MPU_InitStruct.Size = MPU_REGION_SIZE_16MB;
    MPU_InitStruct.SubRegionDisable = 0x0;
    MPU_InitStruct.TypeExtField = MPU_TEX_LEVEL0;
    MPU_InitStruct.AccessPermission = MPU_REGION_PRIV_RO;
    MPU_InitStruct.DisableExec = MPU_INSTRUCTION_ACCESS_DISABLE;
    MPU_InitStruct.IsShareable = MPU_ACCESS_NOT_SHAREABLE;
    MPU_InitStruct.IsCacheable = MPU_ACCESS_CACHEABLE;
    MPU_InitStruct.IsBufferable = MPU_ACCESS_NOT_BUFFERABLE;

    HAL_MPU_ConfigRegion(&MPU_InitStruct);

    /* Enables the MPU */
    HAL_MPU_Enable(MPU_PRIVILEGED_DEFAULT);
}
```

7.3 Reference boards with LCD-TFT panel

ST offers a wide range of reference boards such as Nucleo, Discovery, and Evaluation boards. Many of them embed display panels.

For STM32 reference boards featuring an on-board display but not embedding an LTDC, the DBI (FMC or SPI) interface is used to connect the STM32 with the display.

For the other STM32 boards, the LTDC is used to interface with the display panel.

These reference boards can be used to evaluate the graphic capability in specific hardware/software configurations.

Table 24 summarizes the STM32 reference boards embedding LTDC and featuring an on-board TFT-LCD panel.

Table 24. STM32 reference boards embedding LTDC and featuring an on-board LCD-TFT panel

Product	Board	LCD-TFT panel					Int. SRAM (Kbyte)	Ext. SDRAM (bit)	Ext. SRAM (bit)	Quad-SPI (Mbyte)
		Interface	Size (Inch)	Resolution	Color depth	Touch sensor				
STM32F429/439	32F429I DISCOVERY	DPI	2.4	240 x 320	RGB666	Resistive	256	16	NA	NA
	STM32439I-EVAL2	DPI	5.7	640 x 480	RGB666	Capacitive		32	16	NA
	STM32429I-EVAL1	DPI	4.3	480 x 272	RGB888	Resistive				
STM32F469/479	32F469I DISCOVERY	MIPI-DSI	4	800 x 480	RGB888	Capacitive	384	32	NA	16
	STM32469I-EVAL(1)	MIPI-DSI	4	800 x 480	RGB888	Capacitive		32	16	64
STM32F7x6	32F746G DISCOVERY	DPI	4.3	480 x 272	RGB888	Capacitive	320	16	NA	16
	STM32746G-EVAL	DPI	5.7	640 x 480	RGB666	Capacitive		32	16	64
		DPI	4.3	480 x 272	RGB888	Resistive				
STM32 F7x9(1)	STM32F769I-DISCO(2)	MIPI-DSI	4	800 x 480	RGB888	Capacitive	512	32	NA	64
	STM32F779I-EVAL STM32F769I-EVAL	MIPI-DSI	4	800 x 480	RGB888	Capacitive		32	16	64

1. *An available board B-LCDAD-HDMI1 (that can be purchased separately), allows the DSI conversion into HDMI format to connect HDMI consumer displays.*
   A DSI to LCD adapter board B-LCDAD-RPI1 (that can be purchased separately) provides a flexible connector from the microcontroller motherboard to the standard display connector (TE 1-1734248).
2. *Another discovery board is available STM32F769I-DISC1 but with no embedded display. The display can be purchased separately as B-LCD40-DSI1 ordering code.*

8 Supported display panels

The display controller embeds a very flexible interface that provides the features below that allow the STM32 MCUs to support multiple-parallel display panels (such as LCD-TFT and OLED displays) available in the market:

- Different signal polarities
- Programmable timings and resolutions

The display panel pixel clock (as indicated in the manufacturer datasheet) must not be higher than the STM32 maximal pixel clock. The user must refer to the display datasheet to ensure that the panel running clock is lower than the maximum pixel clock.

9 Frequently asked questions

This section summarizes the most frequently asked questions regarding the LTDC usage and configurations.

Table 25. Frequently asked questions

Question	Answer
What is the LTDC maximum supported resolution?	There is no absolute maximum resolution since it depends on several parameters such as: • color depth • used SDRAM bus width • system operating speed (HCLK) • number of AHB masters accessing concurrently to memory used for framebuffer See Section 5.2.2.
Does the STM32F4 or the STM32F7 support a 1280 x 720p 60 Hz resolution?	Yes, see examples in Section 5.2.2.
Which SDRAM bus width must be used for a specific resolution?	There is not an exact specific bus width, it depends on the resolution, the color depth and whether the SDRAM is shared with other AHB masters or not. The higher the SDRAM bus width, the better. An SDRAM 32-bit provides the best possible performance.
How to get the maximal supported resolution for a specific hardware?	Refer to Section 5.2.2.
Does LTDC support OLED displays?	Yes, if the OLED display has a parallel RGB interface.
Does LTDC support STN displays?	No, STN displays are not supported by LTDC.
Why the image is displayed with Red and Blue colors swapped?	This is because the image is not stored into memory respecting the configured pixel input format (see Section 5.8.1).
Does LTDC support gray scale?	Yes, it is possible by using the L8 mode and using a correct CLUT (R=G=B).
Why is the display bad (displaying bad visual effects)?	Many factors can lead to a bad visual effect. The user can perform the following checks: • Check if the used display is correctly initialized / configured (some displays need an initialization / configuration sequence). • Check if the LTDC timings and layer parameters are correctly set (see example in Section 7.2.4). • Display an image directly from the internal flash (see example in Section 7.2.5). • Check if there is a nonsynchronization between the LTDC and the framebuffer update (by DMA2D or CPU), see Section 5.2.2.

10 Conclusion

The STM32 MCUs provide a very flexible display controller, used to interface with a wide range of displays at a lower cost and offering high performances.

Thanks to its integration in a smart architecture, the LTDC autonomously fetches the graphical data from the framebuffer and drives them to the display without any CPU intervention.

The LTDC can continue fetching the graphical data and driving the display while the CPU is in Sleep mode, which is ideal for low-power and mobile applications such as smart watches.

This application note described the STM32 graphical capabilities and presented some considerations and recommendations to take fully advantage of the smart system architecture.

Revision history

Table 26. **Document revision history**

Date	Revision	Changes
10-Feb-2017	1	Initial release.
10-Feb-2017	2	Updated code on SDRAM and Quad-SPI MPU configuration example
10-Jul-2020	3	Updated: • Introduction • Product list extended in Table 1 and in the whole doc • Table 3: STM32 MCUs embedding an LTDC and their available graphic portfolio • Table 10 and Table 11 • New Table 13 to Table 15 • Section 6.2.6: FMC SDRAM configuration • Figure 52: FMC SDRAM MPU configuration example • Code in SDRAM and Quad-SPI MPU configuration example
13-Mar-2023	4	Updated Section: Introduction and Section Table 1.: Applicable products to add STM32U5 information. Updated the information in Section Table 15.: STM32L4P/Q maximal supported pixel clock. Edited the whole document to apply minor changes. Added Section Table 16.: STM32U59/A/F/G maximal supported pixel clock
08-Mar-2024	5	Added STM32H7Rx/7Sx lines Updated document title
07-Feb-2025	6	Updated: • Section Introduction • Section 3.2: LTDC and graphic portfolio across STM32 MCUs • Section 3.3: LTDC in a smart architecture • Section 5.2.2: Checking display compatibility considering the memory bandwidth requirements • Section 5.3: STM32 package selection guide

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