# AN4876
# Application note

## SLIC protection without a serial resistor or PTC to meet ITU-T K.20/K.21 and GR-1089-CORE using the LCP154DJF

## Introduction

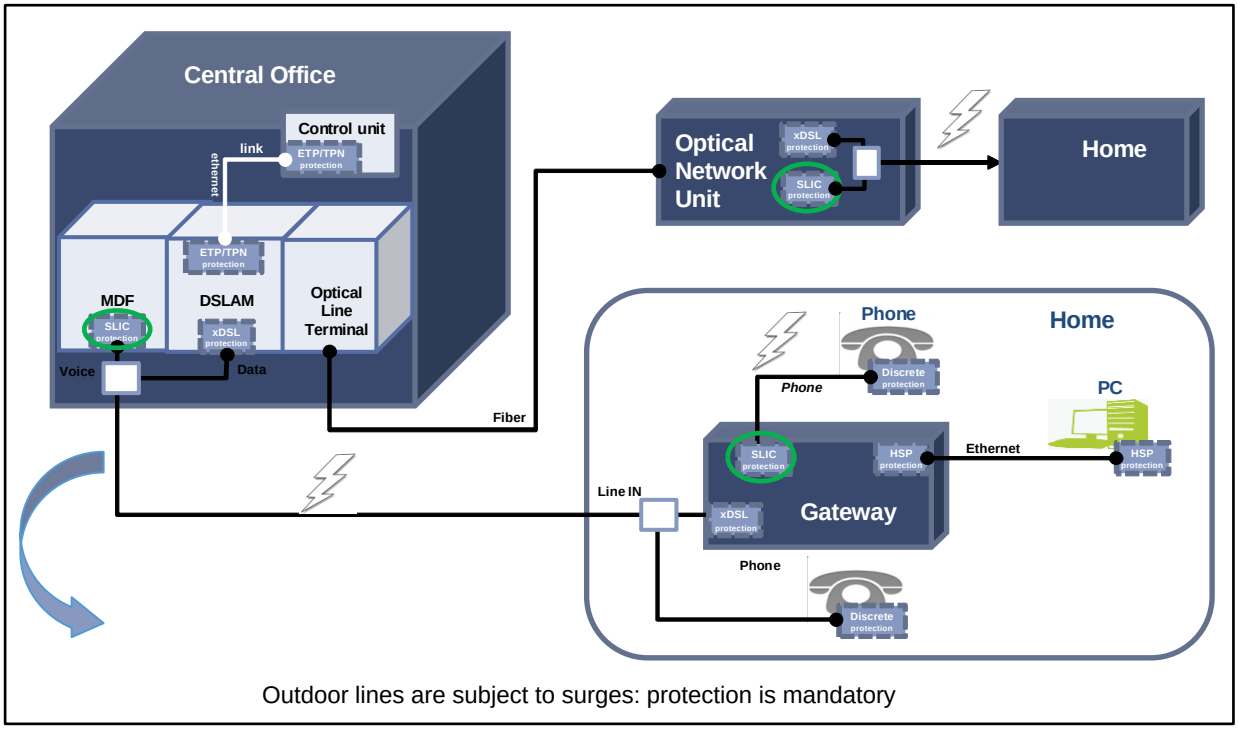
Despite the boom in digital technology and wireless systems, Telecom analog lines managed by SLICs remain the most commonly used method to carry voice communication around the world. These lines are simple and cost-effective, but are subject to overvoltages.

These transients are largely due to three types of disturbances:

- Atmospheric effects (lightning)
- 50/60 Hz mains power lines
- Electrostatic discharge (ESD)

The figure below shows the electrical stress locations.

**Figure 1: Telecom environment**




Outdoor lines are subject to surges: protection is mandatory

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# 1 Overview

Nowadays, simulations of these disturbances are well-defined in national or worldwide standards. According to these standards, telecommunication circuits must withstand various levels of disturbances and additional SLIC protection devices are mandatory. As far as cost-effectiveness and space saving are concerned, ST has introduced a new line card protection, the LCP154DJF to comply with ITU-T K.20/21/45 and GR-1089–CORE standards. This is the strongest LCP on the market.

As explained in application note AN2053, telecommunication lines need to be protected against electrical disturbances. The LCP crowbar concept is the widespread efficient SLIC protection used by telecommunication makers. The above-mentioned application note explains how this family of protection (see sections 2 and 3) works.

Telecom infrastructure equipment must comply with some standards such as GR-1089-CORE (Telcordia) and ITU-T K series for disturbances. These standards are the main worldwide lightning surge and power cross contact standards, dedicated to several telecommunication applications (central office Telecom line cards, extra and intra-building applications, customer premise equipment, etc.).

Protection devices must withstand various stress levels and usually, a resistor or a PTC needs to be added through the TIP and RING lines (see AN2053). The table below shows frequently used surges and power cross tests without failure (criterion A) for ITU-T K (recommendations) and GR-1089-CORE (requirements) standards (this table is not exhaustive).

**Table 1: Frequently used electrical surges (ITU-T K recommendations and GR-1089 requirements)**

| Standard | Surge | Total series R | Voltage basic / enhanced level<br>Maximum peak current per line<br>Topology (transverse / longitudinal) | |
|---|---|---|---|---|
| ITU-T K | 10/700 µs (voltage)<br>5/310 µs (current) | 15 Ω + 25 Ω | 4 kV<br>100 A<br>transverse and longitudinal | 6 kV<br>110 A<br>longitudinal |
| GR-1089 | 10/1000 µs (voltage)<br>10/1000 µs (current) | 10 Ω | 1 kV<br>100 A<br>transverse and longitudinal | |
| | 2/10 µs (voltage)<br>2/10 µs (current) | 5 Ω | 2.5 kV<br>500 A<br>transverse and longitudinal | |

**Table 2: Frequently used power cross (ITU-T K recommendations and GR-1089-CORE requirements)**

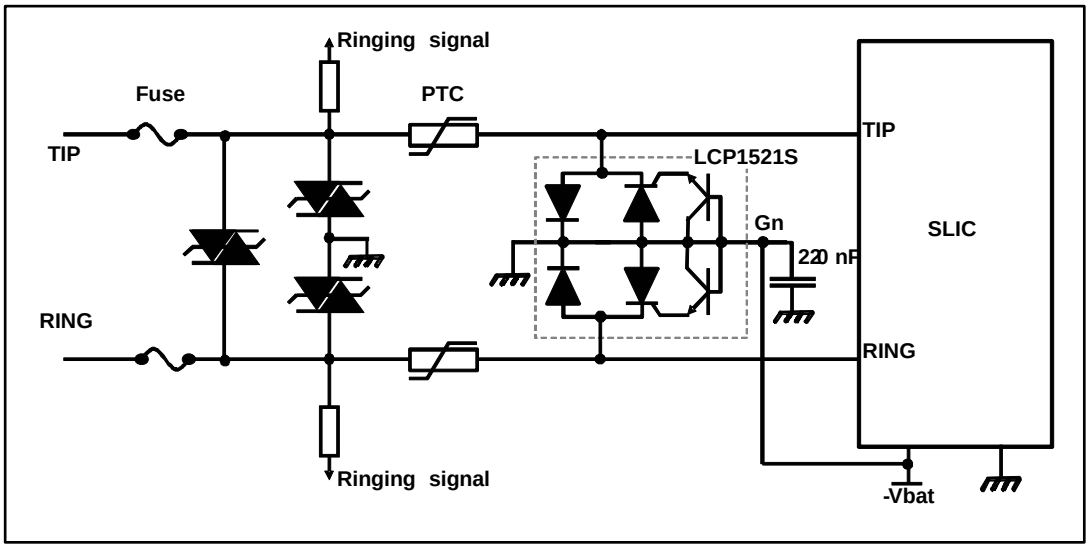
| Standard | Power cross<br>Voltage basic or enhanced level<br>duration | Total series R | Current per line<br>Topology<br>(transverse / longitudinal) |
|---|---|---|---|
| ITU-T K | 600 Vrms<br>1 s | 600 Ω | 1 Arms<br>transverse and longitudinal |
| | 230 Vrms<br>900 s | 160 Ω | 1.4 Arms<br>transverse and longitudinal |
| GR-1089 | 1000 Vrms<br>1 s | 1000 Ω | 1 Arms<br>transverse and longitudinal |
| | 425 Vrms<br>4 s | 850 Ω | 0.5 Arms<br>transverse and longitudinal |

To be compliant with these standards, it requires on-board protection devices, which are not negligible in terms of PCB area (see *Figure 2: "Current solution for SLIC electrical stress protection"*). On the other hand, there is a trend to implement more and more lines per board, then space saving is important.

# 2 Current and new solutions

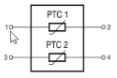
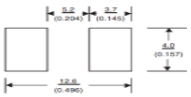
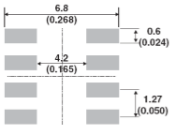
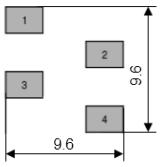
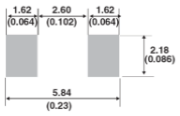
The figure below shows the current topology. It uses 8 components: the LCP1521S + 2 x PTC (250V/3A) + 3 x Trisil + 2 fuses.

**Figure 2: Current solution for SLIC electrical stress protection**



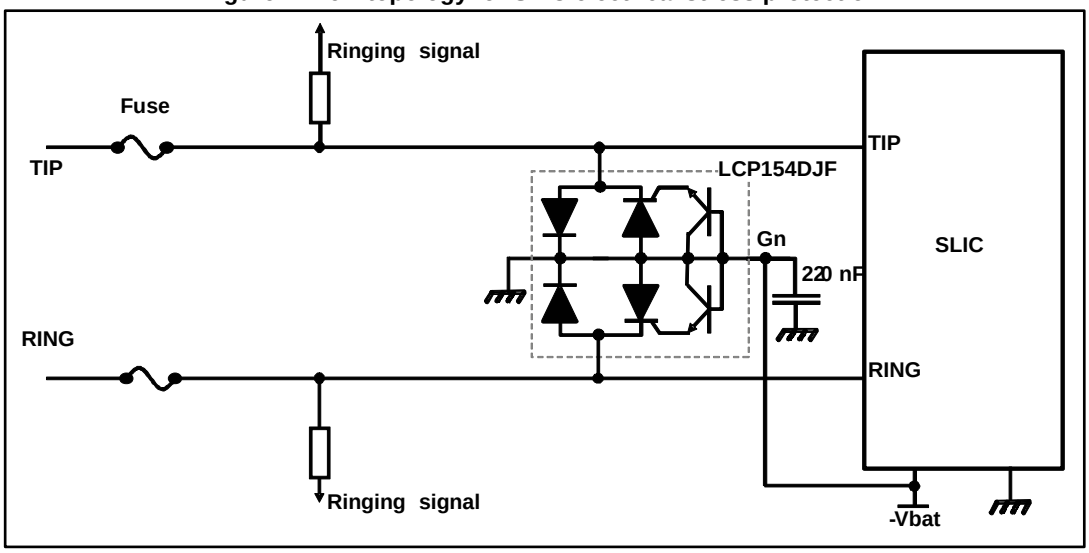

As shown in the figure below, the footprint of each device leads to a PCB area of 260 mm².

**Figure 3: Footprint surface for the current solution**

| | Fuse  | LCP1521S  | PTC  | SMB Trisil  |
|---|---|---|---|---|
| Footprint |  |  |  |  |
| Surface on PCB | 50.4 mm² | 30 mm² | 92 mm² | 12.7 mm² |
| Number of part | x 2 | x 1 | x 1 | x 3 |
| Total surface on PCB | = 100 mm² | = 30 mm² | = 92 mm² | 38 mm² |

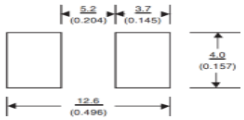
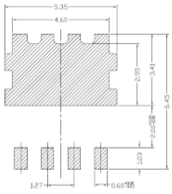
The new LCP154DJF withstands all standards whatever voltage level and schematic configuration (metallic and longitudinal see figure 3 from AN2053) without any resistor or PTC in serial. The figure below shows the new topology. With its high surge peak current capability and power cross withstanding, the LCP154DJF allows the number of components to be limited to 3 (the LCP154DJF + 2 fuses) instead of 8 components.

**Figure 4: New topology for SLIC electrical stress protection**




This new solution gives a 50% space saving on the PCB with only 134 mm² as shown in the figure below.

**Figure 5: Footprint area for the new solution topology**

| | Fuse  | LCP154DJF = LCP1521S + PTC + SMB Trisil |
|---|---|---|
| Footprint |  |  |
| Surface on PCB | 50.4 mm² | 34 mm² |
| Number of part | x 2 | x 1 |
| Total surface on PCB | = 100 mm² | 34mm² |

In addition, the LCP154DJF package is compliant with clearance requirements as defined in IEC 60950.

# 3 The LCP154DJF tests: lightning surges and power cross (or induction)

## 3.1 Standard lightning surge tests

The two schematics below have been used for all surge measurements made in the following pages. They come from ITU-T K and GR-1089-CORE standards.

**Figure 6: ITU-T K.20 surge schematic**

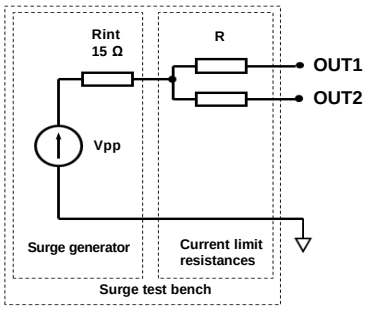



**Figure 7: GR-1089-CORE surge schematic**

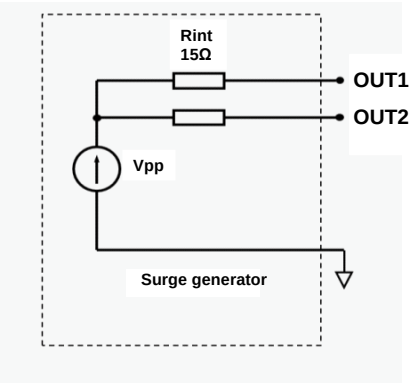



**Figure 8: Surge circuit**

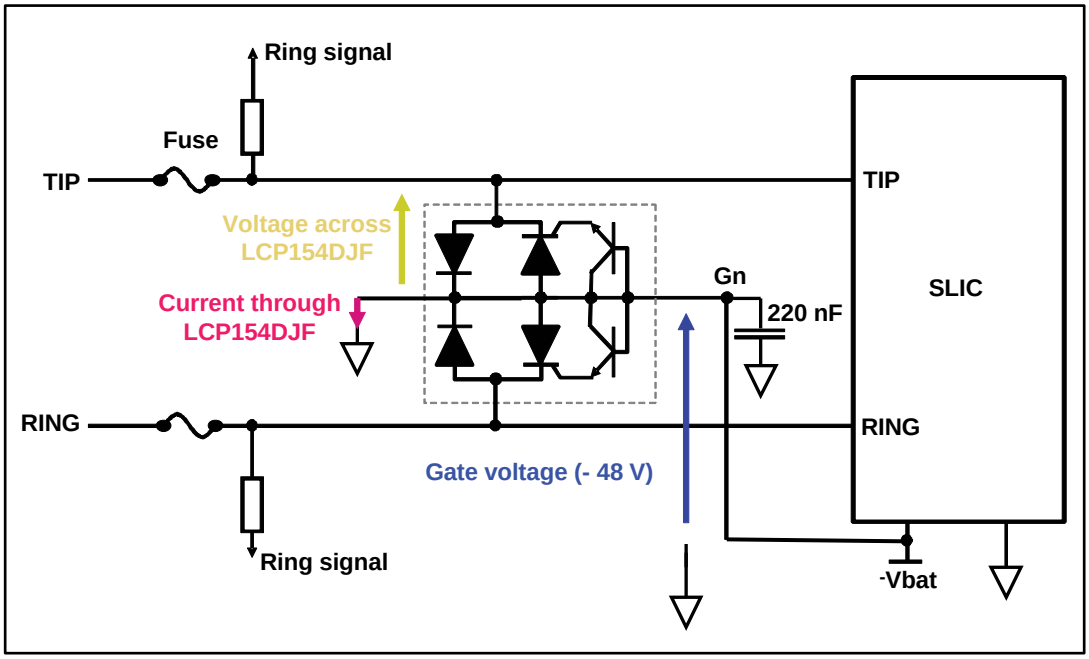


**Table 3: Test configurations**

| Test | Connection |
|---|---|
| Metallic (transverse) | Test 1: OUT1 to TIP; RING to GND (positive and negative surges)<br>Test 2: OUT1 to RING; TIP to GND (positive and negative surges) |
| Longitudinal | OUT1 to TIP; OUT2 to RING (positive and negative surges) |

The LCP154DJF current has been measured through the GND pin so it is equal to $I_{TIP}$ + $I_{RING}$. The standard defines the acceptance criterion of these tests as A: “the equipment continues operating properly after the test”. So, no component should be damaged after surges.

For positive surge, the diode of the LCP154DJF runs: the maximum voltage across the SLIC protection is the peak forward voltage ($V_{FP}$) during the surge. For negative surge, the thyristor turns on when negative voltage has reached the battery voltage adding the $V_{DGL}$ overvoltage. When the thyristor is turned on, voltage across SLIC protection is equal to ON-state voltage.

### 3.1.1 Frequently used surge waveforms (ITU-T K.20)

During these tests, a surge generator of combined 10/700 µs voltage waveforms and 5/310 µs current waveforms is used. Neither external PTC nor serial resistance has been plugged in.

The figures below show the remaining voltage across the LCP154DJF during +/- 4 kV 10/700 µs ITU-T K.20 surges in the metallic configuration. The peak current reaches 100 A through the SLIC protection (104 A peak measured on the current waveform (red curve)).

**Figure 9: Positive 4 kV surge response in metallic configuration induces 4 V $V_{FP}$**

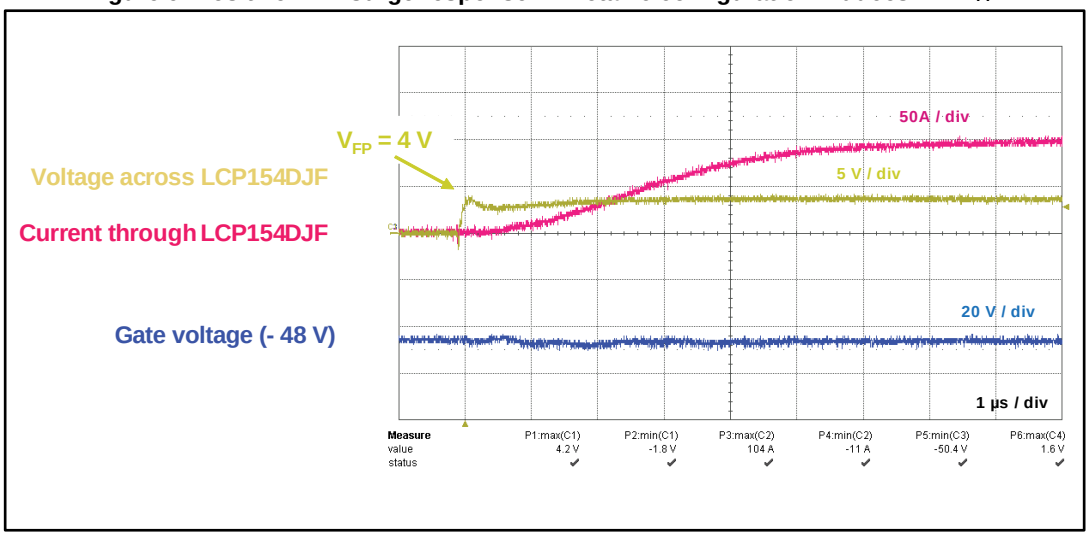
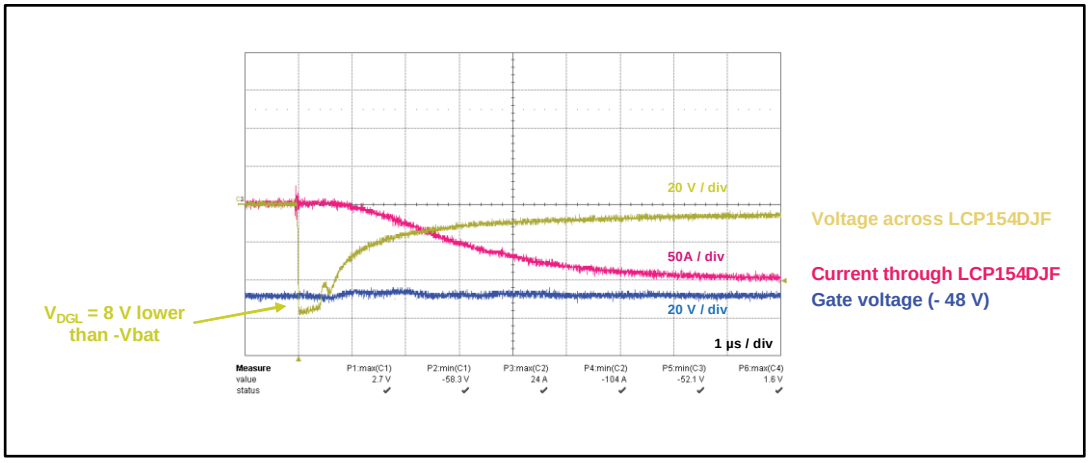


**Figure 10: Negative 4 kV surge response in metallic configuration induces 8 V $V_{DGL}$**




The following figures show the remaining voltage across the LCP154DJF during +/- 4 kV 10/700 µs ITU-T K.20 surges in the longitudinal configuration. The total current is split into both lines and reaches +/- 158 A peak current (measured value on red curve) through the SLIC protection. The calculated value gives around 150 A peak. So, each line has to withstand around 75 A peak current (calculated value).

**Figure 11: Positive 4 kV surge response in longitudinal configuration causes 4 V $V_{FP}$**

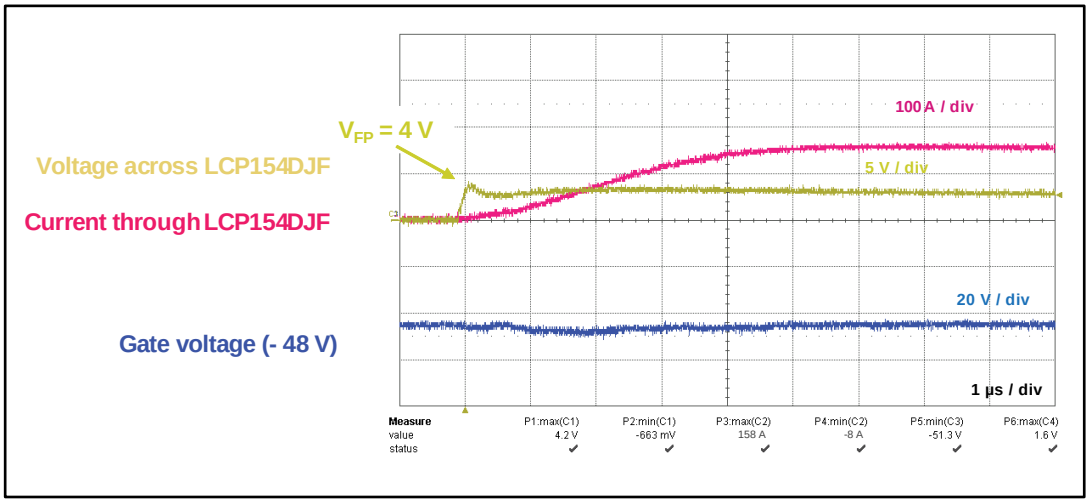
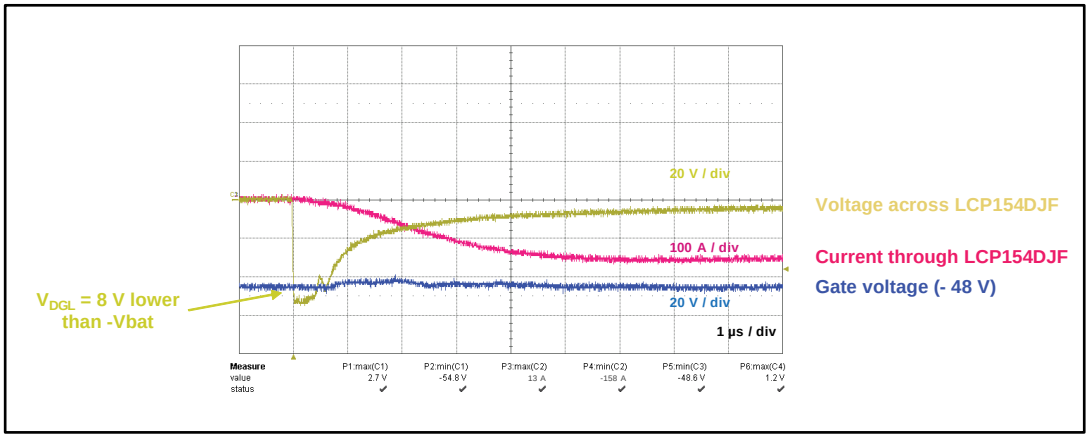



**Figure 12: Negative 4 kV surge response in longitudinal configuration induces 8 V $V_{DGL}$**



The figures below show the remaining voltage across the LCP154DJF during +/- 6 kV 10/700 µs ITU-T K.20 surges in the metallic configuration. The peak current reaches 150 A through the SLIC protection (152 A and -148 A measured on red curves). This configuration has been tested on one line even if it is required only for multiple lines by the standard.

Measurements show that the LCP154DJF can withstand the highest peak surge current in one line without any damage.

**Figure 13: Positive 6 kV surge response in metallic configuration causes 5 V $V_{FP}$**

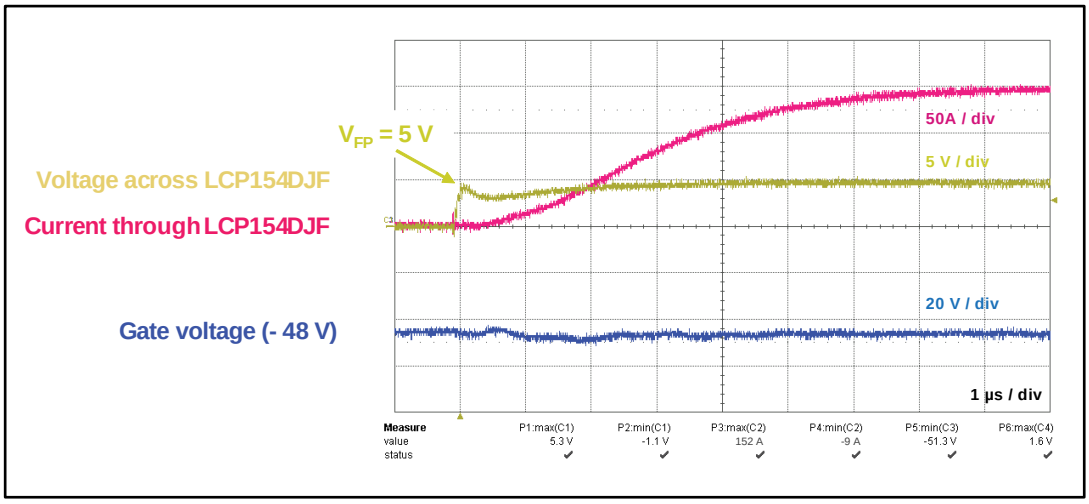
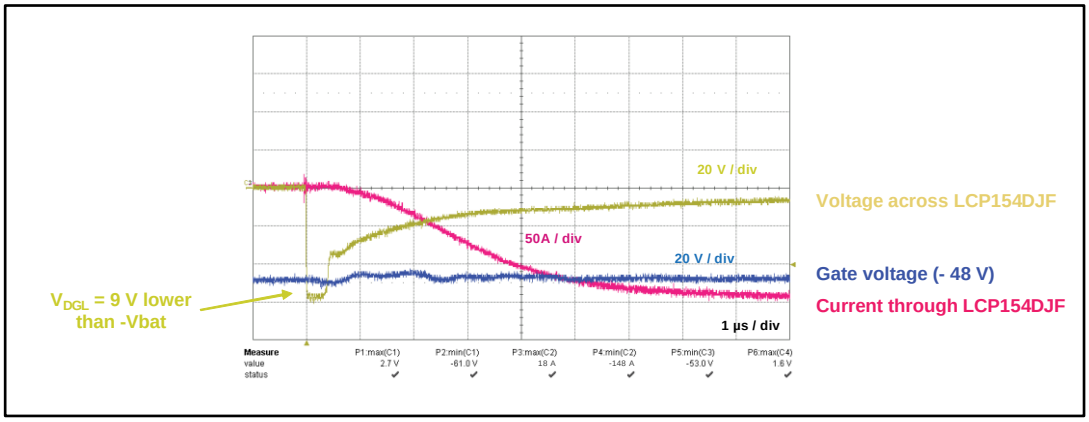



**Figure 14: Negative 6 kV surge response in metallic configuration causes 9 V $V_{DGL}$**




The following figures show the voltage across the LCP154DJF during +/- 6 kV 10/700 µs ITU-T K.20 surges in the longitudinal configuration. The total current is split into both lines and reaches 227 A and -223 A on red curves (218 A peak calculated value) through the SLIC protection. So, each line has to withstand 109 A peak current (calculated value).

**Figure 15: Positive 6 kV surge response in longitudinal configuration induces 5 V $V_{FP}$**

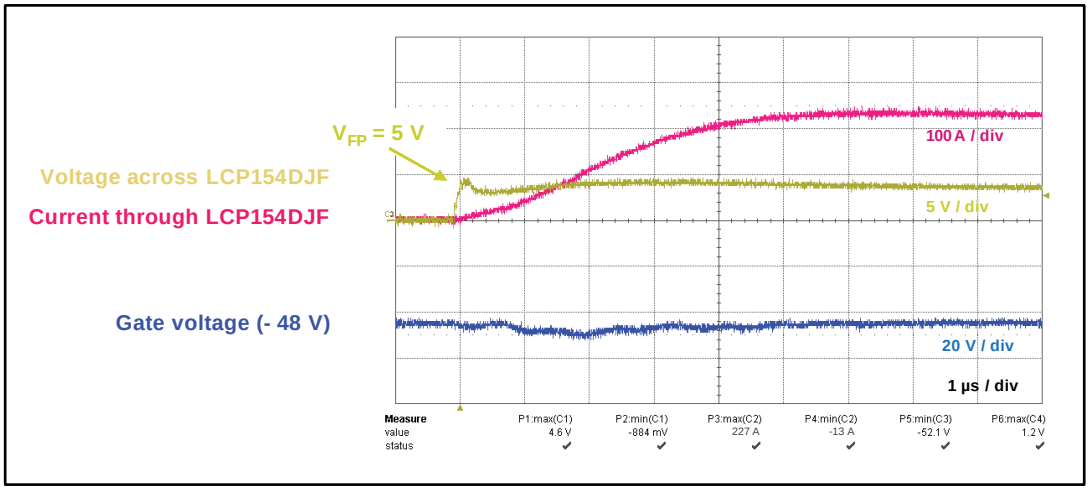
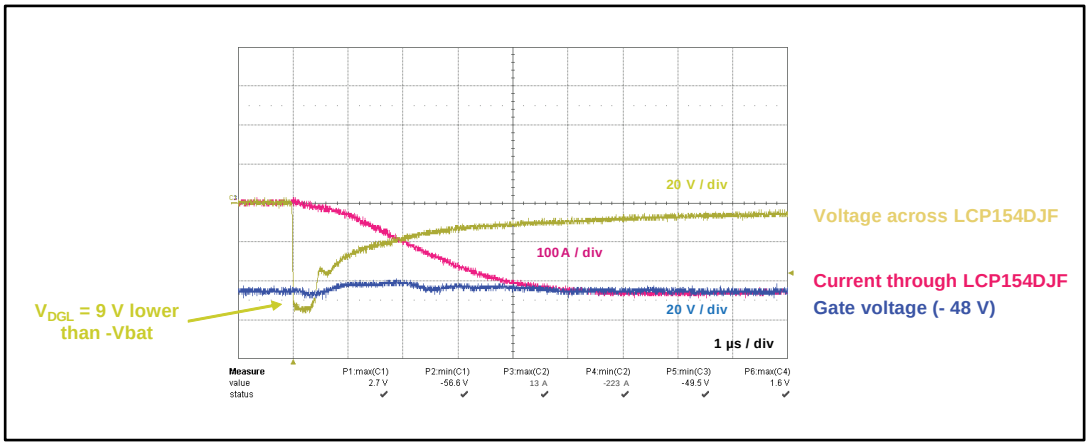



**Figure 16: Negative 6 kV surge response in longitudinal configuration induces 9 V $V_{DGL}$**




During these 10/700 µs surges, gate voltage remains stable and criterion A is respected: no component is damaged after surges.

### 3.1.2 Frequently used surge waveforms (GR-1089-CORE)

During these tests, a 10/1000 µs surge generator is used and neither external PTC nor serial resistance has been plugged in.

The figures below show the voltage across the LCP154DJF during +/- 1 kV 10/1000 µs GR-1089-CORE surges in the metallic configuration. The peak current reaches 100 A (+/- 98 A measured on red curves) through the SLIC protection.

**Figure 17: Positive 1 kV surge response in metallic configuration induces 4 V $V_{FP}$**

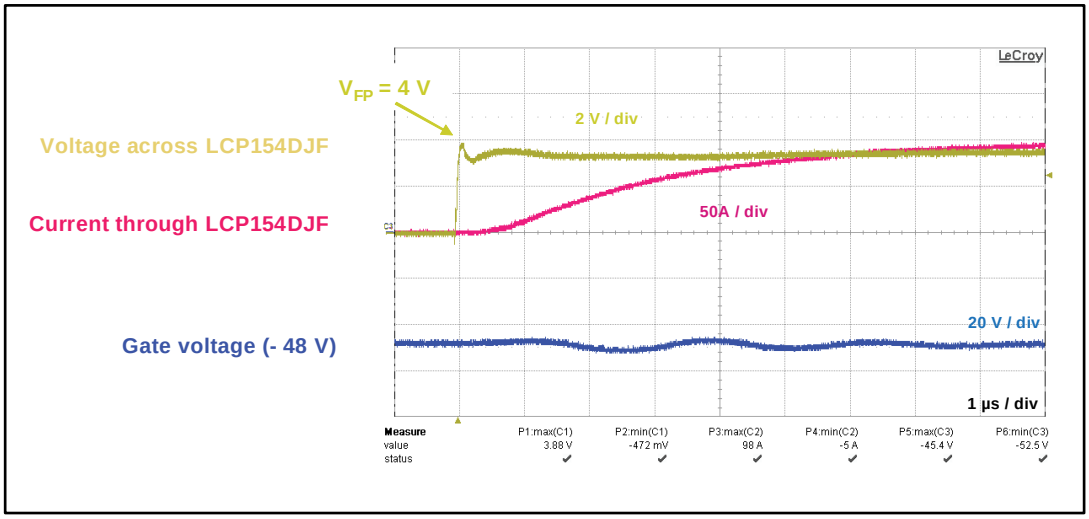
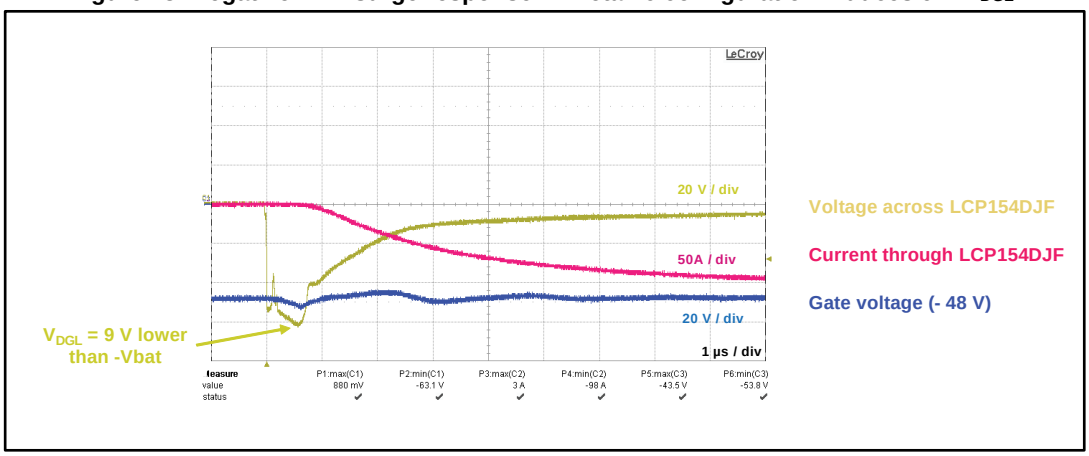



**Figure 18: Negative 1 kV surge response in metallic configuration induces 9 V $V_{DGL}$**




The figures that follow show the voltage across the LCP154DJF during +/- 1 kV 10/1000 µs GR-1089-CORE surges in the longitudinal configuration. The total current is split into both lines and reaches +/- 203 A on red curves (200 A peak calculated value) through the SLIC protection. So, each line must withstand 100 A peak current (calculated value).

**Figure 19: Positive 1 kV surge response in longitudinal configuration induces 4 V $V_{FP}$**

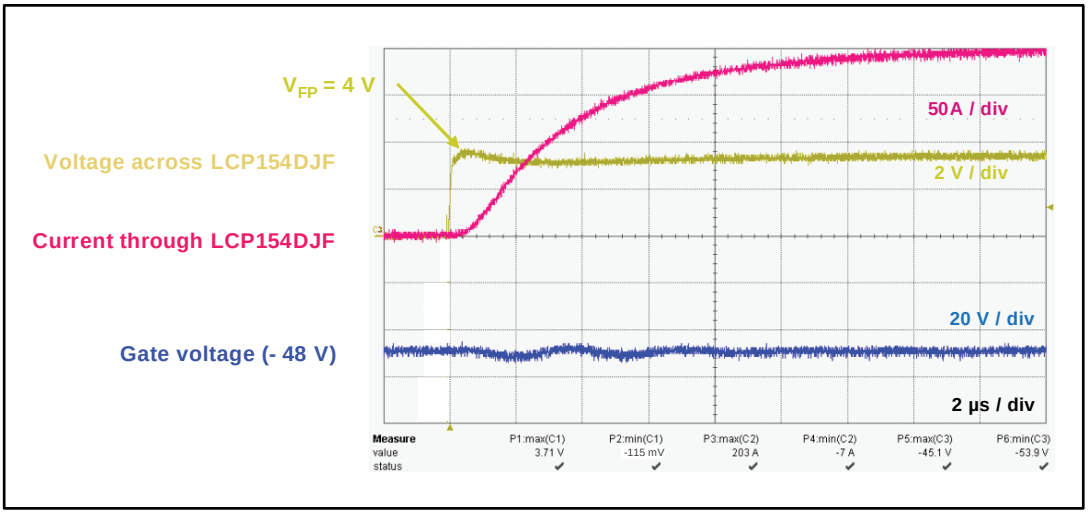
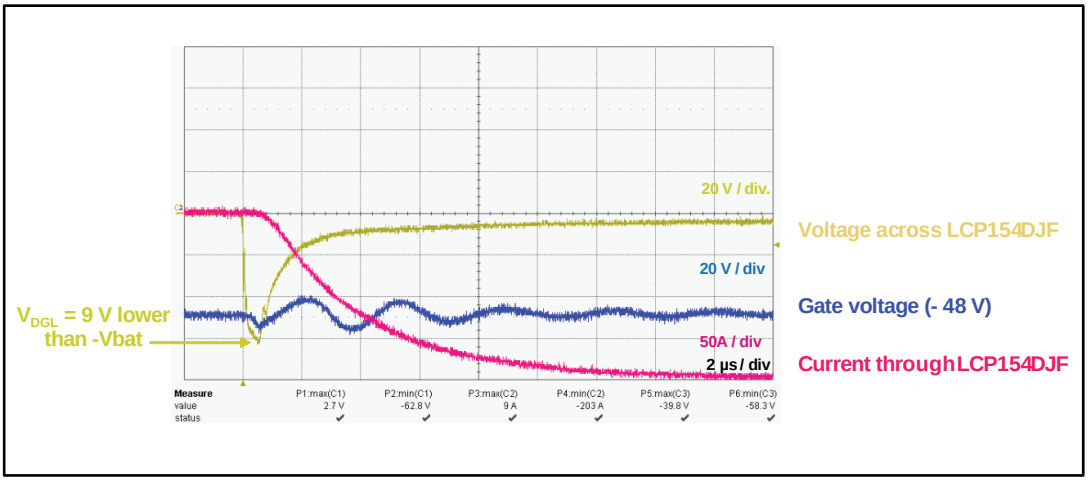



**Figure 20: Negative 1 kV surge response in longitudinal configuration induces 9 V $V_{DGL}$**




During these 10/1000 µs surges, the gate voltage waveform is slightly affected. The criterion A is respected and no component is damaged after surges.

During next tests, a 2/10 µs surge generator is used and neither external PTC nor serial resistance has been plugged in.

The figures below show the voltage across the LCP154DJF during +/- 2.5 kV 2/10 µs GR-1089-CORE surges in the metallic configuration. The peak current reaches 500 A (+ 509 A and – 514 A measured on red curves) through the SLIC protection.

**Figure 21: Positive 2.5 kV surge response in metallic configuration induces 14 V $V_{FP}$**

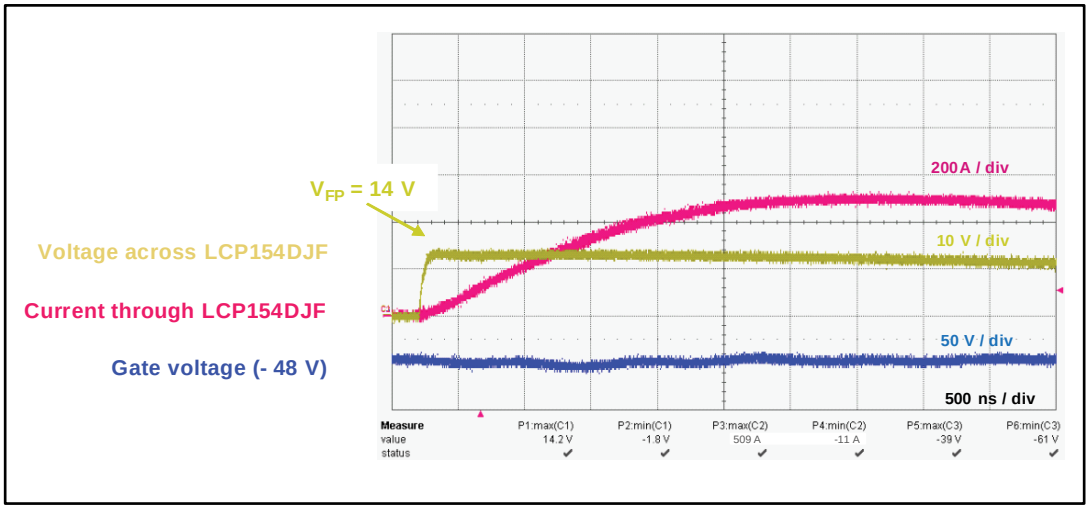
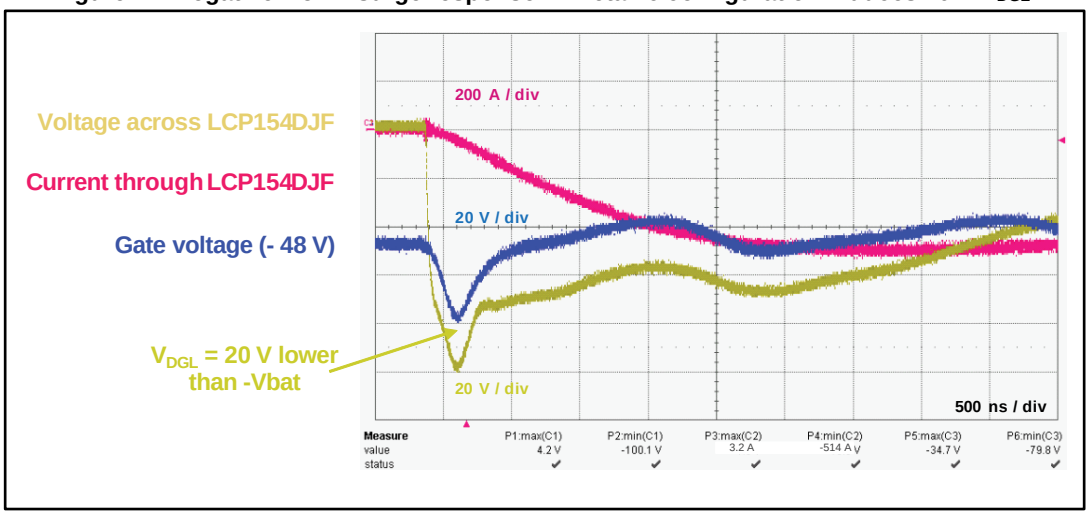



**Figure 22: Negative 2.5 kV surge response in metallic configuration induces 20 V $V_{DGL}$**




The figures below show the voltage across the LCP154DJF during +/- 2.5 kV 2/10 µs GR-1089-CORE surges in the longitudinal configuration. Total current is split into both lines and reaches + 1032 A and - 1028 A on red curves (1000 A peak calculated value) through the SLIC protection. So, each line has to withstand 500 A peak current (calculated value).

**Figure 23: Positive 2.5 kV surge response in longitudinal configuration induces 15 V $V_{FP}$**

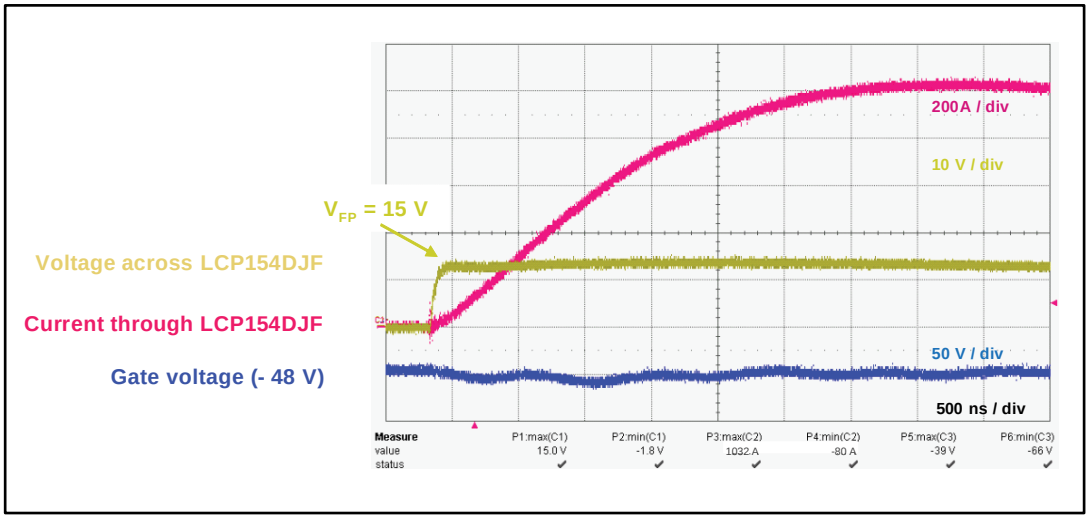
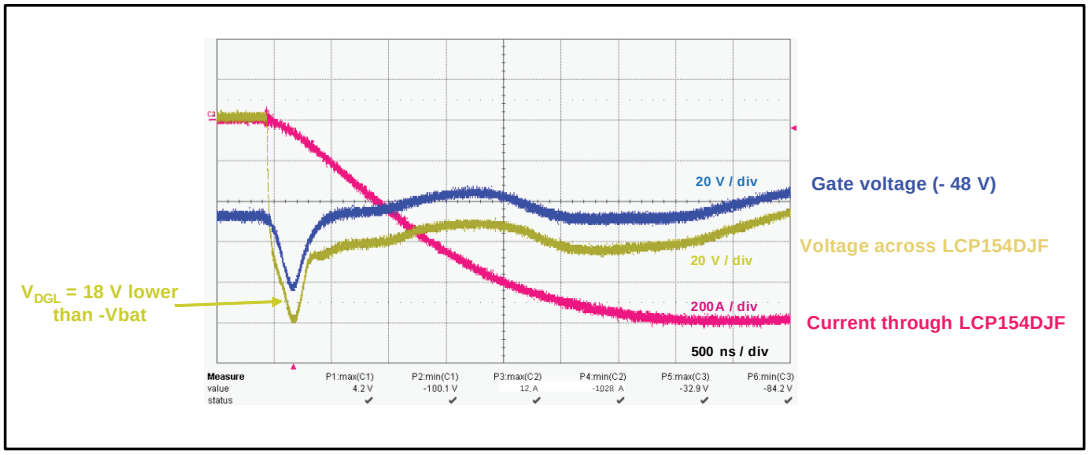



**Figure 24: Negative 2.5 kV surge response in longitudinal configuration induces 18 V $V_{DGL}$**

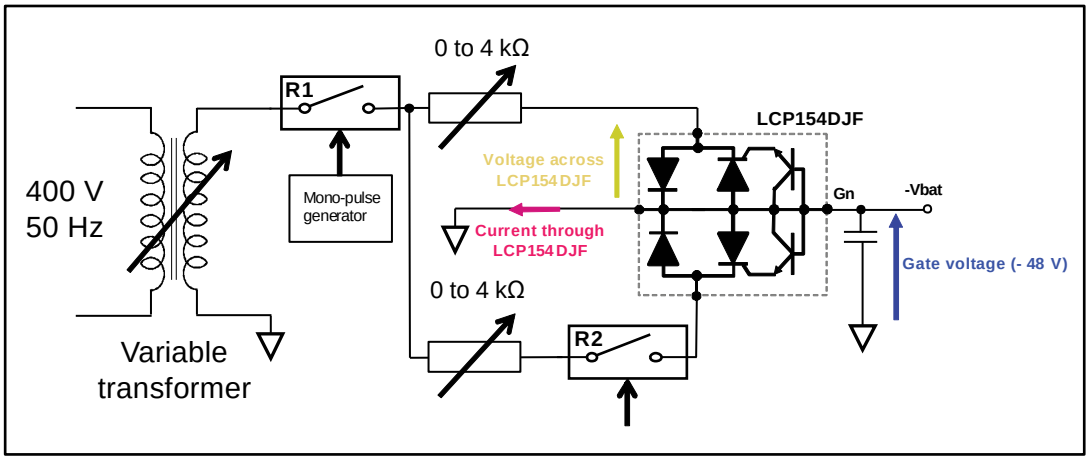



During these 2/10 µs surges, the gate voltage waveform is affected due to high di/dt and dV/dt applied across the LCP154DJF. The criterion A is respected and no component is damaged after surges.

## 3.2 Power cross (or induction) tests

The following figure shows the circuit used for power cross (or induction) tests.

**Figure 25: Power cross test schematic**



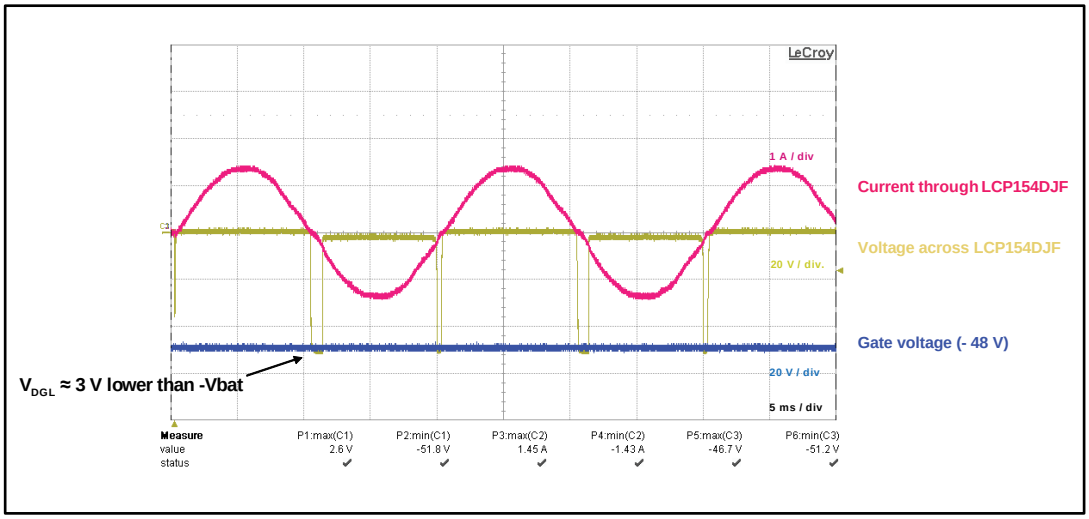

The main voltage 400 V 50 Hz is applied to the test assembly through a variable transformer, which is able to set the required rms voltage. A first relay R1 driven by a monopulse generator allows the conducting time to be adjusted. The current through the device is set by a series resistor. The second relay R2 could select the metallic or longitudinal mode configuration.

During ITU-T K.20 and GR-1089-CORE power cross (or induction) tests, neither external PTC nor serial resistance has been plugged in. For positive half sine wave, the diode of the LCP154DJF runs: voltage across the SLIC protection is the forward voltage of the diode. For negative half sine wave, the thyristor turns on when this negative voltage has reached the battery voltage. When the thyristor is turned on, voltage across SLIC protection drops to ON-state voltage.

### 3.2.1 Frequently used power cross waveforms (ITU-T K.20)

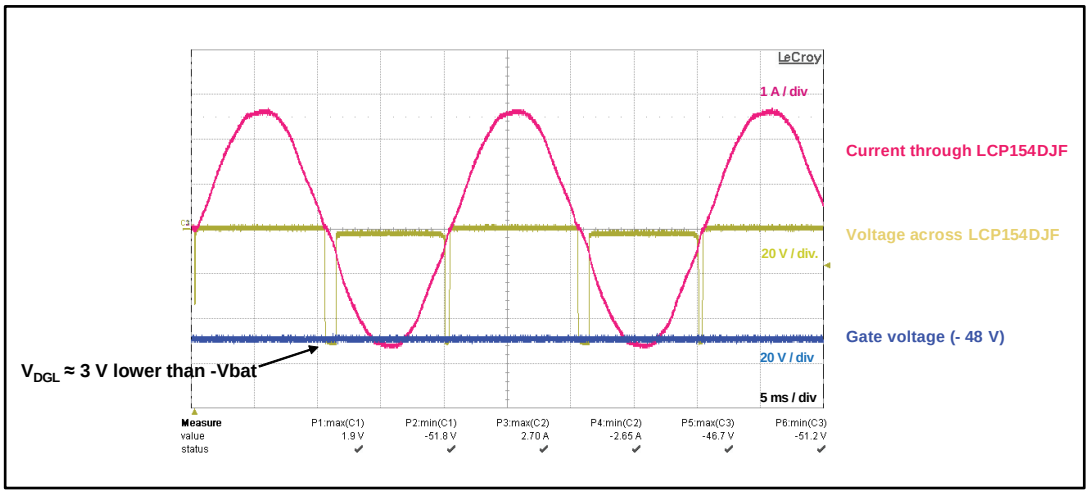
The two figures below show current and voltage across the LCP154DJF during 600 Vrms with a serial resistor equal to 600 Ω in metallic and longitudinal configurations. The test lasts 1 second.

**Figure 26: Power cross response in metallic configuration (600 Vrms)**



Only one line runs. The current through the LCP154DJF is around 1 Arms. In negative polarity, the thyristor turns off when the current is lower than the holding current ($I_H$) and the voltage reappears across the LCP154DJF.

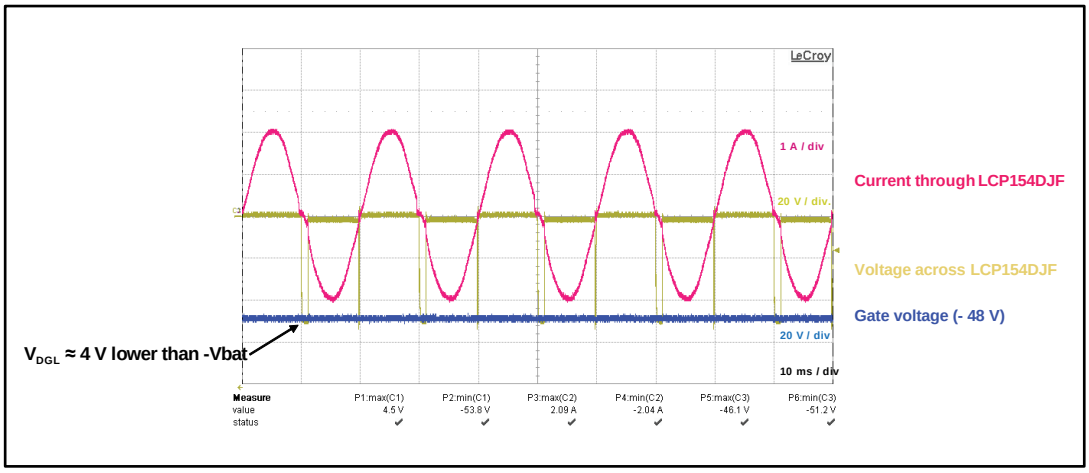
**Figure 27: Power cross response in longitudinal configuration**




In this case, both lines work. Total current is around 2 Arms.

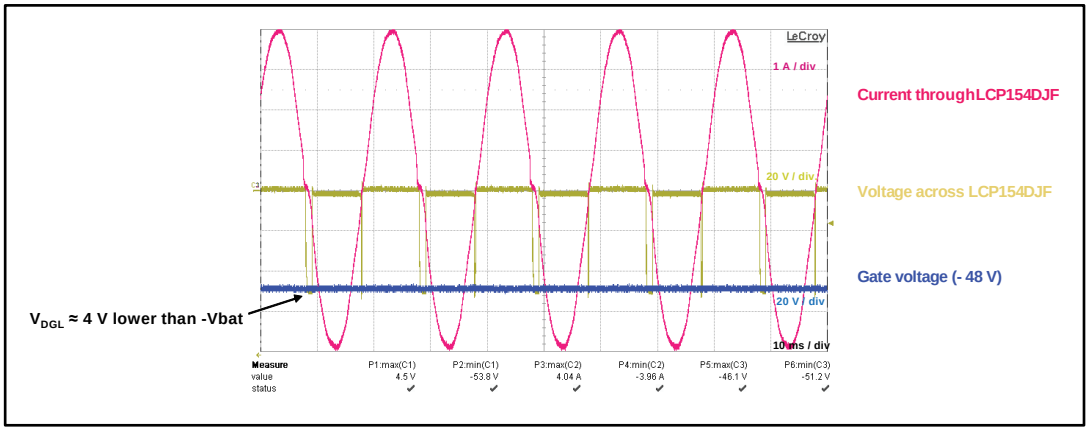
The next two figures show current and voltage across the LCP154DJF during 230 Vrms with a serial resistor equal to 160 Ω metallic and longitudinal configurations. The test lasts 900 seconds (15 minutes).

**Figure 28: Power cross response in metallic configuration (230 Vrms)**




Only one line runs. The current through the LCP154DJF is around 1.4 Arms.

**Figure 29: Power cross response in longitudinal configuration (230 Vrms)**

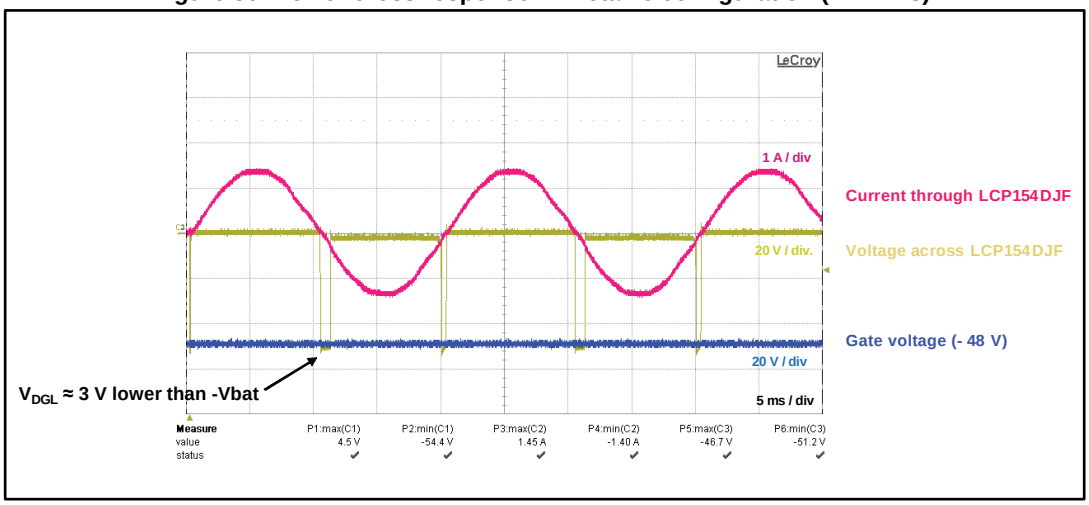



In this case, the 2 lines work. The total current is around 2.8 Arms.

### 3.2.2 Frequently used power cross waveforms (GR-1089-CORE)

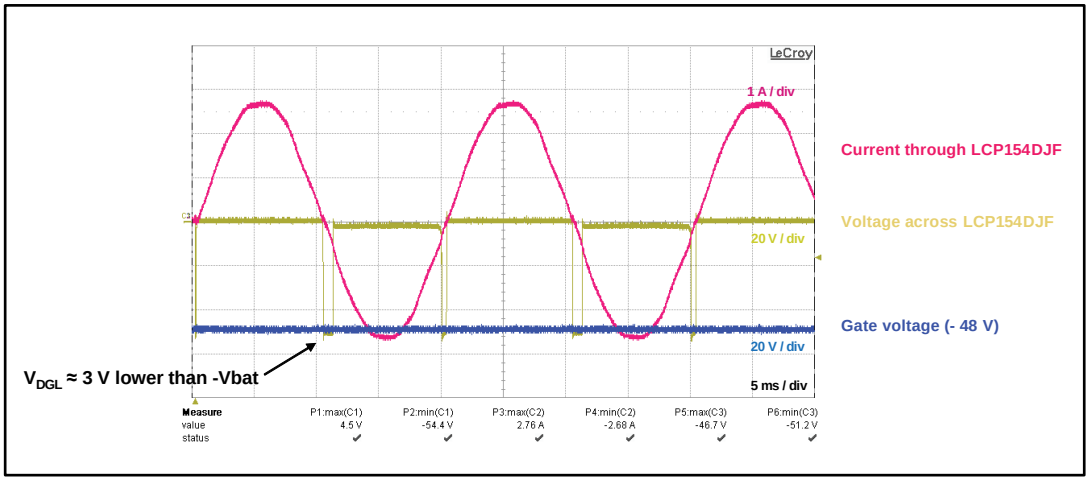
The two figures show current and voltage across the LCP154DJF during 1 kVrms. The series resistor is set to obtain 1 Arms through the line for the metallic configuration or in each line for longitudinal configurations. The series resistor value is 1 kΩ. The test lasts 1 second.

**Figure 30: Power cross response in metallic configuration (1 kVrms)**




Only one line runs. The current through the LCP154DJF is 1 Arms.

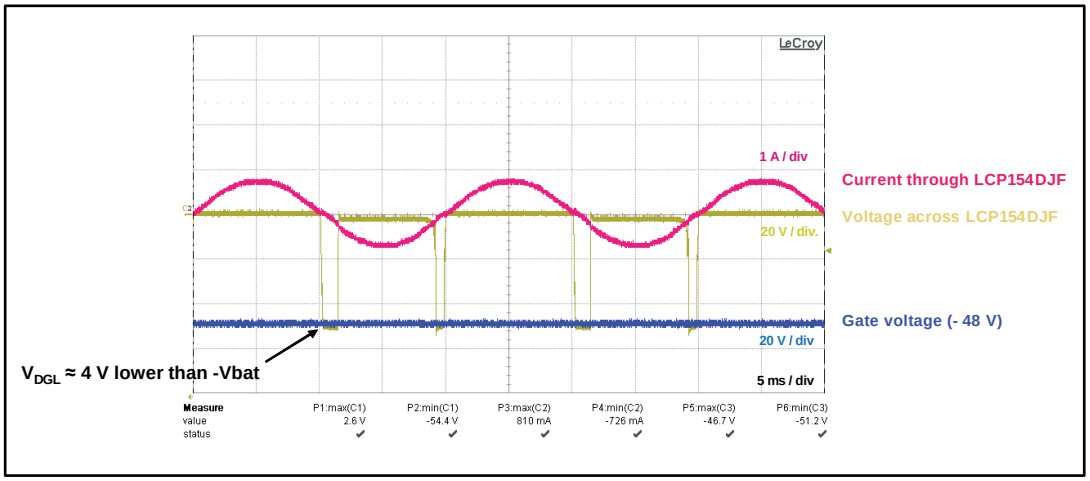
**Figure 31: Power cross response in longitudinal configuration (1 kVrms)**




In this case, both lines work. Total current is around 2 Arms.

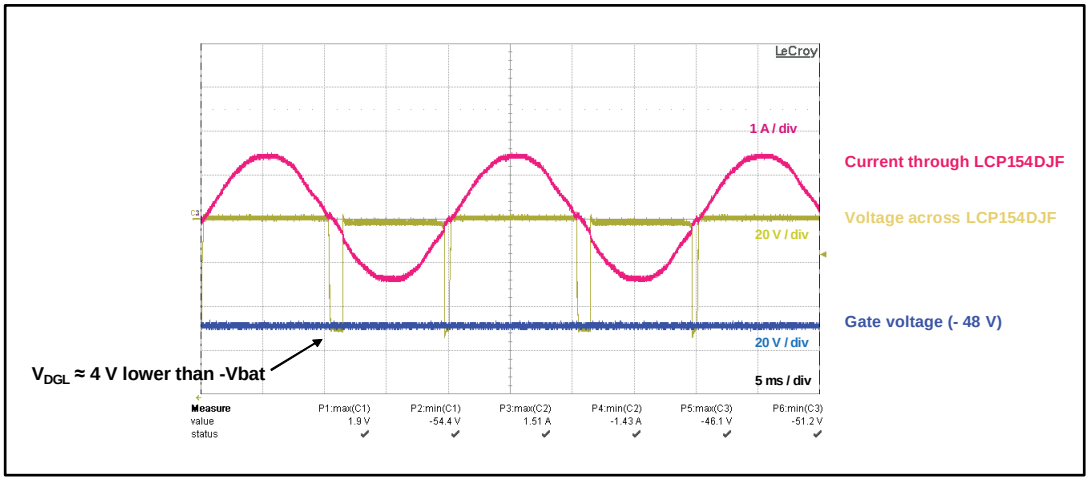
The next two figures show current and voltage across the LCP154DJF during 425 Vrms. The series resistor is set to obtain 0.5 Arms through the line for the metallic configuration or in each line for longitudinal configurations. The series resistor value is 850 Ω. The test lasts 4 s.

**Figure 32: Power cross response in metallic configuration (425 Vrms)**




Only one line runs. The current through the LCP154DJF is 0.5 Arms.

**Figure 33: Power cross response in longitudinal configuration (425 Vrms)**




In this case, the 2 lines work. The total current is around 1 Arms.

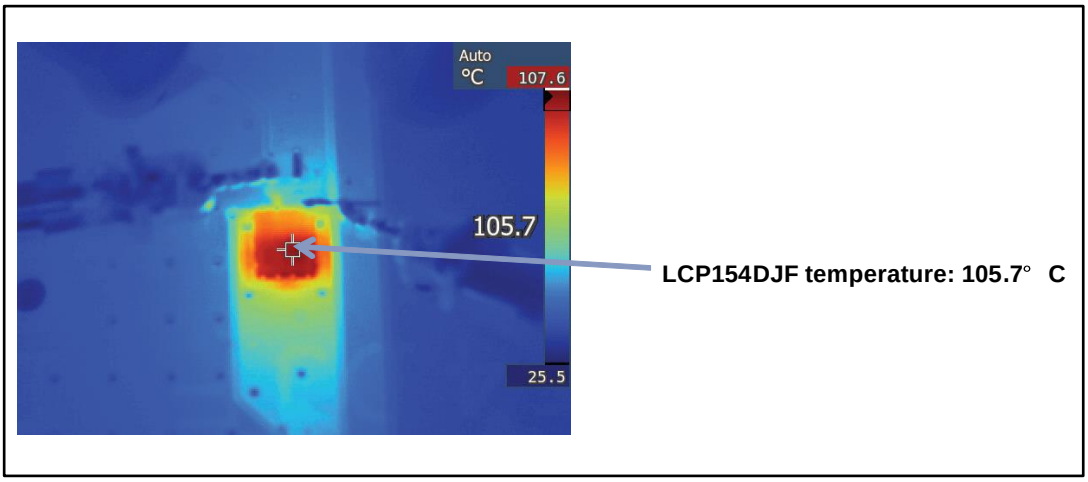
During tests, current and voltage waveforms have the same behavior for ITU-T K.20 and GR-1089-CORE, metallic and longitudinal tests. There is not any $V_{FP}$ as the slopes of voltage and current are low. $V_{DGL}$ is between 3 and 4 V.

# 4 The LCP154DJF temperature advantage

During power cross (or induction), new solution LCP154DJF device limits the maximum temperature value and expansion.

The following figure shows a temperature below 110 °C with around 1.4 Arms current power cross in the metallic mode after 15 minute running.

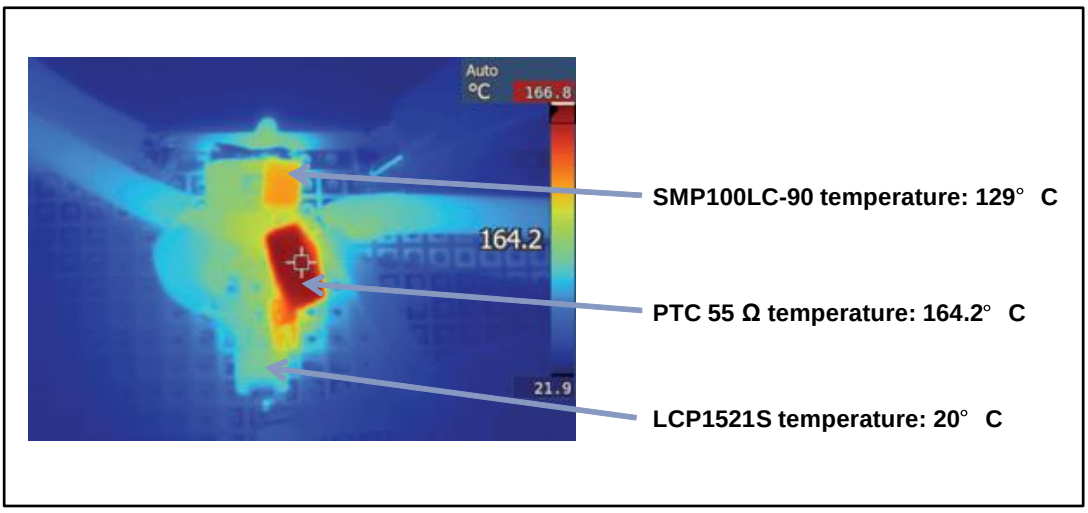
**Figure 34: LCP154DJF maximum temperature after 15 minutes with 1.4 Arms current power cross in metallic mode**




To make a comparison with the usual solution for SLIC protection (*Figure 2: "Current solution for SLIC electrical stress protection"*), next figure shows the temperature spread among components (PTC 55 Ω, Trisil SMP100LC-90, LCP1521S).

At the same power conditions, temperature values are higher than the LCP154DJF in the figure above.

**Figure 35: Current solution for SLIC electrical stress protection with temperature through PTC 55 Ω, Trisil SMP100LC-90, LCP1521S after 15 minutes with 1.4 Arms current power cross in metallic mode**




In case of power cross, the LCP154DJF thermal dissipation capability allows temperature dissipation to be limited on the PCB and in the environment. So, ambient temperature is

lower with the LCP154DJF than with the current solution. With the LCP154DJF, Telecom circuits are more reliable, with a longer lifetime.

# 5 Clearance requirements

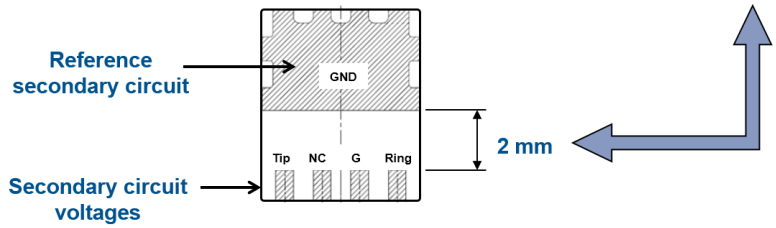
Telecommunication equipment is generally used:

- In an environment where there is only non-conductive pollution that might temporarily become conductive due to occasional condensation: this corresponds to pollution degree 2
- In a secondary circuit, which has not any direct connection to a primary circuit (directly connected to the AC mains supply) and derives its power from a transformer, converter or equivalent isolation device, or from a battery
- With a peak working voltage limited to 175 V (maximum voltage of the LCP154DJF)
- With a maximum transient voltage in secondary circuit equal to 4 kV (according to ITU-T K.20/21)

The figure below shows a table extracted from IEC 60950. As the peak working voltage (175 V on the TIP or RING) does not exceed the peak value of the AC mains supply voltage and is lower than 210 V, the highest transient overvoltage in the secondary circuit is 4 kV: 2 millimeters are required to be compliant with the insulation F level (functional insulation necessary for the correct working of the equipment).

**Figure 36: IEC60950 definition table 2K: minimum clearance in mm for insulation in primary and between primary and secondary circuits**

| Peak working voltage up to and including V | Mains transient voltage | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1500 V | | | | | | 2500 V | | | | | | 4000 V | | |
| | Pollution degree | | | | | | | | | | | | | | |
| | 1 and 2 | | | 3 | | | 1 and 2 | | | 3 | | | 1, 2 and 3 | | |
| | F | B/S | R | F | B/S | R | F | B/S | R | F | B/S | R | F | B/S | R |
| 71 | 0.4 | 1 | 2 | 0.8 | 1.3 | 2.6 | 1 | 2 | 4 | 1.3 | 2 | 4 | 2 | 3.2 | 6.4 |
| 210 | 0.5 | 1 | 2 | 0.8 | 1.3 | 2.6 | 1.4 | 2 | 4 | 1.5 | 2 | 4 | 2 | 3.2 | 6.4 |




Definitions:

- F: functional insulation
- B: basic insulation
- R: reinforced insulation
- 1: pollution degree 1 applies where there is not any pollution or only dry, non-conductive pollution occurs. The pollution has not any effect
- 2: pollution degree 2 applies where there is only non-conductive pollution that might temporarily become conductive due to occasional condensation
- 3: pollution degree 3 applies where a local environment within the equipment is subject to conductive pollution, or to dry non-conductive pollution that could become conductive due to expected condensation

As the LCP154DJF is used in secondary circuit, IEC60950 table 2M is the clearance reference but as the highest transient overvoltage is higher than 2.5 kV, the table 2M uses another table 2K, which is shown in the previous figure.

# 6 Series protections

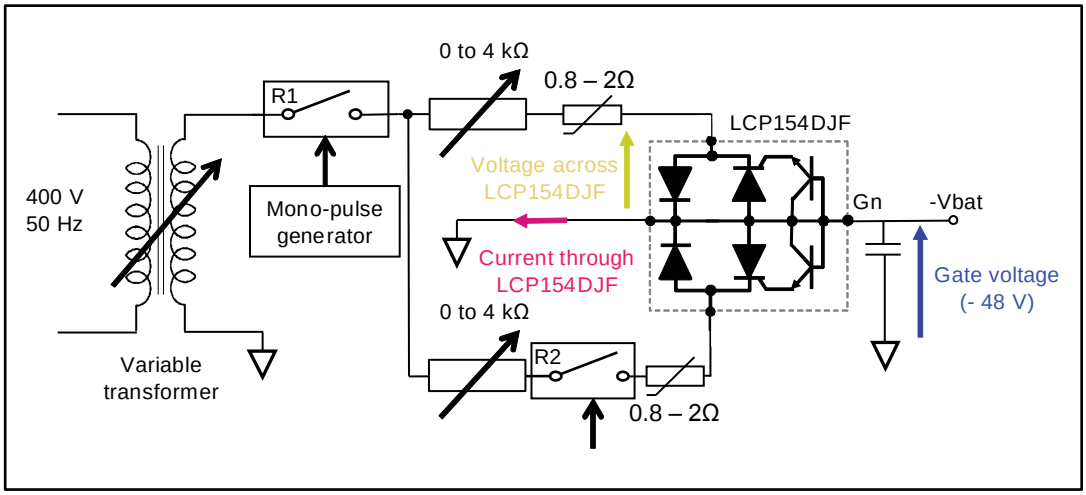
According to different countries, Telecom laws require series protection (fuses, resistances or PTCs) even if the SLIC protection withstands electrical constraints according to standards without series protection. One solution is to use a fuse but in case of high overcurrent, a human intervention is mandatory.

PTC in combination with the LCP154DJF can allow a very aggressive power cross (or power induction) level to be reached with the best acceptance criteria A without human intervention in case of high overcurrent. For example, ITU-T K.20, for basic and enhanced levels, only criterion B is required for U = 230 Vrms and series resistance = 80, 40, 20 and 10 Ω. In these cases, with series protection and the LCP154DJF, criteria A is reached.

With the same conditions, additional power cross tests have been performed with these extreme power cross conditions.

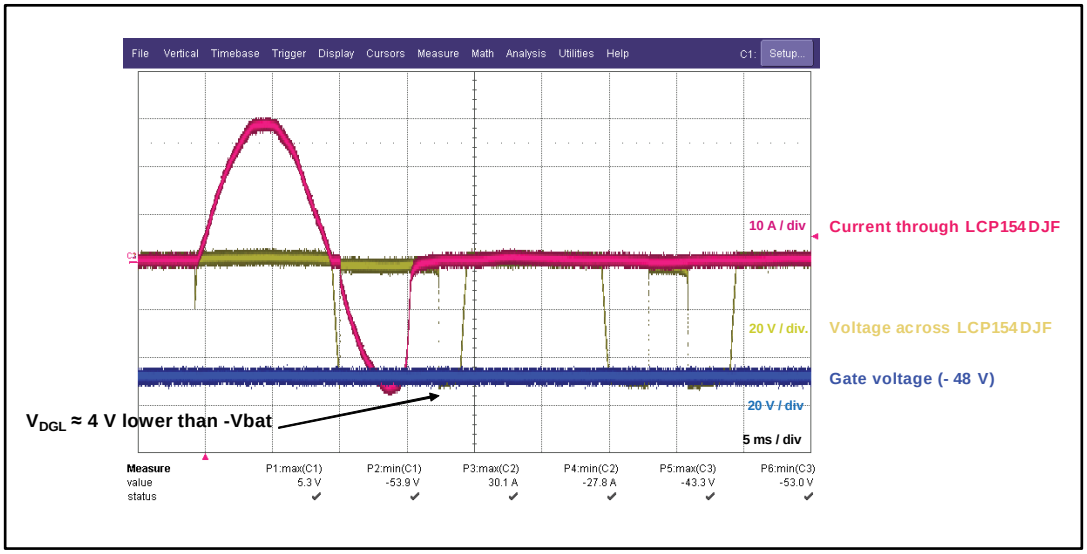
The same previous power cross circuit is used but a PTC (0.8 -2 Ω) is added to each line as shown by the figure below.

**Figure 37: Power cross test schematic with series PTC**




The figure below shows current and voltage across the LCP154DJF during 230 Vrms with a serial resistor equal to 10 Ω (the lower resistance value, the worse case for peak current) and PTC 0.8 – 2 Ω in the metallic configuration. This test lasts 15 minutes.

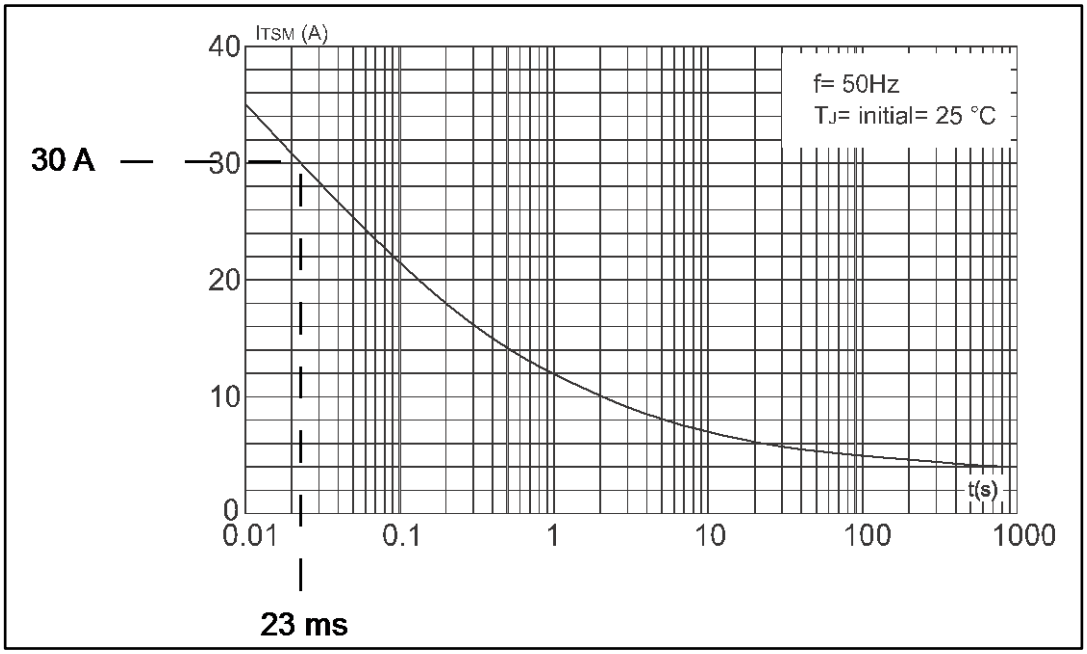
**Figure 38: Power cross response in metallic configuration (230 Vrms, R = 10 Ω and 1 PTC 0.8 -2 Ω in series)**




Only one line runs. The current through the LCP154DJF lasts around 15 ms and the peak current is around 30 A. After 15 ms, the current is limited closed to zero by PTC resistance value rise.

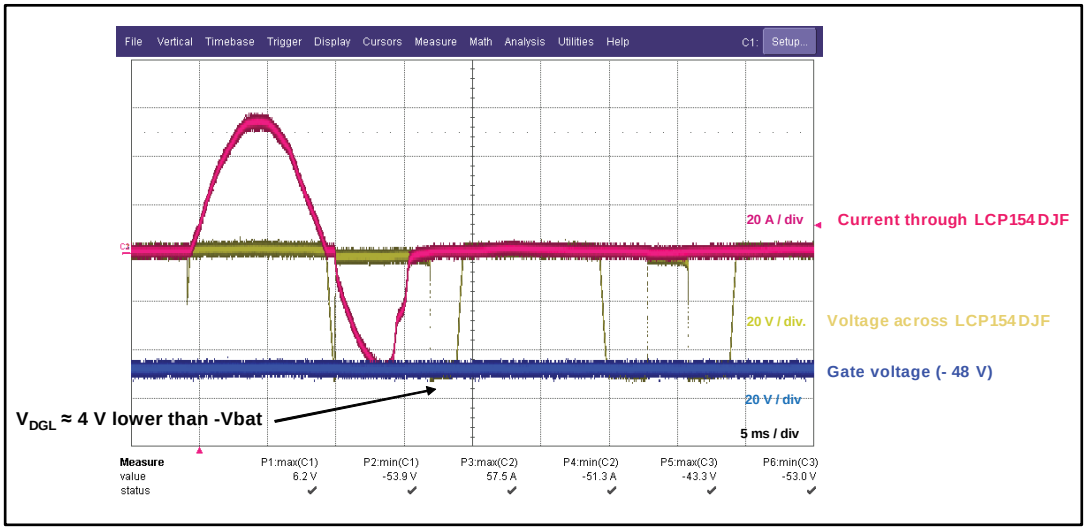
As shown by next figure, the LCP154DJF datasheet gives the $I_{TSM}$ surge capability: for 30 A peak current, the LCP154DJF withstands around 23 ms duration that is higher than 15 ms measured. So, the LCP154DJF is suitable to withstand the power contact 230 Vrms with R = 10 Ω and PTC 0.8 - 2 Ω in series.

**Figure 39: Surge peak current vs. duration (extract from the LCP154DJF datasheet)**




The figure below shows current and voltage across the LCP154DJF during 230 Vrms with a serial resistor equal to 10 Ω (the lower resistance value, the worse case for peak current) and PTC 0.8 – 2 Ω in longitudinal configurations. This test lasts 15 minutes.

**Figure 40: Power cross response in longitudinal configuration (230 Vrms, R = 10 Ω and 1 PTC 0.8 -2 Ω in series)**



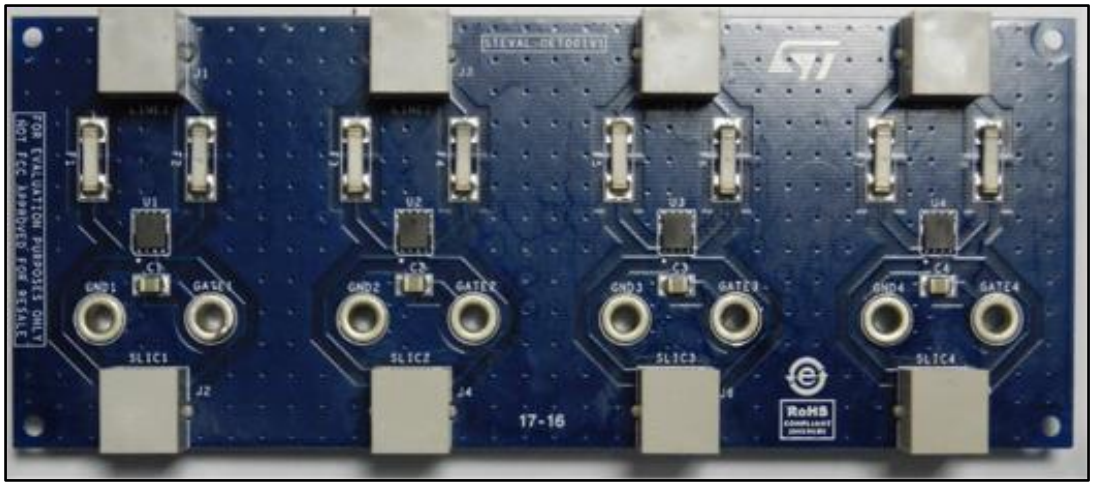

In this case, the 2 lines work. The total peak current is around 58 A which is split into both lines. So, each line withstands around 30 A as already measured in the metallic configuration. So, the LCP154DJF is suitable to withstand this stress as shown in the metallic study.

After 15 minutes for each configuration metallic and longitudinal test, the criterion A is respected and no component is damaged after this power cross (or power induction) test. There is not any $V_{FP}$ as the slopes of voltage and current are low. $V_{DGL}$ is equal to 4 V.

# 7 The LCP154DJF evaluation board

In order to easily verify the functionality of the LCP154DJF, an evaluation board is available. The board can be ordered from www.st.com: *www.st.com/steval-oet001v1*.

**Figure 41: LCP154DJF evaluation board**



# 8 Conclusions

To meet the electrical constraints according to standards (and even beyond surge standard with 6 kV applied to only 1 line (metallic mode)), the new LCP154DJF SLIC protection makes your board compliant with the following tests:

**Table 4: Summary of tests**

| Standard | Surge | Test |
|---|---|---|
| ITU-T K | 4 kV and 6 kV<br>10/700 µs (voltage)<br>5/310 µs (current) | Pass |
| GR-1089 | 1 kV, 100 A<br>10/1000 µs (voltage)<br>10/1000 µs (current) | Pass |
| GR-1089 | 2.5 kV, 500 A<br>2/10 µs (voltage)<br>2/10 µs (current) | Pass |
| ITU-T K | 600 Vrms, 600 Ω,1 s | Pass |
| ITU-T K | 230 Vrms, 160 Ω, 900 s | Pass |
| GR-1089 | 1000 Vrms, 1 A, 1 s | Pass |
| GR-1089 | 425 Vrms, 0.5 A, 4 s | Pass |

Moreover, this SLIC protection solution permits:

- Saving money and purchasing time by ordering 3 components only versus 8
- Implementing more lines per board for compact equipment (a complete integration)
- Being compliant with IEC 60950 thanks to the LCP154DJF package

# 9 Revision history

**Table 5: Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Jun-2017 | 1 | Initial release. |

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