

AN4896 Application note

15 W, 5 V output USB adapter using STCH02

Introduction

This application note describes a 15 W (5 V-3 A) wide range mains USB adapter demo board, based on STCH02, the new STMicroelectronics CC-mode primary sensing switching controller. The results of its bench evaluation are also shown.

The STCH02 is a current-mode quasi-resonant controller which combines a high-performance low-voltage PWM controller chip with a 650 V HV start-up cell in the same package.

The device provides constant output current (CC) regulation by using primary-sensing feedback: this eliminates the need of a dedicated current reference IC and of a current sensor, still maintaining quite accurate output current regulation.

The power supply is has an extremely high power density per watt, providing very high efficiency, low standby power (less than 10 mW), excellent EMI performances and a complete set of integrated protection features that considerably increase end-product safety and reliability.

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1 Test board: main features

The main features of the demonstration board are shown below.

Table 1: Demonstration board electrical specification

Parameter	Min.	Тур.	Max
AC Main Input voltage	90 V _{AC}		265 V _{AC}
Mains frequency	50 Hz		60 Hz
Output voltage	4.75 V	5 V	5.25 V
Output current		3.1 A	
Output voltage during transient load	4.3 V		5.85V
Output overvoltage protection	5.98 V	6.3 V	6.62 V
Rated output power		15 W	
Input power in standby @230V _{AC}			10 mW
Active mode efficiency (1)	81.84%		
Active mode efficiency @10% nameplate O/P (1)	72.48%		
Start-up time			200 ms
Rise time			40 ms
Ambient operating temperature			50 °C

Notes:

 $^{^{(1)}}$ Compliant with the European Code of Conduct rev.5 (Energy-efficiency criteria for active mode for low voltage external power supplies – Tier 2)

Figure 1: Electrical schematic 5V-3A GND 9 1 uF -[[l-R11 130k R12 43k + 1C8 560 u F 10 nF C10 R10 12k + | C7 | 560 u F R13 82k IC2 TS432 % ¥ FERD30S50DJF <u>۾</u> ₹ = TF 7508111123 rev. 6A R1 220k Ī D1 MRA4007T3G Q1 STD7N80K5 Z20 R3 R8 10 BAT41ZFILM C4 22 uF S In R15 2 2 GD SENSE R7 0.47 C2 12uF CURRENT VDD GND 470uH CS 2.2 nF \Box C1 12uF C6 33nF В ⋛ 30k STCH02 2.5V ZCD R14 56k OPTO1 SFH610A-2 NTC NTC Ē R4 100k ₹ 54

GSPG2507161330SG

AC IN

AC IN

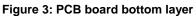
Figure 2: PCB board top layer dimensions (height 15 mm)

R3
WARNING

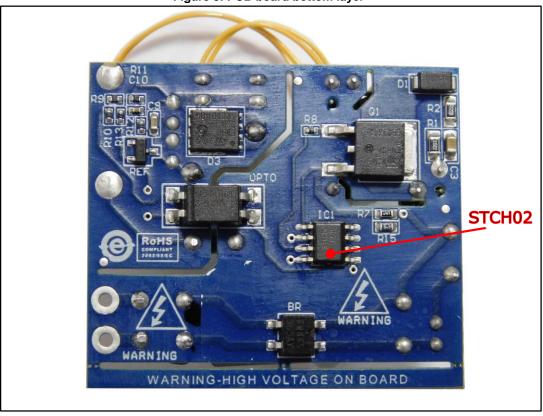
WARNING

C2
C11
STEVAL-ISA193V1

FOR EVALUATION ONLY: NOT FCC APPROVED FOR RESALE



35mm



Test board: main features AN4896

Figure 4: PCB board top layer layout (not in scale)

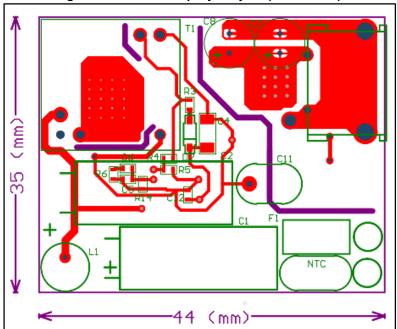


Figure 5: PCB board bottom layer layout (not in scale)

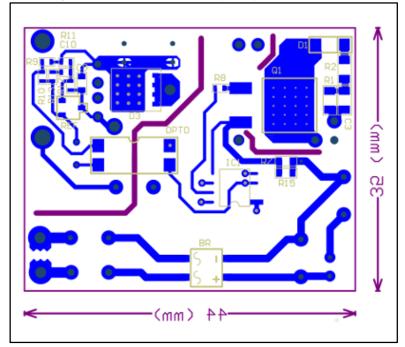


Table 2: STCH02 demonstration board: bill of material

Reference	Part	monstration board: bill Manufacturer	Description Description
C1	400AX12M8X20		-
	400AX12M8X20 400AX12M8X20	Rubycon	Elcap 12 µF-400 V
C2		Rubycon	Elcap 12 μF-400 V
C3	C0805X102KDRACTU	Kemet	MLCC capacitor 1 nF-1 KV
C4	C3216X5R1V226M160AC	TDK	MLCC capacitor 22 µF-35 V
C5	VJ0402Y222KNAAJ	Vishay	MLCC capacitor 2.2 nF-50 V
C6	C0402C333K4RACTU	Kemet	MLCC capacitor 33 nF-16 V
C7	6SEPC560MW	Panasonic	OS-CON capacitor 560 μF-6.3 V
C8	6SEPC560MW	Panasonic	OS-CON capacitor 560 μF-6.3 V
C9	GRM188C81E105KAADD	Murata	MLCC capacitor 1 µF-25 V
C10	GRM155R71H103KA88D	Murata	MLCC capacitor 10 nF-50 V
C11	DE2E3KY222MA2BM01	Murata	Ceramic Y-capacitor 2.2 nF 250 V _{AC}
C12	GRM1555C1H101JZ01D	Murata	MLCC capacitor 100 pF-50 V
D1	MRA4007T3G	ON Semiconductor	1 A-1000 V Power rectifier diode
D2	BAT41ZFILM	STMictroelectronics	Signal Schottky 0.15 A-100 V
D3	FERD30S50DJF	STMictroelectronics	Field effect rectifier 30 A-50 V
L1	7447462471	Wurth Elektronik	470 μH radial inductor
R1	ERJP06F2203V	Panasonic	220 kΩ ± 1% - 0.5 W - 400 V
R2	ERJP06F2200V	Panasonic	220 Ω±1% - 0.5 W – 400 V
R3	ERJ-2GEJ3R0X	Panasonic	3 Ω ± 5% - 0.1 W
R4	ERJ-2RKF1303X	Panasonic	130 kΩ ±1% - 0.1W
R5	ERJ-2RKF2702X	Panasonic	27 kΩ ± 1% - 0.1 W
R6	ERJ-2RKF3002X	Panasonic	30k Ω ± 1% - 0.1 W
R7	ERJ3BQFR47V	Panasonic	0.47 Ω ± 1% - 0.2 W
R8	CRCW040210R0FKEDHP	Vishay Dale	10 Ω ± 1% - 0.125 W
R9	ERJ-2RKF1001X	Panasonic	1 kΩ ± 1% - 0.1 W
R10	ERJ-2RKF1202X	Panasonic	12 kΩ ± 1% - 0.1 W
R11	ERJ-2RKF1303X	Panasonic	130 kΩ ± 1% - 0.1 W
R12	ERJ2RKF4302X	Panasonic	43 kΩ ± 1% - 0.1 W
R13	ERJ-2RKF8202X	Panasonic	82 kΩ ± 1% - 0.1 W
R14	ERJ-2RKF2402X	Panasonic	56 kΩ ± 1% - 0.1 W
R15	ERJ-3RQF3R3V	Panasonic	3.3 Ω ± 1% - 0.1 W
T1	7508111123 rev. 6A	Wurth Elektronik	Flyback transformer
ОРТО	SFH6106-2T	Vishay	Optocoupler
Q1	STD7N80K5	STMicroelectronics	800 V-1.2 Ω Power MOSFET

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Reference	Part	Manufacturer	Description
REF	TS432ILT	STMictroelectronics	Reference
IC1	STCH02	STMictroelectronics	Switching controller
BR	RMB6S	Taiwan Semiconductor	Bridge rectifier
OUT	614104150121	Wurth Elektronik	Flyback transformer
NTC	SL08 20002	Ametherm	20 Ω
FS	SS-5H-2-5A-BK	Cooper Bussmann	2.5 A fuse
USB	614104150121	Wurth Elektronik	USB type A connector

Table 3: Transformer characteristics

Parameter	Description	
Manufacturer	Wurth Elektronik	
Order code	7508111123 rev. 6A	
Core	RM6	
Primary inductance	900 μH ± 10%	
Saturation current	950 mA (20% roll-off from initial)	
Leakage inductance	40 μH max	
Primary-to-auxiliary turns ratio	6.55 ± 1%	
Primary-to-secondary turns ratio	14.4 ± 1%	

Figure 6: Transformer electrical scheme

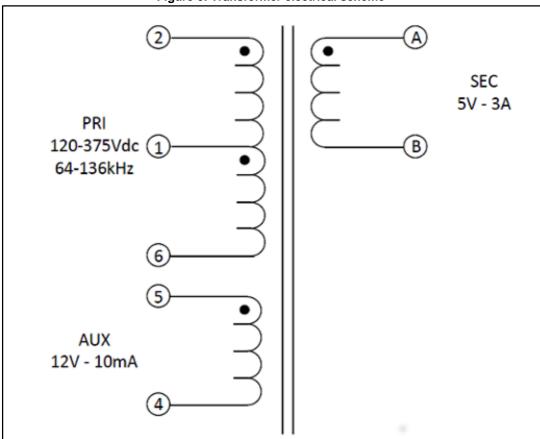
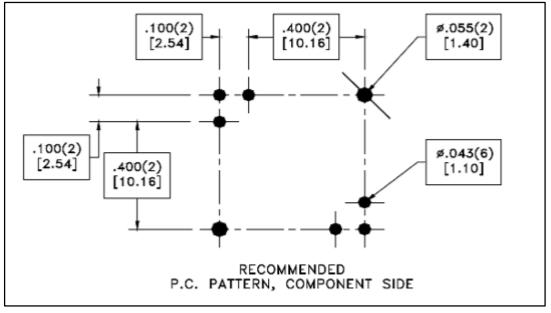


Figure 7: Transformer footprint (bottom view)



O12 x .030 REF.(2)

[.30 x .76]

.100 MIN.

[2.54]

TERM. NO.'s FOR REF. ONLY

SURFACE A IN RECOMMENDED GRID

Figure 8: Transformer mechanical drawing

AN4896 Circuit description

2 Circuit description

2.1 Input stage and filtering

The input stage comprises a fuse F1 to prevent catastrophic failure and an input NTC to limit the capacitor inrush current at plug-in and protect the bridge rectifier (BR).

A low cost π -filter (C1 – L1 – C2) is implemented to filter the differential mode conducted EMI.

2.2 Snubber network

The clamping network (R1 - C3 - D1) limits the leakage inductance voltage spike peak, by dissipating the related energy at MOSFET turn-off, ensuring reliable power supply operation.

The R2 resistor helps to reduce further the transformer ringing, damping the resonance oscillations at turn-off, between leakage inductance and equivalent drain capacitance.

2.3 PWM controller and MOSFET

The PWM controller is a current mode QR controller with embedded HV start-up circuit with zero power consumption which, together with the device extremely low quiescent current, helps minimizing the residual input consumption.

The R4 and R5 voltage dividers are used to sense both the zero-crossing signal for proper QR operations and the auxiliary voltage for OVP protection.

The CV regulation is achieved adjusting the voltage on the FB pin, which transfers, the output voltage information via the optocoupler. The FB pin capacitors and resistors are used for proper loop compensation.

The CC loop is fully integrated into the IC and no external components are required, except the resistors connected to the sense pins (R7 and R8), used to adjust the CC set point.

During normal operation, the VDD pin is powered by the transformer auxiliary winding, whose output is rectified by the D2 diode and the C4 capacitor.

The R3 resistor is used to filter the auxiliary spikes at turn-off, limiting the pin voltage fluctuation.

The C12 capacitor is used to filter any narrow voltage spike entering in the VDD pin.

The power MOSFET Q1 is a 800 V BV_{dss} SuperMESHTM 5, with a R_{DS(on)} \leq 1.2 Ω , which ensures a good compromise between low conduction losses and switching characteristics.

2.4 Output stage

The secondary transformer signal is rectified by the D3 diode and filtered by the C7 and C8 output capacitors, which are designed to minimize ESR as much as possible and provide sufficient AC ripple capability.

The C9 capacitor is used to reduce further the output switching noise.

The output voltage is sensed by the R11 and R12 voltage dividers and compared with the internal TS432 shunt voltage reference (1.24 V); its output is then converted via the optocoupler into a current signal control for the primary PWM IC.

Performance data AN4896

3 Performance data

The power supply main performances are shown below.

3.1 CV/CC output voltage characteristics

The board V-I characteristic is measured at the PCB output connector, at both 115 and 230 V_{AC} , under different line and load conditions.

The figures below show the measurement results: the load regulation is very accurate and barely affected by the USB connector contact resistance (\approx 30 m Ω).

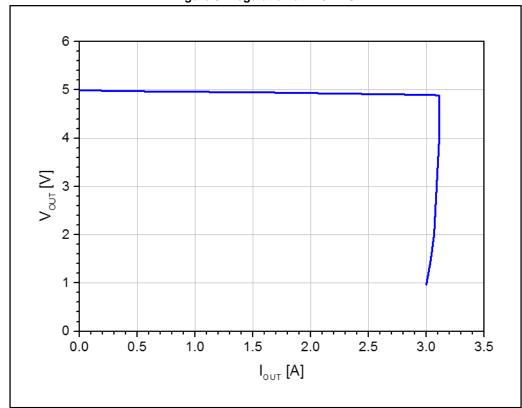


Figure 9: Regulation at 115 VAC

AN4896 Performance data

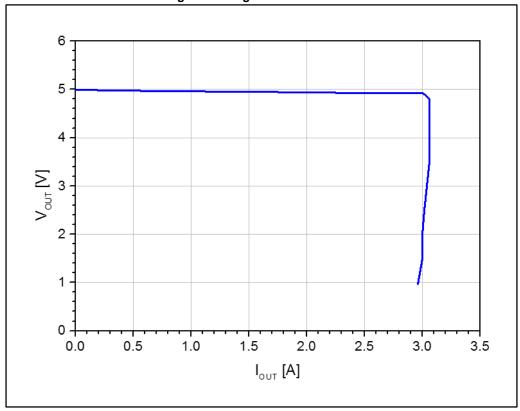


Figure 10: Regulation at 230 VAC

3.2 Efficiency and light load measurements

The converter efficiency and no-load consumption are measured at nominal input voltage (115 and 230 V_{AC}): the rated power average and 10% are compared with the European Code of Conduct revision 5 - Tier 2 (EuCoC) requirements (effective since the 1st of January 2016).

The figure and tables below show all the obtained results.

Performance data AN4896

87 86 85 84 Efficiency [%] 83 82-81 - 115Vac - 230Vac 80 average @115Vac average @230Vac EuCoC Tier 2 79 78 10 12 14 16 Output power [W]

Figure 11: Efficiency vs output power

Table 4: Average efficiency of the rated output load

9/ of roted nower	E	Efficiency		
% of rated power	115 V _{AC}	230 V _{AC}		
25%	84.48%	81.71%		
50%	84.96%	83.63%		
75%	84.48%	83.98%		
100%	82.80%	84.58%		
Average	84.18%	83.47%		
EU Code of Conduct rev. 5 – Tier 2 limit: 81.84%				

Table 5: Efficiency at 10% of the rated output load

Input voltage	Efficiency	
115 V _{AC}	81.20%	
230 V _{AC}	77.01%	
EU Code of Conduct rev. 5 – Tier 2 limit: 72.48%		

Table 6: No load consumption

Input voltage	Input power
115 V _{AC}	7.3 mW
230 V _{AC}	7.5 mW

AN4896 Typical waveforms

4 Typical waveforms

The converter typical waveforms are measured at nominal input voltages (115 and 230 V_{AC}) as shown in the sections below.

4.1 Dynamic load regulation response

The board V-I characteristic is measured at the PCB output connector, at both 115 V_{AC} and 230 V_{AC} , under different line and load conditions.

The board is submitted to dynamic load variations from 0 to 100% of the nominal load (as shown in the figures below): the output gives no abnormal oscillation and the over/undershoot values are quite acceptable.

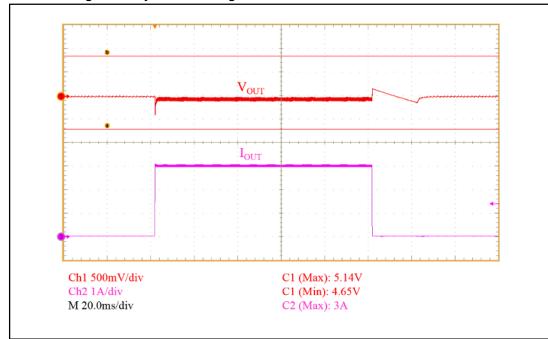


Figure 12: Dynamic load regulation from no load to full load at 115 VAC

Typical waveforms AN4896

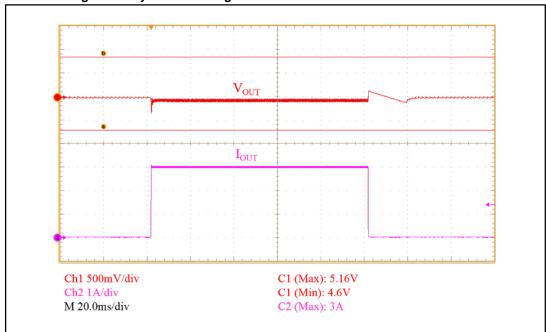


Figure 13: Dynamic load regulation from no load to full load at 230 VAC

4.2 Switching waveforms

Figures Figure 1: "Electrical schematic", Figure 16: "Normal operation at full load and 115 VAC", Figure 17: "Normal operation at full load and 230 VAC", Figure 18: "Normal operation at full load and 264 VAC" show the drain voltage and the drain current waveforms for the two nominal input voltages and the converter input operating range minimum/maximum voltage.

In order to simulate the operation constant current mode, the electronic load has been set in CV mode at 3V, so that this voltage is imposed on the charger output from the E-load: the charger is forced to enter CC mode, thus regulating the output current at its nominal value. Figures Figure 19: "CV mode at 115 VAC" and Figure 20: "CV mode at 230 VAC" show the CC mode typical waveforms.

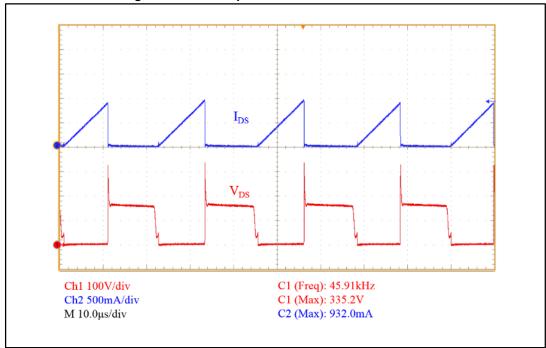
The converter is also tested in short-circuit: as the integrated CC mode loop is able to regulate even when the output voltage falls to zero, the output current is maintained close to the nominal value, thus ensuring safe and reliable operations.

Figures Figure 21: "Short-circuit at 115 VAC" and Figure 22: "Short-circuit at 230 VAC" show the short-circuit typical waveforms.

AN4896 Typical waveforms

Figure 14: Normal operation at full load and 90 VAC I_{DS} V_{DS} Ch1 100V/div C1 (Freq): 45.91kHz Ch2 500mA/div C1 (Max): 335.2V C2 (Max): 932.0mA $M~10.0\mu s/div$





Typical waveforms AN4896

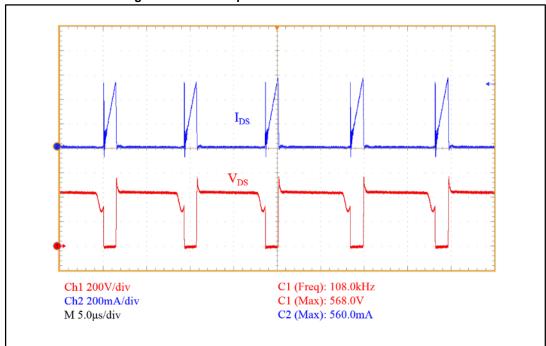
 I_{DS} V_{DS} Ch1 200V/div C1 (Freq): 98.31kHz Ch2 200mA/div C1 (Max): 528.0V

Figure 16: Normal operation at full load and 230 VAC



 $M~5.0\mu s/div$

C2 (Max): 584.0mA



AN4896 Typical waveforms

Figure 18: CV mode at 115 VAC

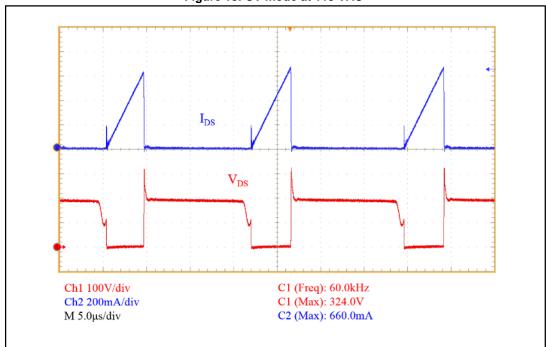
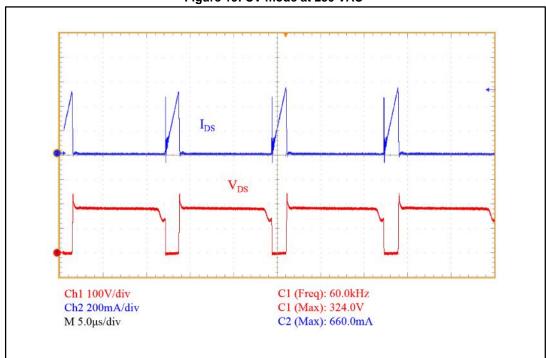


Figure 19: CV mode at 230 VAC



Typical waveforms AN4896

Figure 20: Short-circuit at 115 VAC

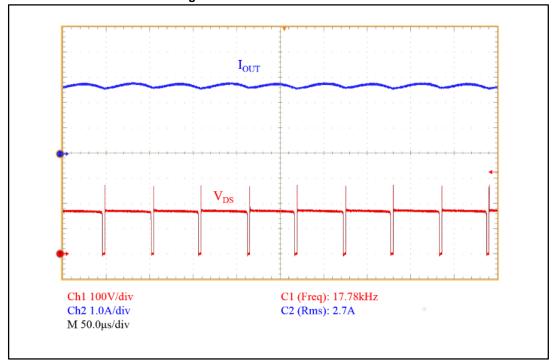
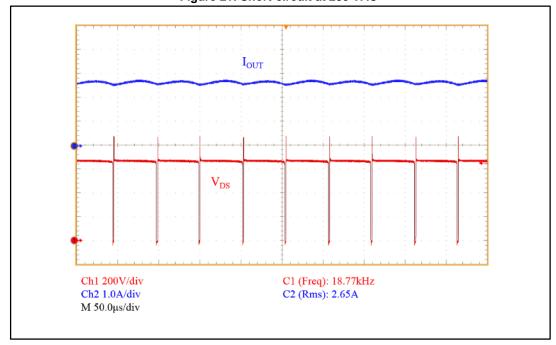


Figure 21: Short-circuit at 230 VAC



4.3 Startup waveforms and delay to AC power on

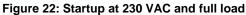
This section shows the adapter typical waveforms during startup in no-load, full load, and nominal input voltage conditions.

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AN4896 Typical waveforms

The maximum drain voltage is below the MOSFET BV_{DSS}, with sufficient safety margin, and the output voltage overshoot is always well below the limit.

The delay to AC power-on and the output voltage rise time are within the specifications.



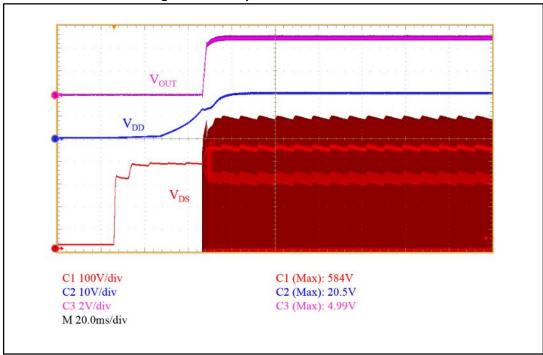
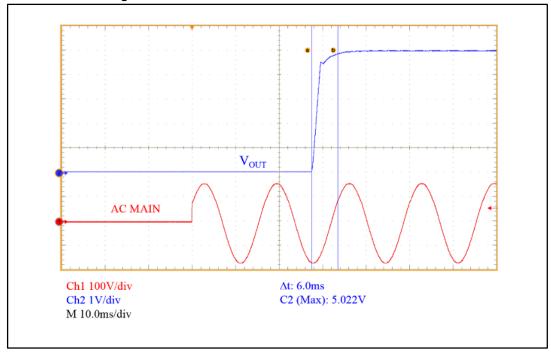


Figure 23: Power on at no load and 115 VAC resistive load



Typical waveforms AN4896

Figure 24: Power on at no load and 230 VAC resistive load

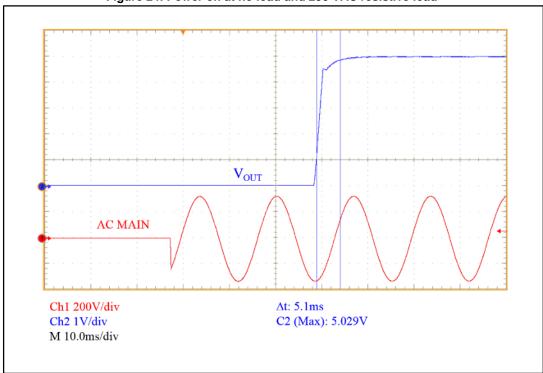
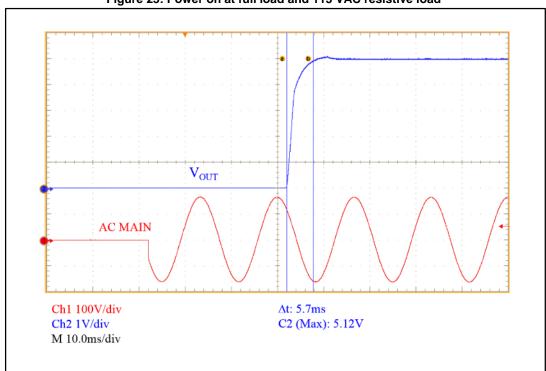


Figure 25: Power on at full load and 115 VAC resistive load



AN4896 Typical waveforms

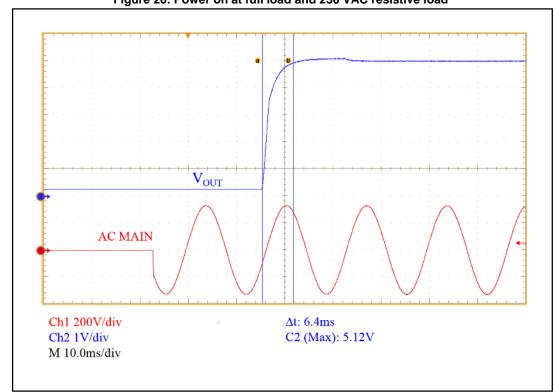


Figure 26: Power on at full load and 230 VAC resistive load

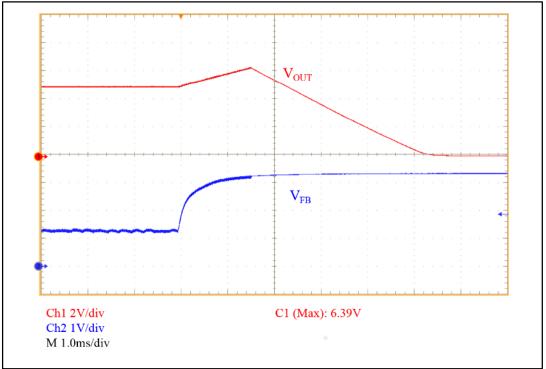
4.4 Output overvoltage protection

The output overvoltage protection is tested by shorting the opto-diode, so the converter operates in open loop and the power excess (with respect to the load) charges the output capacitance, increasing the output voltage as the OVP is tripped and the converter stops switching.

The figure below shows that output voltage increases and the converter stops switching and enters protection mode when the voltage reaches OVP threshold set by the R4 and R5 voltage dividers.

Typical waveforms AN4896

Figure 27: OVP at 230 VAC and 115 VAC



5 Conducted noise measurements

A pre-compliance test for EN55022 (Class B) European normative was performed using average measurements detector of the conducted noise emissions, at full load and nominal mains voltages.

The figures below show the results: under all test conditions, there is a very good margin between the measurements and the respective limits.

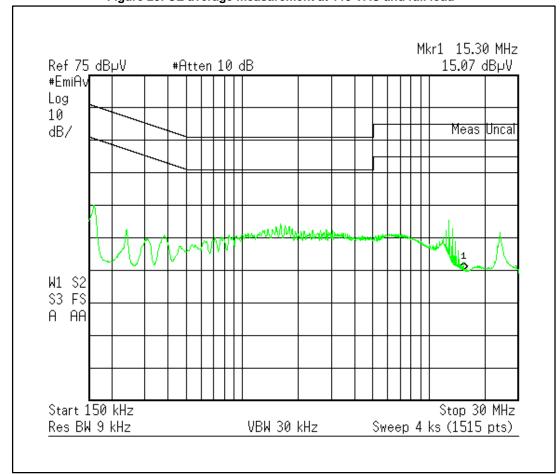
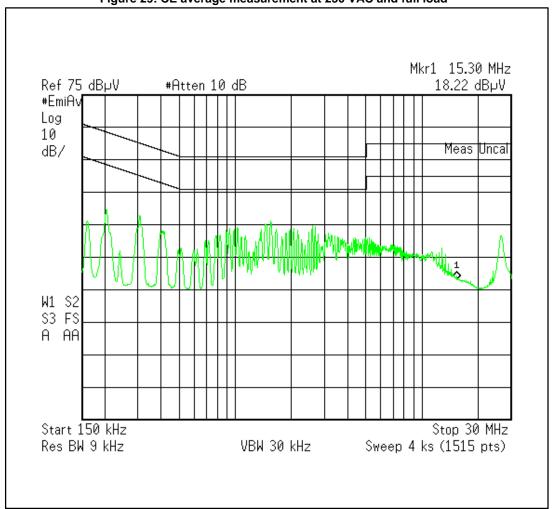


Figure 28: CE average measurement at 115 VAC and full load

Figure 29: CE average measurement at 230 VAC and full load



AN4896 Immunity tests

6 Immunity tests

The board was submitted to immunity tests according to IEC61000 and their results are classified according to the standard criteria:

- A: normal performance;
- B: temporary degradation or loss of function or performance, with automatic return to normal operation;
- C: temporary degradation or loss of function, with external intervention to re-cover normal operation
- D: degradation or loss of function, necessary substitution of damaged components to recover normal operation

6.1 ESD immunity test (IEC 61000-4-2)

The test was performed on a single test board. The input voltage was set to 230 V_{AC} , the output was loaded to full load and the proper operation was verified by connecting a current probe to the output.

The test conditions are:

- Contact discharge and air discharge methods
- Discharge circuit150 pF/330 Ohm
- Polarity: positive / negative

The test results are listed in the following tables.

Table 7: ESD contact discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
L vs. PE	10 kV	Positive	PASS	Α
L vs. PE	10 kV	Negative	PASS	Α
N vs. PE	10 kV	Positive	PASS	Α
N vs. PE	10 kV	Negative	PASS	Α

Table 8: ESD contact discharge test results with PE connected on secondary GND

Noise injection	ESD level	Polarity	Result	Criterion
L vs. GND	8 kV	Positive	PASS	Α
L vs. GND	8 kV	Negative	PASS	Α
N vs. GND	8 kV	Positive	PASS	Α
N vs. GND	8 kV	Negative	PASS	Α

Table 9: ESD air discharge test results

Noise injection	ESD level	Polarity	Result	Criterion
Horizontal coupling plane	20 kV	Positive	PASS	Α
Horizontal coupling plane	20 kV	Negative	PASS	Α
Vertical coupling plane	20 kV	Positive	PASS	Α
Vertical coupling plane	20 kV	Negative	PASS	А

Immunity tests AN4896

6.2 Surge immunity test (IEC 61000-4-5)

The test was performed on a single test board. The input voltage was set to 230 V_{AC} , the output was loaded with 10% of the nominal load and the proper operation was verified by connecting a current probe to the output.

The test conditions are:

- repetition rate: 1 minute
- applied to input lines vs. EARTH common mode
- applied to input line (L vs. N) and differential mode
- a network made up by a varistor and two Y1 capacitors is connected across the AC line connector according to the norm.

The test results are listed in the following tables.

Table 10: Common mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. PE	2 kV	Positive	PASS	Α
N vs. PE	2 kV	Positive	PASS	Α
L vs. PE	2 kV	Negative	PASS	Α
N vs. PE	2 kV	Negative	PASS	Α

Table 11: Differential mode surge test results

Noise injection	Surge level	Polarity	Result	Criterion
L vs. N	2 kV	Positive	PASS	Α
L vs. N	2 kV	Negative	PASS	Α

Performed tests show that the board withstands the lightning disturbances applied to input line in common mode and differential mode for each severity level.

According to the standard, the application can be classified as level 3.

6.3 Burst immunity test (IEC 61000-4-4)

The test was performed on a single test board. The input voltage was set to 230 V_{AC} , the output was loaded with 10% of the nominal load and the proper operation was verified by connecting a current probe to the output.

The test conditions are:

- polarity: positive/negative
- burst duration: 15 ms ± 20 % at 5 kHz
- burst period: 300 ms ± 20 %
- duration time: 1 minute
- applied to: AC lines through integrated capacitive coupling clamp.

The test results are listed in the following table.

Table 12: Burst test results

Noise injection	Burst level	Polarity	Result	Criterion
L/PE	4 kV	Positive	PASS	Α
N/PE	4 kV	Positive	PASS	Α

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Noise injection	Burst level	Polarity	Result	Criterion
L/N	4 kV	Positive	PASS	Α
L/PE	4 kV	Negative	PASS	Α
N / PE	4 kV	Negative	PASS	Α
L/N	4 kV	Negative	PASS	Α

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7 Thermal tests

The board thermal analysis was performed by using an IR camera.

The board was submitted to full load at nominal input voltage and the thermal map was taken 30 min. after the power on at ambient temperature (25 °C). The following figures show the results.

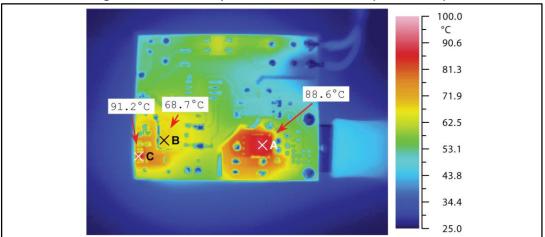
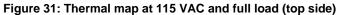
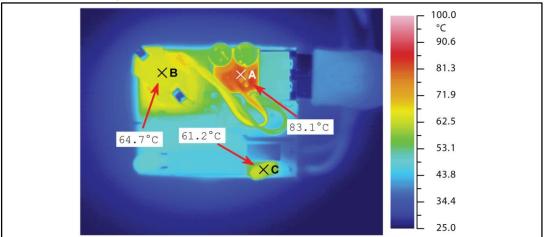


Figure 30: Thermal map at 115 VAC and full load (bottom side)





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Figure 32: Thermal map at 115 VAC and full load (transformer) 100.0 °C 90.6

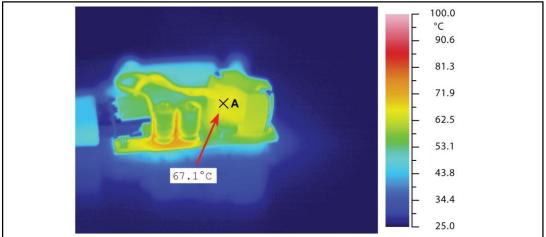


Figure 33: Thermal map at 230 VAC and full load (bottom side)

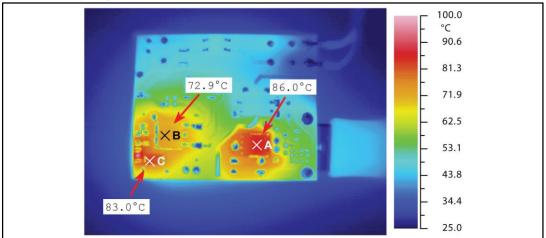
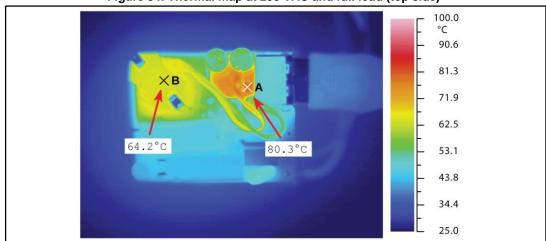


Figure 34: Thermal map at 230 VAC and full load (top side)



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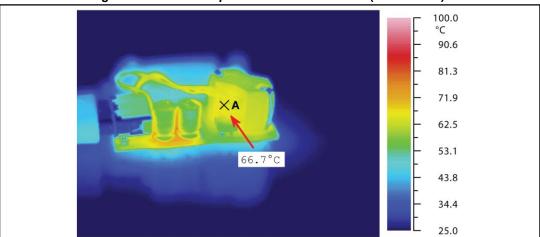


Figure 35: Thermal map at 230 VAC and full load (transformer)

AN4896 Conclusions

8 Conclusions

A 15 W wide range mains USB adapter using the new STCH02 has been introduced and the testing results shown.

The excellent electrical performance, very high efficiency and extremely low standby consumption make the STCH02 the most suitable IC to build low/medium power level output USB adapters for a wide class of high performance and low cost chargers (for mobile phones, tablet and hand-held equipment).

Revision history AN4896

9 Revision history

Table 13: Document revision history

Date	Revision	Changes
03-Aug-2016	1	Initial release.

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