# AN4936
# Application note

# Migration of microcontroller applications from STM32F7 Series to STM32H7x3 line microcontrollers

## Introduction

Designers of STM32 microcontroller applications must be able to easily replace one microcontroller type with another one from the same product family, or products from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill extended product requirements, extra demands on memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require a switch to smaller components and a shrunk PCB area.

This application note analyzes the steps required to migrate from an existing STM32F7 Series to a design based on an STM32H7x3 line device.

This application note provides a guideline on both hardware and peripheral migration. To better understand the information inside this application note, the user should be familiar with the STM32 microcontroller family.

For additional information, refer to the following documents available on *www.st.com*:

- *STM32F75xxx and STM32F74xxx advanced ARM®-based 32-bit MCUs* reference manual (RM0385)
- *STM32F76xxx and STM32F77xxx advanced ARM®-based 32-bit MCUs* reference manual (RM0410)
- *STM32H7x3 advanced ARM®-based 32-bit MCUs* reference manual (RM0433)

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# 1 STM32H7x3 line device overview

Taking advantage of an L1-cache, the STM32H7x3 line devices deliver the maximum theoretical performance of the Cortex-M7 core, regardless if the code is executed from the embedded Flash or external memory: 2010 CoreMark / 856 DMIPS at 400 MHz fCPU.

The STM32H7x3 line devices are offering to the customers some extra performance versus the STM32F7 Series devices without additional complexity.

The STM32H7x3 line devices, as Cortex-M7 variants, are compatible (for the common packages) with the STM32F7 Series devices. This compatibility allows to customers to straightforward use a similar device to the STM32F7 Series and to benefit from the significantly higher performance of the STM32H7x3 line devices and advanced peripherals.

The STM32H7x3 line devices are also the entry point of the wider STM32H7 Series, which can be seen as an easy stepladder to benefit from the high performance, the rich connectivity and the enhanced features of this advanced platform.

The STM32H7x3 line devices include a larger set of peripherals with advanced features and optimized power consumption compared to the STM32F7 series:

- High-Resolution Timer (HRTIM)
- Low-Power Universal Asynchronous Receiver Transmitter (LPUART)
- Single Wire Protocol Master Interface (SWPMI)
- FD Controller Area Network (FDCAN)
- Operational amplifiers (OPAMP)
- Ultra-low-power
- Comparator (COMP)
- Voltage reference buffer (VREFBUF)

This migration guide is only covering the migration from the STM32F7 Series to STM32H7x3 line. As a consequence the new features present on the STM32H7x3 line devices but not already present on the STM32F7 Series devices are not covered in this document (refer to the *STM32H7x3* reference manual and datasheets for more details).

## 1.1 System architecture differences between STM32F7 Series and STM32H7x3 line devices

One single domain is available in the STM32F7 Series devices which embed an AHB bus matrix while in the STM32H7x3 line devices there are 3 domains: an AXI bus matrix, two AHB bus matrices and bus bridges allow interconnecting the bus masters with the bus slaves:

- **D1 domain**: is the high bandwidth / high performance domain with the Cortex-M7 core and acceleration mechanisms. This domain encompasses the high bandwidth features and smart management thanks to the AXI bus matrix.
- **D2 domain**: is the “I/O processing” domain. It encompasses most peripherals that are less bandwidth demanding.
- **D3 domain**: is designed to manage the low-power mode (embeds the system configuration block to keep the system state, the GPIO status). This domain is

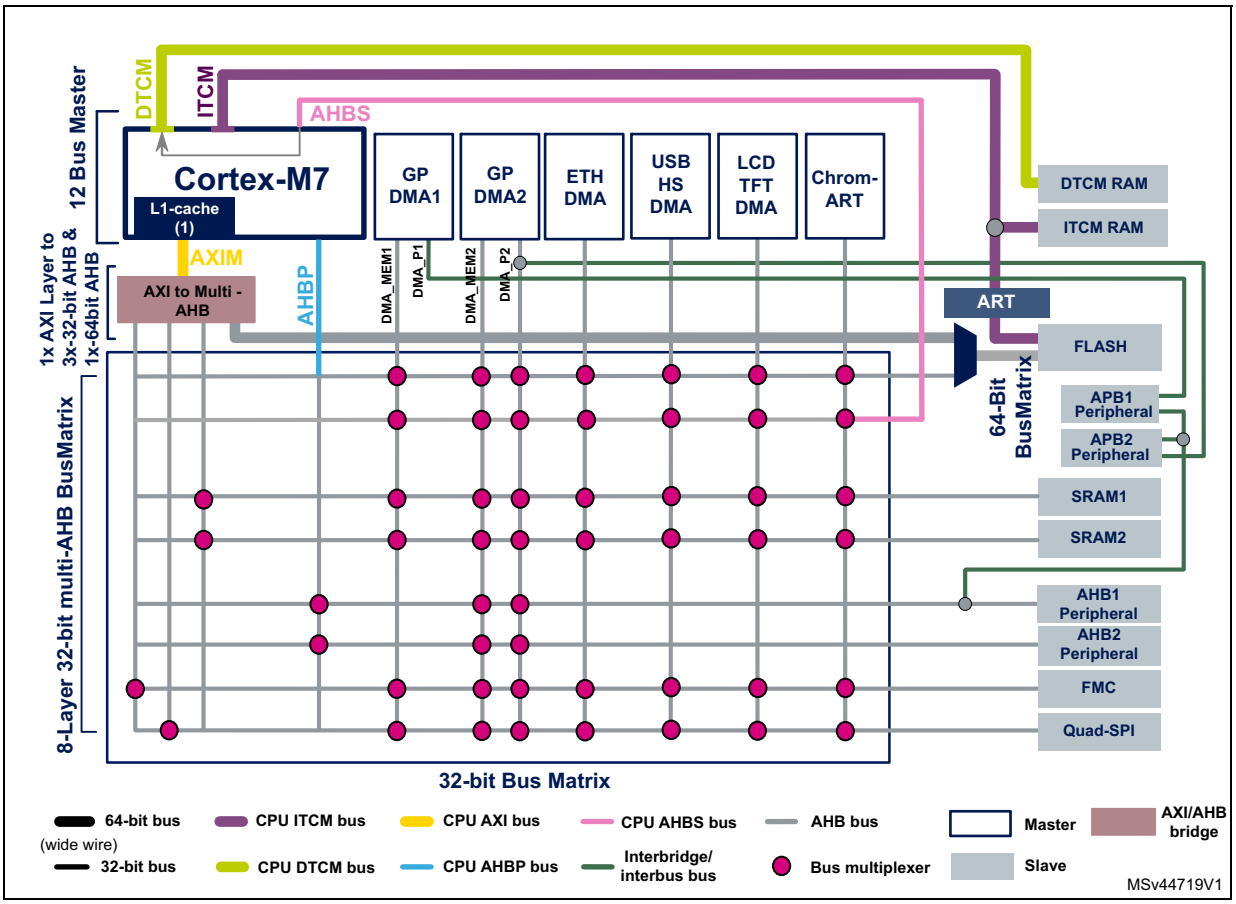
designed to be autonomous: it embeds 64-Kbyte RAM and has a subset of peripheral to run the basic functions while the domains 1 and 2 can be shut-off to save power.

*Table 1*, *Figure 1* and *Figure 2* illustrate the system architecture differences between the STM32F7 Series and the STM32H7x3 line devices.

**Table 1. Available bus matrix on STM32F7 Series and STM32H7x3 line devices**

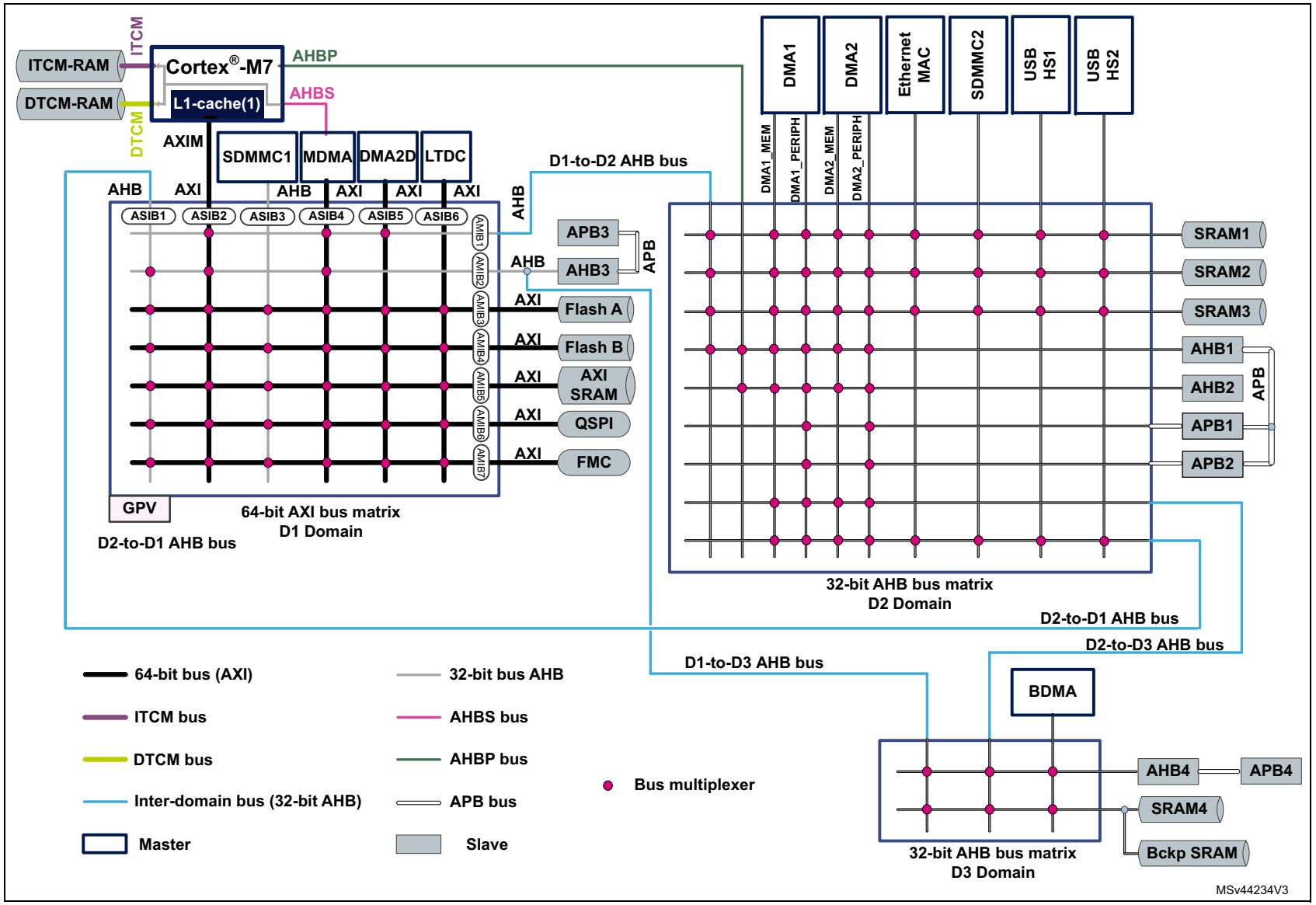
| Device | AHB bus matrix | AXI b us matrix |
|---|---|---|
| STM32F7 Series | 1 | NA |
| STM32H7x3 line | 2 | 1 |

**Figure 1. STM32F7 Series system architecture**




1. I/D cache size:
   - For STM32F74xxx and STM32F75xxx devices: 4 Kbytes.
   - For STM32F72xxx and STM32F73xxx devices: 8 Kbytes.
   - For STM32F76xxx and STM32F77xxx devices: 16 Kbytes.

**Figure 2. STM32H7x3 line system architecture**




1. I/D cache size: For the STM32H7x3 line devices: 16 Kbytes.

# 2 Hardware migration

## 2.1 Available packages

The available packages on the STM32F7 Series and STM32H7x3 line devices are listed in *Table 2*.

**Table 2. Available packages on STM32F7 Series and STM32H7x3 line devices (1)**

| Package | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| LQFP64 | X | NA |
| LQFP100 | | X |
| TFBGA100 | | NA |
| WLCSP143 | | NA |
| LQFP144 | | X |
| UFBGA176 | | X |
| LQFP176 | | X |
| LQFP208 | | X |
| TFBGA216 | | NA |
| TFBGA240 | NA | X |

1. X = available.

## 2.2 Pinout compatibility

The STM32F7 Series devices are pin to pin compatible with the STM32H7x3 line devices except for the BYPASS_REG pin in LQFP176 and UFBGA176 packages which is no longer available on the STM32H7x3 line devices.

On the STM32H7x3 line devices, the BYPASS_REG pin is connected to VSS and the regulator bypass mode is managed by software with the LDOEN and BYPASS bits located in the PWR_CR3 register.

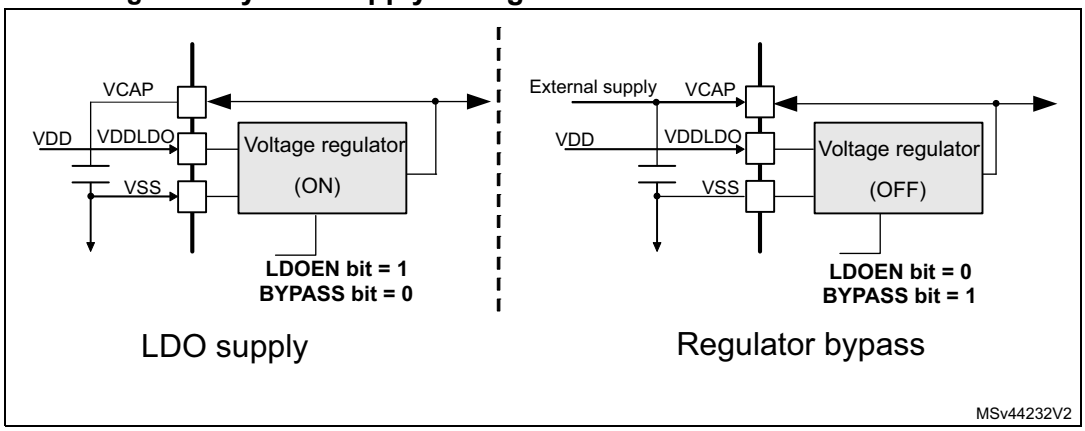
At system startup, the MCU starts under LDO then the user can switch to the regulator bypass mode by modifying the LDOEN and bypass bits with the software.

*Table 3* and *Figure 1* illustrate the BYPASS_REG pin incompatibility in LQFP176 and UFBGA176 packages and the system supply configuration on the STM32H7x3 line devices.

**Table 3. BYPASS_REG pin incompatibility in LQFP176 and UFBGA176 packages**

| Package | Pin/ball | STM32F7 Series | STM32H7x3 line | Comment |
|---|---|---|---|---|
| LQFP176 | Pin 48 | BYPASS_REG | VSS | Impacts only the boards designed with STM32F7 Series in the regulator bypass mode |
| UFBGA176+25 | Ball L4 | | | |

**Figure 3. System supply configuration on STM32H7x3 line devices**




## 2.3 System bootloader

The system bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces.

*Table 4* shows the supported communication peripherals by the system bootloader.

**Table 4. STM32F7 Series and STM32H7x3 line bootloader communication peripherals**

| System bootloader peripherals | STM32F7 Series I/O pin | STM32H7x3 line I/O pin |
|---|---|---|
| DFU | USB OTG FS (PA11 / PA12) in the device mode | |
| USART1 | PA9 / PA10 | PA9 / PA10<br>PB14 / PB15 |
| USART 2 | NA | PA2 / PA3 |
| USART3 | PB10 / PB11<br>PC10 / PC11 | PB10 / PB11 |
| I2C1 | PB6 / PB9 | |
| I2C2 | PF0 / PF1 | |
| I2C3 | PA8 / PC9 | |
| SPI1 | PA7 / PA6 / PA5 / PA4 | |
| SPI2 | PI3 / PI2 / PI1 / PI0 | |
| SPI3 | NA | PC12 / PC11/ PC10 / PA15 |
| SPI4 | PE14 / PE13 / PE12 / PE11 | |
| CANx | PB5 / PB13(1)<br>PD0 / PD1(2) | NA |

1. Available on the STM32F74xxx/75xxx and STM32F76xxx/77xxx devices.
2. Available on the STM32F2xxx/73xxx devices.

# 3 Boot mode compatibility

The STM32F7 Series and the STM32H7x3 line boot space are based on BOOT0 and boot address option bytes as described in *Table 5*.

For the STM32F7 Series the boot base address supports any address in the range from 0x0000 0000 to 0x3FFF FFFF while in the STM32H7x3 line the boot base address supports any address in the range from 0x0000 0000 to 0x3FFF 0000.

**Table 5. Boot mode compatibility between STM32F7 Series and STM32H7x3 line devices**

| Boot mode selection | | STM32F7 Series | STM32H7x3 line |
|---|---|---|---|
| BOOT | Boot address option bytes | | |
| 0 | BOOT_ADD0[15:0] | Boot address defined by user option byte BOOT_ADD0[15:0]<br>ST programmed value:<br>Flash on ITCM at 0x0020 0000 | Boot address defined by user option byte BOOT_ADD0[15:0]<br>ST programmed value:<br>Flash memory at 0x0800 0000 |
| 1 | BOOT_ADD1[15:0] | Boot address defined by user option byte BOOT_ADD1[15:0]<br>ST programmed value: System bootloader at 0x0010 0000 | Boot address defined by user option byte BOOT_ADD1[15:0]<br>ST programmed value: System bootloader at 0x1FF0 0000 |

# 4 Peripheral migration

## 4.1 STM32 product cross-compatibility

The STM32 series embed a set of peripherals which can be classed in three categories:

- The first category is for the peripherals which are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals which are shared by all STM32 products but have only minor differences (in general to support new features), so the migration from one product to another is very easy and does not need any significant new development effort.
- The third category is for peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, the migration will require a new development at application level.
- The SW compatibility mentioned in the *Table 6* only refers to the register description for "low level" drivers.

The Cube Hardware Abstraction Layer (HAL) is compatible between the STM32F7 Series and the STM32H7x3 line devices.

*Table 6* shows the STM32 peripheral compatibility between the STM32F7 Series and the STM32H7x3 line devices.

**Table 6. Peripheral summary of STM32F7 Series and STM32H7x3 line devices**

| | | STM32F7 Series | STM32H7x3 line | Compatibility<br>Comments |
|---|---|---|---|---|
| Power supply | | – Power supply for I/Os 1.71 to 3.6 V<br>– Internal regulator VDD = 1.7 to 3.6 V | – Power supply for I/Os 1.62 to 3.6 V<br>– Internal regulator VDDLDO = 1.62 to 3.6 V | More power supply supervision added |
| Maximum frequency | | 216 MHz | 400 MHz | - |
| MPU region number | | 8 | 16 | - |
| Flash | | 2 Mbytes | | - |
| | | – Singe Bank<br>– Dual Bank | – Dual Bank | – Mapped on AXI bus<br>– With ECC protection in STM32H7x3 line |
| SRAM | System | 512 Kbytes | ~1 Mbyte (992 Kbytes) | With ECC protection in STM32H7x3 line |
| | Instruction | 16 Kbytes | 64 Kbytes | |
| | Backup | 4 Kbytes | | |
| Common Peripherals | FMC | Yes | | Mapped on AXI bus |
| | QSPI | Yes | | Mapped on AXI bus |
| | Ethernet | Yes | | Wakeup from stop capability |

**Table 6. Peripheral summary of STM32F7 Series and STM32H7x3 line devices (continued)**

| | | STM32F7 Series | STM32H7x3 line | Compatibility<br>Comments |
|---|---|---|---|---|
| Timers | High resolution | NA | 1 | New feature |
| | General purpose | 10 | | - |
| | PWM | 2 | | - |
| | Basic | 2 | | - |
| | Low-power | 1 | 5 | Wakeup from stop capability |
| RNG | | Yes | | - |
| Communication interfaces | SPI/I²S | 4/3 (simplex) | 6/3(simplex) | Wakeup from stop capability in STM32H7x3 line |
| | I2C | 4 | | Wakeup from stop capability in STM32H7x3 line |
| | USART/UART | 4/4 | | – New synchronous slave mode, Tx and Rx FIFOs<br>– Wakeup from stop capability in STM32H7x3 line |
| | LPUART | NA | 1 | New feature |
| | SAI | 2 | 4 | PDM interface, supporting up to 8 microphones in STM32H7x3 line |
| | SPDIFRX | 4 inputs | | - |
| | SWPMI | NA | Yes | New feature |
| | MDIO | Yes | | Wakeup from stop capability |
| | SDMMC | Yes | | – With DMA capability<br>– Wakeup from stop<br>– eMMC boot support |
| | CAN | 3 × CANs (2.0B Active) | 2x CAN FD<br>(FDCAN1 supports TTCAN) | New feature |
| | USB OTG FS | Yes | | With DMA capability |
| | USB OTG HS | Yes | | - |
| | HDMI-CEC | Yes | | Wakeup from stop capability |
| | DFSDM | Yes | | - |
| Digital camera interface | | Yes | | - |

**Table 6. Peripheral summary of STM32F7 Series and STM32H7x3 line devices (continued)**

| | | STM32F7 Series | STM32H7x3 line | Compatibility<br>Comments |
|---|---|---|---|---|
| MIPI-DSI Host | | Yes | No | - |
| Graphics | LCD-TFT | Yes | | - |
| | Chrom-ART Accelerator™ (DMA2D) | Yes | | YCbCr to RGB color space conversion on STM32H7x3 line |
| | JPEG Codec | Yes | | - |
| GPIOs | | Up to 168 I/O ports with interrupt capability | | - |
| Analog peripherals | ADC | Power supply:1.7 V to 3.6 V<br>X3 (8 to 12-bit)<br>Number of channels: up to 24 | Power supply:1.62 V to 3.6 V<br>X3 (8 to 16-bit)<br>Number of channels: 20 | – VREF+ is provided from the internal VREFBUF. |
| | 12-bit DAC | Yes | | |
| | Operational amplifiers | NA | 2 | New feature |
| | Ultra-low-power comparator | NA | 2 | New feature |
| DMA | General-purpose DMA: 16-stream DMA controller with FIFOs and burst support | | 4 DMA controllers to unload the CPU<br>– 1x high-speed general-purpose master direct memory access controller (MDMA)<br>– 2x dual-port DMAs with FIFO and request router capabilities for optimal peripheral management<br>– 1 basic DMA with resquest router capabilities | – No limitation for peripheral requests thanks to DMAMUX.<br>– DMA1 can access to peripherals in APB1/APB2 buses.<br>– Peripheral request mapping is no more managed by the DMA controller but by the DMAMUX controller |
| Crypto graphic acceleration | – AES 128, 192, 256, DES/TDES<br>– HASH (MD5, SHA-1, SHA-2), HMAC<br>– True random number generator | | | 32-bit true random numbers, produced by an analog entropy source conditioned with block cipher AES-CBC. |
| Security | ROP, active tamper | | ROP, PC-ROP, active tamper | - |

## 4.2 Memory organization

### 4.2.1 RAM size

*Table 7* illustrates the difference of RAM size between the STM32F7 Series and STM32H7x3 line devices.

**Table 7. Comparison of RAM size between STM32F7 Series and STM32H7x3 line devices**

| Memory | STM32F7 Series | STM32H7x3 line | Unit |
|---|---|---|---|
| ITCM-RAM | 16 | 64 | Kbyte |
| DTCM-RAM | 128 | 128 | |
| AXI-SRAM | - | 512 | |
| SRAM1 | 368 | 128 | |
| SRAM2 | 16 | 128 | |
| SRAM3 | NA | 32 | |
| SRAM4 | NA | 64 | |
| Backup SRAM | 4 | 4 | |
| Total | 532 | 1060 | |

### 4.2.2 Memory map and peripherals register boundary addresses

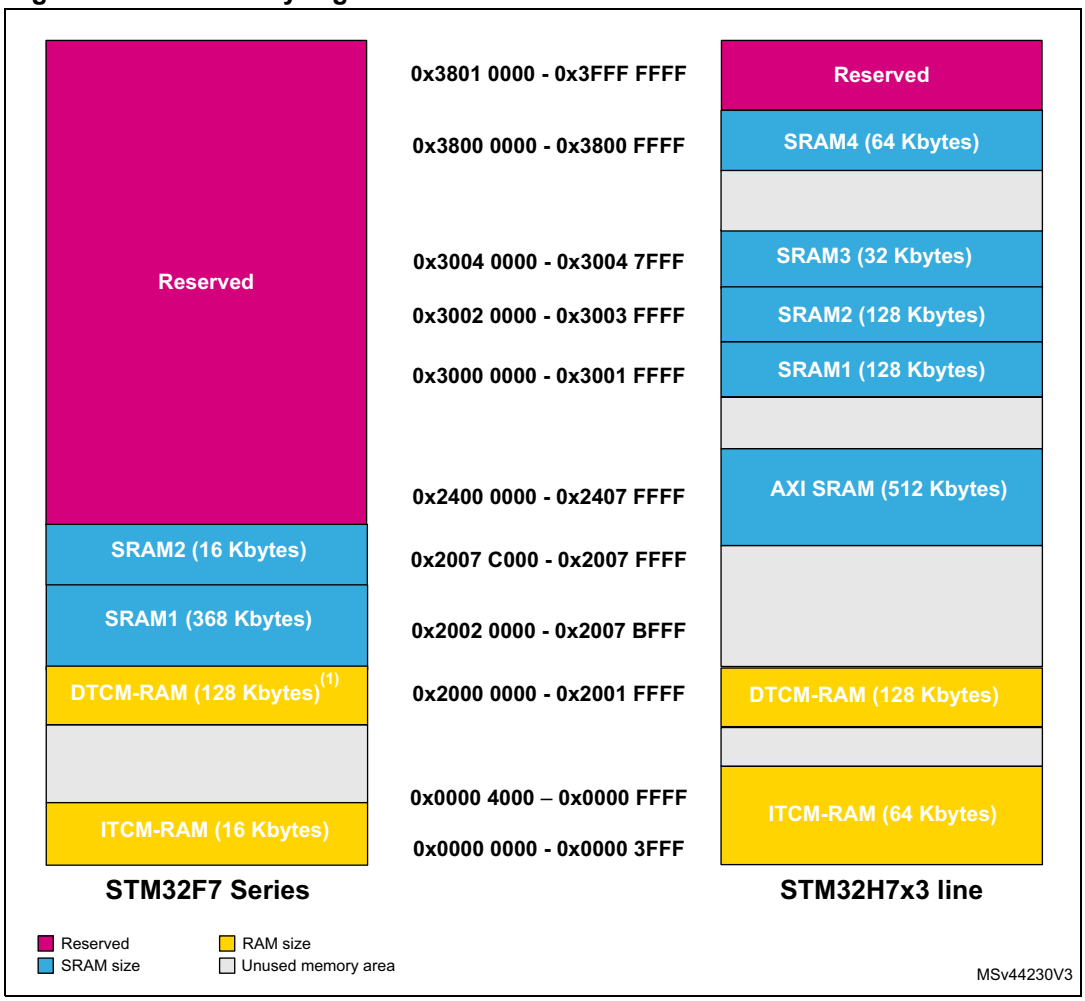
*Table 8* and *Figure 4* give a comparison of the memory addresses between the STM32F7 Series and STM32H7x3 line devices.

**Table 8. Memory organization and compatibility between STM32F7 Series and STM32H7x3 line devices (1)**

| Memory | STM32F7 Series | STM32H7x3 line | Compatibility |
|---|---|---|---|
| ITCM-RAM | 0x0000 0000 – 0x0000 3FFF | 0x0000 0000 – 0x0000 FFFF | X |
| DTCM-RAM | 0x2000 0000 – 0x2001 FFFF | 0x2000 0000 – 0x2001 FFFF | X |
| FLASH | Flash - AXI<br>0x0800 0000 – 0x081F FFFF | Flash A<br>0x0800 0000 – 0x080F FFFF<br>Flash B<br>0x0810 0000 – 0x081F FFFF | X |
| | Flash - ITCM<br>0x0020 0000 – 0x002FF FFFF | NA | - |
| System memory | 0x1FF0 0000 – 0x1FF0 EDBF | Bank 1<br>0x1FF0 0000 – 0x1FF1 FFFF<br>Bank 2<br>0x1FF4 0000 – 0x1FF5 FFFF | - |
| | 0x0010 0000 – 0x0010 EDBF | NA | - |

1. X = compatible.

**Figure 4. RAM memory organization of STM32F7 Series and STM32H7x3 line devices**




1. DTCM-RAM size:
   - 128 Kbytes for the STM32F76xxx and STM32F77xxx devices.
   - 64 Kbytes for the STM32F75xxx and STM32F74xxx devices.

### 4.2.3 Peripheral register boundary addresses

The peripheral address mapping has been changed for most of peripherals in the STM32H7x3 line versus the STM32F7 series.

*Table 9* shows an example of some peripherals address mapping changed in STM32H7x3 line devices.

For more details about registers boundary addresses differences refer to *Memory map and register boundary addresses* section of RM0410, RM0385 and RM0433 reference manuals.

**Table 9. Examples of peripheral address mapping differences between STM32F7 Series and STM32H7x3 line devices**

| Peripheral | STM32F7 Series | | STM32H7x3 line | |
|---|---|---|---|---|
| | Bus | Base address | Bus | Base address |
| QUADSPI control | AHB3 | 0xA000 1000 - 0xA0001FFF | AHB3 | 0x52005000 - 0x52005FFF |
| CRC | AHB1 | 0x4002 3000 - 0x4002 33FF | AHB4(D3) | 0x58024C00 - 0x58024FFF |
| GPIOA | | 0x4002 0000 - 0x4002 03FF | | 0x58020000 - 0x580203FF |
| RCC | | 0x4002 3800 - 0x4002 3BFF | | 0x58024400 - 0x580247FF |

## 4.3 FLASH memory

*Table 10* presents the differences between the Flash memory interface of STM32F7 Series and STM32H7x3 line.

The STM32H7x3 line devices instantiate a different Flash module both in terms of architecture and interface. For more information on programming, erasing and protection of the STM32H7x3 Flash memory, refer to *STM32H7x3 advanced ARM®-based 32-bit MCUs* reference manual (RM0433).

**Table 10. Flash memory differences between STM32F7 Series and STM32H7x3 line devices**

| Flash | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Mapping | AHB | AXI |
| FLASH address | **STM32F76xxx/STM32F77xxx**<br>Flash - AXI<br>0x0800 0000 – 0x081F FFFF<br>**STM32F746xx/STM32F756xx**<br>Flash - AXI<br>0x0800 0000 – 0x080F FFFF | Flash A<br>0x0800 0000 – 0x080F FFFF<br>Flash B<br>0x0810 0000 – 0x081F FFF |
| | **STM32F76xxx/STM32F77xxx**<br>Flash – ITCM<br>0x0020 0000 – 0x003F FFFF<br>**STM32F746xx/STM32F756xx**<br>Flash – ITCM<br>0x0020 0000 – 0x002FF FFFF | NA |

**Table 10. Flash memory differences between STM32F7 Series and STM32H7x3 line devices (continued)**

| Flash | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Main / Program memory | **STM32F76xxx/STM32F77xxx:**<br>Up to 2 Mbytes (single/Dual Bank)<br>Single bank: up to 256 Kbyte sector size<br>Dual bank: up to 128 Kbyte sector size<br>**STM32F746xx/STM32F56xx:**<br>Up to 1 Mbyte (single bank)<br>Up to 256 Kbyte sector size | Up to 2 Mbytes (Dual Bank)<br>128 Kbytes size sector |
| | Programming granularity:64 bits<br>Flash line width: 256 bits or 128 bits | Programming granularity: 256 bits<br>Flash line width: 256 bits |
| Wait State | Up to 9 (depending on the supply voltage and frequency) | Up to 4 (depending on the core voltage and frequency) |
| Option bytes | 32 bytes | 2 Kbytes |
| OTP | 1024 bytes | NA |
| Features | **STM32F76xxx/STM32F77xxx:**<br>– Read While Write (RWW)<br>– Supports dual boot mode<br>– Sector, mass erase and bank mass erase (only in dual bank mode) | – Error Code Correction (ECC)<br>– Double-word, word, half-word and byte read / write operations<br>– Sector erase, Bank erase and Mass erase<br>– Dual-bank organization supporting simultaneous operations: two read/program/erase operations can be executed in parallel on the two banks<br>– Bank swapping: the address mapping of the user Flash memory of each bank can be swapped. |
| Protection mechanisms | Readout protection (RDP) | |
| | NA | – 2 PCROP protection area (1 per bank, execute-only memory)<br>– 2 secure area in user Flash memory (1 per bank)<br>– Sector write protection. |

## 4.4 NVIC

*Table 11* presents the interrupt vector differences between the STM32F7 Series and STM32H7x3 line devices.

**Table 11. Interrupt vector differences between STM32F7 Series and STM32H7x3 line devices**

| Position | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| 3 | RTC_WKP | RTC_TAMP_STAMP_CSS_LSE |
| 18 | ADC | ADC1_2 |
| 19 | CAN1_TX | FDCAN1_IT0 |
| 20 | CAN1_RX0 | FDCAN2_IT0 |
| 21 | CAN1_RX1 | FDCAN1_IT1 |
| 22 | CAN1_SCE | FDCAN2_IT1 |
| 24 | TIM1_BRK_TIM9 | TIM1_BRK |
| 25 | TIM1_UP_TIM10 | TIM1_UP |
| 26 | TIM1_TRG_COM_TIM11 | TIM1_TRG_COM |
| 42 | OTG_FS WKUP | Reserved |
| 63 | CAN2_TX | FDCAN_CAL |
| 64 | CAN2_TX | Reserved |
| 65 | CAN2_RX1 | Reserved |
| 66 | CAN2_SCE | Reserved |
| 67 | OTG_FS | Reserved |
| 98 | DSIHOST | OTG_FS_EP1_OUT |
| 99 | DFSDM1_FLT1 | OTG_FS_EP1_IN |
| 100 | DFSDM1_FLT2 | OTG_FS_WKUP |
| 101 | DFSDM1_FLT3 | OTG_FS |
| 102 | DFSDM1_FLT4 | DMAMUX1_OV |
| 103 | SDMMC2 | HRTIM1_MST |
| 104 | CAN3_TX | HRTIM1_TIMA |
| 105 | CAN3_RX0 | HRTIM_TIMB |
| 106 | CAN3_RX1 | HRTIM1_TIMC |
| 107 | CAN3_SCE | HRTIM1_TIMD |
| 108 | JPEG | HRTIM_TIME |
| 109 | MDIOS | HRTIM1_FLT |

**Table 11. Interrupt vector differences between STM32F7 Series and STM32H7x3 line devices (continued)**

| Position | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| 110 | NA | DFSDM1_FLT0 |
| 111 | | DFSDM1_FLT1 |
| 112 | | DFSDM1_FLT2 |
| 113 | | DFSDM1_FLT3 |
| 114 | | SAI3 |
| 115 | | SWPMI1 |
| 116 | | TIM15 |
| 117 | | TIM16 |
| 118 | | TIM17 |
| 119 | | MDIO_WKUP |
| 120 | | MDIO |
| 121 | | JPEG |
| 122 | | MDMA |
| 124 | | SDMMC |
| 125 | | HSEM0 |
| 127 | | ADC3 |
| 128 | | DMAMUX2_OVR |
| 129 | | BDMA_CH1 |
| 130 | | BDMA_CH2 |
| 131 | | BDMA_CH3 |
| 132 | | BDMA_CH4 |
| 133 | | BDMA_CH5 |
| 134 | | BDMA_CH6 |
| 135 | | BDMA_CH7 |
| 136 | | BDMA_CH8 |
| 137 | | COMP |
| 138 | | LPTIM2 |
| 139 | | LPTIM3 |
| 140 | | LPTIM4 |
| 141 | | LPTIM5 |
| 142 | | LPUART |

**Table 11. Interrupt vector differences between STM32F7 Series and STM32H7x3 line devices (continued)**

| Position | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| 143 | NA | WWDG1_RST |
| 144 | | CRS |
| 145 | | Reserved |
| 146 | | SAI4 |
| 147 | | Reserved |
| 148 | | Reserved |
| 149 | | WKUP |

## 4.5 EXTI

### 4.5.1 EXTI main features in STM32H7x3 line

The Extended Interrupt and event controller (EXTI) manages the wakeup through configurable and direct event inputs. It provides wakeup requests to the power control, generates interrupt requests to the CPU NVIC and to the D3 domain DMAMUX2, and generates events to the CPU event input.

The asynchronous event inputs are classified in 2 groups:

- Configurable events (active edge selection, dedicated pending flag, trigger-able by software)
- Direct events (interrupt and wakeup sources from other peripherals, requiring to be cleared in the peripheral) with the following features:
  - Fixed rising edge active trigger
  - No interrupt pending status register bit in the EXTI (the interrupt pending status is provided by the peripheral generating the event)
  - Individual interrupt and event generation mask
  - No SW trigger possibility
  - Direct system D3 domain wakeup events, that have a D3 pending mask and status register and may have a D3 interrupt signal

*Table 12* describes the difference of EXTI event input types between the STM32F7 Series and the STM32H7x3 line devices.

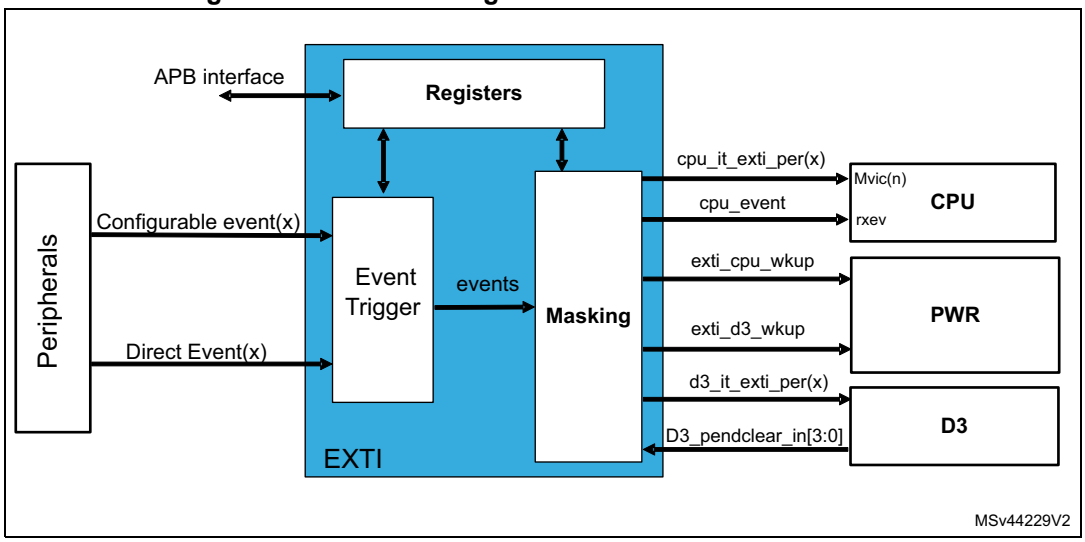
**Table 12. EXTI event input types differences between STM32F7 Series and STM32H7x3 line devices**

| Main Features | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Configurable events | Available | Available |
| Direct events | - | Available |

### 4.5.2 EXTI block diagram in STM32H7x3 line

As shown in *Figure 5*, the EXTI consists of a register block accessed via an APB interface, an event input trigger block, and a Masking block. The Register block contains all the EXTI registers. The event input trigger block provides an event input edge triggering logic.

**Figure 5. EXTI block diagram on STM32H7x3 line devices**




*Note: For more details about EXTI functional description and registers description, refer to RM0433 available on www.st.com.*

*Table 13* presents the EXTI line differences between the STM32F7 Series and STM32H7x3 line devices.

**Table 13. EXTI line differences between STM32F7 Series and STM32H7x3 line devices**

| EXTI line | STM32F7 Series | STM32H7x3 line | |
|---|---|---|---|
| | | Source | Event input type |
| 0 - 15 | EXTI[15:0] | EXTI[15:0] | Configurable |
| 16 | PVD output | PVD and AVD | Configurable |
| 17 | RTC Alarm event | RTC alarms | Configurable |
| 18 | USB OTG FS Wakeup event | RTC tamper, RTC timestamp, RCC LSECSS | Configurable |
| 19 | Ethernet Wakeup event | RTC wakeup timer | Configurable |
| 20 | USB OTG HS (configured in FS) Wakeup event | COMP1 | Configurable |
| 21 | RTC Tamper and TimeStamp events | COMP2 | Configurable |
| 22 | RTC Wakeup event | I2C1 wakeup | Direct |
| 23 | LPTIM1 asynchronous event | I2C2 wakeup | Direct |
| 24 | MDIO Slave asynchronous interrupt | I2C3 wakeup | Direct |

**Table 13. EXTI line differences between STM32F7 Series and STM32H7x3 line devices (continued)**

| EXTI line | STM32F7 Series | STM32H7x3 line | |
|---|---|---|---|
| | | Source | Event input type |
| 25 | NA | I2C4 wakeup | Direct |
| 26 | | USART1 wakeup | Direct |
| 27 | | USART2 wakeup | Direct |
| 28 | | USART3 wakeup | Direct |
| 29 | | USART6 wakeup | Direct |
| 30 | | UART4 wakeup | Direct |
| 31 | | UART5 wakeup | Direct |
| 32 | | UART7 wakeup | Direct |
| 33 | | UART8 wakeup | Direct |
| 34 | | LPUART1 RX wakeup | Direct |
| 35 | | LPUART1 TX wakeup | Direct |
| 36 | | SPI1 wakeup | Direct |
| 37 | | SPI2 wakeup | Direct |
| 38 | | SPI3 wakeup | Direct |
| 39 | | SPI4 wakeup | Direct |
| 40 | | SPI5 wakeup | Direct |
| 41 | | SPI6 wakeup | Direct |
| 42 | | MDIO wakeup | Direct |
| 43 | | USB1 wakeup | Direct |
| 44 | | USB2 wakeup | Direct |
| 47 | | LPTIM1 wakeup | Direct |
| 48 | | LPTIM2 wakeup | Direct |
| 49 | | LPTIM2 output | Configurable |
| 50 | | LPTIM3 wakeup | Direct |
| 51 | | LPTIM3 output | Configurable |
| 52 | | LPTIM4 wakeup | Direct |
| 53 | | LPTIM5 wakeup | Direct |
| 54 | | SWPMI wakeup | Direct |
| 55 | | WKUP1 | Direct |
| 56 | | WKUP2 | Direct |
| 57 | | WKUP3 | Direct |

**Table 13. EXTI line differences between STM32F7 Series and STM32H7x3 line devices (continued)**

| EXTI line | STM32F7 Series | STM32H7x3 line | |
|---|---|---|---|
| | | Source | Event input type |
| 58 | NA | WKUP4 | Direct |
| 59 | | WKUP5 | Direct |
| 60 | | WKUP6 | Direct |
| 61 | | RCC interrupt | Direct |
| 62 | | I2C4 Event interrupt | Direct |
| 63 | | I2C4 Error interrupt | Direct |
| 64 | | LPUART1 global Interrupt | Direct |
| 65 | | SPI6 interrupt | Direct |
| 66 | | DMA1 CH0 interrupt | Direct |
| 67 | | DMA1 CH1 interrupt | Direct |
| 68 | | DMA1 CH2 interrupt | Direct |
| 69 | | DMA1 CH3 interrupt | Direct |
| 70 | | DMA1 CH4 interrupt | Direct |
| 71 | | DMA1 CH5 interrupt | Direct |
| 72 | | DMA1 CH6 interrupt | Direct |
| 73 | | DMA1 CH7 interrupt | Direct |
| 74 | | DMAMUX2 interrupt | Direct |
| 75 | | ADC3 interrupt | Direct |
| 76 | | SAI4 interrupt | Direct |
| 85 | | HDMICEC wakeup | Configurable |
| 86 | | ETHERNET wakeup | Configurable |
| 87 | | HSECSS interrupt | Direct |

*Note: For more details about EXTI events input mapping, refer to EXTI event input mapping section of RM0433 reference manual.*

## 4.6 Reset and clock control

### 4.6.1 Clock management

*Table 14* presents the source clock differences between the STM32F7 Series and the STM32H7x3 line devices.

**Table 14. Different source clock in STM32F7 Series and STM32H7x3 line devices**

| Source clock | | STM32F7 Series | STM32H7x3 line |
|---|---|---|---|
| Internal oscillators | HSI | 16 MHz | 64 MHz |
| | HSI48 | NA | 48 MHz |
| | CSI | NA | 4 MHz |
| | LSI | 32 kHz | 40 kHz |
| External oscillators | HSE | 4-26 MHz | 4-48 MHz |
| | LSE | 32.768 kHz | |
| PLLs | | x3<br>without fractional mode | x3<br>With fractional mode<br>(13-bit fractional multiplication factor) |

### 4.6.2 Peripheral clock distribution

The peripheral clocks are the clocks provided by the RCC to the peripherals. Two kinds of clocks are available:

- The bus interface clocks
- The kernel clocks

On the STM32H7x3 line devices, the peripherals generally receive:

- One or several bus clocks.
- One or several kernel clocks.

*Figure 6* describes the peripheral clock distribution on the STM32H7x3 line devices.

**Figure 6. Peripheral clock distribution on STM32H7x3 line devices**

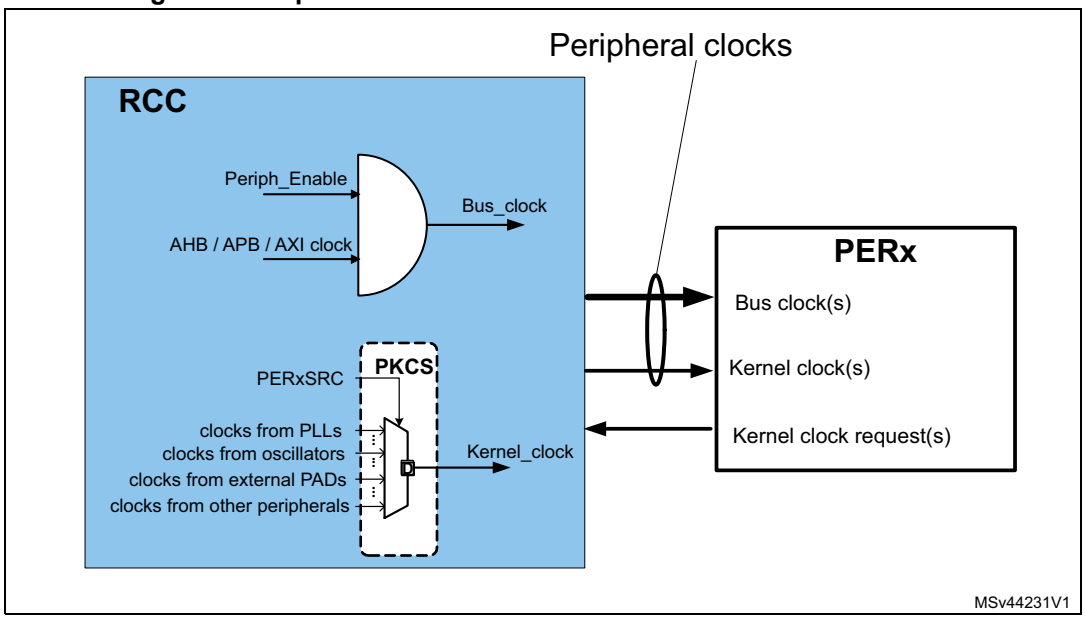



*Table 15* describes an example of peripheral clock distribution for the STM32F7 Series and the STM32H7x3 line devices.

For more details about the kernel peripheral clock distribution, refer to *Kernel clock distribution overview* table of RM0433 reference manual

**Table 15. Peripheral clock distribution example**

| Peripheral | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| **SPI1** | APB2_Clock | **Bus clock**<br>– APB2_Clock<br>**Kernel clock**<br>– Pll1_q_ck/Pll2_p_ck/Pll3_p_ck/I2S_CKIN/ Per_ck |
| **USART1** | **Bus clock**<br>– APB2_Clock<br>**Kernel clock**<br>– LSE<br>– HSI<br>– SYSCLK<br>– PCLK2 | **Bus clock**<br>– APB2_Clock<br>**Kernel clock**<br>– Pll2_q_ck/pll3_q_ck/hsi_ker_ck/csi_ker_ck/lse_ck |

## 4.7 Operating conditions

*Table 16* illustrates the maximum operating frequency of the STM32F7 Series and STM32H7x3 line devices.

**Table 16. General operating conditions for STM32F7 Series and STM32H7x3 line devices**

| Scale | STM32F7 Series max frequency | STM32H7x3 line max frequency | | Unit |
|---|---|---|---|---|
| | | Max CPU | Max D1/D2/D3 | |
| Scale 1 | 216 | 400 | 200 | MHz |
| Scale 2 | 180 | 300 | 150 | |
| Scale 3 | 144 | 200 | 100 | |

# 5 PWR

*Table 17* presents the PWR controller differences between the STM32F7 Series and the STM32H7x3 line devices.

**Table 17. PWR controller differences between STM32F7 Series and STM32H7x3 line devices**

| PWR | | | STM32F7 Series | STM32H7x3 line |
|---|---|---|---|---|
| Power supplies | External power supply for I/Os | | VDD = 1.7 to 3.6 V | VDD = 1.62 to 3.6 V |
| | Internal regulator supplying VCORE | | VDD = 1.7 to 3.6 V | VDDLDO= 1.62 to 3.6 V |
| | External Analog power supply | | – VDDA = 1.7 to 3.6 V<br>– VREF- | |
| | | | – VREF+ : a separate reference voltage, available on VREF+ pin for ADC and DAC | – VREF+: a separate reference voltage, available on VREF+ pin for ADC and DAC<br>– When enabled by ENVR bit in the VREFBUF control and status register(1), VREF+ is provided from the internal voltage reference buffer. |
| | USB power supply | | – VDD33USB = 3.0 to 3.6V | – VDD33USB = 3.0 to 3.6 V<br>– VDD50USB |
| | Backup domain | | VBAT = 1.65 to 3.6 V | VBAT = 1.2 to 3.6 V |
| | Independent power supply | | VDDSDMMC = 3.3V<br>VDDDSI = VDD | NA |
| | VCORE supplies | | 1.08 V ≤ VCAP_1 and VCAP_2 ≤ 1.40 V | 1.05 V ≤ VCAP1 and VCAP2 and VCAP3 ≤ 1.2 V |
| | Reg bypass: must be supplied from external regulator on VCAP pins | VOS1 | 1.32 V | 1.2 V |
| | | VOS2 | 1.26 V | 1.12 V |
| | | VOS3 | 1.14 V | 1.05 V |
| Peripheral supply regulation | | | DSI voltage regulator | USB regulator |
| Power supply supervision | | | – POR/PDR monitor<br>– BOR monitor<br>– PVD monitor | |
| | | | NA | – AVD monitor(2)<br>– VBAT thresholds(3)<br>– Temperature thresholds(4) |

1. For more details about VREFBUF (see *Voltage reference buffer (VREFBUF)* section of RM0433 reference manual).
2. Analog voltage detector (AVD): to monitor the VDDA supply by comparing it to a threshold selected by the ALS[1:0] bits in the PWR_CR1 register. The AVD is enabled by setting the AVDEN bit in the PWR_CR1 register.
3. Battery voltage thresholds (VBAT thresholds): indicate if VBAT is higher or lower than the threshold. The VBAT supply monitoring can be enabled/disabled via MONEN bit in the PWR_CR2 register.
4. Temperature thresholds: the temperature monitoring can be enabled/disabled via MONEN bit in the PWR_CR2 register. It indicates whether the device temperature is higher or lower than the threshold.

# 6 System configuration controller

*Table 18* illustrates the SYSCFG main differences between the STM32F7 Series and the STM32H7x3 line devices.

**Table 18. SYSCFG main features differences between STM32F7 Series and STM32H7x3 line devices**

| | **STM32F7 Series** |
|---|---|
| **SYSCFG** | – Remap the memory areas<br>– Managing Class B feature |
| | **STM32F7 Series and STM32H7x3 line** |
| | – Select the Ethernet PHY interface<br>– Managing the external interrupt line connection to the GPIOs<br>– Managing I/O compensation cell feature<br>– I2C Fast mode + configuration |
| | **STM32H7x3 line** |
| | New features added in STM32H7x3 line:<br>– Analog switch configuration management<br>– Getting readout protection and Flash memory bank swap informations<br>– Management of boot sequences and boot addresses<br>– Getting BOR reset level<br>– Getting Flash memory secured and protected sector status<br>– Getting Flash memory write protections status<br>– Getting DTCM secured section status<br>– Getting independent watchdog behavior (hardware or software / freeze)<br>– Reset generation in Stop and Standby mode<br>– Getting secure mode enabling/disabling |

*Note: For more details, refer to SYSCFG register description section of RM0433 reference manual.*

# 7 SDMMC

*Table 19* presents the differences between the SDMMC interface of the STM32F7 Series and STM32H7x3 line devices

**Table 19. SDMMC differences between STM32F7 Series and STM32H7x3 line devices**

| SDMMC | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Features | – Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit | – Full compliance with MultiMediaCard System Specification Version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit |
| | – Full compliance with SD Memory Card Specifications Version 2.0 | – Full compliance with SD memory card specifications version 4.1. |
| | – Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit | – Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit. |
| | – Data transfer up to 200 Mbyte/s for the 8-bit mode. | – Data transfer up to 208 Mbyte/s for the 8-bit mode.(1) |
| | NA | – SDMMC IDMA: is used to provide high speed transfer between the SDMMC FIFO and the memory. The AHB master optimizes the bandwidth of the system bus. The SDMMC internal DMA (IDMA) provides one channel to be used either for transmit or receive. |

1. Depending of the maximum allowed IO speed. for more details refer to datasheet.

# 8 U(S)ART

The STM32H7x3 line devices implement several new features on the U(S)ART compared to the STM32F7 Series devices. *Table 20* shows the U(S)ART differences.

**Table 20. U(S)ART differences between STM32F7 Series and STM32H7x3 line devices**

| U(S)ART | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| **Instances** | – 4 x USART<br>– 4 x UART | – 4 x USART<br>– 4 x UART<br>– 1 x LPUART |
| **Clock** | – Dual clock domain with dedicated kernel clock for peripherals independent from PCLK | |
| **Wakeup** | NA | – Wakeup from low-power mode |
| **Features** | | – SPI slave transmission, underrun flag<br>– Two internal FIFOs for transmit and receive data<br>– Each FIFO can be enabled/disabled by software and come with a status flag. |

# 9 SPI

The STM32H7x3 line devices implement some enhanced SPI compared to the STM32F7 Series devices. *Table 21* shows the SPI differences.

**Table 21. SPI differences between STM32F7 Series and STM32H7x3 line devices**

| SPI | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Instances | x4 | x6 |
| Clock | Single clock domain | Dual clock domain with dedicated kernel and serial interface clock independent from PCLK with transmission and reception capability at low-power stop |
| Wakeup | NA | Wakeup from low-power mode |
| Features | – Full-duplex synchronous transfers on three lines (with two separated data lines)<br>– Half-duplex synchronous transfer on two lines (with single bidirectional data line)<br>– Simplex synchronous transfers on two lines (with unidirectional data line)<br>– 8 master mode baud rate prescalers up to fPCLK/2.<br>– Slave mode frequency up to fPCLK/2.<br>– NSS management by hardware or software for both master and slave<br>– Master and slave capability, multi-master multi-slave support<br>– Programmable clock polarity and phase<br>– Programmable data order with MSB-first or LSB-first shifting<br>– Dedicated transmission, reception and error flags with interrupt capability<br>– SPI Motorola and TI formats support<br>– Hardware CRC feature for reliable communication (at the end of transaction):<br>- Configurable size and polynomial<br>- Autommatic CRC upend in Tx mode<br>- Automatic CRC check in Rx mode<br>– Configurable RxFIFO threshold, data packeting support<br>– Configurable data size (4-32 bit) | |

**Table 21. SPI differences between STM32F7 Series and STM32H7x3 line devices (continued)**

| SPI | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Features (continued) | – Two 32-bit embedded Rx and Tx FIFOs with DMA capability<br>– CRC pattern size 8 or 16 bit<br>– RxFIFO threshold 8 or 16 bit | – Protection of configuration and setting<br>– Adjustable minimum delays between data and between SS and data flow at master<br>– Configurable SS signal polarity and timing, MISO x MOSI swap capability<br>– Programmable number of data within a transaction to control SS and CRC<br>– Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability<br>– Programmable number of data in transaction<br>– Configurable behavior at slave underrun condition (support of cascaded circular buffers)<br>– Master automatic suspend at receive mode<br>– Master start/suspend control<br>– Alternate function control of associated GPIOs<br>– Selected status and error flags with wake up capability<br>– CRC pattern size configurable from 4 to 32 bit<br>– CRC polynomial length configurable<br>– RxFIFO threshold from 1 to 16 data |

# 10 I2S

*Table 22* presents the I2S differences between the STM32F7 Series and STM32H7x3 line devices.

**Table 22. I2S differences between STM32F7 Series and STM32H7x3 line devices**

| I2S | STM32F7 Series | STM32H7x3 Line |
|---|---|---|
| Features | – Full duplex only when the extension module is implemented | – Full duplex native |
| | – Minimum allowed value = 4 | – More flexible clock generator (division by 1,2 are possible) |
| | – Sampling edge is not programmable | – Programmable sampling edge for the bit clock |
| | – Frame sync polatiry cannot be selected | – Programmable frame sync polarity |
| | – Receive buffer accessible in half-word | – Receive buffer accessible in half-word and words |
| | – Data are right aligned into the receive buffer | – Various data arrangement available into the receive buffer |
| | – Error flags signaling for Underrun, Overrun and Frame Error | – Error flags signaling for Underrun, Overrun and Frame Error |
| | NA | – Improved reliability: Automatic resynchronization to the frame sync in case of frame error |
| | | – Improved reliability: Re-alignement of left and right samples in case of underrun or overrun situation |
| | | – MSb/LSb possible in the serial data interface |
| | – 16 or 32 bits channel length in MASTER | – 16 or 32 bits channel length in MASTER |
| | – 16 or 32 bits channel length in SLAVE | – Any channel length in SLAVE |
| | NA | – Embedded RX and TX FIFOs |
| | – DMA capabilities (16-bit wide) | – DMA capabilities (16-bit and 32-bit wide) |

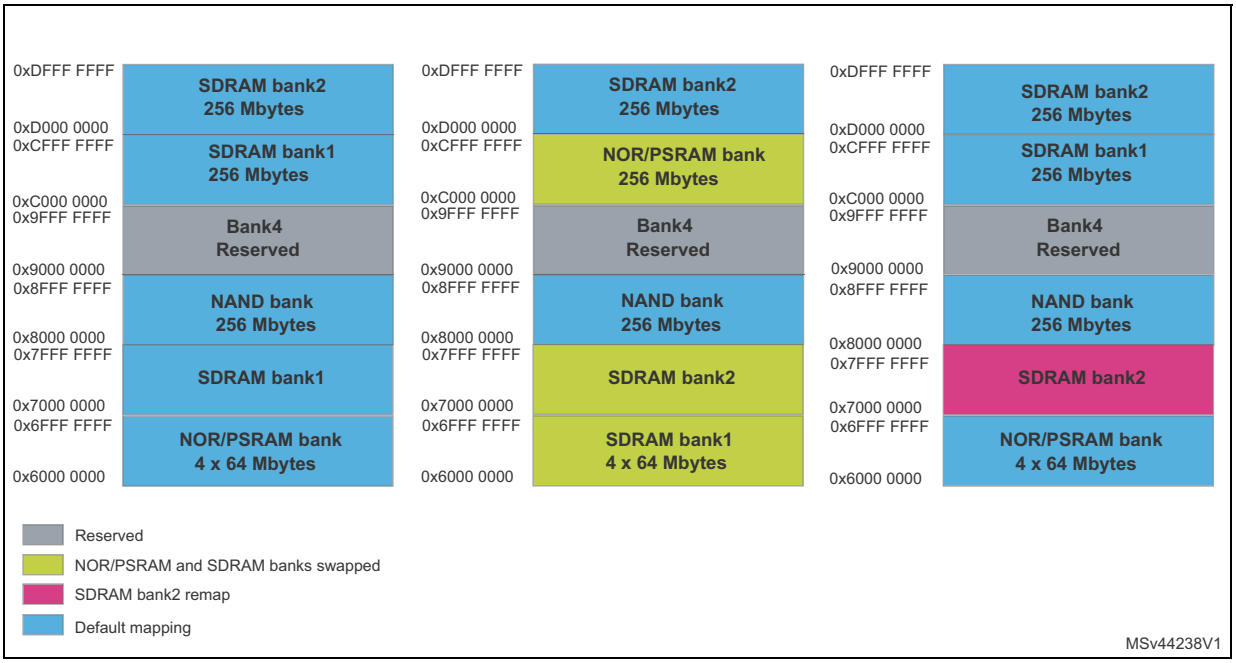
# 11 FMC

*Table 23* presents the FMC differences between the STM32F7 Series and STM32H7x3 line devices.

**Table 23. FMC differences between STM32F7 Series and STM32H7x3 line devices**

| FMC | STM32F7 Series | STM32F7 Series |
|---|---|---|
| Mapping | AHB | AXI |
| Clock | Single clock domain | Dual clock domain with dedicated kernel clock for peripherals independent from AXI clock |
| Bank remap | **SYSCFG_MEMRMP register:**<br>– FMC bank mapping can be configured by software through the SWP_FMC[1:0] bits. | **FMC_BCR1 register:**<br>– FMC bank mapping can be configured by software through the BMAP[1:0] bits. (see *Figure 7*) |
| Features | NA | – **FMCEN bit**: FMC controller Enable bit added in the FMC_BCR1 register.<br>– To modify some parameters while FMC is enabled follow the below sequence:<br>1. First disable the FMC controller to prevent any further accesses to any memory controller during register modification.<br>2. Update all required configurations.<br>3. Enable the FMC controller again.<br>When the SDRAM controller is used, if the SDCLK Clock ratio or refresh rate has to be modified after initialization phase, the following procedure must be followed.<br>– Put the SDRAM device in Self-refresh mode.<br>– Disable the FMC controller by resetting the FMCEN bit in the FMC_BCR1 register.<br>– Update the required parameters.<br>– Enable the FMC controller once all parameters are updated.<br>– Then, send the Clock Configuration Enable command to exit Self-fresh mode. |

**Figure 7. FMC bank address mapping on STM32H7x3 line devices**



# 12 ADC

*Table 24* presents the differences between the ADC peripheral of the STM32F7 Series and the STM32H7x3 devices.

**Table 24. ADC differences between STM32F7 Series and STM32H7x3 line devices**

| ADC | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Instances | X3 | X3 |
| Clock | Single clock domain | Dual clock domain with dedicated kernel clock for peripherals independent from CLK or HCLK |
| Number of channels | Up to 24 channels | Up to 20 channels |
| Resolution | 12, 10, 8 or 6-bit | 16, 14, 12, 10 or 8-bit |
| Conversion modes | – Single<br>– Continuous<br>– Scan<br>– Discontinuous<br>– Dual and triple mode | |
| DMA | YES | |
| New features | NA | – Input voltage reference from VREF+ pin or internal VREFBUF reference<br>– ADC conversion time is independent from the AHB bus clock frequency<br>– Self-calibration (both offset and the linearity)<br>– Low-power features<br>– 3 analog watchdogs per ADC<br>– Internal dedicated channels:<br>- The internal DAC channel 1 and channel 2 are connected to ADC2<br>– Oversampler:<br>- 32-bit data register<br>- Oversampling ratio adjustable from 2 to 1024<br>- Programmable data right and left shift<br>– Data can be routed to DFSDM for post processing |

*Table 25* and *Table 26* present the differences of external trigger for regular channels and injected channels between the STM32F7 Series and STM32H7x3 line. devices.

**Table 25. External trigger for regular channel differences between STM32F7 Series and STM32H7x3 line devices**

| Type | EXTSEL[3:0] STM32F7 Series | EXTSEL[4:0] STM32H7x3 line3 | Source | |
|---|---|---|---|---|
| | | | STM32F7 Series | STM32H7x3 line |
| Internal signal from on-chip timers | 0000 | 00000 | TIM1_CC1 event | |
| | 0001 | 00001 | TIM1_CC2 event | |
| | 0010 | 00010 | TIM1_CC3 event | |
| | 0011 | 00011 | TIM2_CC2 event | |
| | 0100 | 00100 | TIM5_TRGO event | TIM3_TRGO event |
| | 0101 | 00101 | TIM4_CC4 event | |
| | 0110 | 00110 | TIM3_CC4 | EXTI line 11 |
| | 0111 | 00111 | TIM8_TRGO event | |
| | 1000 | 01000 | TIM8_TRGO(2) event | |
| | 1001 | 01001 | TIM1_TRGO event | |
| | 1010 | 01010 | TIM1_TRGO(2) event | |
| | 1011 | 01011 | TIM2_TRGO event | |
| | 1100 | 01100 | TIM4_TRGO event | |
| | 1101 | 01101 | TIM6_TRGO event | |
| | NA | 01110 | EXTI line11 | TIM15_TRGO event |
| | 1111 | 01111 | NA | TIM3_CC4 event |
| | NA | 10000 | | HRTIM1_ADCTRG1 event |
| | | 10001 | | HRTIM1_ADCTRG3 event |
| | | 10010 | | LPTIM1_OUT event |
| | | 10011 | | LPTIM2_OUT event |
| | | 10100 | | LPTIM3_OUT event |

**Table 26. External trigger for injected channel differences between STM32F7 Series and STM32H7x3 line devices**

| Type | JEXTSEL[3:0] STM32F7 Series | JEXTSEL[4:0] STM32H7x3 line | Source | |
|---|---|---|---|---|
| | | | STM32F7 Series | STM32H7x3 line |
| Internal signal from on-chip timers | 0000 | 00000 | TIM1_TRGO event | |
| | 0001 | 00001 | TIM1_CC4 event | |
| | 0010 | 00010 | TIM2_TRGO event | |
| | 0011 | 00011 | TIM2_CC1 event | |
| | 0100 | 00100 | TIM3_CC4 event | |
| | 0101 | 00101 | TIM4_TRGO event | |
| | NA | 00110 | NA | EXTI line 15 |
| | 0111 | 00111 | TIM8_CC4 event | |
| | 1000 | 01000 | TIM1_TRGO(2) event | |
| | 1001 | 01001 | TIM8_TRGO event | |
| | 1010 | 01010 | TIM8_TRGO(2) event | |
| | 1011 | 01011 | TIM3_CC3 event | |
| | 1100 | 01100 | TIM5_TRGO event | |
| | 1101 | 01101 | TIM3_CC1 event | |
| | 1110 | 01110 | TIM6_TRGO event | TIM6_TRGO event |
| | NA | 01111 | NA | TIM15_TRGO event |
| | | 10000 | | HRTIM1_ADCTRG2 event |
| | | 10001 | | HRTIM1_ADCTRG4 event |
| | | 10010 | | LPTIM1_OUT event |
| | | 10011 | | LPTIM2_OUT event |
| | | 10100 | | LPTIM3_OUT event |

# 13 DAC

The STM32H7x3 line devices implement some enhanced DAC compared to the STM32F7 Series devices. *Table 27* shows the DAC differences.

**Table 27. DAC differences between STM32F7 Series and STM32H7x3 line devices**

| DAC | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Clock | Single clock domain | Single clock domain (APB),<br>LSI is used for sample and hold mode |
| Features | – Input voltage reference, VREF+ | – Input voltage reference from VREF+ pin or internal VREFBUF reference |
| | NA | – Buffer offset calibration<br>– DAC output connection to on chip peripherals<br>– Sample and hold mode for low power operation in Stop mode |

# 14 USB_OTG

The STM32H7x3 line devices embed two instances of USB_OTG_HS while the STM32F7 Series devices embed one instance of USB_OTG_HS and one instance of USB_OTG_FS.

*Table 28* summarizes the difference of USB_OTG_HS between the STM32F7 Series and the STM32H7x3 line devices.

**Table 28. USB_OTG_HS differences between STM32F7 Series and STM32H7x3 line devices**

| USB_OTG_HS | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Instance | x1 | x2(1) |
| Device bidirectional endpoints (including EP0) | 9 | |
| Host mode channels | 16 | |
| Size of dedicated SRAM | 4 Kbytes | |
| USB 2.0 Link Power Management (LPM) support | Yes | |
| OTG revision supported | 1.3, 2.0 | 2.0 |
| Attach Detection Protocol (ADP) support | Not supported | |
| Battery Charging Detection (BCD) support | No | Yes |
| ULPI available to primary IOs via, muxing | Yes | |
| DMA availability | Yes | |

1. On the STM32H7 Series devices although both OTG_HS1 and OTG_HS2 can potentially be programmed for HS operation, only OTG_HS1 has an accessible ULPI interface which will allow a High Speed operation using an external HS transceiver.

# 15 Ethernet

The STM32H7x3 line devices implement several new features on the Ethernet compared to the STM32F7 Series devices. *Table 29* shows the Ethernet differences.

**Table 29. Ethernet differences between STM32F7 Series and STM32H7x3 line devices**

| Ethernet | STM32F7 Series | STM32H7x3 line |
|---|---|---|
| Operation modes and PHY support | – 10/100 Mbps data rate<br>– Full-duplex and half-duplex operations<br>– MII and RMII interface to external PHY | |
| Processing control | NA | – Multi-layer filtering (Layer 3 and 4, VLAN and MAC filtering)<br>– Double VLAN support (C-VLAN+ S-VLAN) |
| Offload processing | NA | – Automatic ARP response<br>– TCP segmentation |
| Low-power mode | – Remote wakeup packet and AMD Magic Packet™ detection | |
| | NA | – Energy Efficient Ethernet (EEE) |

# 16 Digital filter for sigma delta modulators (DFSDM)

The STM32H7x3 line devices implement several new features on the DFSDM compared to the STM32F76xxx and STM32F77xxx devices. *Table 30* shows the DFSDM differences.

**Table 30. DFSDM differences between STM32F76xxx and STM32F77xxx devices and STM32H7x3 line devices**

| DFSDM | STM32F76xxx / STM32F77xxx | STM32H7x3 line |
|---|---|---|
| Number of channels | 8 | |
| Number of filters | 4 | |
| Input from ADC | NA | Yes |
| Supported trigger sources | 12 | 16 |

*Table 31* presents the DFSDM internal signals differences between the STM32F76xxx and STM32F77xxx devices and the STM32H7x3 line devices.

**Table 31. DFSDM internal signal differences between STM32F76xxx and STM32F77xxx devices and STM32H7x3 line devices**

| Name | STM32F76xxx / STM32F77xxx | STM32H7x3 line |
|---|---|---|
| Internal/ external trigger signal | Refer to *Table 32* for DFSDM triggers signals connections | |
| break signal output | Refer to *Table 33* for DFSDM break signal connections | |
| DMA request signal | 4 DMA request from DFSDM_FLTx (x =0..3) | |
| Interrupt request signal | 4 interrupt request from each DFSDM_FLTx (x=0..3) | |
| ADC input data | NA | dfsdm_dat_adc[15:0] |

*Table 32* describes the DFSDM triggers connection differences between the STM32F76xxx and STM32F77xxx devices and the STM32H7x3 line devices.

**Table 32. DFSDM trigger connection differences between STM32F76xxx and STM32F77xxx devices and STM32H7x3 line devices**

| Trigger name | STM32F76xxx / STM32F77xxx | STM32H7x3 line |
|---|---|---|
| DFSDM_JTRG[0] | TIM1_TRGO | |
| DFSDM_JTRG[1] | TIM1_TRGO2 | |
| DFSDM_JTRG[2] | TIM8_TRGO | |
| DFSDM_JTRG[3] | TIM8_TRGO2 | |
| DFSDM_JTRG[4] | TIM3_TRGO | |
| DFSDM_JTRG[5] | TIM4_TRGO | |
| DFSDM_JTRG[6] | TIM10_OC1 | TIM16_OC1 |
| DFSDM_JTRG[7] | TIM6_TRGO | |
| DFSDM_JTRG[8] | TIM7_TRGO | |
| DFSDM_JTRG[9] | Reserved | HRTIM1_ADCTRG1 |
| DFSDM_JTRG[10] | Reserved | HRTIM1_ADCTRG3 |
| DFSDM_JTRG[23 :11] | Reserved | |
| DFSDM_JTRG[24] | EXTI11 | |
| DFSDM_JTRG[25] | EXTI15 | |
| DFSDM_JTRG[26] | LPTIMER1 | |
| DFSDM_JTRG[27] | Reserved | LPTIMER2 |
| DFSDM_JTRG[28] | Reserved | LPTIMER3 |
| DFSDM_JTRG[31 :29] | Reserved | |

*Table 33* presents the DFSDM break connections differences between the STM32F76xxx and STM32F77xxx devices and the STM32H7x3 line devices.

**Table 33. DFSDM break connection differences between STM32F76xxx and STM32F77xxx devices and STM32H7x3 line devices**

| Break name | STM32F76xxx / STM32F77xxx | STM32H7x3 line |
|---|---|---|
| DFSDM_BREAK[0] | TIM1 break | TIM15 break |
| DFSDM_BREAK[1] | TIM1 break2 | TIM16 break2 |
| DFSDM_BREAK[2] | TIM8 break | TIM1/TIM17/TIM8 break |
| DFSDM_BREAK[3] | TIM8 break2 | TIM1/TIM8 break2 |

# 17 Conclusion

This application note is a useful complement to the datasheets and the reference manuals, which gives a simple guideline to migrate an existing product based on the STM32F7 Series to the STM32H7x3 line.

# 18 Revision history

Table 34. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 30-May-2017 | 1 | Initial release. |