AN5034
Application note

12 V - 210 W converter based on STCMB1, combo TM PFC, HB LLC and SRK2001, adaptive SR controller

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Introduction

This application note describes the EVLCMB1-AIO210W demonstration board, a 12 V - 210 W converter tailored for the typical specification of an AC/DC adapter for all in one computers, with a wide input mains range and very low power consumption at the light load.

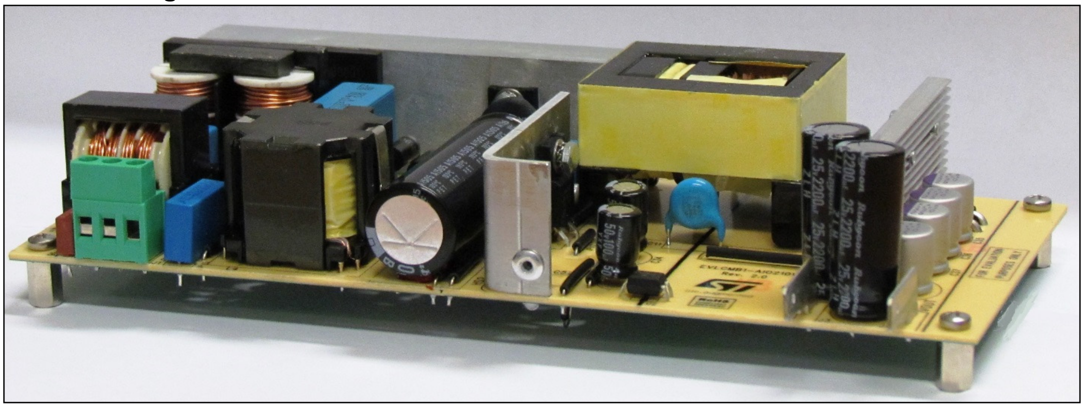
The architecture is based on a two-stage approach: a front-end transition mode PFC pre-regulator and a downstream LLC resonant half bridge converter. At secondary, synchronous rectification is controlled by the SRK2001 that allows an overall efficiency improvement with a very low external component count.

The PFC and LLC controllers are both integrated in the STCMB1 combo integrated circuit that also integrates a high voltage start-up generator, an X-capacitor discharge circuit, the AC brownout/in function and a complete set of protections as detailed later on.

The PFC section of the STCMB1 uses a proprietary constant-on-time control methodology that does not require a sinusoidal input reference, thereby reducing the system cost and external component count. It also includes burst mode function that is independent on the LLC, cycle-by-cycle overcurrent protection on the whole input current, output overvoltage protection, latched feedback failure protection, boost inductor saturation and inrush current detection at both the start-up and after mains sags or missing cycles.

The LLC section of the STCMB1 is based on a proprietary time shift control method that improves dynamic behavior and input ripple rejection resulting in a cleaner output voltage. It includes the adaptive dead time function, burst mode function that masters on the PFC, proprietary safe-start procedure, hard-switching protection, anti-capacitive protection, two-level cycle-by-cycle overcurrent protection the with automatic restart, DC brownout protection.

Figure 1. EVLCMB1-AIO210W:210W SMPS demonstration board



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1 Main characteristics, converter architecture and controller description

In this section, the main characteristics and the converter architecture are summarized. Moreover, a brief description is given of the STCMB1, the controller on which the EVLCMB1-AIO210W is based. Main features of the EVLCMB1-AIO210W are listed in *Table 1*.

Table 1. Main features of EVLCMB1-AIO210W

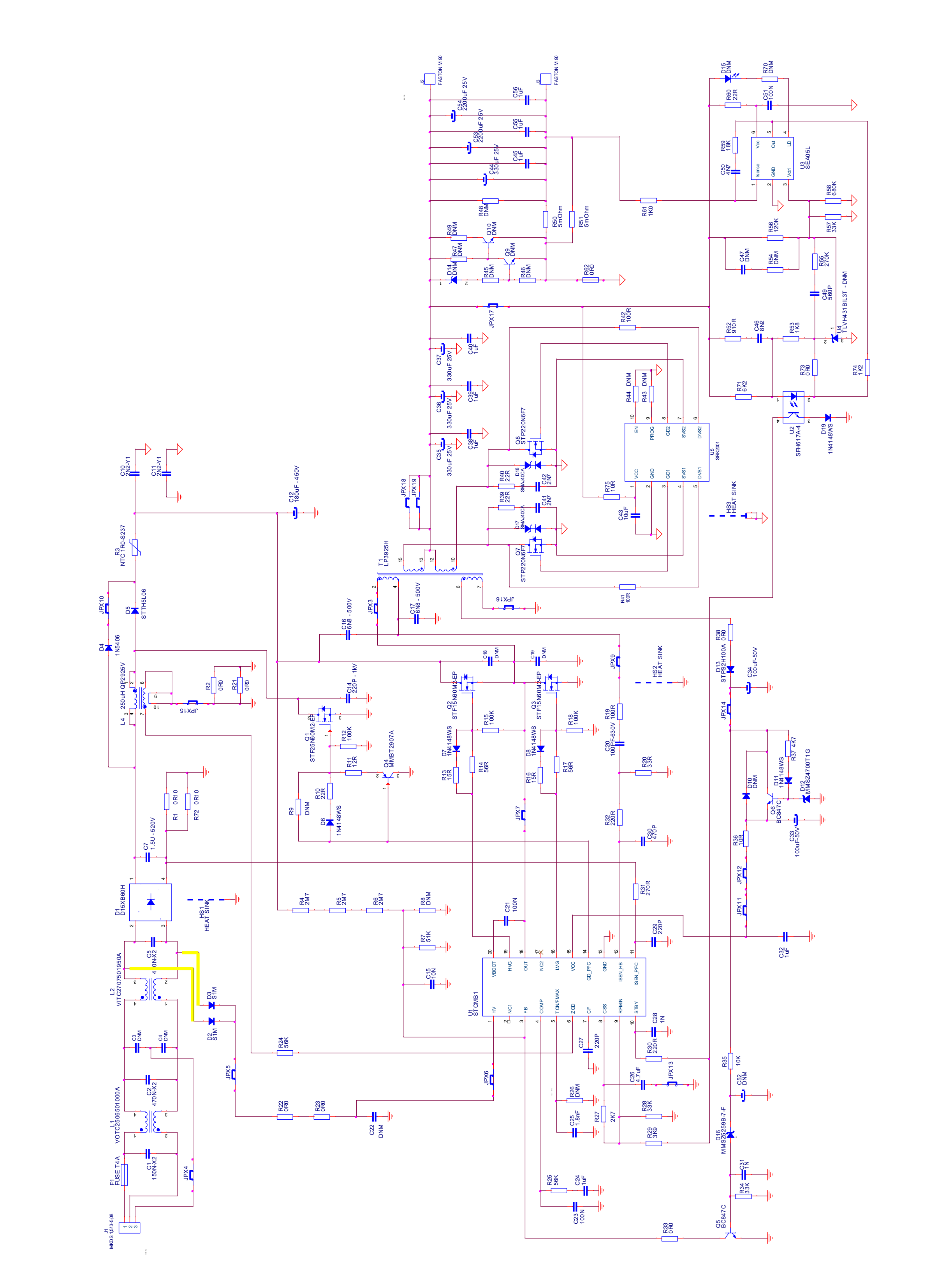
Parameter	Value
Input mains range	90 ÷ 264 Vac - frequency 45 ÷ 65 Hz
Output voltage	12 V at 17.5 A, continuous operation
Full load efficiency	> 90% at 115 / 230 Vac
Avg. efficiency (at 25, 50, 75, 100% of full load)	> 90% at 115 / 230 Vac
Efficiency (at 250 mW)	> 60% at 115 / 230 Vac
No load mains consumption	< 90 mW
Mains harmonics according to	EN61000-3-2 Class-D and JEITA-MITI, Class-D
EMI	According to EN55022 Class-B
Safety	According to EN60950
Dimensions	190 x 82 mm, height = 32
PCB	Single side, 70 μm, CEM-1, mixed PTH/SMT

The EVLCMB1-AIO210W is a two-stage converter: a front-end transition mode PFC pre-regulator and a downstream LLC resonant half bridge converter, both controlled by the STCMB1 combo IC. The PFC section of the STCMB1 is a proprietary constant-on-time PFC controller operating in transition mode. The LLC section of the STCMB1 integrates all the functions necessary to operate the resonant converter with the 50% duty cycle and variable working frequency, based a proprietary time shift control method. At secondary side, synchronous rectification is controlled by the SRK2001. The control loop is based on the SEA05L: the CV loop is active up to about 19.5 A, then the CC loop starts to limit the output current while the output voltage decreases.

The STCMB1 also integrates a comprehensive set of features that allows the design of a robust and safe SMPS, for both the final user and the supplied system, while keeping a reduced external component count. Such features are the high voltage start-up generator, the X-capacitor discharge circuit, the AC and DC brownout/in functions, cycle-by-cycle overcurrent protections on the whole boost inductor current and on the resonant tank current, the latched feedback failure protection, the boost inductor saturation and inrush current detection.

In order to reach very low power consumption at the light loads, burst mode management functions are also embedded in the STCMB1. The PFC section can enter in the burst load driven by its feedback signal and independently on the LLC: this is especially useful when the converter operates in the high mains range with the moderate output load. The system level burst mode is mastered by the LLC section when the output load becomes very low. In this case, the STCMB1 enters in an idle state driven by the decreasing feedback signal (from the secondary side to the primary side, through the optocoupler) below a threshold. As the feedback signal rises again above the threshold plus a hysteresis, the STCMB1 exits the idle state and switching restarts. In this way, negative feedback is of course maintained, but the control changes from continuous to discrete. Last but not least, the system level burst mode includes a proprietary IP that allows minimizing the number of cycles in the burst packet and so minimizing the switching losses. Details about the burst mode management are given in *Section 6.3 on page 21*, *Section 6.4 on page 22* and in the datasheet of the STCMB1. The schematic of the EVLCMB1-AIO210W is shown in *Figure 2*.

Figure 2. EVLCMB1-AIO210W demonstration board schematic



2 Efficiency measurements

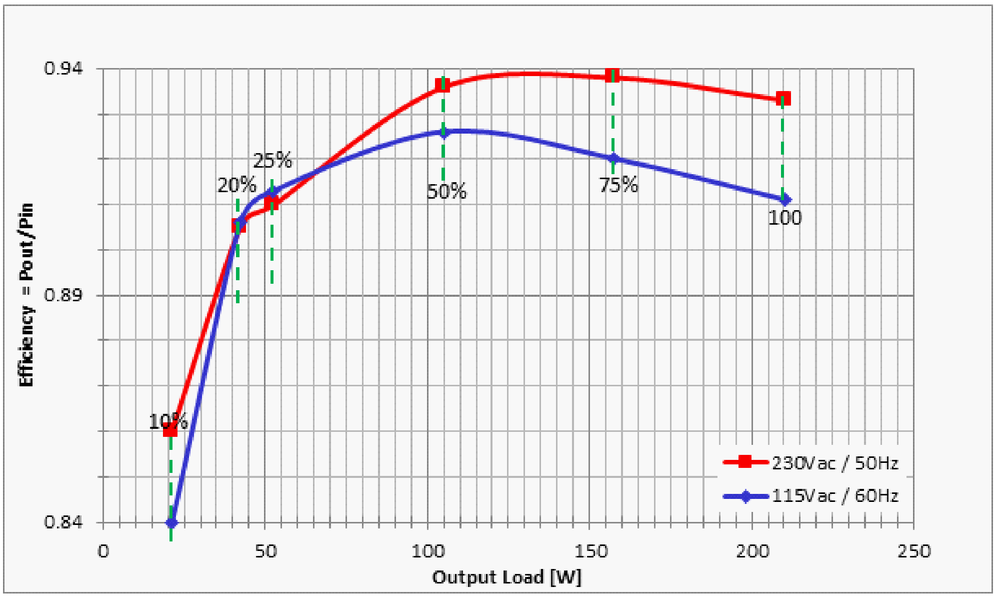
2.1 Overall efficiency

Table 2 and *Figure 3* show the overall efficiency of the EVLCMB1-AIO210W demonstration board, measured at the nominal mains voltages, after a warm up time of about 1h at 230Vac and 115Vac, 210W, after which each measurement point has been kept for about ½h, starting from heavy loads down to light loads. The active load has been set in the CC mode with output voltage sensing. The output voltage and power have been read on the active load display, while the output current has been computed as Pout / Vout. The input power has been measured by means of a power meter with the voltage probe at the Vac inlet of the converter. Oscilloscope probes have been placed on output voltage and half bridge node to check the operation of the adapter.

Table 2. Overall efficiency

Output load	230 Vac / 50 Hz					115 Vac / 60 Hz				
	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η
10%	11.933	1.77	21.07	24.51	0.86	11.951	1.76	21.04	25.07	0.839
20%	11.897	3.54	42.16	46.58	0.905	11.917	3.54	42.15	46.51	0.906
25%	11.876	4.42	52.49	57.68	0.91	11.892	4.41	52.44	57.42	0.913
50%	11.787	8.91	105.03	112.17	0.936	11.788	8.91	105.05	113.48	0.926
75%	11.698	13.47	157.61	168.06	0.938	11.701	13.47	157.66	171.29	0.92
100%	11.608	18.09	210.03	225.07	0.933	11.612	18.1	210.13	230.74	0.911
-	Average (100, 75, 50 25%) =				0.929	Average (100, 75, 50 25%) =				0.918

Figure 3. Overall efficiency vs. output load



2.2 Efficiency at light load operation

Light load performances are pretty much important because the power consumption of the appliances during the stand-by and off-mode has decreased. *Table 3* and *Figure 4* show the light load consumption of the EVLCMB1-AIO210W demonstration board, measured at the nominal mains voltages.

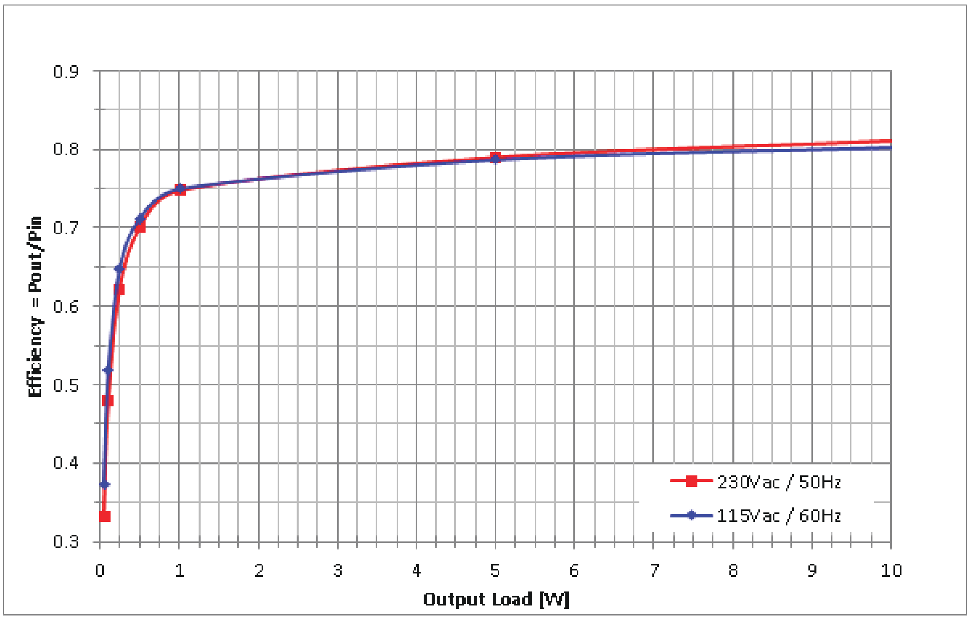
Measurement procedure

1. The board under the test is supplied by an AC source and it is loaded by an active load set in the CP mode with VOUT sensing. The input power and voltage are measured by a power meter while the output power and voltage are read on the active load display. The power meter connection is such that the current probing is toward the board under the test, while the voltage probing is toward the AC source.
2. At light loads, the current drawn by the board under the test from the AC source is irregular and its measurement is typically unstable. To overcome this issue, the active energy consumption is measured, in mWh, by integration and the corresponding input power is computed as energy by time. For the very light loads, i.e. from the open load to 500 mW, integration time has been 6 min.; conversely, for loads between 1 W and 10 W, the integration time has been 36 s.
3. In order to control the proper operation of the converter during the test, a high voltage oscilloscope probe is connected to the HB node. Each measurement point is kept for about 5min., hence the values are taken. Loads have been applied increasing the output power from minimum to maximum. The output current is computed as the output power divided by the output voltage.

Table 3. Light load efficiency

Output load	230 Vac / 50 Hz					115 Vac / 60 Hz				
	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η	Vout [V]	Iout [A]	Pout [W]	Pin [W]	η
0 mW	12.004	-	-	0.081	-	12.004	-	-	0.076	-
50 mW	12.004	0.004	0.049	0.147	0.333	12.004	0.004	0.049	0.131	0.374
100 mW	12.004	0.009	0.103	0.215	0.479	12.004	0.009	0.103	0.199	0.518
250 mW	12.004	0.021	0.247	0.397	0.622	12.004	0.021	0.247	0.382	0.647
500 mW	12.004	0.042	0.5	0.714	0.7	12.004	0.042	0.499	0.701	0.712
1 W	12	0.084	1.006	1.345	0.748	12.001	0.084	1.006	1.342	0.75
5 W	11.995	0.417	5.001	6.334	0.79	12.997	0.417	5	6.353	0.787
10 W	11.988	0.834	10.001	12.337	0.811	12.989	0.834	10.003	12.464	0.803

Figure 4. Light load efficiency vs. output load



3 Eco-design requirement verification

The following tables show the compliance of the regulation requirements for Eco-design of the EVLCMB1-AIO210W.

Table 4. ENERGY STAR® requirements for computers ver. 6.1

ENERGY STAR for computers ver. 6.1	Test results		Limits	Status
	230 Vac / 50 Hz	115 Vac / 60 Hz		
Efficiency at 20% load	90.5	90.6	> 82%	Pass
Efficiency at 50% load	93.6	92.6	> 85%	
Efficiency at 100% load	93.3	91.1	> 82%	
Power factor at 100% load	0.979	0.997	> 0.9	

Table 5. EuP Lot 6 Tier 2 requirements for household and office equipment

EuP Lot 6 Tier 2	Test results		Limits	Status
	230 Vac / 50 Hz	115 Vac / 60 Hz		
Avg. efficiency measured at 25, 50, 75, 100%	92.9	91.8	> 87%	Pass
Efficiency at 250 mW load	62.2	64.7	> 50%	
Efficiency at 100 mW load	47.9	51.8	> 33%	

Table 6. European CoC ver. 5 Tier 2 requirements for external power supplies

European CoC ver. 5 Tier-2 for ext. pow. sup.	Test results		Limits	Status
	230 Vac / 50 Hz	115 Vac / 60 Hz		
Avg. efficiency measured at 25, 50, 75, 100%	92.8	91.8	> 89%	Pass
Efficiency at 10% load	86.0	83.9	> 79%	
No load input power [W]	0.09	0.08	< 0.15 W	

Table 7. Ecos consulting 80 plus GOLD

Ecos consulting 80 plus	Test results		Limits			Status
	230 Vac / 50 Hz	115 Vac / 60 Hz	115 Vac internal non red. PLATINUM	230 Vac internal redundant GOLD	230 Vac EU internal non red. GOLD	
Efficiency at 20% load	90.5	90.6	> 90%	> 88%	> 90%	PASS
Efficiency at 50% load	93.6	92.6	> 92%	> 92%	> 92%	
Efficiency at 100% load	93.3	91.1	> 89%	> 88%	> 89%	
Power factor at 50% load	0.917	0.992	> 0.95	> 0.9	> 0.9	

4 THD and PF measurement

As a check of the overall operation of the converter, the total harmonic distortion and the power factor have been measured against the mains voltage, at the full, half and quarter load. The results are summarized in *Figure 5* and *Figure 6*. Note that PFC is operating in its own burst mode in the case 265 Vac / 52.5 W.

Figure 5. Total harmonic distortion vs. Vac

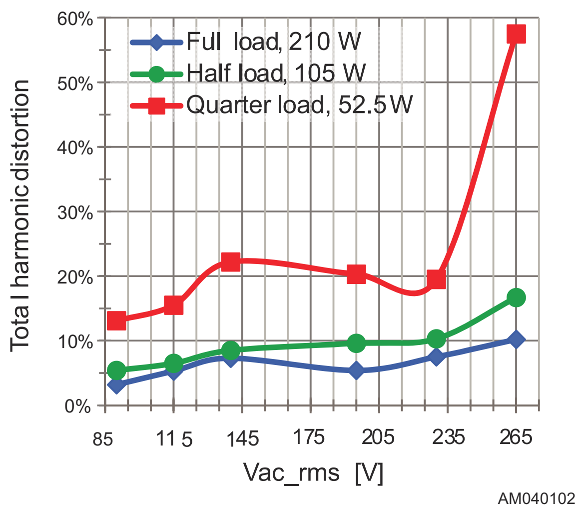
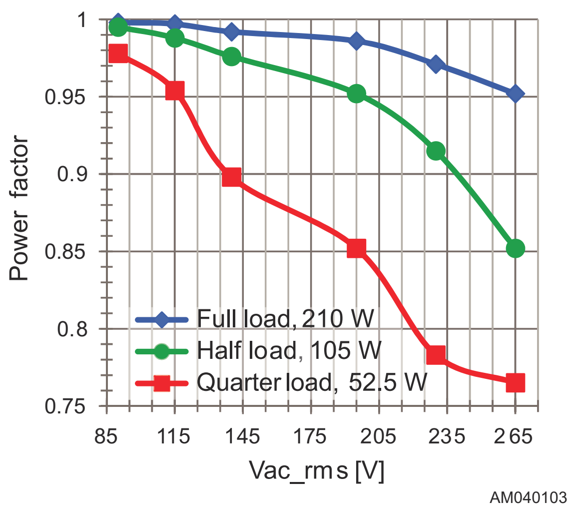


Figure 6. Power factor vs. Vac



5 Harmonic content measurement

The board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI Class-D, at the nominal input voltage mains. Results are reported in *Figure 7* and *Figure 8*.

Figure 7. Compliance to EN61000-3-2 Class-D

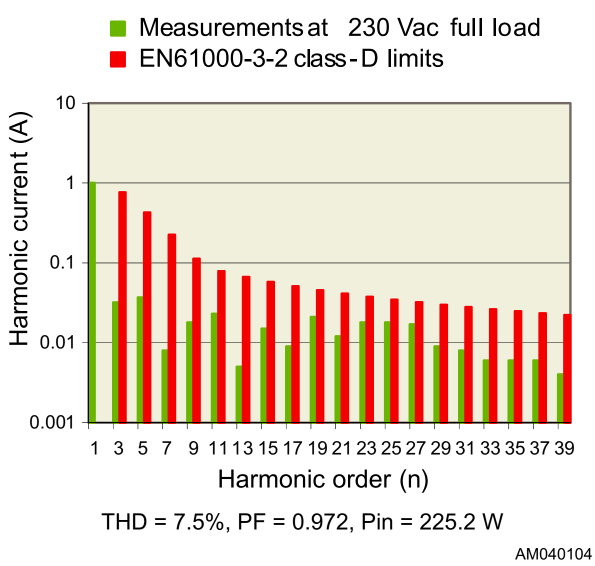
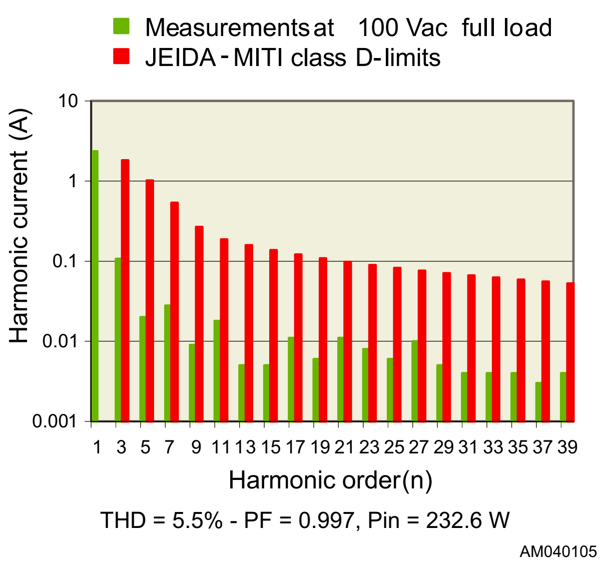


Figure 8. Compliance to JEITA-MITI Class-D



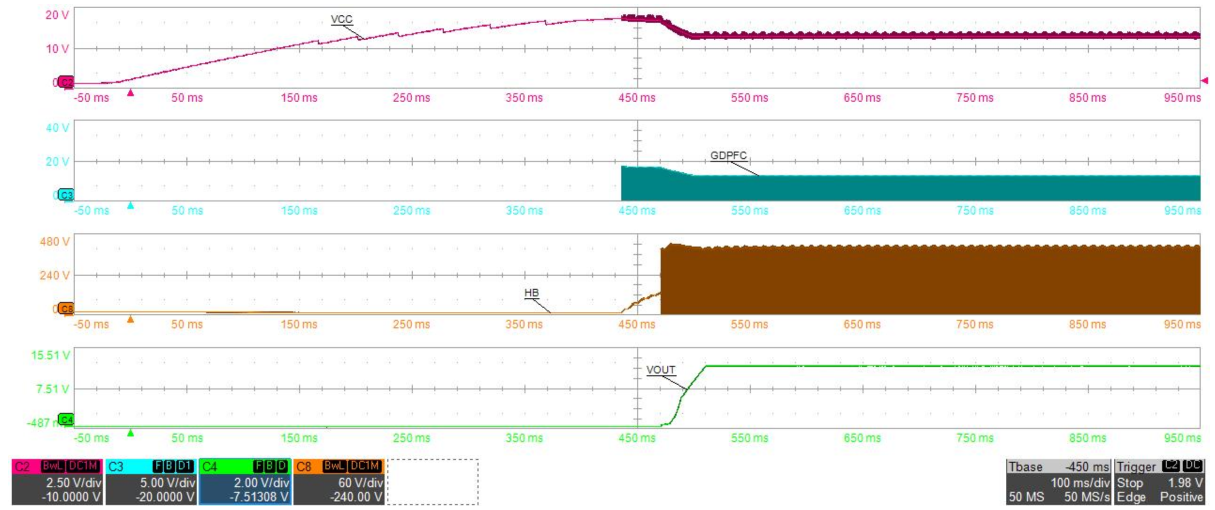
6 Functional check

6.1 PCB turn-on and LLC start-up

As the mains voltage, in the operating range, is applied to the EVLCMB1-AIO210W, the high voltage start-up (HVSU) generator of the STCMB1 brings the VCC pin to the VCCon threshold at which the PFC starts working. The output voltage of the PFC (VPFC on C9) increases up to the enabling voltage of the LLC that is about 380 V (corresponding to the FB_E threshold on the FB pin). As the LLC starts switching, VOUT begins to increase and the self-supply circuitry based on the auxiliary winding of the LLC transformer takes over the HVSU generator.

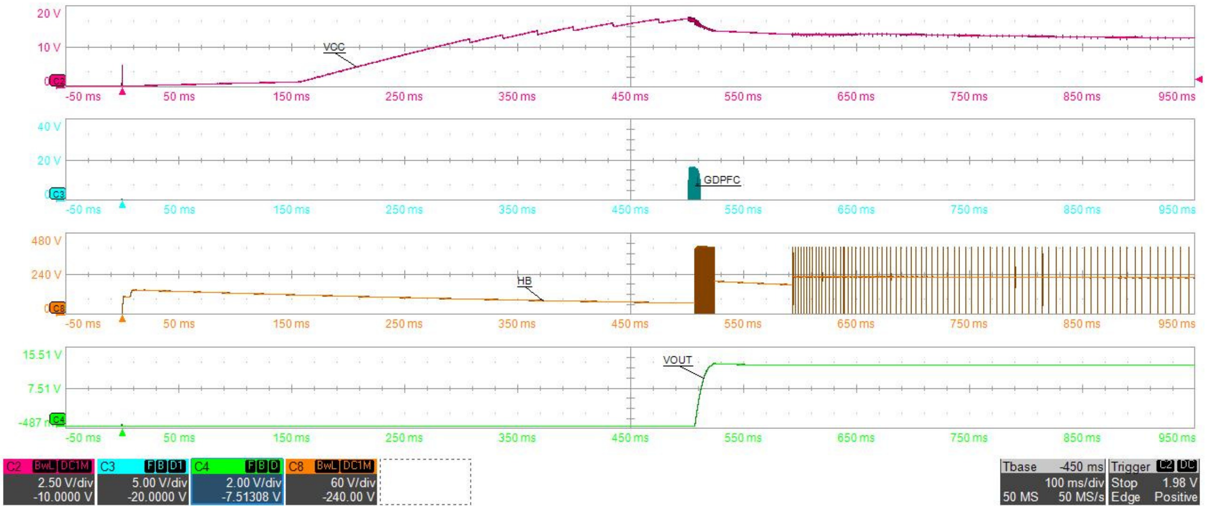
Figure 9 and *Figure 10* show PFC and LLC driving signals with VOUT and VCC, when the EVLCMB1-AIO210W is turned on at the limits of the input voltage range and with the full / open load.

Figure 9. Turn-on at 90 Vac - full load



CH2: VCC, CH3: GDPFC, CH4: VOUT, CH8: HB - Vout rise time ~ 20 ms

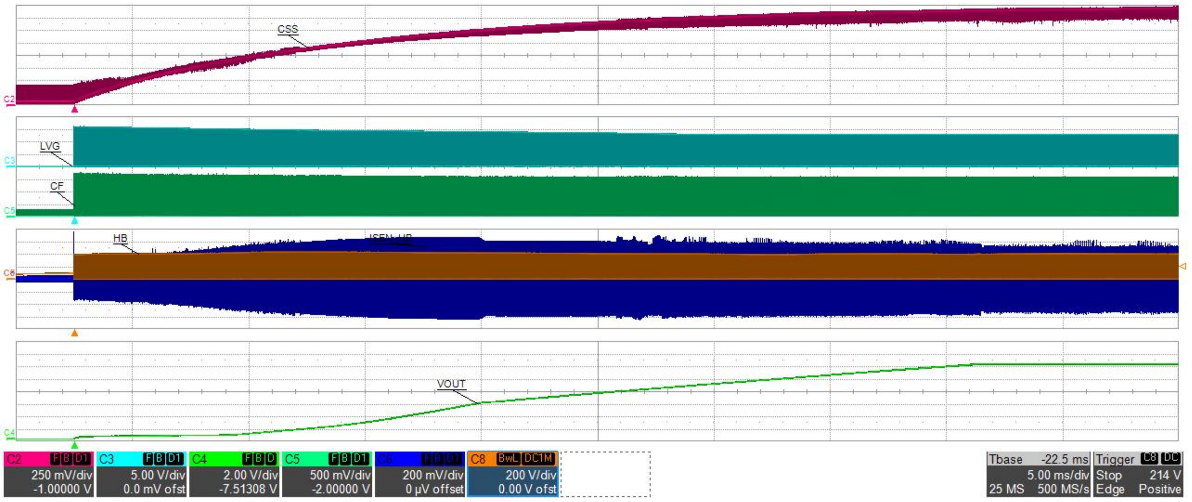
Figure 10. Turn-on at 265 Vac - open load



CH2: VCC, CH3: GDPFC, CH4: VOUT, CH8: HB - Vout rise time ~ 10 ms

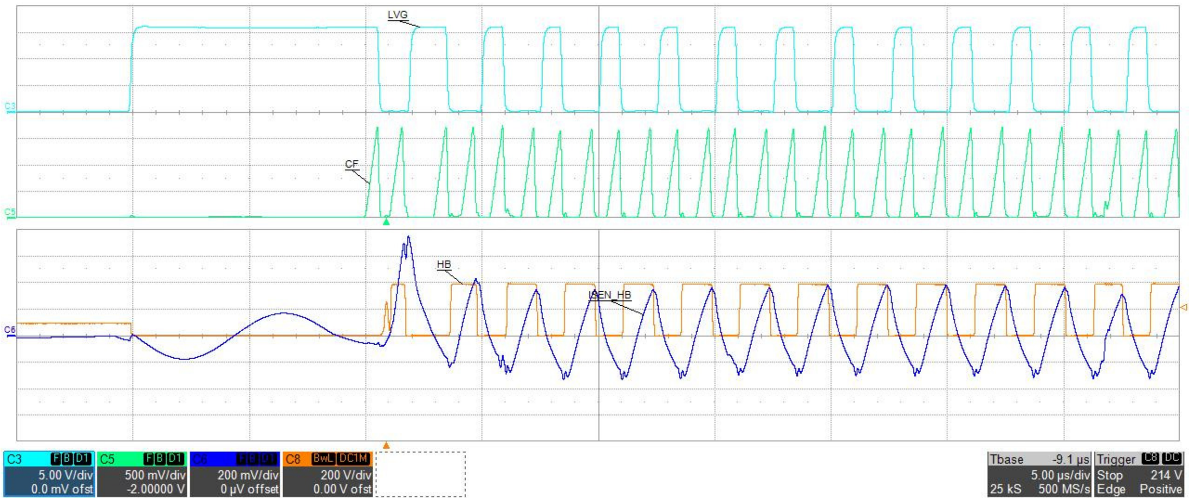
It is worth to highlight an important peculiarity of the resonant converter start-up that comes from the time shift control methodology implemented in the LLC section of the STCMB1 and that makes the implementation of a proprietary hard switching prevention function straightforward. In other words, on one side, a transition of the half bridge is allowed only when the resonant tank current has properly reversed; on the other side, in the time shift control, being the oscillator ramps synchronous with the zero crossings of the resonant tank current, a ramp in a half cycle starts only after the resonant tank current has reversed in that half cycle. So, the proprietary hard switching prevention method is naturally integrated in the time shift control. As a result, the duty cycle of the initial cycles is less than 50% until the DC voltage across the resonant capacitor reaches VPFC/2 which eliminates the typical initial V * s start-up imbalance and ensures soft switching. Furthermore, the traditional soft-start mechanism based on the frequency shift through the charge of a capacitor connected to the CSS pin, is implemented as well. A typical LLC start-up as driven by the STCMB1 is shown in *Figure 11* and *Figure 12*.

Figure 11. LLC startup at 115 Vac - full load



CH2: CSS, CH3: LVG, CH5: CF, CH6: ISEN_HB, CH4: VOUT, CH8: HB

Figure 12. Detail of first LLC cycles



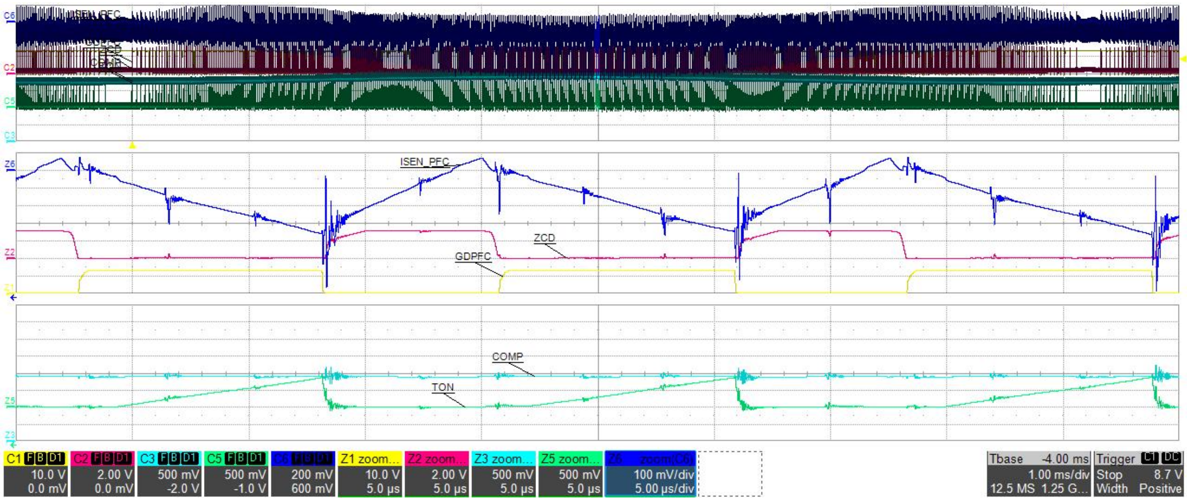
CH3: LVG, CH5: CF, CH6: ISEN_HB, CH8: HB

6.2 Steady state operation at heavy loads (PFC and LLC in continuous switching)

At heavy loads, both stages of the converter work in continuous switching to deliver the required power from the mains to the load. Some waveforms relevant to the steady state operation of the EVLCMB1-AIO210W in continuous switching are shown from *Figure 13* to *Figure 15*.

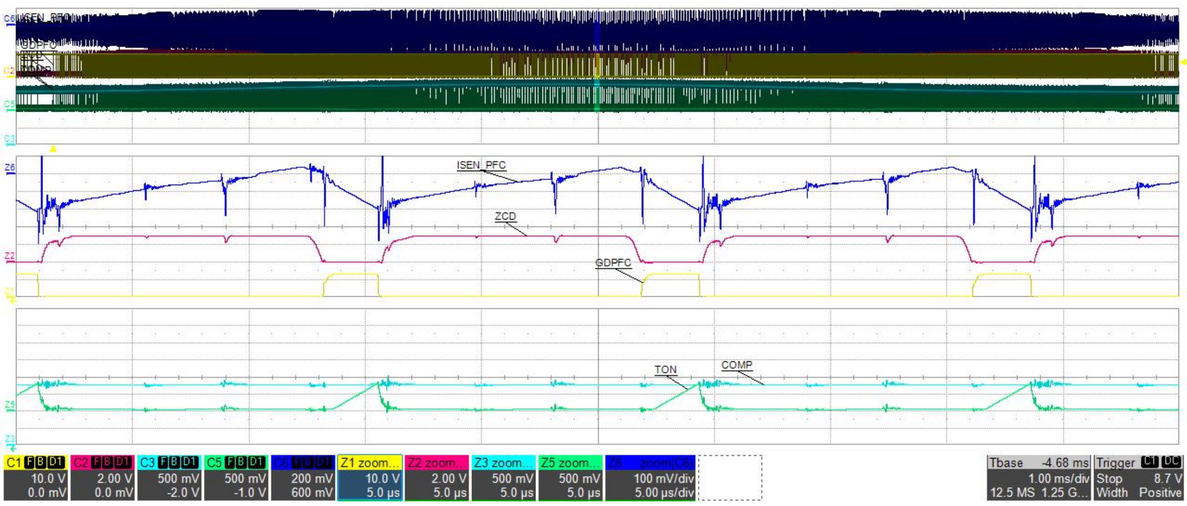
For the PFC stage, note that the whole input current is sensed through the resistor (R2) placed on the return path to the negative pin of the bridge rectifier and that the comparison between TON ramps and the COMP signal is exactly at COMP-1V. The charge current ITON is used to implement a discrete voltage feed forward compensation: in the high mains range is about four times than in the low mains range.

Figure 13. PFC at 115 Vac - full load



CH1: GDPFC, CH2: ZCD, CH3: COMP, CH5: TON, CH6: ISEN_PFC

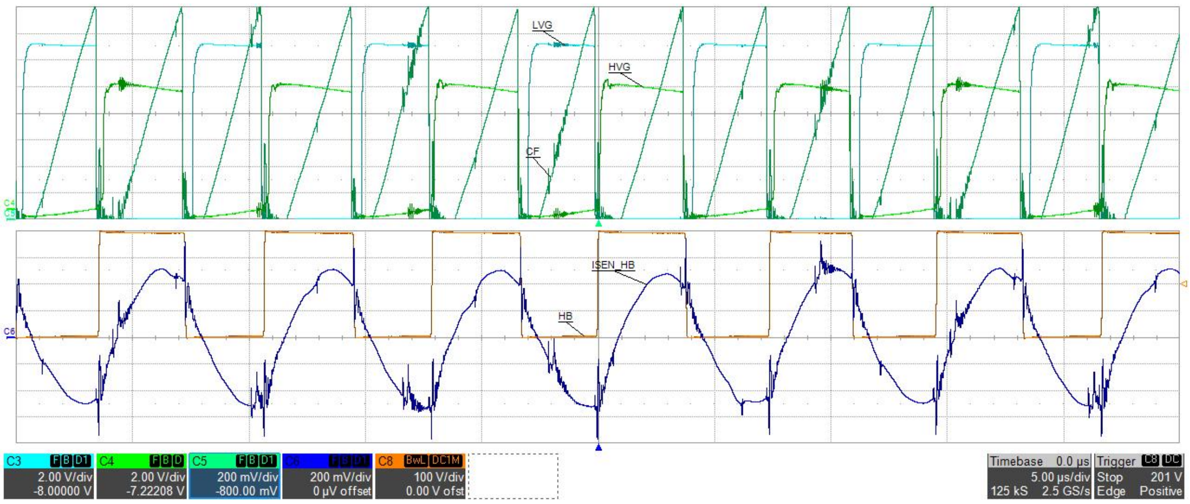
Figure 14. PFC at 230 Vac - full load



CH1: GDPFC, CH2: ZCD, CH3: COMP, CH5: TON, CH6: ISEN_PFC

For the LLC stage, at the full load, the oscillator and driving signals and the half bridge node are shown with the resonant tank current as the voltage at the ISEN_HB pin.

Figure 15. LLC signals at full load



CH3: LVG, CH4: HVG, CH5: CF, CH6: ISEN_HB, CH8: HB

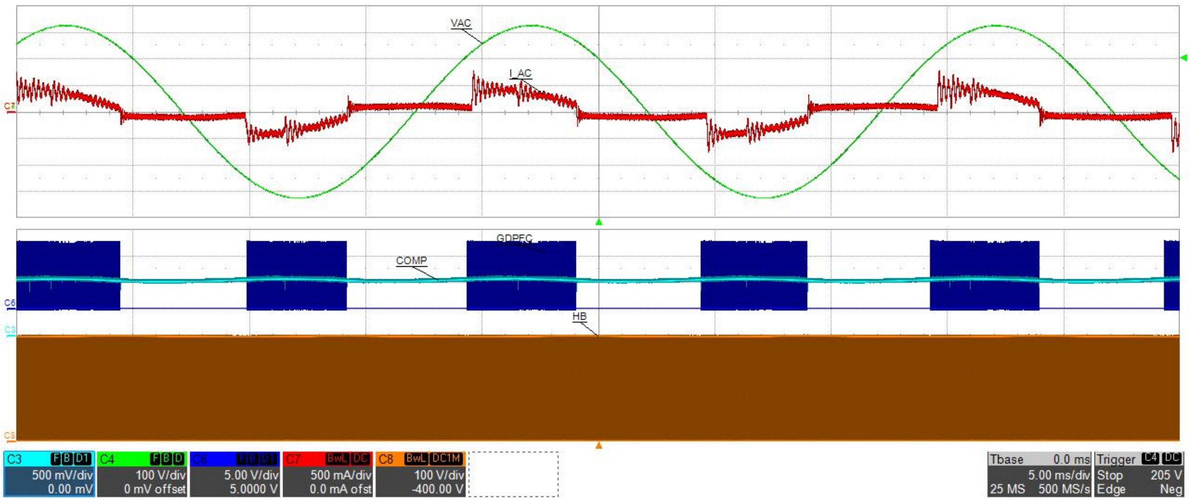
6.3 Steady state operation at moderate loads (PFC in burst mode, LLC in continuous switching)

When working at the moderate output loads and at the high mains voltage, to prevent an unwanted rising of the PFC output voltage and the consequent activation off the PFC OVP, especially during the operation at the higher mains range, the PFC stage can work in its own burst mode, while the LLC stage is still working in continuous switching. The PFC gate driver is stopped as the COMP pin voltage falls across 1 V, while the LLC may proceed in its own operation in continuous switching. PFC switching restarts as COMP rises across 1 V; a small hysteresis (20 mV) is provided to avoid bouncing.

This operating mode (PFC in burst mode and LLC in continuous switching) can take place until the output load level is higher than the LLC burst mode set point (programmed by the RFmax resistor) or in case the burst mode by the LLC is inhibited by connecting the STBY pin to the RFmin pin. If the load is decreased below the LLC burst mode set point the LLC will begin working in the burst mode too and it will take over the burst mode of both converters that will work synchronized, as described in *Section 6.4*.

Some waveforms relevant to the steady state operation of the EVLCMB1-AIO210W in this condition are shown in *Figure 16*.

Figure 16. PFC in burst mode, 230 Vac - 3 A



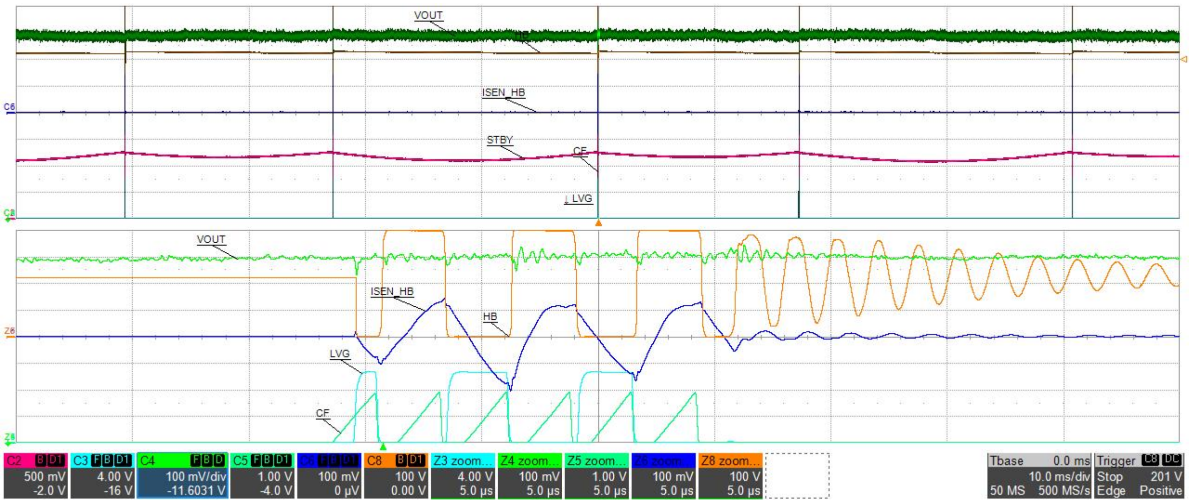
CH3: COMP, CH4: VAC, CH6: GDPFC, CH7: I_AC, CH8: HB

6.4 Steady state operation at light loads (system level burst mode operation)

At light loads, the LLC stage works in the burst mode and it is the master on the PFC stage: when STBY falls across 1.25 V because of the light load, LLC switching is stopped as soon as the HVG pulse is completed; then, the control loop, through the error amplifier and the optocoupler, makes STBY increasing; LLC switching is restarted as STBY rises across 1.25 V plus its hysteresis (40 mV).

The detailed waveforms of the EVLCMB1-AIO210W at light loads are shown in *Figure 17*. During the burst mode operation, the VOUT variation is less than 40 mV.

Figure 17. Open load (230 Vac)



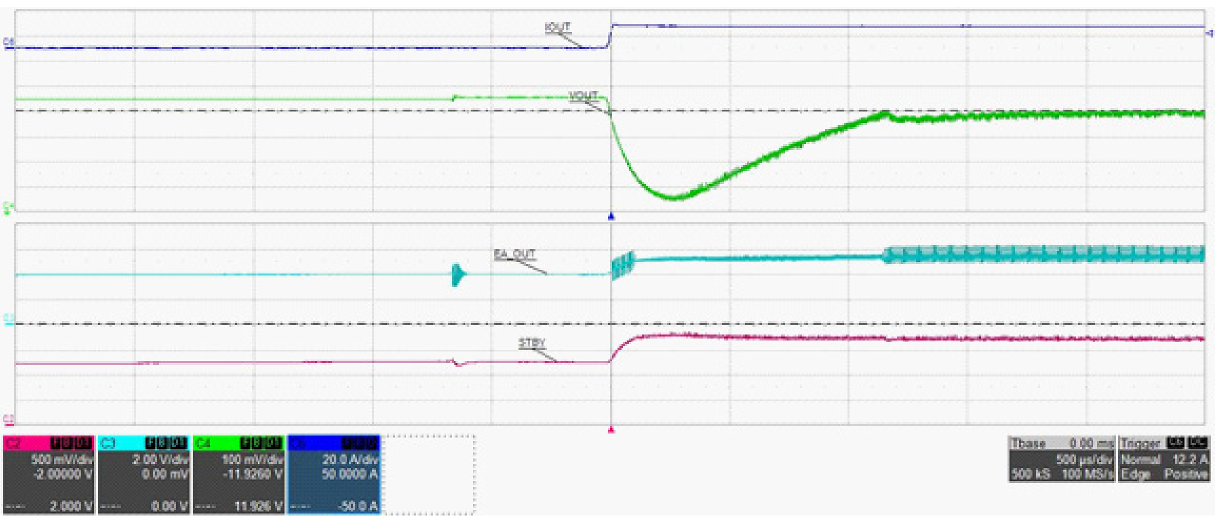
CH2: STBY, CH3: LVG, CH4: VOUT, CH5: CF, CH6: ISEN_HB, CH8: HB

CH2 is not shown in the zoom, CH4 is 100 mV/div., -11.6 V offset.

6.5 Dynamic load response

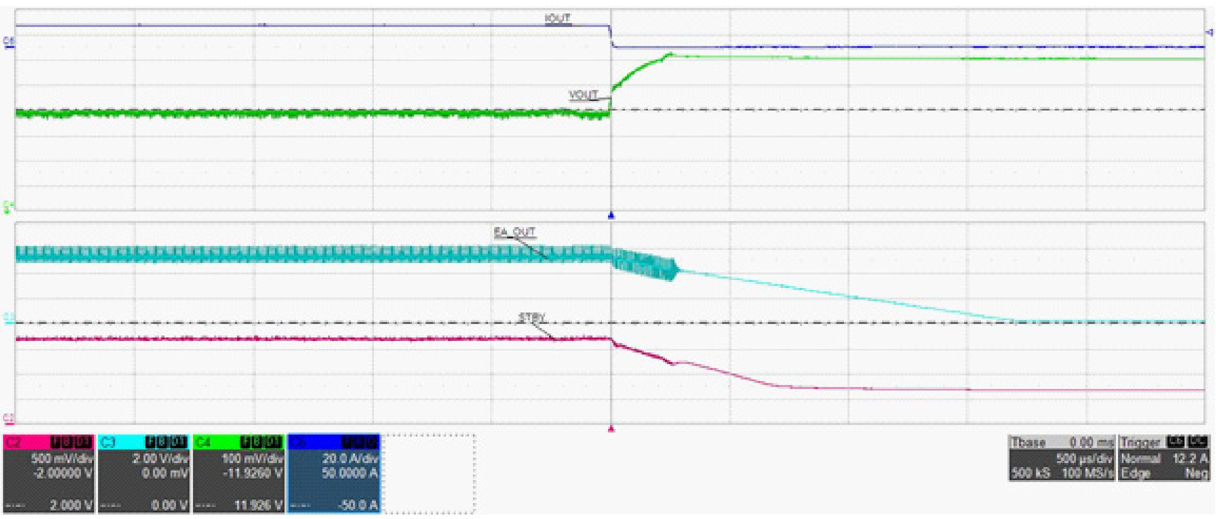
The EVLCMB1-AIO210W has been exposed to dynamic loads to measure the output voltage variation. In detail, when the load is changed every 400 ms, at 2.5 A / µs, from full to open and vice versa, the output voltage variation is about +200 mV / -400 mV with respect to the output voltage value at the full load.

Figure 18. Detail - open load to full load, 400 msec / 400 msec, 2.5 A/µs



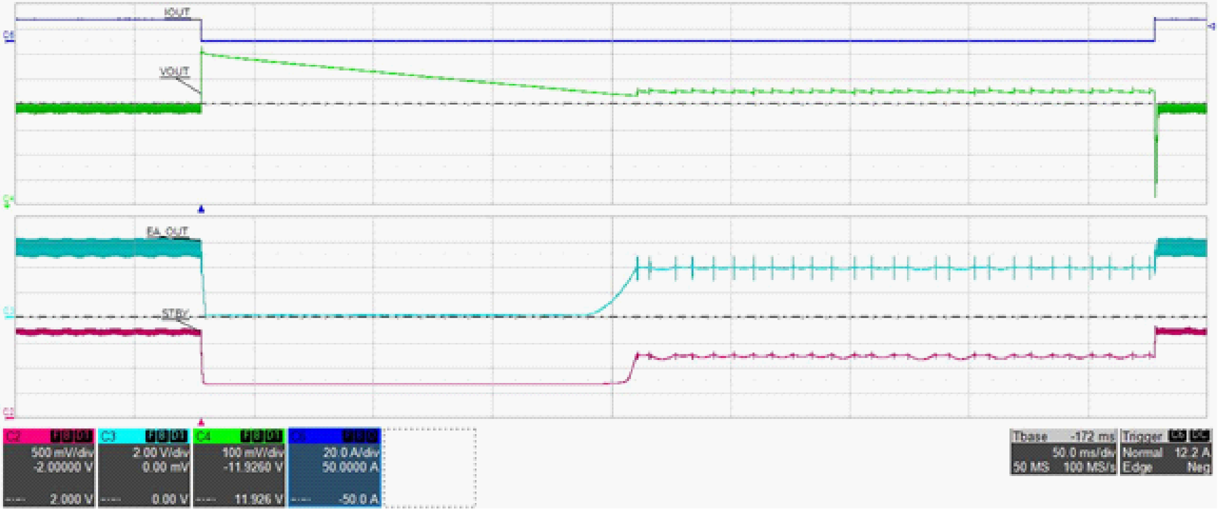
CH2: STBY, CH3: ERROR AMPLIFIER OUTPUT (U3, pin 5), CH4: VOUT, CH6: I_OUT
CH4 is 100 mV/div., -11.9 V offset (horizontal cursor is at VOUT level during full load).

Figure 19. Detail - full load to open load, 400 msec / 400 msec, 2.5 A/µs



CH2: STBY, CH3: ERROR AMPLIFIER OUTPUT (U3, pin 5), CH4: VOUT, CH6: I_OUT
CH4 is 100 mV/div., -11.9 V offset (horizontal cursor is at VOUT level during full load).

Figure 20. Dynamic load applied - full load / open load, 400 msec / 400 msec, 2.5 A/µs



CH2: STBY, CH3: ERROR AMPLIFIER OUTPUT (U3, pin 5), CH4: VOUT, CH6: I_OUT

CH4 is 100 mV/div., -11.8 V offset (horizontal cursor is at VOUT level during full load).

Figure 6.6 and *Figure 19*, that are the details at load transitions, highlight the good dynamic characteristic of the control loop: apart from the limited voltage variation, the response is clean and monotonic, that are signs of the appropriate margin phase of the regulation loop.

Note that the full load to open load transition drives the feedback system to saturate low because of the overshoot of the output voltage. Some precautions (D19, R53, R74) have been implemented to prevent the full saturation at both secondary and primary side, but they are not enough to guarantee the reported output voltage drop (400 mV) in case the open load period is less than about 300 ms, that is the time the converter takes to recover from saturation.

Applicative improvement

The way to improve the converter behavior in these cases is to limit the error amplifier output to a value that allows the burst mode operation of the converter. A simple solution is to divide the upper resistor of the output divider (R56) to have the desired limit voltage for the error amplifier output. The intermediate node of the upper branch of the output divider can be then connected to the error amplifier output by means of a signal diode (1N4148 or Schottky).

With respect to the converter schematic (*Figure 2 on page 9*), the error amplifier output is at about 6 V at the burst mode threshold so its excursion can be limited to about 5 V. So, R56 = 120 kΩ can be divided in 91 kΩ and 30 kΩ, keeping the larger toward the output voltage and the smaller toward the reference node. In this way, the output voltage drop at the open to full load transition is limited to about 600 mV, for open load periods down to about 1 ms.

6.6 Turn-off by mains disconnection: X-cap function and LLC behavior

When the mains are disconnected, two requirements have to be satisfied: one is safety related, while the other is application related.

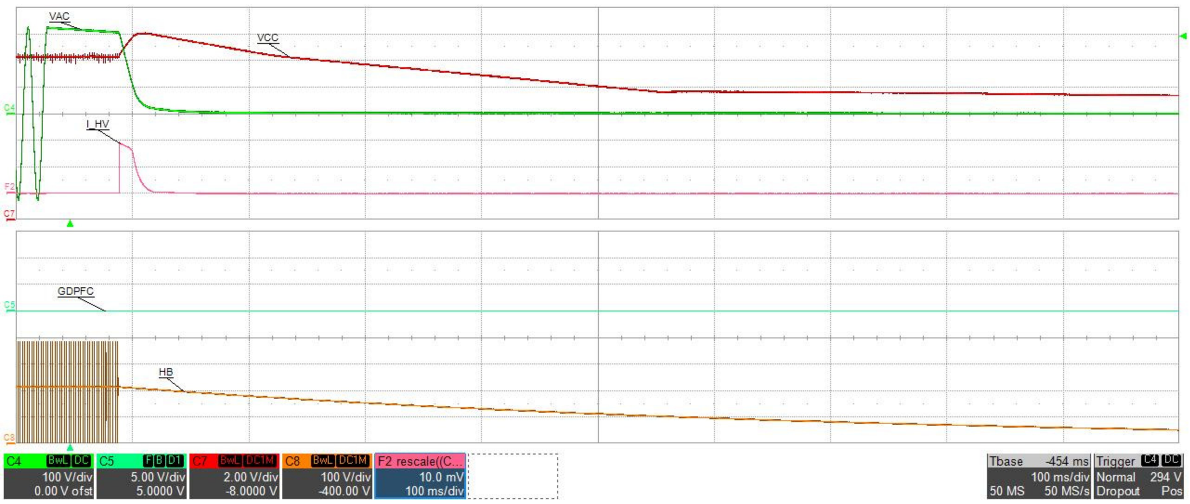
6.6.1 X-cap function

As the converter is turned off by mains disconnection, the XCAP function plays the essential role of bringing the mains input of the converter at a safe voltage level for the user, avoiding the use of the safety discharging resistors in parallel to the Cx filter capacitors that would dissipate a significant power during light load operation, thus affecting the efficiency.

Waveforms in the following image show the operation of the XCAP function integrated in STCMB1. Tests have been done in the whole input voltage range and from open load to full load. However, the reported example is at light load and high mains because it is definitely the worst condition. In fact, at heavy loads, the XCAP discharge would be helped by the operation of the converter while at low mains, the Cx residual voltage to discharge would be lower.

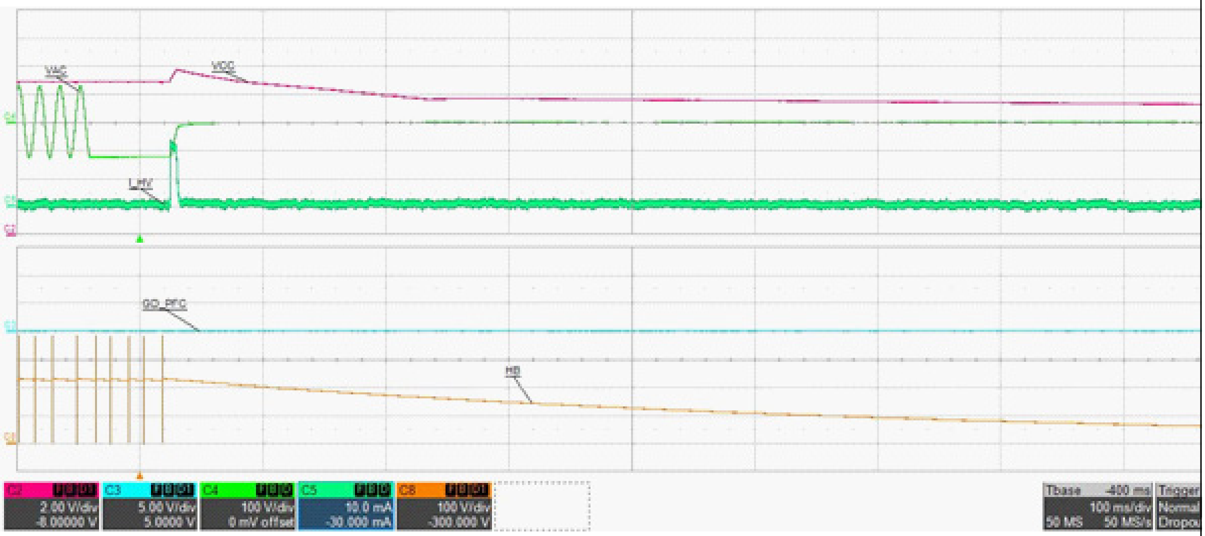
In all the cases, at mains disconnection the Cx are discharged within the safety limit in few hundred milliseconds. Note that the function does not require any external dedicated component and, above all, it does not burn any power during the converter operation. Finally, note that the removed charge is delivered onto VCC pin but an internal clamp is activated to limit the pin voltage below its AMR.

Figure 21. Vac removed at 265 Vac / no load



CH2: VAC, CH3: GDPFC, CH4: VCC, CH5: I_HV, CH8: HB

Figure 22. Vac removed at 90 Vac / no load

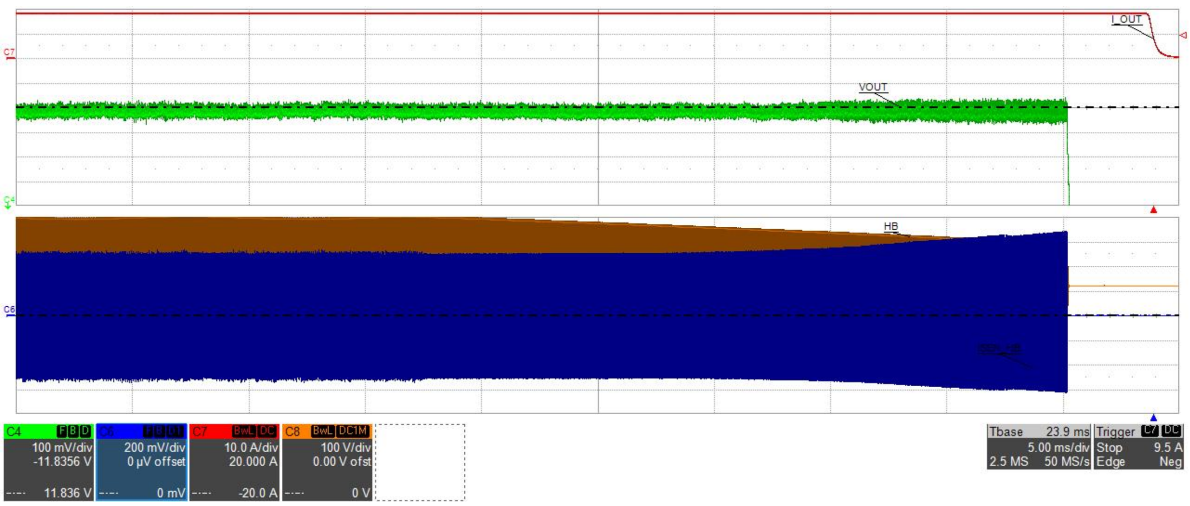


CH2: VAC, CH3: GDPFC, CH4: VCC, CH5: I_HV, CH8: HB

6.6.2 LLC behavior

The general request for a converter is that the output voltage is maintained constant for few tens of ms after the mains disconnection; obviously, the worst case is the mains disconnection during the full load operation. Furthermore, the behavior of the tank current during such turn-off is a good indicator of the stability of the control loop. The output voltage and current tank of the EVLCMB1-AIO210W at the mains disconnection during the full load operation are shown in *Figure 23* and *Figure 24*.

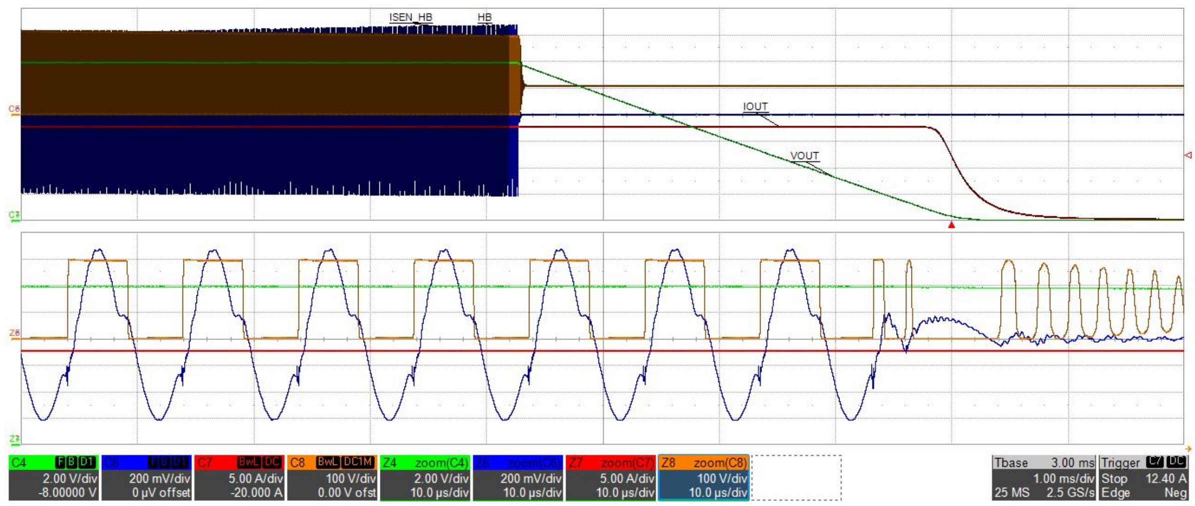
Figure 23. Mains disconnection at 90 Vac / full load



CH4: VOUT, CH6: ISEN_HB, CH7: I_OUT, CH8: HB

CH4 is 100 mV/div., -11.8 V offset (horizontal cursor is at VOUT level during full load).

Figure 24. Mains disconnection at 90 Vac / full load - detail of last LLC cycles



CH4: VOUT, CH6: ISEN_HB, CH7: IOUT, CH8: HB

6.7 Turn-off/on by ACBO/BI function

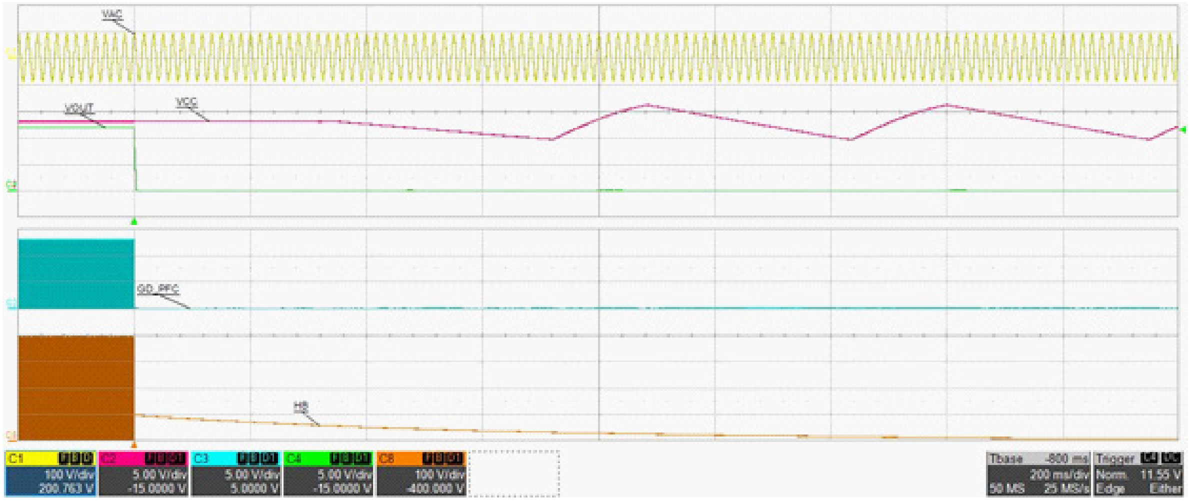
Here, the EVLCMB1-AIO210W has been turned off/on by the AC brownout/in function respectively. The test is done by slowly reducing the mains voltage from 90 Vac to the converter turn-off; then, the mains voltage has been slowly increased up to the converter turn-on.

Note that turn on by ACBI is conditioned by two events: voltage at HV pin higher than ACBI threshold for more than about 2 ms (debounce filter on ACBI) and VCC pin reaching VCCon threshold after the charge phase. In application, the way ACBI function is implemented has some effects: ACBI threshold for the final user shows a weak linear function of the line frequency and it would depend on high voltage start up current when a resistor is placed in series to HV pin; the payback is a robust ACBI function.

If the test is done at heavy loads, the ACBO action is mixed with the overcurrent protection of the PFC: its output power is consequently limited and so its output voltage is no more regulated at the nominal level. In this condition, if the PFC output voltage drops below the DCBO threshold, then it might possible to observe bouncing of the output voltage because the DCBO turns off the LLC only when the ACBO is not yet reached. Afterward, because the PFC rapidly brings its output to the enabling threshold of the LLC (DCBI) causing a restarting attempts.

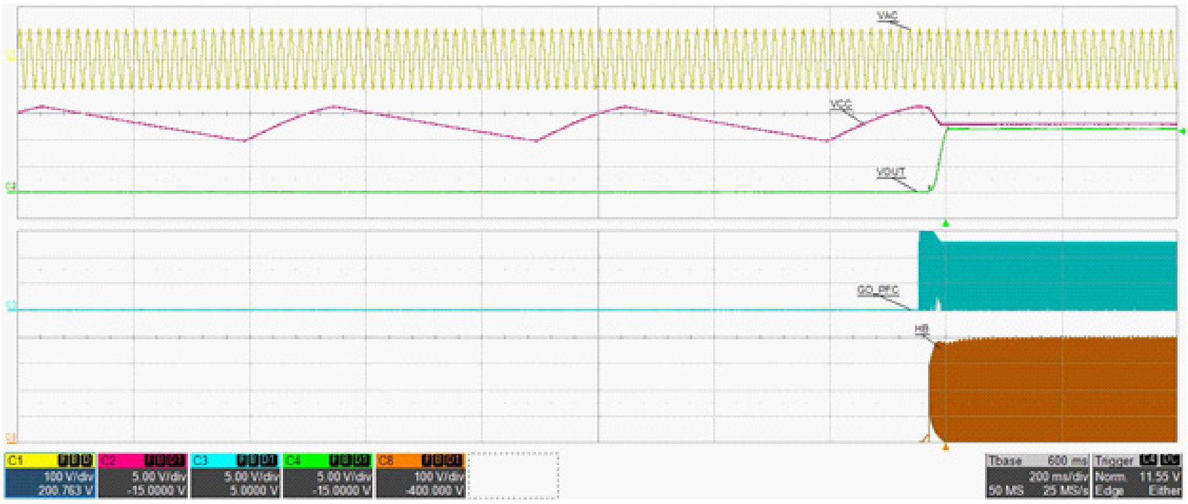
If the user wanted to avoid this behavior, then the PFC overcurrent protection limit and the boost inductor size should be designed at the minimum AC brownout voltage rather than at the AC minimum mains voltage. However, it is worth highlighting that this design criterion would result in a bigger size of the boost inductor size that should carry a larger mains current.

Figure 25. Turn-off by ACBO at 9 A - 69 Vac (mains voltage read on the AC source display)



CH1: VAC, CH2: VCC, CH3: GDPFC, CH4: VOUT, CH8: HB

Figure 26. Turn-on by ACBI at 9 A - 79 Vac (mains voltage read on the AC source display)

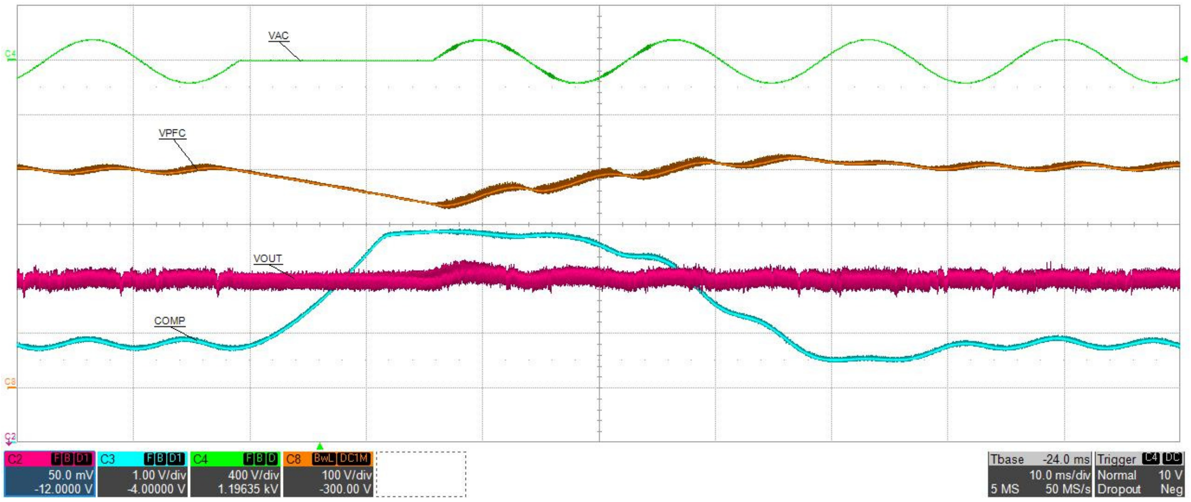


CH1: VAC, CH2: VCC, CH3: GDPFC, CH4: VOUT, CH8: HB

6.8 Mains dips at full load

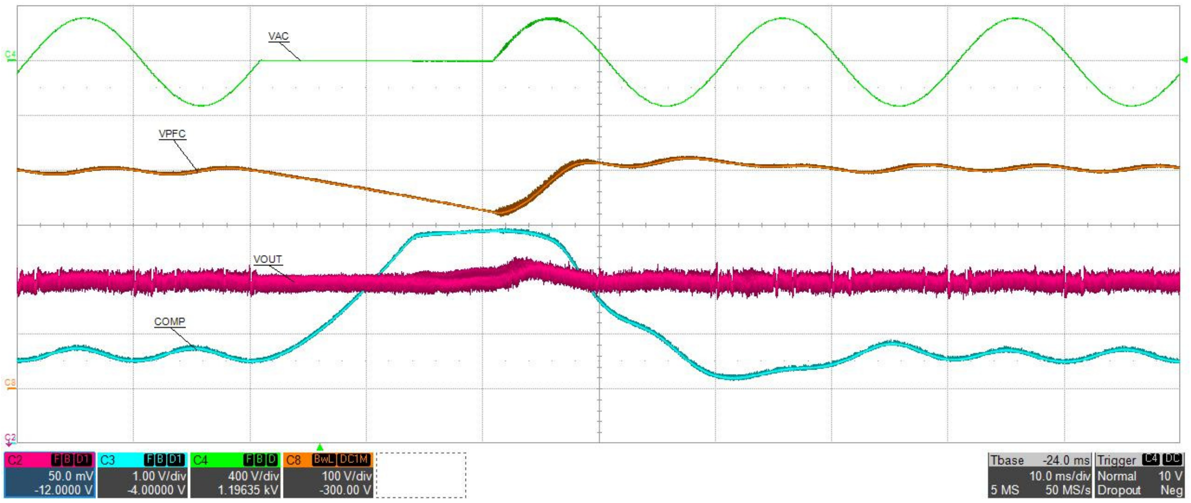
Here, the EVLCMB1-AIO210W has been checked against a 0% mains dip (single line cycle, according to IEC61000-4-11), at both nominal mains voltages while operating at the full load: the output voltage variation is within about 20 mV in both cases.

Figure 27. Single cycle, 100% mains dip at 115 Vac / 60 Hz - full load



CH2: VOUT (50 mV/div.), CH3: COMP, CH4: VAC (on input Cx), CH8: VPFC

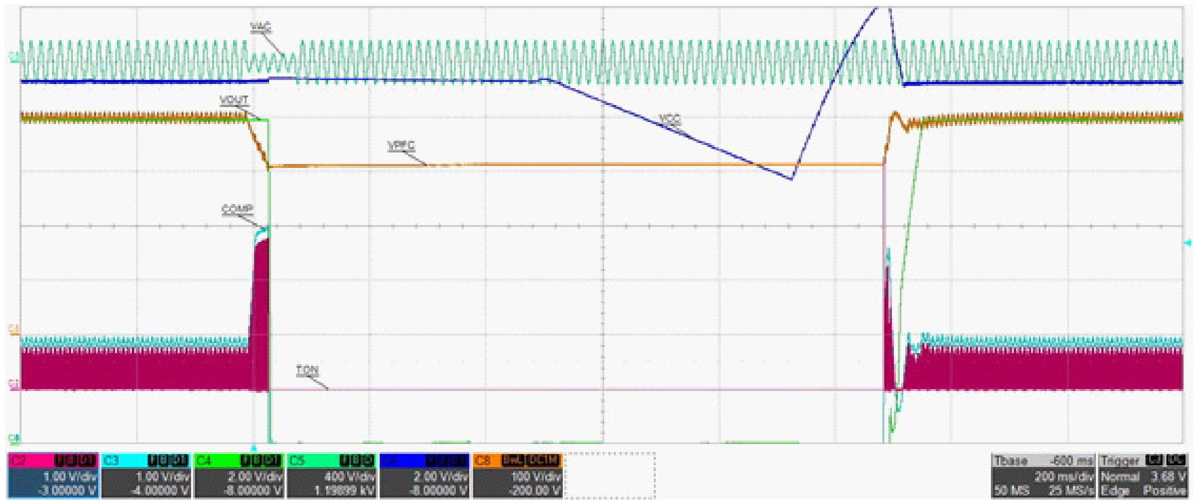
Figure 28. Single cycle, 100% mains dip at 230 Vac / 50 Hz - full load



CH2: VOUT (50 mV/div.), CH3: COMP, CH4: VAC (on input Cx), CH8: VPFC

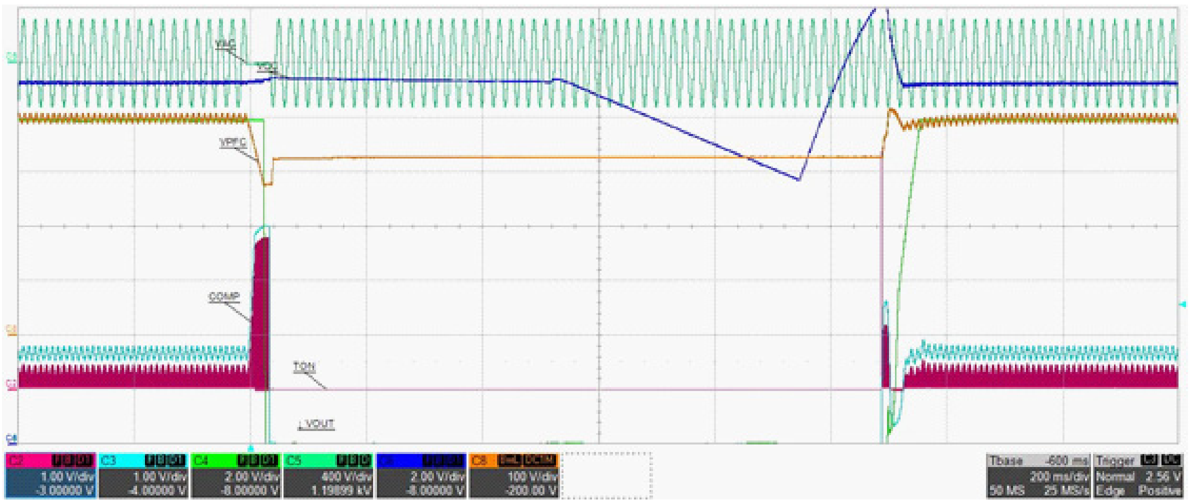
Because of the way ACBI function is implemented, if the line drop is below ACBO threshold and lasts for at least 2 line cycles and less than the VCC discharge time, then a delay is observed between the end of the line drop (mains voltage back to the nominal value) and the restart of the adapter. It is due to the fact that turn on by ACBI can only occur after a VCC charge phase, when VCC pin reaches VCCon (and ACBI threshold at HV pin is valid for more than about 2 ms). Examples of the described behaviour are shown in the following figures.

Figure 29. Five cycles, 46Vac mains dip at 115Vac / 60Hz - full load



CH2: TON, CH3: COMP, CH4: VOUT, CH5: VAC, CH6: VCC, CH8: VPFC

Figure 30. Two cycles, 0Vac mains dip at 230Vac / 50Hz - full load



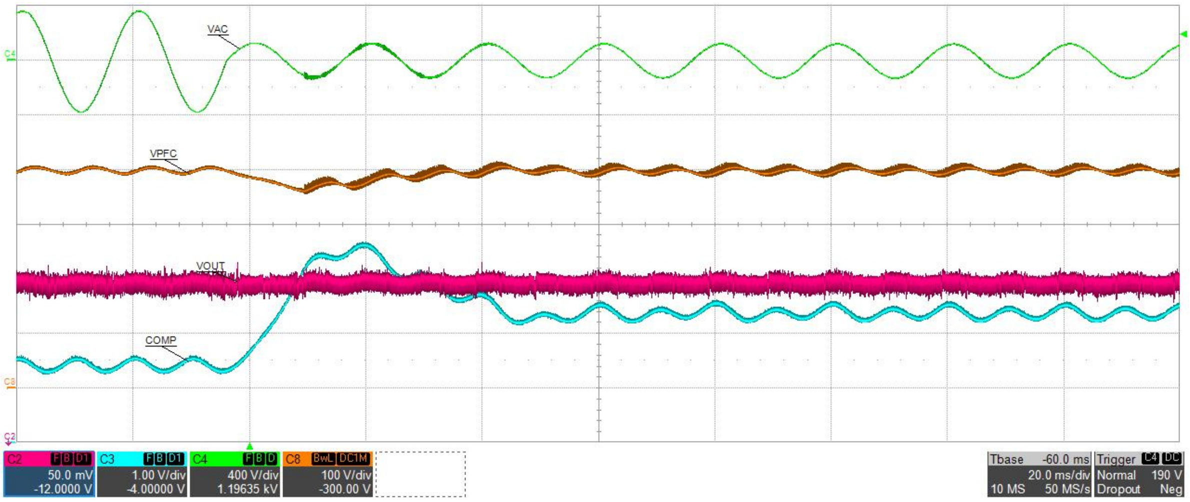
CH2: TON, CH3: COMP, CH4: VOUT, CH5: VAC, CH6: VCC, CH8: VPFC

6.9 Line transitions at full load

Here, the EVLCMB1-AIO210W has been exposed to a full range line transition in both directions, i.e. from 265 Vac to 90 Vac and vice versa, while operating at the full load: in both cases, the output voltage variation is definitely negligible.

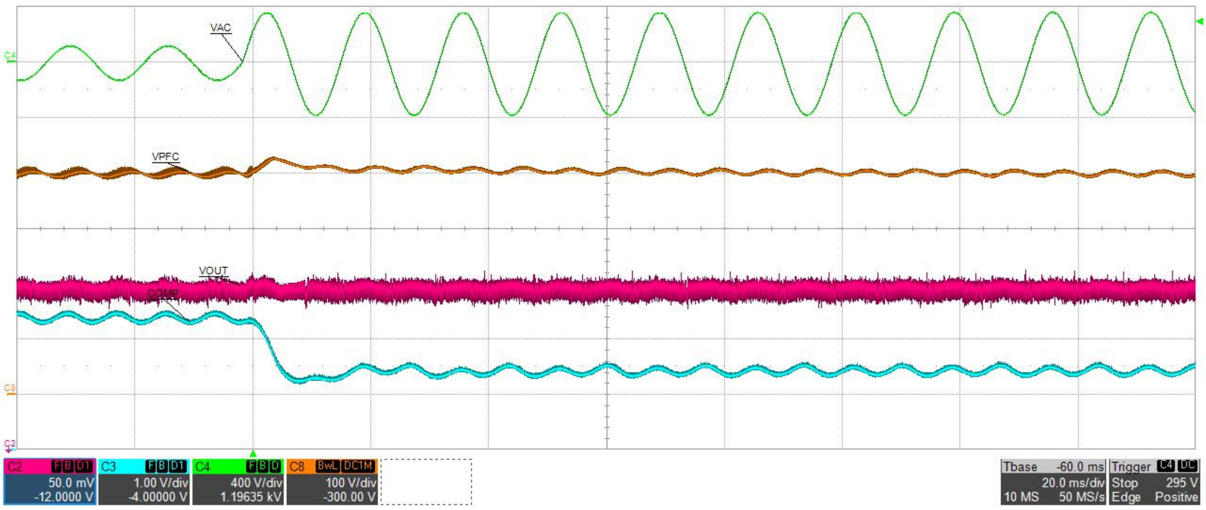
The transient of the COMP pin during the high to low mains transition is subject to the time required by the peak detector to update its value and the internal logic to update the ITON value. Conversely, the peak detection and the ITON value update is practically instantaneous during the low to high mains transition.

Figure 31. Line transition: full load, 265 → 90 Vac (50 Hz)



CH2: VOUT (50 mV/div.), CH3: COMP, CH4: VAC (on input Cx), CH8: VPFC

Figure 32. Line transition: full load, 90 → 265 Vac (60 Hz)



CH2: VOUT (50 mV/div.), CH3: COMP, CH4: VAC (on input Cx), CH8: VPFC

6.10 Overcurrent management

The EVLCMB1-AIO210W device is also equipped with the CC loop that takes control when the output load is about 110% of the full load. When the CC loop takes control, as the load is further increased, the output current is kept constant while VOUT falls down. The output load at which the control changes from CV to CC is set by a resistor (R80) at the secondary side that senses the whole return current.

From the controller viewpoint, in the STCMB1, overcurrent management is based on the resonant tank current sensing on the ISEN_HB pin and, for the proper operation, the instantaneous current has to be sensed: this means that the recommended RC filter nearby the ISEN_HB pin should have time constant limited to few hundreds nanoseconds, to avoid too much delay between the sensed signal on the R78 and the signal at the ISEN_HB pin. When longer time constants are used, it is recommended to carefully verify the converter behavior close to the capacitive mode boundary and when the short-circuit is applied.

Two overcurrent thresholds can be triggered at the ISEN_HB pin: OCP1 (0.8 V) and OCP2 (1.5 V). The first level protection activates a frequency shift based mechanism and, in some cases, an internal overload protection based on digital counters. The second level protection is for the immediate stop of the converter.

6.10.1 Constant current (CC) loop

The output load at which the control changes from CV to CC is set by a pair of parallel resistors (R50/R51) at the secondary side that senses the whole return current.

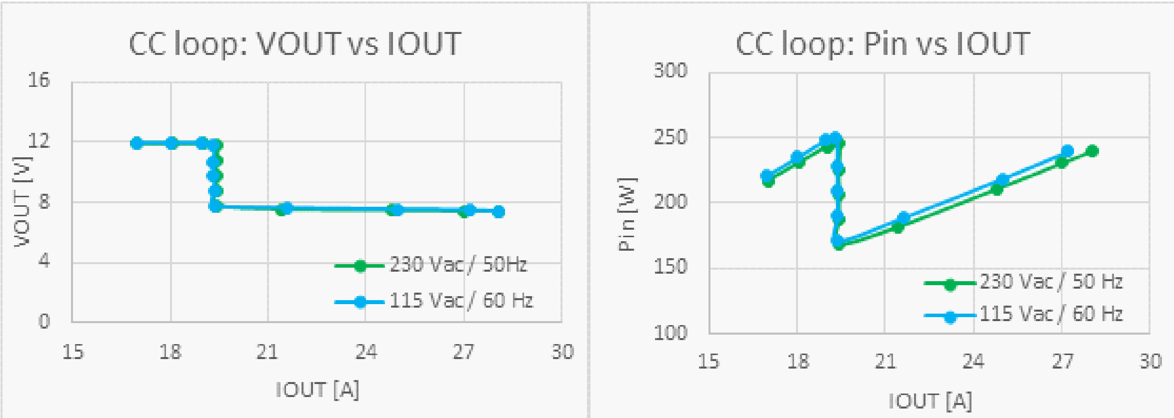
With R50 = R51 = 5mΩ, a handshake between CV and CC loops occurs at about 19.5 A. Note that, in order to properly test the CC loop, the active load has to be set in the CR mode rather than in the CC mode; this to avoid the conflict by the board CC loop and the active load constant current operation.

Once the CC loop is active, further reduction of Rout, results in VOUT decreasing while the output current is kept constant. However, when VOUT is about 7.5V, the CC loop cannot regulate anymore since the error amplifier has used up its dynamic: the output current will increase at constant, but not regulated, output voltage till operation is turn off by internal protection mechanism of STCMB1.

Also note that, during CC loop control, at low mains voltage ($\leq$ 115 Vac), the PFC can lose regulation due to the operation of current limiting (OCP of PFC). In this case, VPFC can go down to 320 V (> 280 V = DC brownout), but the overall behavior is as described above.

Figure 33 shows the typical VOUT vs. IOUT and the pin vs. IOUT diagrams when the CC loop is active.

Figure 33. EVLCMB1-AIO210W operation in constant current control loop



Active load in CR mode, Rout from about 0.70Ω to about 0.25Ω

6.10.2 First level OCP

If the signal at the ISEN_HB pin exceeds 0.8 V (OCP1 threshold), then the soft-start capacitor CSS (C3) is discharged for 5 µs and, as a consequence, the oscillator frequency quickly increases; correspondingly, the resonant peak current and therefore the signal at the ISEN_HB pin will decrease. This mechanism limits the energy transfer to the output and occurs each time the OCP1 threshold is triggered.

Under the overload or output short-circuit condition, this overcurrent protection results in a peak primary current that periodically oscillates around the maximum value allowed by the sense resistor (R78) and is effective in limiting the primary-to-secondary energy flow in case of the overload or a “soft” output short-circuit.

However, this frequency shift based mechanism cannot last indefinitely because it could jeopardize the safety of the converter. So, in order to prevent any damage, the operation during the overload, as described above, has limited duration; afterward, the converter is forced to work intermittently (hiccup mode), which brings the average output current to values such that the thermal stress is within safe limits.

Internal overload protection is described in the datasheet of the STCMB1 device . Only note that the actual duration of the allowed overload depends on the occurrence of the OCP1 events, therefore on CSS, RSS and characteristics of the resonant circuit and the short-circuit impedance. Its value is usually few tens of milliseconds.

6.10.3 Second level OCP

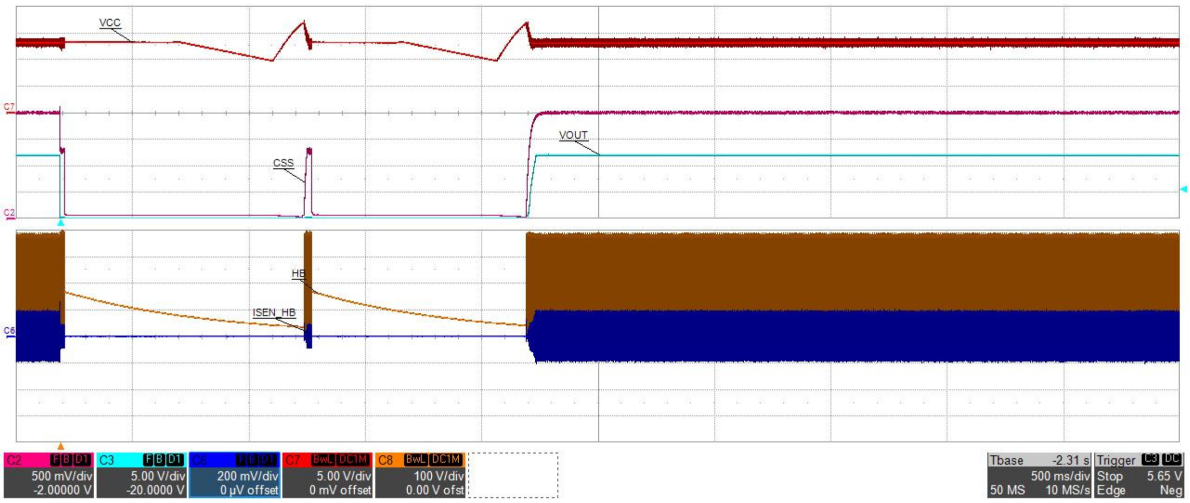
In case of a particularly severe dead short-circuit the resonant tank current can rise very quickly to very high levels. In such cases it would be dangerous for the converters to wait the timing set up by the procedure described above, so the STCMB1 provides second level overcurrent protection.

If the signal at the ISEN_HB pin exceeds 1.5 V (OCP2 threshold), then the converter is immediately stopped, right after the ongoing half bridge cycle is completed, and CSS is completely discharged. Then, the converter is forced to work intermittently (hiccup mode), following the dynamic of VCC driven by the HVSU generator.

In order to avoid that the second level overcurrent protection is triggered during the start-up, because of any initial transient or spike, the protection is inhibited until the voltage on CSS is higher than 0.3 V.

In general, the behavior of the converter when a short-circuit is applied does depend on the impedance of the short-circuit itself, but also on the reaction of the current loop control and on the dynamic of the voltage on the auxiliary winding of the LLC transformer that could trigger the rough feedback failure protection implemented by sensing such voltage. In general, a short-circuit kept at the output of the EVLCMB1-AIO210W makes the converter to work in the hiccup mode; however, in case of a severe hard short-circuit , the converter can be turned off in the latch. In this case, it is necessary to disconnect and reconnect the mains to restart the converter. *Figure 34* shows an example of the short-circuit applied and removed to the output of the EVLCMB1-AIO210W.

Figure 34. Hard short-circuit applied and removed (by a panel switch soldered at output)

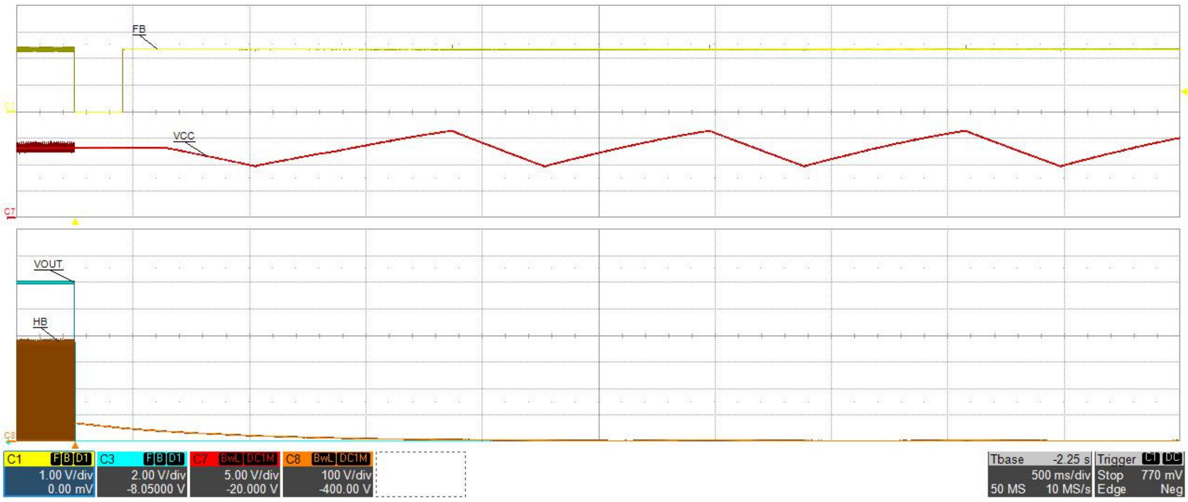


CH2: CSS, CH3: VOUT, CH6: ISEN_HB, CH7: VCC, CH8: HB

6.11 Feedback failure disconnection (latch by FB pin)

Here, the EVLCMB1-AIO210W has been shut down in the latch by opening the PFC feedback divider, as pulling down to ground the FB pin: the converter immediately stops and the latch is maintained by the VCC cycling between VCCoff and VCCon, driven by the HVSU generator. The latch is removed by the disconnection of the mains voltage (or when the mains voltage is pulled below the high voltage start-up threshold because VCC is no longer sustained in this case).

Figure 35. Latch by FB at 90 Vac / full load

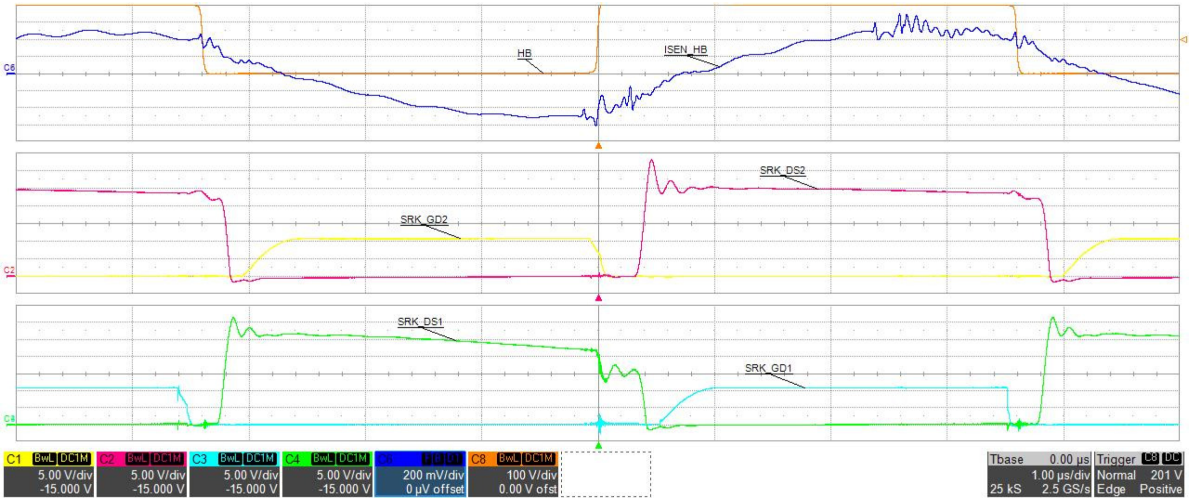


6.12 Synchronous rectification

The synchronous rectification is implemented by means of the SRK2001 whose turn-on logic, with adaptive masking time, and adaptive turn-off logic, allow to maximize the conduction time of the synchronous rectifier MOSFET pair, eliminating the need of the compensation circuit for the parasitic inductance. Furthermore, it integrates a proprietary IP that detects the burst mode operation of the LLC stage during light load condition and stops the gate drivers, reducing also its quiescent consumption. This improves the light load efficiency, where the power losses on the rectification body diodes become lower than the power losses in the synchronous rectifier MOSFET pair and those related to their driving. The internal logic is also obviously able to detect a load increase and to restart the normal operation.

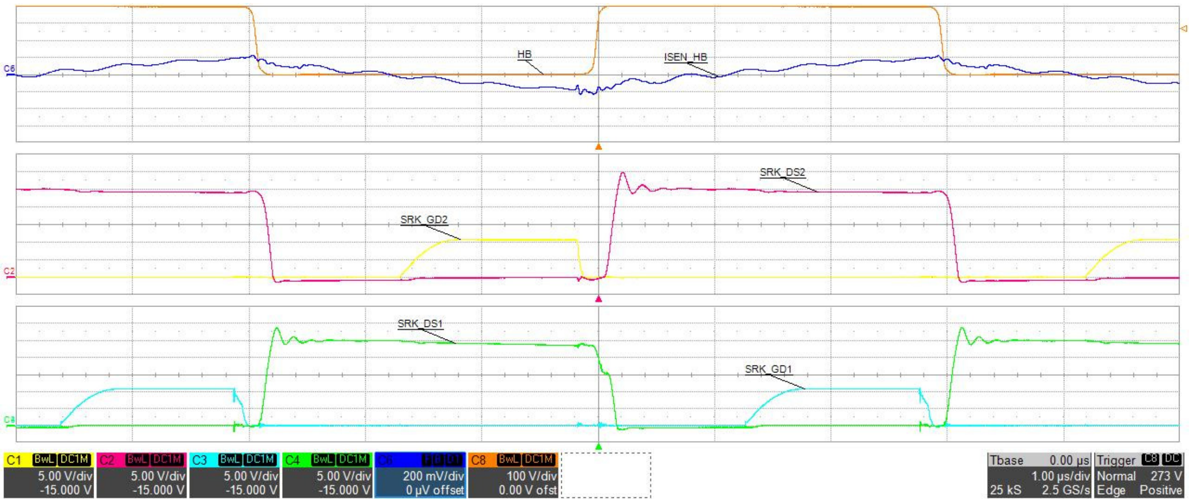
Here, typical waveforms related to the synchronous rectification are shown at the full load and at right before the burst mode operation of the converter. As the load is reduced, the conduction angle of the synchronous rectifier is reduced as well: at the limit, during light load operations, the conduction is via the body diode. An RC snubber, designed to dissipate around 300 mW, has been inserted to smooth the ringing of drain- source voltage, while a Transil™ protection device has been added to protect the synchronous rectifier MOSFET pair.

Figure 36. Full load (210 W) - synchronous rectification signals



SRK2001: CH1: GD2, CH2: DS2, CH3: GD1, CH4: DS1; HB LLC: CH6: ISEN_HB, CH8: HB

Figure 37. 20% load (42 W) - synchronous rectification signals



SRK2001: CH1: GD2, CH2: DS2, CH3: GD1, CH4: DS1; HB LLC: CH6: ISEN_HB, CH8: HB

7 Control loop response

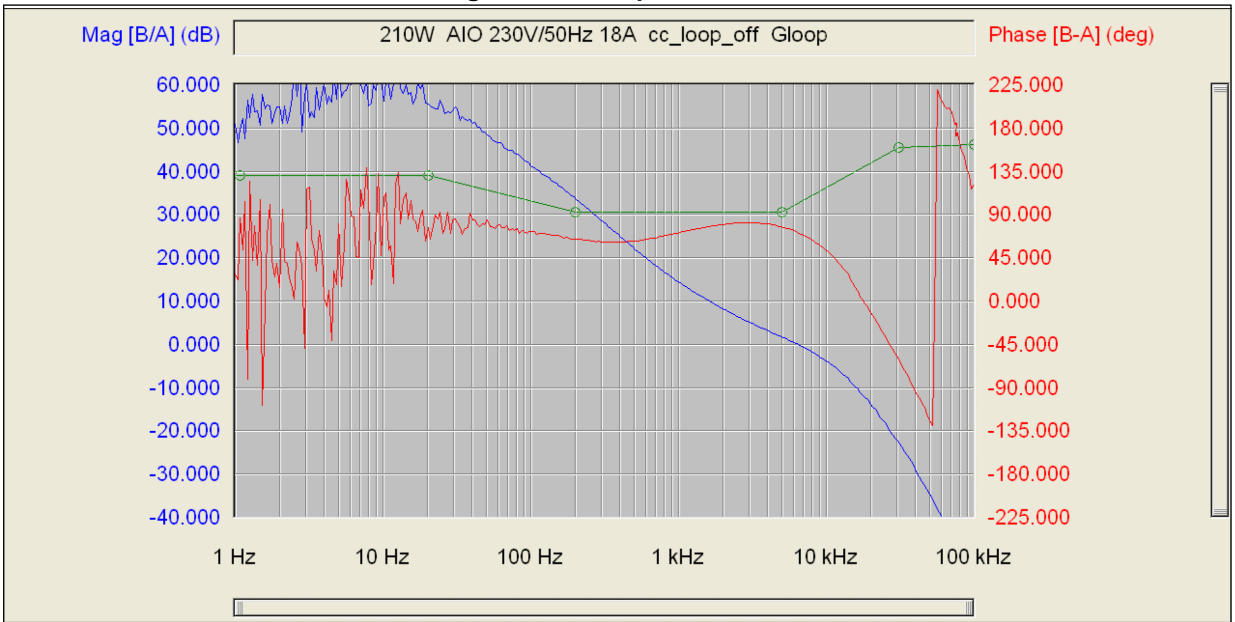
In *Section 6.5 on page 23* and *Section 6.6.2 on page 26*, some signs of the good dynamic response of the control loop have been highlighted (output voltage behavior during load transient, tank current behavior during mains disconnection).

In this section, such expectations find confirmation by the direct measurement of the control loop response, by means of a frequency response analyser (a.k.a. analog network analyser).

With respect to the converter schematic (*Figure 2 on page 9*), the source signal is injected through a transformer onto a 10 Ω resistor that replaces JPX17. Furthermore, the power supplies of U3 (SEA05L) and U5 (SRK2001) have been tied to the output voltage. Finally, the CC loop sensing resistors (R50, R51) have been shorted. The overall loop gain has been measured by probing the two sides of the 10 Ω resistor.

The magnitude and phase of the loop gain are shown in *Figure 38*: the low frequency gain is practically given by the pole in the origin; the 0 dB frequency is about 7 kHz at which the phase is about 70 deg.; the 0 deg. frequency is about 30 kHz at which the gain is about -10 dB.

Figure 38. Gloop at full load



BLUE: amplitude in dB, RED: phase in degrees, GREEN: amplitude mask of the source signal

8 Thermal map

In order to check the design reliability, a thermal mapping by means of an IR camera has been done. *Figure 39* shows the thermal map of the top side of the EVLCMB1-AIO210W after about 2 h at 90 Vac / 210 W. Temperatures of the most relevant elements have been taken and highlighted, in *Figure 39* and in *Table 8*. Then, the converter has been kept on at the full load, 210 W, for about another 1 h at 115 Vac and another further 1 h at 230 Vac. The temperatures of the most relevant points has been taken by means of an IR contact probe. The room temperature was around 25 °C. Reflecting surfaces have been covered with rubber insulating the black ribbon.

Figure 39. 90 Vac / 60 Hz - full load

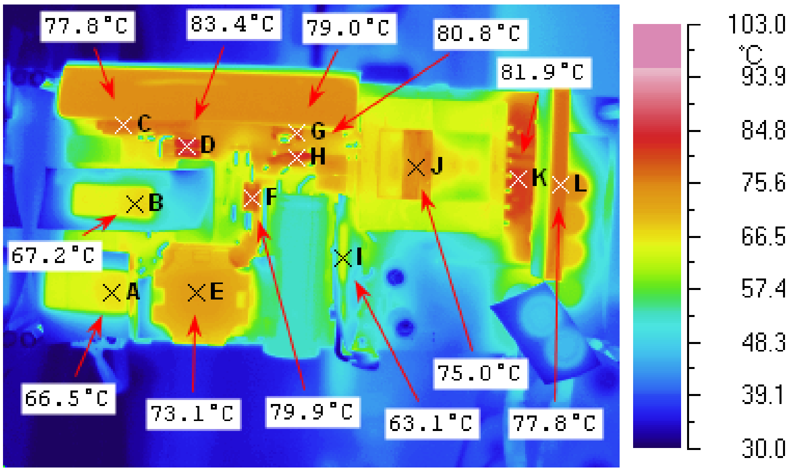


Table 8. Thermal maps reference points

Point	Sch. ref.	Description	T [°C] at 90 Vac / 210 W	T [°C] at 115 Vac / 210 W	T [°C] at 230 Vac / 210 W
A	L1	1st Input common mode choke	66.5	65	35
B	L2	2nd Input common mode choke	67.2	65	38
C	D1	Bridge rectifier	77.8	75	64
D	R1 / R72	PFC sensing resistors	83.4	-	-
E	L4	PFC inductor	73.1	70	53
F	D5	PFC boost diode	79.9	75	62
G	Q1	PFC switch	79.0	75	54
H	R3	NTC resistor	80.8	78	63
I	Q2 / Q3	LLC switches (sinker)	63.1	61	62
J	T1	LLC transformer	75.0	74	72
K	-	Secondary side hot region	81.9	-	-
L	Q7 / Q8	Synchronous rectifiers (sinker)	77.8	74	75
-	C16 / C17	Resonant capacitors	-	72	74

9 Conducted emission pre-compliance test

A pre-compliance test (testing environment not compliant) on conducted emission has been carried on. From *Figure 40* to *Figure 43* show the average measurement of the conducted emission at the full load and nominal mains voltages, for both the conductors (PHASE and NEUTRAL), compared to the EN55022-Class-B limits. The converter is fed by the AC line, through an isolation transformer and the LISN. With respect to the proposed schematic (see *Figure 2 on page 9*), the Y capacitor, C10, between the PFC output and the secondary ground has been removed because it could take the peak at about 12 MHz above the limit. However, it is worthwhile to highlight that such peak seems to be related to the activity of the active load (see *Figure 44* and *Figure 45* showing the floor noise of the test bench).

Figure 40. 115 Vac / full load - PHASE

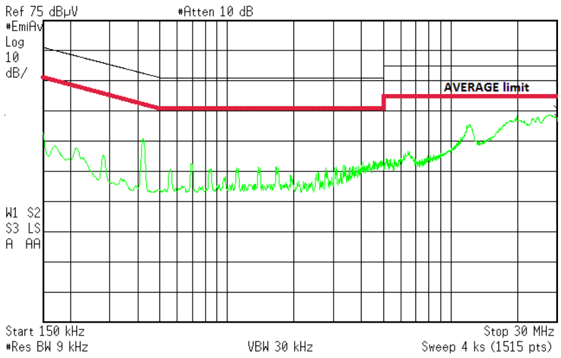


Figure 41. 115 Vac / full load - NEUTRAL

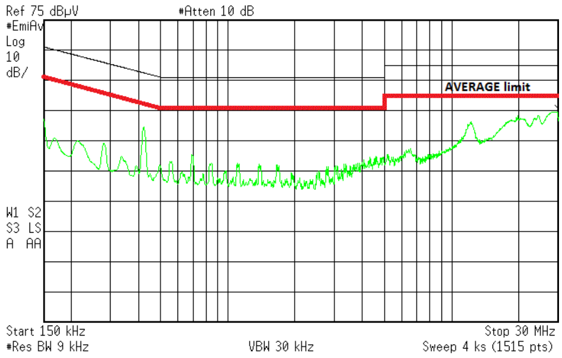


Figure 42. 230 Vac / full load - PHASE

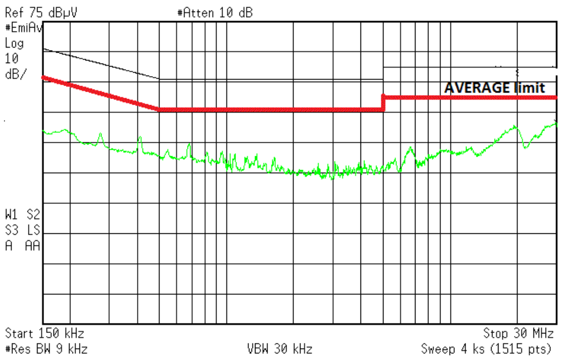


Figure 43. 230 Vac / full load - NEUTRAL

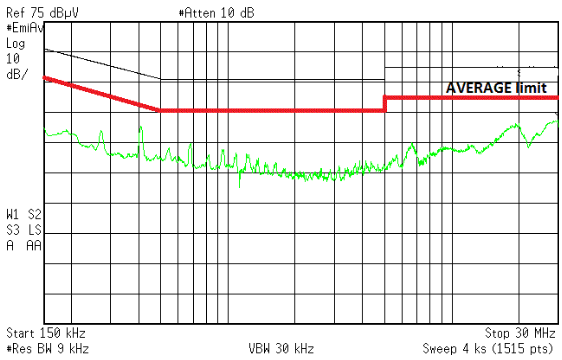


Figure 44. Floor noise: converter off, active load on

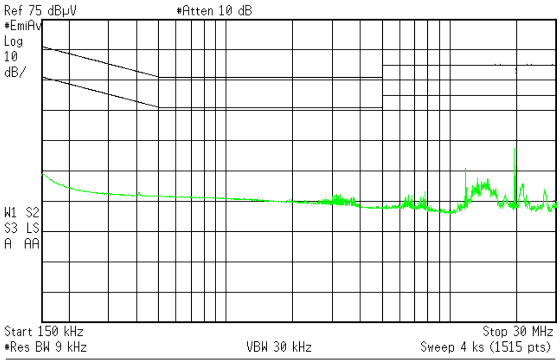
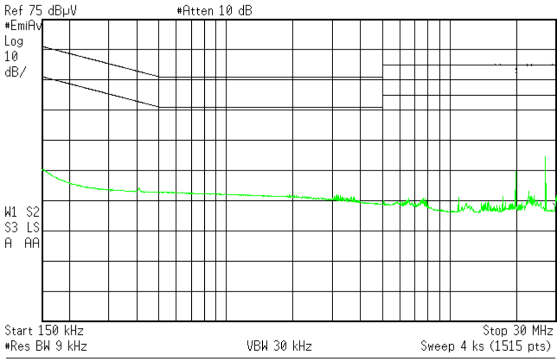


Figure 45. Floor noise: converter off, active load off



10 Bill of material

Table 9. EVLCMB1-AIO210W BOM

Sch. ref.	Part no.	Case	Description	Supplier
C1	150 N - X2	6.0 x 18.0, p. 15 mm	X2 film cap. B32922C3154K	EPCOS
C2	470 N - X2	9.0 x 18.0, p. 15 mm	X2 film cap. B32922C3474K	EPCOS
C5	470 N - X2	9.0 x 18.0, p. 15 mm	X2 film cap. B32922C3474K	EPCOS
C7	1.5 U, 520 V	12.0 x 26.5.0, p. 22.5 mm	520 V film cap. B32673Z5155K	EPCOS
C10	2.2 N - Y1	P. 10 mm	Y1 safety cap. DE1E3KX222M	MURATA
C11	2.2 N - Y1	P. 10 mm	Y1 safety cap. DE1E3KX222M	MURATA
C12	180 µF, 450 V	Dia. 18 x 50 mm	450 V alu. ELCAP BXW series 105 °C	RUBYCON
C14	220 P, 1 kV	1206	1000 V CERCAP	-
C15	10 N	0805	50 V CERCAP general purpose	AVX
C16	6.8 N, 500 V	6 x 10.3, p.7.5 mm	500 V MKP film cap. B32620A682J	EPCOS
C17	6.8 N, 500 V	6 x 10.3, p.7.5 mm	500 V MKP film cap. B32620A682J	EPCOS
C20	100 PF - 630 V	1206	630 V CERCAP GRM31A7U2J101JW31D	MURATA
C21	100 N	0805	50 V CERCAP general purpose	AVX
C23	100 N	0805	50 V CERCAP general purpose	AVX
C24	1 µF	0805	50 V CERCAP X7R general purpose	TDK
C25	1.8 nF	0805	50 V CERCAP general purpose	AVX
C26	4.7 µF	0805	10 V CERCAP general purpose	AVX
C27	220 P	0805	50 V 5% C0G CERCAP	AVX
C29	220 P	0805	50 V 5% C0G CERCAP	AVX
C28	1 N	0805	50 V CERCAP general purpose	AVX
C31	1 N	0805	50 V CERCAP general purpose	AVX
C30	470 P	0805	50 V 5% C0G CERCAP	AVX
C32	1 µF	1206	50 V CERCAP X7R 10%	TDK
C38	1 µF	1206	50 V CERCAP X7R 10%	TDK
C39	1 µF	1206	50 V CERCAP X7R 10%	TDK
C40	1 µF	1206	50 V CERCAP X7R 10%	TDK
C45	1 µF	1206	50 V CERCAP X7R 10%	TDK
C55	1 µF	1206	50 V CERCAP X7R 10%	TDK
C56	1 µF	1206	50 V CERCAP X7R 10%	TDK
C33	100 µF - 50 V	Dia. 8 x 11.5, p. 3.5 mm	Aluminium ELCAP YXF series 105 °C	RUBYCON
C34	100 µF - 50 V	Dia. 8 x 11.5, p. 3.5 mm	Aluminium ELCAP YXF series 105 °C	RUBYCON
C35	330 µF - 25 V	D.10.0 x H13.0, p. 5.0 mm	25 V OSCON ELCAP SEPF series 105 °C	PANASONIC

Table 9. EVLCMB1-AIO210W BOM (continued)

Sch. ref.	Part no.	Case	Description	Supplier
C36	330 µF - 25 V	D.10.0 x H13.0, p. 5.0 mm	25 V OSCON ELCAP SEPF series 105 °C	PANASONIC
C37	330 µF - 25 V	D.10.0 x H13.0, p 5.0mm	25 V OSCON ELCAP SEPF series 105 °C	PANASONIC
C44	330µF - 25 V	D.10.0 x H13.0, p 5.0mm	25 V OSCON ELCAP SEPF series 105 °C	PANASONIC
C41	2.7 N	0805	50 V CERCAP X7R general purpose	AVX
C42	2.7 N	0805	50 V CERCAP X7R general purpose	AVX
C43	10 µF	1206	35 V CERCAP X5R general purpose	TDK
C46	8.2 N	0805	25 VCERCAP general purpose	AVX
C49	560 P	0805	50 V CERCAP general purpose	AVX
C50	4.7 N	0805	50 V 5% C0G CERCAP	AVX
C51	100 N	1206	50 V CERCAP general purpose	AVX
C53	2200 µF - 25 V	D.12.5 x H30.0, p. 5.0 mm	25 V ALU ELCAP ZLH series 105 °C	RUBYCON
C54	2200 µF - 25 V	D.12.5 x H30.0, p. 5.0 mm	25 V ALU ELCAP ZLH series 105 °C	RUBYCON
D1	D15XB60H	5S	Single phase bridge rectifier	SHINDENGEN
D2	S1M	DO214AC	General purpose rectifier, SMT	FAIRCHILD
D3	S1M	DO214AC	General purpose rectifier, SMT	FAIRCHILD
D4	1N5406	DO201	General purpose rectifier	VISHAY
D5	STTH5L06	DO201	Ultrafast high voltage rectifier	ST
D6	1N4148WS	SOD-323	High speed signal diode	VISHAY
D7	1N4148WS	SOD-323	High speed signal diode	VISHAY
D8	1N4148WS	SOD-323	High speed signal diode	VISHAY
D11	1N4148WS	SOD-323	High speed signal diode	VISHAY
D19	1N4148WS	SOD-323	High speed signal diode	VISHAY
D12	MMSZ4700T1G	SOD-123	Zener diode	DIODES
D13	STPS2H100A	SMA	Power Schottky diode	ST
D16	MMSZ5259B-7-F	SOD-123	Zener diode	DIODES
D17	SMAJ40CA	SMA	TVS diode SMAJ series	ST
D18	SMAJ40CA	SMA	TVS diode SMAJ series	ST
F1	Fuse T4A	8.5 x 4, p. 5.08 mm	FUSE 4A TIME LAG 3921400	LITTELFUSE
HS1	Heatsink	DWG	Heatsink for D1, Q1	-
HS2	Heatsink	DWG	Heatsink for Q2, Q3	-
HS3	Heatsink	DWG	Heatsink for Q7, Q8	-
JPX3	Shorted	-	Wire jumper	-
JPX5	Shorted	-	Wire jumper	-
JPX6	Shorted	-	Wire jumper	-

Table 9. EVLCMB1-AIO210W BOM (continued)

Sch. ref.	Part no.	Case	Description	Supplier
JPX7	Shorted	-	Wire jumper	-
JPX9	Shorted	-	Wire jumper	-
JPX10	Shorted	-	Wire jumper	-
JPX11	Shorted	-	Wire jumper	-
JPX12	Shorted	-	Wire jumper	-
JPX13	Shorted	-	Wire jumper	-
JPX14	Shorted	-	Wire jumper	-
JPX15	Shorted	-	Wire jumper	-
JPX16	Shorted	-	Wire jumper	-
JPX17	Shorted	-	Wire jumper	-
JPX4	Shorted	-	Wire jumper	-
JPX18	Shorted	-	Wire power jumper	-
JPX19	Shorted	-	Wire power jumper	-
J1	MKDS 1,5/ 3 -5,08	DWG	PCB screw conn. 5 MM, 3 W.	PHOENIX CONTACT
J2	FASTON M 90	DWG	FASTON connector	-
J3	FASTON M 90	DWG	FASTON connector	-
L1	VOTC2506501000A	DWG	Toroidal EMI CM filter	YUJING
L2	VITC2707501950A	DWG	Toroidal EMI CM filter	YUJING
L4	QP2925V	DWG	PFC inductor 250 µH	YUJING
Q1	STF25N60M2-EP	TO-220FP	N-channel power MOSFET	ST
Q2	STF15N60M2-EP	TO-220FP	N-channel power MOSFET	ST
Q3	STF15N60M2-EP	TO-220FP	N-channel power MOSFET	ST
Q4	MMBT2907A	SOT-23	PNP small signal BJT	VISHAY
Q5	BC847C	SOT-23	NPN small signal BJT	VISHAY
Q6	BC847C	SOT-23	NPN small signal BJT	VISHAY
Q7	STP220N6F7	TO-220	N-channel power MOSFET	ST
Q8	STP220N6F7	TO-220	N-channel power MOSFET	ST
R1	0R10	PTH RSMF1TB	Metal film res. 1 W, 2%, 200 ppm/°C	AKANEOHM
R72	0.10 Ω	PTH RSMF1TB	Metal film res. 1 W, 2%, 200 ppm/°C	AKANEOHM
R2	0 Ω	1206	SMD STD film res. 1/4 W, 5%, 200 ppm/°C	VISHAY
R21	0 Ω	1206	SMD STD film res. 1/4 W, 5% ,200 ppm/°C	VISHAY
R38	0 Ω	1206	SMD STD film res. 1/4 W, 5% ,200 ppm/°C	VISHAY
R62	0 Ω	1206	SMD STD film res. 1/4 W, 5%, 200 ppm/°C	VISHAY

Table 9. EVLCMB1-AIO210W BOM (continued)

Sch. ref.	Part no.	Case	Description	Supplier
R73	0 Ω	1206	SMD STD film res. 1/4 W, 5%, 200 ppm/°C	VISHAY
R3	NTC 1R0-S237	Dia. 15 x 7 p. 7.5 mm	NTC resistor P/N B57237S0109M000	EPCOS
R4	2.7 MΩ	PTH	PTH STD film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R5	2.7 MΩ	1206	SMD STD film res. 1/4 W, 1%, 100 ppm/°C	VISHAY
R6	2.7 MΩ	1206	SMD STD film res. 1/4 W, 1%, 100 ppm/°C	VISHAY
R7	51 KΩ	0805	SMD STD film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R10	22 Ω	0805	SMD STD film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R60	22 Ω	0805	SMD STD film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R11	12 Ω	0805	SMD STD film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R12	100 KΩ	0805	SMD STD film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R15	100 KΩ	0805	SMD STD film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R18	100 KΩ	0805	SMD STD film res. 1/8 W, 1% ,100 ppm/°C	VISHAY
R13	15 Ω	0805	SMD STD film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R16	15 Ω	0805	SMD STD film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R14	56 Ω	0805	SMD STD film res.1/8 W, 5%, 200 ppm/°C	VISHAY
R17	56 Ω	0805	SMD STD film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R19	100 Ω	0805	SMD STD film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R20	33 Ω	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R22	0R0	1206	SMD std. film res. 1/4 W, 5%, 200 ppm/°C	VISHAY
R23	0R0	1206	SMD std. film res. 1/4 W, 5%, 200 ppm/°C	VISHAY
R24	56 KΩ	1206	SMD std. film res. 1/4 W, 5%, 200 ppm/°C	VISHAY
R25	56 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R27	2.7 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R28	33 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R34	33 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R57	33 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R29	3.9 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R30	220 Ω	0805	SMD std. film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R32	220 Ω	0805	SMD std. film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R31	270 Ω	1206	SMD std. film res. 1/4 W, 5%, 200 ppm/°C	VISHAY
R33	0 Ω	0805	SMD std. film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R35	10 KΩ	0805	SMD std. film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R36	10 Ω	0805	SMD std. film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R37	4.7 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY

Table 9. EVLCMB1-AIO210W BOM (continued)

Sch. ref.	Part no.	Case	Description	Supplier
R39	22 Ω	1206	SMD std. film res. 1/4 W, 1%, 100 pm/°C	VISHAY
R40	22 Ω	1206	SMD std. film res. 1/4 W, 1%, 100 ppm/°C	VISHAY
R41	100 Ω	1206	SMD std. film res. 1/4 W, 1% ,100 ppm/°C	VISHAY
R42	100 Ω	1206	SMD std. film res. 1/4 W, 1% ,100 ppm/°C	VISHAY
R50	5 mΩ	2010	SMD current sense resistor WSLP	VISHAY
R51	5 mΩ	2010	SMD current sense resistor WSLP	VISHAY
R52	910 Ω	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R53	1.8 KΩ	0805	SMD std. film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R55	270 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R56	120 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R58	680 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R59	18 KΩ	0805	SMD std. film res. 1/8 W, 1%, 100 ppm/°C	VISHAY
R61	1 KΩ	1206	SMD std. film res. 1/4 W, 1%,100 ppm/°C	VISHAY
R71	6.2 KΩ	0805	SMD std. film res. 1/8 W, 5%, 200 ppm/°C	VISHAY
R74	1.2 KΩ	1206	SMD std. film res. 1/4 W, 5%, 200 ppm/°C	VISHAY
R75	10 Ω	1206	SMD std. film res. 1/4 W, 1%, 100 ppm/°C	VISHAY
T1	LP3925H	DWG	Resonant transformer LP3925H	YUJING
U1	STCMB1A	SO20W	TM PFC and HB LLC res. COMBO contr.	ST
U2	SFH617A-4	DIP-4 10.16 MM	Optocoupler	VISHAY
U3	SEA05L	SOT23-6L	CV/CC contr. with LED driver	ST
U5	SRK2001	SSOP10	SRK2001 SR controller	ST

11 PFC coil specification

General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: vertical type, 8 pins
- Max. temp. rise: 45ºC
- Max. operating ambient temperature: 60ºC
- Mains insulation: N.A.
- Unit finishing: varnished

Electrical characteristics

- Converter topology: transition mode boost
- Core type: QP2925 - 3C94
- Min. operating frequency: 40 kHz
- Typical operating frequency: 150 kHz
- Primary inductance: 250 μH ± 8% at 100 kHz - 0.25 V
- Peak primary current: 7.7 A_{PK}
- RMS primary current 3.08 A_{RMS}

Electrical diagram and winding characteristics

Figure 46. PFC coil electrical diagram

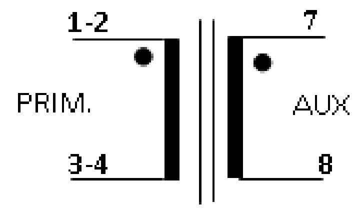


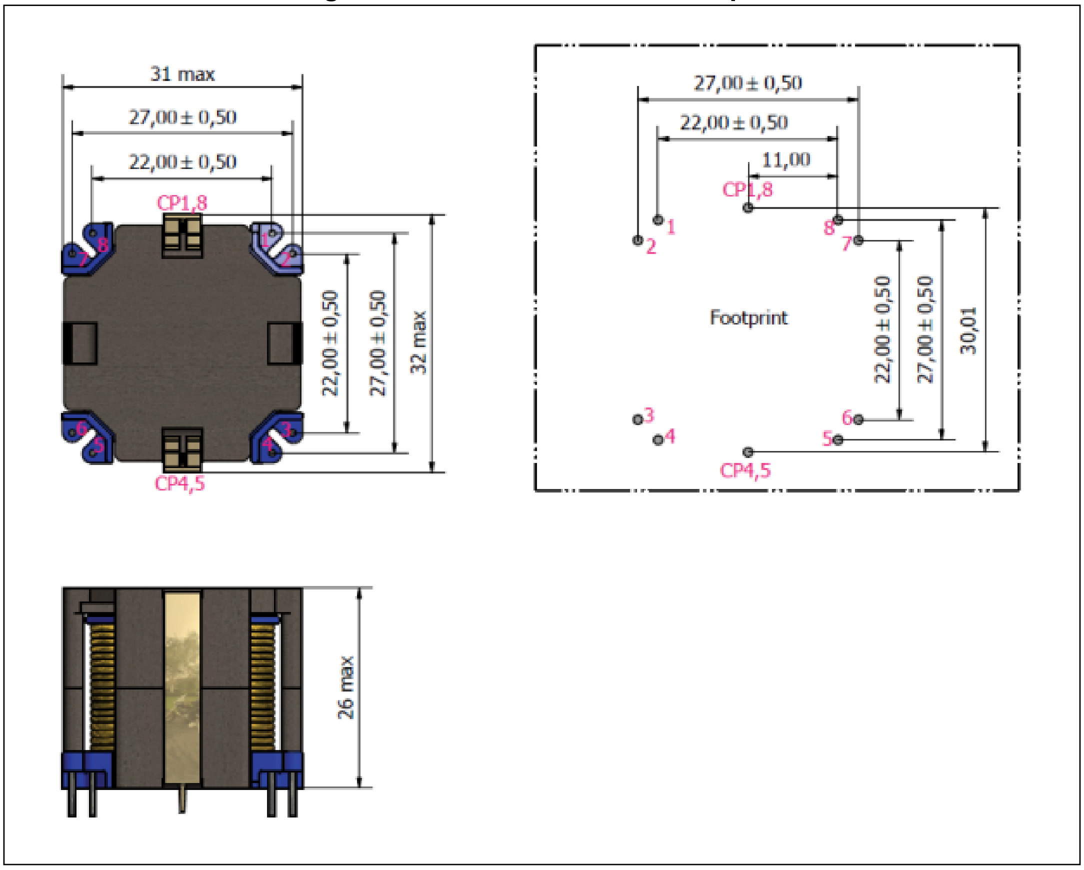
Table 10. PFC coil winding data

Pins	Windings	RMS current	Number of turns
1, 2 - 3, 4	PRIMARY	2.65 A_{RMS}	50
7 - 8	AUX	0.05 A_{RMS}	5

Mechanical aspect and pin numbering

- Maximum height from PCB: 25 mm
- Coil former type: vertical, 8 pins
- Pin distance: see mechanical drawing
- Row distance: see mechanical drawing
- Pin 6 removed for insertion polarity key
- Ferrite grounding: grounded by two clamps fixed to core and soldered to PCB.

Figure 47. PFC coil mechanical aspect



Manufacturer

- YUJING Taiwan
- Inductor P/N: QP2925V

12 LLC transformer specification

General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: horizontal type, 8+8 pins, 2 slots
- Max. temp. rise: 45 °C
- Max. operating ambient temperature: 60 °C
- Mains insulation: in accordance with EN60065 - EN60950

Electrical characteristics

- Converter topology: resonant half bridge
- Core type: LP3925 - 3C94
- Min. operating frequency: 116 kHz
- Typical operating frequency: 160 kHz
- Primary inductance: 490 µH ±10% at 100 kHz - 0.25 V
- Leakage inductance: 68 µH ±10% at 100 kHz - 0.25 V
- Difference between the two measured leakage inductances < 5%

Electrical diagram and winding characteristics

Figure 48. Transformer electrical diagram

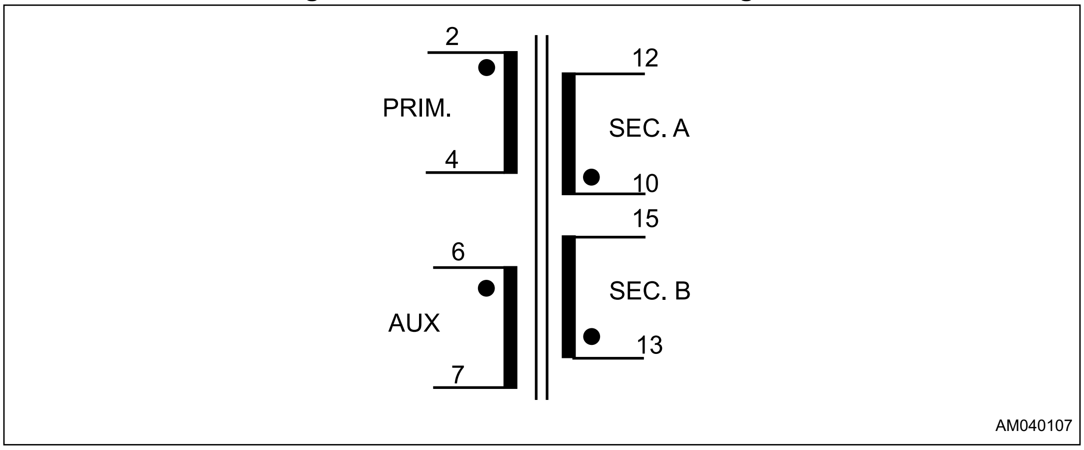


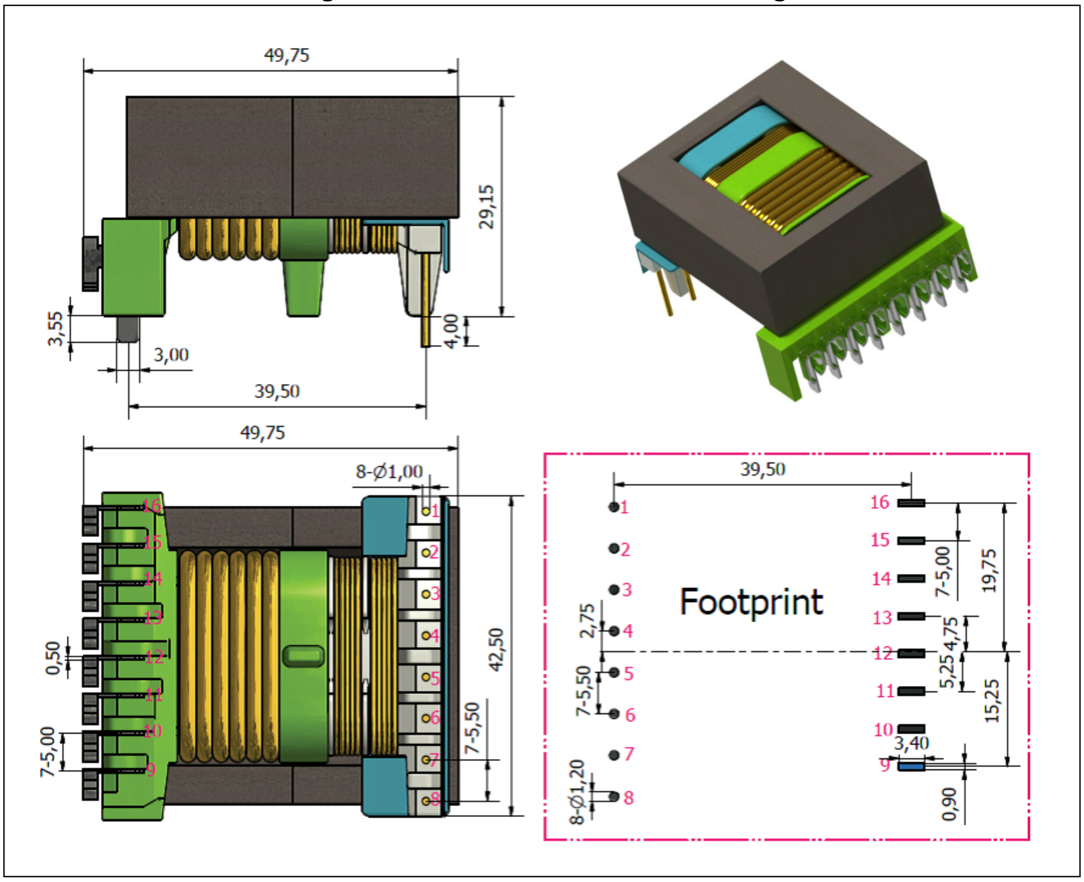
Table 11. Transformer winding data

Pins	Winding	RMS current	Number of turns
2 - 4	PRIMARY	1.33 A_{RMS}	33
10 - 12	SEC-D1	13.8 A_{RMS}	2
13 - 15	SEC-D2	13.8 A_{RMS}	2
6 - 7	AUX	0.05 A_{RMS}	2 spaced

Mechanical aspect and pin numbering

- Maximum height from PCB: 31 mm
- Pin distance: see mechanical drawing
- Pin distance: see mechanical drawing
- Row distance: see mechanical drawing
- Pins 3, 8, 16 removed

Figure 49. Transformer overall drawing



Manufacturer

- YUJING Taiwan
- Transformer P/N: LP3925H

13 Revision history

Table 12. Document revision history

Date	Revision	Changes
14-Jun-2017	1	Initial release.
02-Mar-2020	2	*Figure 2*, *3*, and *4* updated. Text change to *Section 2.1*. *Table 1*, *2*, *3*, *4*, *5*, and *6* updated. *Section 6.6.1* updated. Text change to *Section 6.7*, *6.8*, *6.10*, and *6.11*.