Application note

Getting started with STM32G0 Series hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as the power supply, the clock management, the reset control, the boot mode settings and the debug management. It shows how to use the STM32G0 Series devices and describes the minimum hardware resources required to develop an application.

This document also includes detailed reference design schematics with the description of the main components, interfaces and modes.

1 Power supplies and reset sources on STM32G0 Series

This section describes the power supply schemes and the reset and power supply supervisor on STM32G0 Series devices.

STM32G0 Series are Arm® based devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Power supplies on STM32G0 Series

The STM32G0 Series devices require a 1.7 V to 3.6 V operating supply voltage (V_{DD}). Several different power supplies are provided to specific peripherals:

- V_{DD} = 1.7 V (1.60 V) to 3.6 V

  V_{DD} is the external power supply for the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD/VDDA pin.

  Note that the minimum voltage of 1.7 V corresponds to power-on reset release threshold $V_{POR(MAX)}$. Once this threshold is crossed and power-on reset is released, the functionality is guaranteed down to power-down reset threshold $V_{PDR(MIN)}$.
- V_{DDA} = 1.62 V (ADC and COMP) / 1.8 V (DAC) / 2.4 V (VREFBUF) to 3.6 V

  V_{DDA} is the analog power supply for the A/D converter, D/A converters, voltage reference buffer and comparators. V_{DDA} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{DDIO1} = V_{DD}

  V_{DDIO1} is the power supply for the I/Os. V_{DDIO1} voltage level is identical to V_{DD} voltage as it is provided externally through VDD/VDDA pin.
- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply (through a power switch) for RTC, TAMP, low-speed external 32.768 kHz oscillator and backup registers when V_{DD} is not present. V_{BAT} is provided externally through VBAT pin. When this pin is not available on the package, it is internally bonded to VDD/VDDA.
- V_{REF+} is the input reference voltage for the ADC and DAC, or the output of the internal voltage reference buffer (when enabled). When V_{DDA} < 2V, V_{REF+} must be equal to V_{DDA}. When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}. It can be grounded when the ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which is configured with VRS bit of the VREFBUF_CSR register:
  - V_{REF+} around 2.048 V (requiring V_{DDA} equal to or higher than 2.4 V)
  - V_{REF+} around 2.5 V (requiring V_{DDA} equal to or higher than 2.8 V)

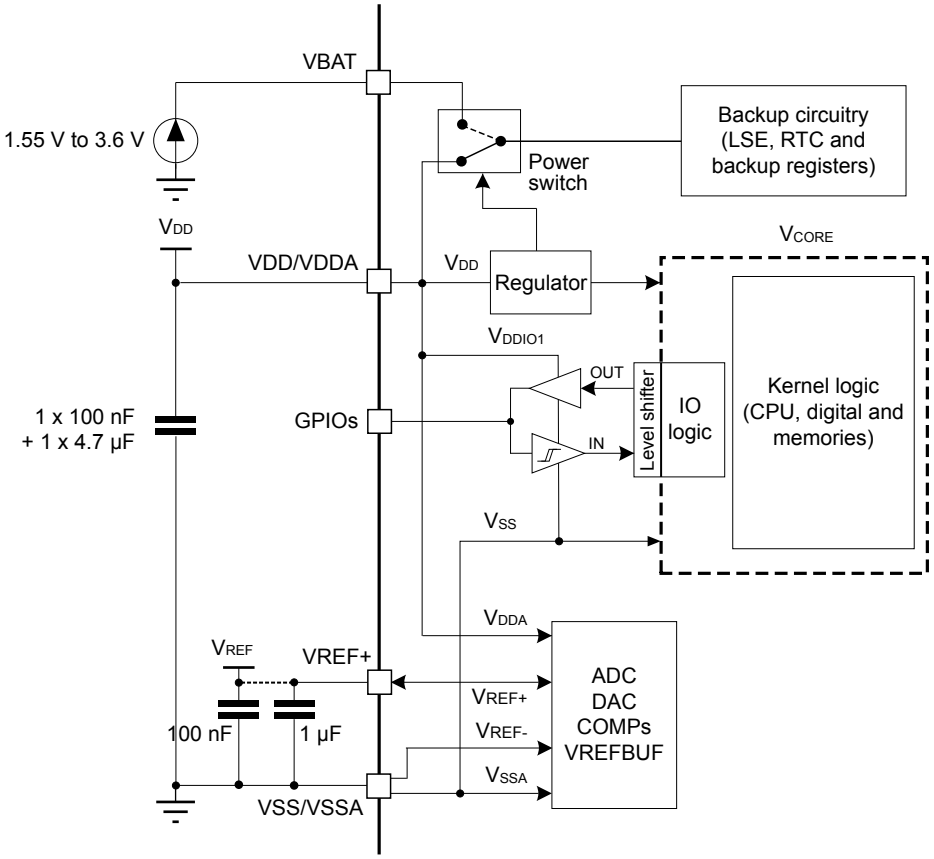
  V_{REF+} is delivered through VREF+ pin. On packages without VREF+ pin, V_{REF+} is internally connected with V_{DD}, and the internal voltage reference buffer must be kept disabled (refer to datasheets for package pinout description).
- V_{CORE}

  An embedded linear voltage regulator is used to supply the V_{CORE} internal digital power. V_{CORE} is the power supply for digital peripherals, SRAM and Flash memory. The Flash memory is also supplied by V_{DD}.

Table 1. Power supplies of STM32G0 Series

Power supply	STM32G0 Series
V_{DD}	1.7 to 3.6 V
V_{REF+}	When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}. When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}
V_{BAT}	1.55 to 3.6 V

Figure 1. STM32G0 Series power supply



Note: Power supply pin pair (VDD/VDDA and VSS/VSSA) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

1.1.1 Independent analog converter supply

To improve conversion accuracy and to extend the supply flexibility, the analog domain has an independent power supply which can be separately filtered and shielded from noise on the PCB.

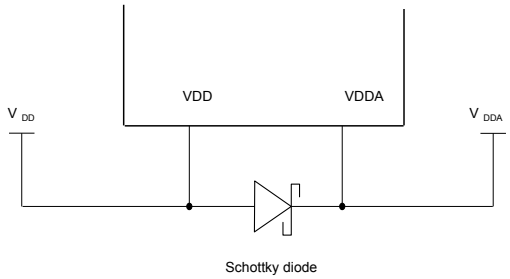
- The ADC and DAC voltage supply input is available on a separate VDDA pin.
- A separated supply ground connection is provided on pin VSSA.

The V_{DDA} supply can be equal to or higher than V_{DD}. This allows V_{DD} to stay low while still providing the full performance for the analog blocks.

When a single supply is used, V_{DDA} must be externally connected to V_{DD}. It is recommended to use an external filtering circuit in order to ensure a noise free V_{DDA}.

When V_{DDA} is different from V_{DD}, V_{DDA} must be always higher or equal to V_{DD}. To keep safe potential difference between V_{DDA} and V_{DD} during power-up/power-down, an external Schottky diode may be used between V_{DD} and V_{DDA}. Refer to the datasheet for the maximum allowed difference.

Figure 2. Schottky diode connection



1.1.2 Battery backup

To retain the content of the Backup registers when V_{DD} is turned off, the VBAT pin can be connected to an optional standby voltage supplied by a battery or another source.

The VBAT pin also powers the RTC unit, allowing the RTC to operate even when the main digital supply (V_{DD}) is turned off.

The switch to the V_{BAT} supply is controlled by the POR/PDR circuitry embedded in the reset block.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

1.1.3 Voltage regulator

The voltage regulator, when available on the device, is always enabled after reset.

It works under two different modes:

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode the regulator is in power-down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption and the loss of the register and SRAM contents. However, the following features are available if configured:

- Independent watchdog (IWDG): the IWDG is started by writing to its key register or by a hardware option. Once started it cannot be stopped except by a reset.
- Real-time clock (RTC): configured by the RTCEN bit in the RTC domain control register (RCC_BDCR).
- Internal low-speed oscillator (LSI): configured by the LSION bit in the control/status register (RCC_CSR).
- External 32.768 kHz oscillator (LSE): configured by the LSEON bit in the RTC domain control register (RCC_BDCR).

1.2 Power supply supervisor on STM32G0 Series

1.2.1 Power-on reset (POR) / power-down reset (PDR) / brown-out reset (BOR)

The devices feature an integrated power-on reset (POR) / power-down reset (PDR), coupled with a brown-out reset (BOR) circuitry. The POR/PDR is active in all power modes.

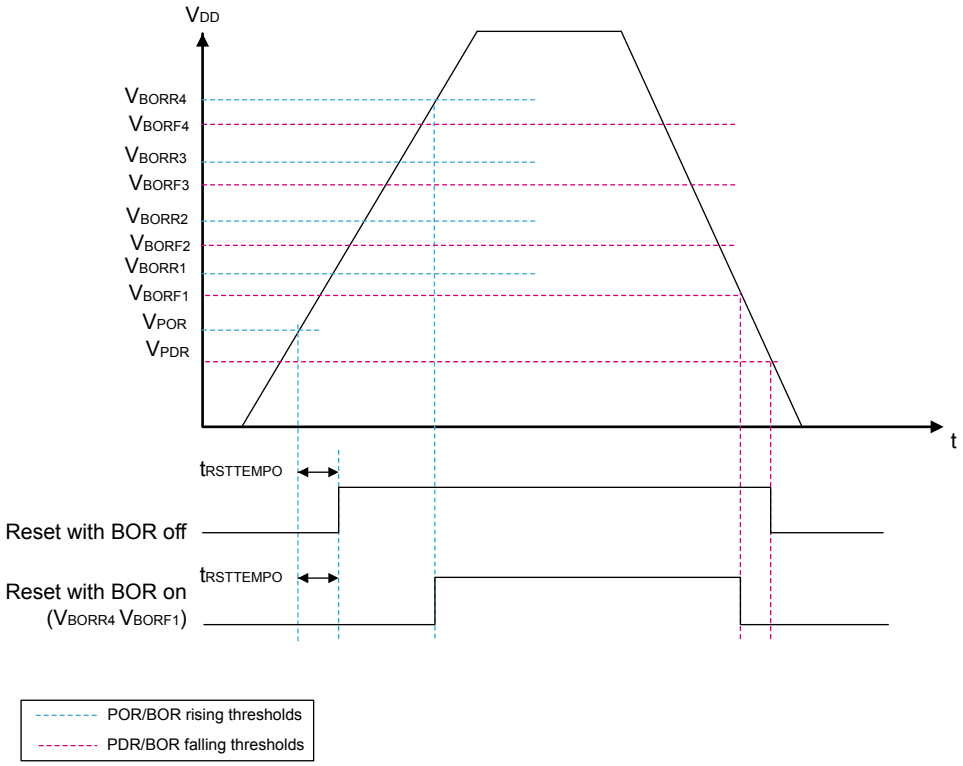
The BOR can be enabled or disabled only through option bytes. It is not available in Shutdown mode.

When the BOR is enabled, four BOR levels can be selected through option bytes, with independent configuration for rising and falling thresholds. During power-on, the BOR keeps the device under reset until the V_{DD} supply voltage reaches the specified BOR rising threshold (V_{BORRx}). At this point, the device reset is released and the system can start.

During power-down, when V_{DD} drops below the selected BOR falling threshold (V_{BORFx}),the device is put under reset again.

Note: It is not allowed to configure BOR falling threshold (V_{BORFx}) to a value higher than BOR rising threshold (V_{BORRx}).

Figure 3. POR, PDR, and BOR thresholds



Note: The reset temporization $t_{RSTTEMPO}$ starts when V_{DD} crosses V_{POR} threshold, indifferently from the configuration of the BOR option bits.

For more details on the brown-out reset thresholds, refer to the electrical characteristics section in the corresponding datasheet.

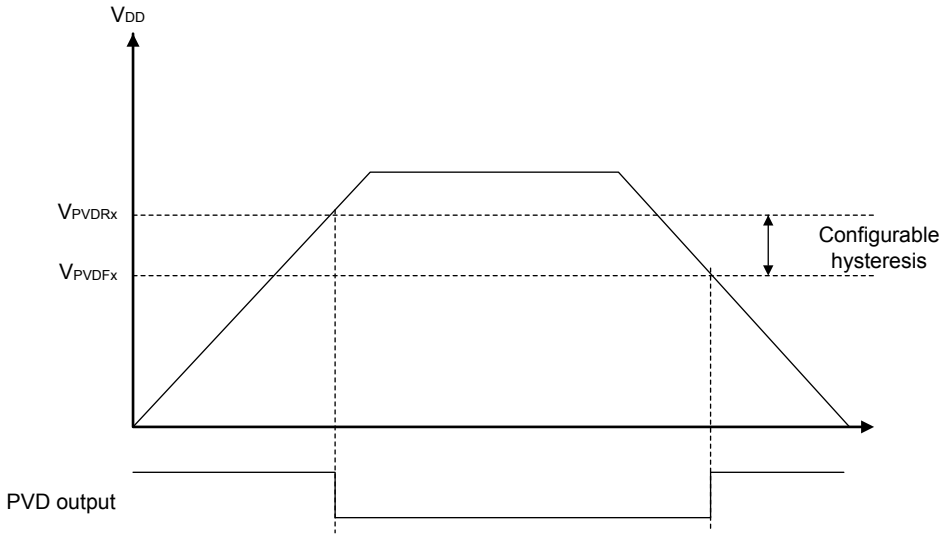
1.2.2 Programmable voltage detector (PVD)

The programmable voltage detector (PVD) can be used to monitor the V_{DD} power supply by comparing it to the thresholds selected through PVDRT[2:0] bits (rising thresholds) and PVDFT[2:0] bits (falling thresholds) in the Power control register 2 (PWR_CR2). V_{PVDFx} should always be set to a lower voltage level than V_{PVDRx}.

The PVD is enabled by setting the PVDE bit.

A PVDO flag is available in the Power status register 2 (PWR_SR2). It indicates if V_{DD} is higher or lower than the PVD threshold. This event is internally connected to the EXTI line16 and can generate an interrupt if enabled through the EXTI registers. The PVD output interrupt can be generated when V_{DD} drops below the PVD threshold and/or when V_{DD} rises above the PVD threshold depending on EXTI line16 rising/falling edge configuration. As an example, the service routine could perform emergency shutdown tasks.

Figure 4. PVD thresholds



1.3 Reset on STM32G0 Series

The following sections describe the three types of reset on STM32G0 Series: power reset, system reset and RTC domain reset.

1.3.1 Power reset

A power reset is generated when one of the following events occurs:

- power-on reset (POR) or brown-out reset (BOR)
- exit from Standby mode
- exit from Shutdown mode

Power and brown-out reset set all registers to their reset values except the registers of the RTC domain.

When exiting Standby mode, all registers in the V_{CORE} domain are set to their reset value.

Registers outside the V_{CORE} domain (RTC, WKUP, IWDG, and Standby/Shutdown mode control) are not impacted.

When exiting Shutdown mode, the brown-out reset is generated, resetting all registers except those in the RTC domain.

1.3.2 System reset

System reset sets all registers to their reset values except the reset flags in the clock control/status register (RCC_CSR) and the registers in the RTC domain.

System reset is generated when one of the following events occurs:

- low level on the NRST pin (external reset)
- window watchdog event (WWDG reset)
- independent watchdog event (IWDG reset)

- software reset (SW reset)
- low-power mode security reset
- option byte loader reset
- power-on reset

The reset source can be identified by checking the reset flags in the RCC_CSR register.

NRST pin (external reset)

Through specific option bits, the NRST pin is configurable for operating as:

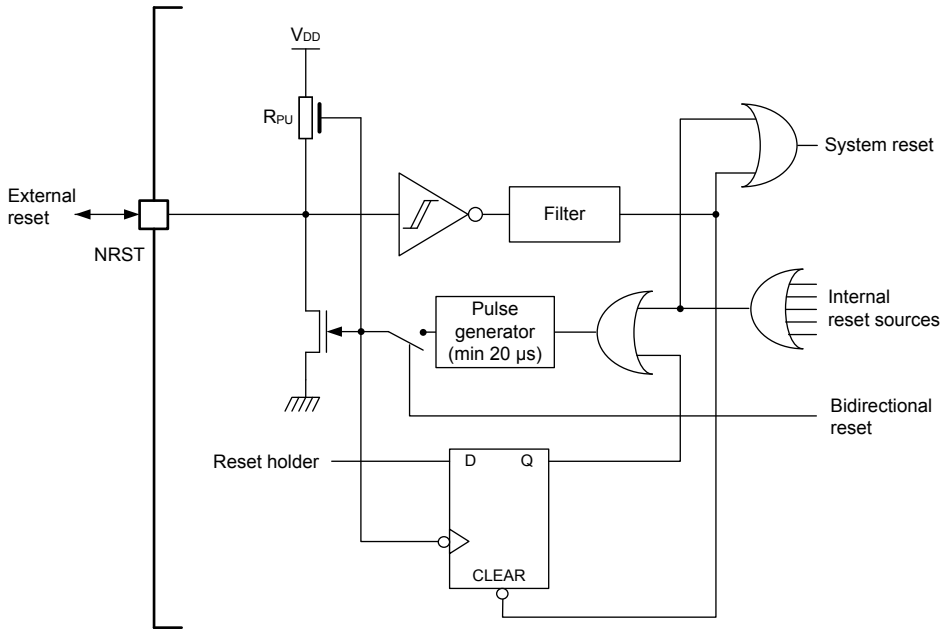
- **Reset input/output** (defautl at device delivery)

  Valid reset signal on the pin is propagated to the internal logic, and each internal reset source is led to a pulse generator the output of which drives this pin. The GPIO functionality (PF2) is not available. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source to be output on the NRST pin. An internal reset holder option can be used, if enabled in the option bytes, to ensure that the pin is pulled low until its voltage meets V_{IL} threshold. This function allows the detection of internal reset sources by external components when the line faces a significant capacitive load.
- **Reset input**

  In this mode, any valid reset signal on the NRST pin is propagated to device internal logic, but resets generated internally by the device are not visible on the pin. In this configuration, GPIO functionality (PF2) is not available.
- **GPIO**

  In this mode, the pin can be used as PF2 standard GPIO. The reset function of the pin is not available. Reset is only possible from device internal reset sources and it is not propagated to the pin.

Figure 5. Simplified diagram of the reset circuit



Note: Upon power reset or wakeup from shutdown mode, the NRST pin is configured as Reset input/output and driven low by the system until it is reconfigured to the expected mode when the option bytes are loaded, in the fourth clock cycle after the end of trstempo.

Software reset

The SYSRESETREQ bit in Cortex®-M0+ application interrupt and reset control register must be set to force a software reset on the device (refer to the STM32G0 and STM32L0 Cortex M0+ programming manual PM0223).

Low-power mode security reset

To prevent that critical applications mistakenly enter a low-power mode, three low-power mode security resets are available. If enabled in option bytes, the resets are generated in the following conditions:

- **Entering Standby mode**

  This type of reset is enabled by resetting nRST_STDBY bit in user option bytes. In this case, whenever a Standby mode entry sequence is successfully executed, the device is reset instead of entering Standby mode.
- **Entering Stop mode**

  This type of reset is enabled by resetting nRST_STOP bit in user option bytes. In this case, whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.
- **Entering Shutdown mode**

  This type of reset is enabled by resetting nRST_SHDW bit in user option bytes. In this case, whenever a Shutdown mode entry sequence is successfully executed, the device is reset instead of entering Shutdown mode.

Option byte loader reset

The option byte loader reset is generated when the OBL_LAUNCH bit (bit 27) is set in the FLASH_CR register. This bit is used to launch the option byte loading by software.

1.3.3 RTC domain reset

The RTC domain has two specific resets. An RTC domain reset is generated when one of the following events occurs:

- Software reset, triggered by setting the BDRST bit in the RTC domain control register (RCC_BDCR).
- V_{DD} or V_{BAT} power on, if both supplies have previously been powered off.

An RTC domain reset only affects the LSE oscillator, the RTC, the backup registers and the RCC RTC domain control register.

2 Clocks

STM32G0 Series provide the following clock sources producing primary clocks:

- **HSI RC** - a high-speed fully-integrated RC oscillator producing HSI16 clock (about 16 MHz)
- **HSE OSC** - a high-speed oscillator with external crystal/ceramic resonator or external clock source, producing HSE clock (4 to 48 LHz)
- **LSI RC** - a low-speed fully-integrated RC oscillator producing LSI clock (about 32 kHz)
- **LSE OSC** - a low-speed oscillator with external crystal/ceramic resonator or external clock source, producing LSE clock (accurate 32.768 kHz or external clock up to 1 MHz)
- **I2S_CKIN** - pin for direct clock input for I2S1 peripheral

Each oscillator can be switched on or off independently when it is not used, to optimize power consumption. Check sub-sections of this section for more functional details. For electrical characteristics of the internal and external clock sources, refer to the device datasheet.

The device produces secondary clocks by dividing or/and multiplying the primary clocks:

- **HSISYS** - a clock derived from HSI16 through division by a factor programmable from 1 to 128
- **PLLPCLK, PLLQCLK and PLLRCLK** - clocks output from the PLL block
- **SYSCLK** - a clock obtained through selecting one of LSE, LSI, HSE, PLLRCLK, and HSISYS clocks
- **HCLK** - a clock derived from SYSCLK through division by a factor programmable from 1 to 512
- **HCLK8** - a clock derived from HCLK through division by eight
- **PCLK** - a clock derived from HCLK through division by a factor programmable from 1 to 16
- **TIMPCLK** - a clock derived from PCLK, running at PCLK frequency if the APB prescaler division factor is set to 1, or at twice the PCLK frequency otherwise
- **LPTIMx_IN** - clock from LPTIMx_INx pins, selectable for the LPTIM peripheral

More secondary clocks are generated by fixed division of HSE, HSI16 and HCLK clocks.

The HSISYS is used as system clock source after startup from reset, with the division by 1 (producing HSI16 frequency).

The HCLK clock and PCLK clock are used for clocking the AHB and the APB domains, respectively. Their maximum allowed frequency is 64 MHz.

The peripherals are clocked with the clocks from the bus they are attached to (HCLK for AHB, PCLK for APB) except:

- **TIMx**, with these clock sources to select from:
  - TIMPCLK (selectable for all timers) running at PCLK frequency if the APB prescaler division factor is set to 1, or at twice the PCLK frequency otherwise
  - PLLQCLK selectable for high-speed TIM1 and TIM15 timers
- **LPTIMx**, with these clock sources to select from:
  - LSI
  - LSE
  - HSI16
  - PCLK (APB clock)
  - LPTIMx_IN selected from LPTIMx_INx pins

  The functionality in Stop mode (including wakeup) is supported only when the clock is LSI or LSE.
- **UCPD**, always clocked with HSI16
- **ADC**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSI16
  - PLLPCLK
- **USARTx / LPUART1**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSI16

  - LSE
  - PCLK (APB clock)

  The wakeup from Stop mode is supported only when the clock is HSI16 or LSE.
- **I2Cx**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSI16
  - PCLK (APB clock)

  The wakeup from Stop mode is supported only when the clock is HSI16.
- **I2S1**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSI16
  - PLLPCLK
  - I2S_CKIN pin
- **RNG**, with these clock sources to select from:
  - SYSCLK (system clock)
  - HSI16 clock divided by 8
  - PLLQCLK

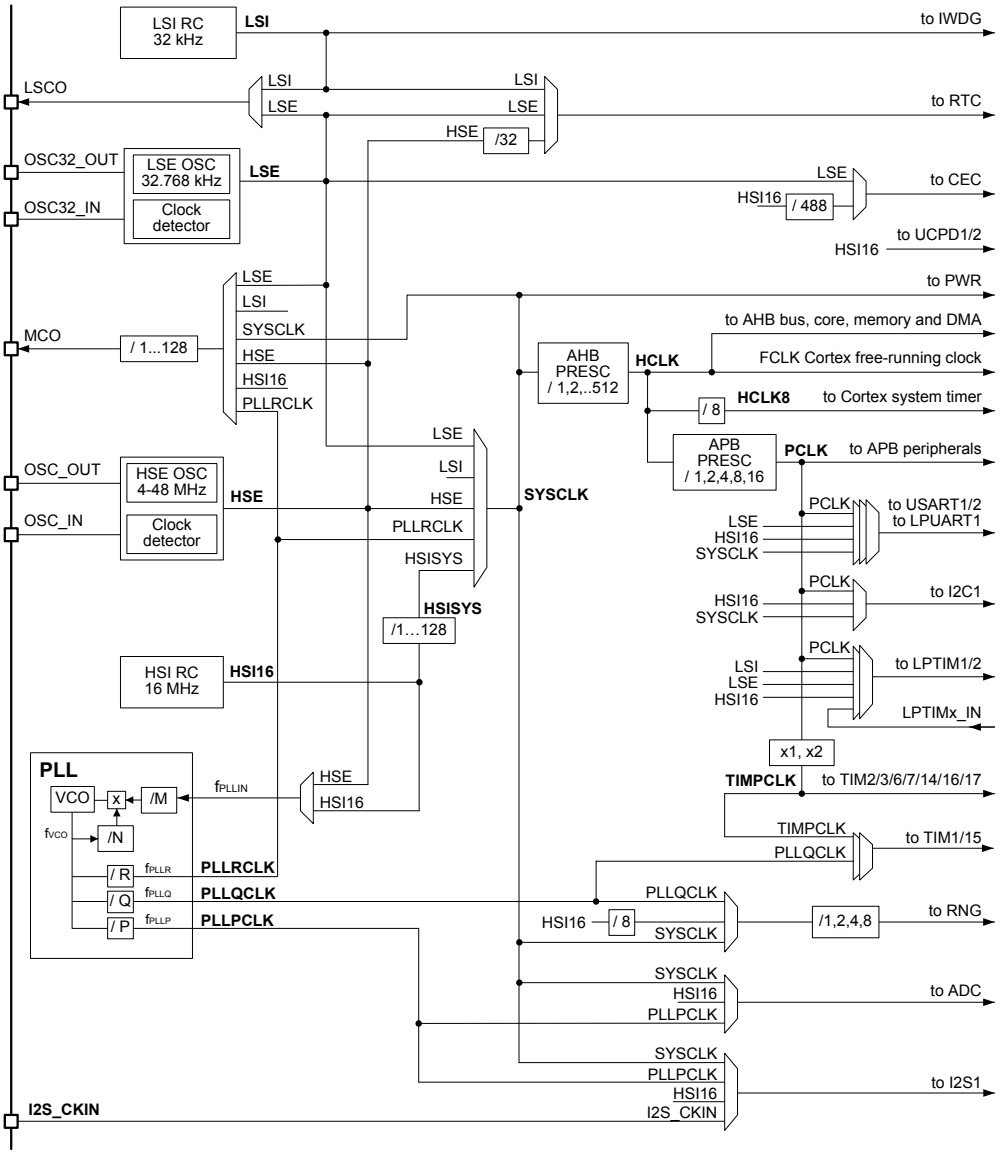
  The RNG clock can additionally be divided by 2,4 or 8, using a dedicated prescaler.
- **CEC**, with these clock sources to select from:
  - HSI16 clock divided by 488
  - LSE
- **RTC**, with these clock sources to select from:
  - LSE
  - LSI
  - HSE clock divided by 32

  The functionality in Stop mode (including wakeup) is supported only when the clock is LSI or LSE.
- **IWDG**, always clocked with LSI clock.
- **SysTick** (Cortex® core system timer), with these clock sources to select from:
  - HCLK (AHB clock)
  - HCLK clock divided by 8

  The selection is done through SysTick control and status register.

HCLK is used as Cortex®-M0+ free-running clock (FCLK). For more details, refer to the STM32G0 and STM32L0 Cortex M0+ programming manual (PM0223).

Figure 6. **Clock tree**



BOLD: clock origin

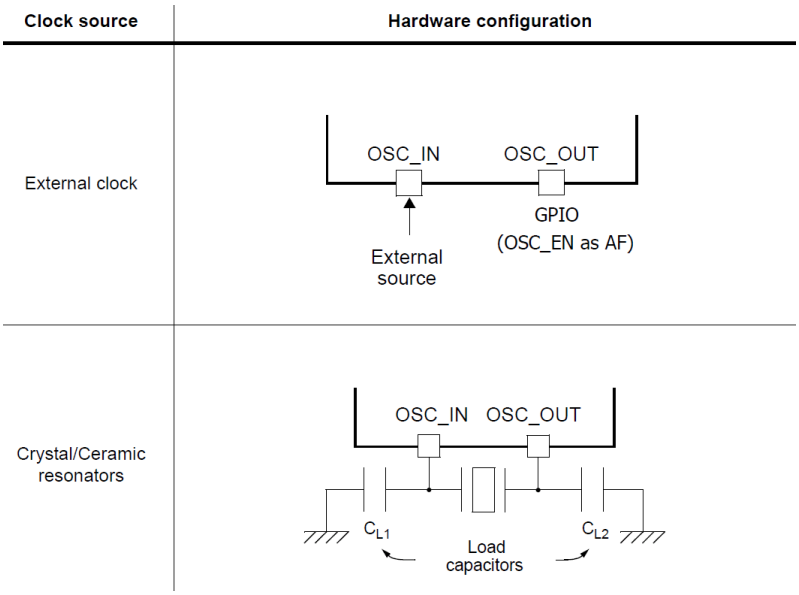
2.1 HSE clock

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Figure 7. **HSE/ LSE clock sources**



External crystal/ceramic resonator (HSE crystal)

The 4 to 48 MHz external oscillator has the advantage of producing a very accurate rate on the main clock.

The associated hardware configuration is shown in the figure above. Refer to the electrical characteristics section of the datasheet for more details.

The HSERDY flag in the clock control register (RCC_CR) indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the clock interrupt enable register (RCC_CIER).

The HSE crystal can be switched on and off using the HSEON bit in the clock control register (RCC_CR).

External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 48 MHz. This mode is selected by setting the HSEBYP and HSEON bits in the clock control register (RCC_CR). The external clock signal (square, sinus or triangle) with ~40-60% duty cycle depending on the frequency (refer to the datasheet) must drive the OSC_IN pin, on devices where OSC_IN and OSC_OUT pins are available (see the figure above).

The OSC_OUT pin can be used as a GPIO or it can be configured as OSC_EN alternate function, to provide an enable signal to external clock synthesizer. It allows stopping the external clock source when the device enters low power modes.

Note: For details on pin availability, refer to the pinout section in the corresponding device datasheet.

To minimize the consumption, it is recommended to use the square signal.

2.2 HSI16 clock

The HSI16 clock signal is generated from an internal 16MHz RC oscillator.

The HSI16 RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator. However, even after calibration, it is less accurate than an oscillator using a frequency reference such as quartz crystal or ceramic resonator.

The HSISYS clock derived from HSI16 can be selected as system clock after wakeup from Stop modes (Stop 0 or Stop 1). It can also be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails.

Calibration

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations. To compensate for this variation, each device is factory calibrated to 1% accuracy at T_A=25°C.

After reset, the factory calibration value is loaded in the HSICAL[7:0] bits in the internal clock sources calibration register (RCC_ICSCR).

Voltage or temperature variations in the application may affect the HSI16 frequency of the RC oscillator. It can be trimmed using the HSITRIM[6:0] bits in the internal clock sources calibration register (RCC_ICSCR).

For more details on how to measure the HSI16 frequency variation, refer to reference manual RM0444.

The HSIRDY flag in the clock control register (RCC_CR) indicates if the HSI16 RC is stable or not. At startup, the HSI16 RC output clock is not released until this bit is set by hardware.

The HSI16 RC can be switched on and off using the HSION bit in the clock control register (RCC_CR).

The HSI16 signal can also be used as a backup source (auxiliary clock) if the HSE crystal oscillator fails.

2.3 PLL

The internal PLL multiplies the frequency of HSI16- or HSE-based clock fetched on its input, to produce three independent clock outputs. The allowed input frequency range is from 2.66 to 16 MHz. The dedicated divider PLLM with division factor programmable from 1 to 8 allows setting a frequency within the valid PLL input range. Refer to Figure 6. Clock tree and to the PLL configuration register (RCC_PLLCFGR) on RM0444.

The PLL configuration (selection of the input clock and multiplication factor) must be done before enabling the PLL. Once the PLL is enabled, these parameters cannot be changed.

To modify the PLL configuration, proceed as follows:

1. Disable the PLL by setting PLLON to 0 in Clock control register (RCC_CR).
2. Wait until PLLRDY is cleared. The PLL is now fully stopped.
3. Change the desired parameter.
4. Enable the PLL again by setting PLLON to 1.
5. Enable the desired PLL outputs by configuring PLLPEN, PLLQEN, and PLLREN in PLL configuration register (RCC_PLLCFGR).

An interrupt can be generated when the PLL is ready, if enabled in the clock interrupt enable register (RCC_CIER).

The enable bit of each PLL output clock (PLLPEN, PLLQEN, and PLLREN) can be modified at any time without stopping the PLL. PLLREN cannot be cleared if PLLRCLK is used as system clock.

2.4 LSE clock

The LSE crystal is a 32.768 kHz low speed external crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The LSE crystal is switched on and off using the LSEON bit in RTC domain control register (RCC_BDCR). The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in the RTC domain control register (RCC_BDCR) to obtain the best compromise between robustness and short start-up time on one side and low-power-consumption on the other side. The LSE drive can be decreased to the lower drive capability (LSEDRV=00) when the LSE is ON. However, once LSEDRV is selected, the drive capability can not be increased if LSEON=1.

The LSERDY flag in the RTC domain control register (RCC_BDCR) indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the clock interrupt enable register (RCC_CIER).

External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. This mode is selected by setting the LSEBYP and LSEON bits in the AHB peripheral clock enable in Sleep/Stop mode register (RCC_AHBSMENR). The external clock signal (square, sinus or triangle) with ~50% duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO. See Figure 6. Clock tree.

2.5 LSI clock

The LSI RC acts as a low-power clock source that can be kept running in Stop and Standby mode for the independent watchdog (IWDG) and RTC. The clock frequency is 32 kHz. For more details, refer to the electrical characteristics section of the datasheets.

The LSI RC can be switched on and off using the LSION bit in the control/status register (RCC_CSR).

The LSIRDY flag in the control/status register (RCC_CSR) indicates if the LSI oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the clock interrupt enable register (RCC_CIER).

2.6 System clock (SYSCLK) selection

One of the following clocks can be selected as system clock (SYSCLK):

- LSI
- LSE
- HSISYS
- HSE
- PLLRCLK

The system clock maximum frequency is 64 MHz. Upon system reset, the HSISYS clock derived from HSI16 oscillator is selected as system clock. When a clock source is used directly or through the PLL as a system clock, it is not possible to stop it.

A switch from one clock source to another occurs only if the target clock source is ready (clock stable after startup delay or PLL locked). If a clock source which is not yet ready is selected, the switch occurs when the clock source becomes ready. Status bits in the internal clock sources calibration register (RCC_ICSCR) indicate which clock(s) is (are) ready and which clock is currently used as a system clock.

2.7 Clock source frequency versus voltage scaling

The following table gives the different clock source frequencies depending on the product voltage range.

Table 2. Clock source frequency

Clock	Maximum clock frequency (MHz)	
	Range 1	Range 2
HSI16	16	16
HSE	48	16
PLLPCLK	122(1)	40(2)
PLLQCLK	128(1)	32(2)
PLLRCLK	64(1)	16(2)

1. *Maximum VCO frequency is 344 MHz.*
2. *Maximum VCO frequency is 128 MHz.*

2.8 Clock security system (CSS)

Clock security system can be activated by software. In this case, the clock detector is enabled after the HSE oscillator startup delay, and disabled when this oscillator is stopped.

If a failure is detected on the HSE clock:

- the HSE oscillator is automatically disabled
- a clock failure event is sent to the break input of TIM1, TIM15, TIM16 and TIM17 timers
- CSSI (clock security system interrupt) is generated

The CSSI is linked to the Cortex®-M0+ NMI (non-maskable interrupt) exception vector. It makes the software aware of a HSE clock failure to allow it to perform rescue operations.

Note: If the CSS is enabled and the HSE clock fails, the CSSI occurs and an NMI is automatically generated. The NMI is executed infinitely unless the CSS interrupt pending bit is cleared. It is therefore necessary that the NMI ISR clears the CSSI by setting the CSSC bit in the clock interrupt clear register (RCC_CICR).

If HSE is selected directly or indirectly (PLLRCLK selected for SYSCLK and HSE selected as PLL input) as system clock, and a failure of HSE clock is detected, the system clock switches automatically to HSISYS and the HSE oscillator is disabled. If the HSE clock (divided or not) is the clock entry of the PLL and PLLRCLK is used as system clock when the failure occurs, the PLL is disabled too.

2.9 Clock security system for LSE clock (LSECSS)

A clock security system on LSE can be activated by setting the LSECSSON bit in RTC domain control register (RCC_BDCR). This bit can be cleared only by a hardware reset or RTC software reset, or after LSE clock failure detection. LSECSSON must be written after LSE and LSI are enabled (LSEON and LSION enabled) and ready (LSERDY and LSIRDY flags set by hardware), and after selecting the RTC clock by RTCSEL.

The LSECSS works in all modes except VBAT. It keeps working also under system reset (excluding power-on reset). If a failure is detected on the LSE oscillator, the LSE clock is no longer supplied to the RTC but its registers are not impacted.

Note: If the LSECSS is enabled and the LSE clock fails, the LSECSSI occurs and an NMI is automatically generated. The NMI is executed infinitely unless the LSECSS interrupt pending bit is cleared. It is therefore necessary that the NMI ISR clears the LSECSSI by setting the LSECSSC bit in the clock interrupt clear register (RCC_CICR).

If LSE is used as system clock, and a failure of LSE clock is detected, the system clock switches automatically to LSI. In low-power modes, an LSE clock failure generates a wakeup. The interrupt flag must then be cleared within the RCC registers.

The software **must** then disable the LSECSSON bit, stop the defective 32 kHz oscillator (by clearing LSEON), and change the RTC clock source (no clock, LSI or HSE, with RTCSEL), or take any appropriate action to secure the application.

The frequency of the LSE oscillator must exceed 30 kHz to avoid false positive detections.

2.10 ADC clock

The ADC clock is derived from the system clock, or from the PLLPCLK output. It can reach 122 MHz and can be divided by the following prescalers values: 1,2,4,6,8,10,12,16,32,64,128 or 256 by configuring the ADC1_CCR register. It is asynchronous to the AHB clock. Alternatively, the ADC clock can be derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2 or 4). This programmable factor is configured using the CKMODE bit fields in the ADC1_CCR.

If the programmed factor is 1, the AHB prescaler must be set to 1.

2.11 RTC clock

The RTCCLK clock source can be either the HSE/32, LSE or LSI clock. It is selected by programming the RTCSEL[1:0] bits in the RTC domain control register (RCC_BDCR). This selection cannot be modified without resetting the RTC domain. The system must always be configured so as to get a PCLK frequency greater then or equal to the RTCCLK frequency for a proper operation of the RTC.

The LSE clock is in the RTC domain, whereas the HSE and LSI clocks are not. Consequently:

- If LSE is selected as RTC clock:
  - The RTC continues to work even if the V_{DD} supply is switched off, provided the V_{BAT} supply is maintained.
- If LSI is selected as the RTC clock:
  - The RTC state is not guaranteed if the V_{DD} supply is powered off.
- If the HSE clock divided by a prescaler is used as the RTC clock:
  - The RTC state is not guaranteed if the V_{DD} supply is powered off or if the internal voltage regulator is powered off (removing power from the V_{CORE} domain).

When the RTC clock is LSE or LSI, the RTC remains clocked and functional under system reset.

2.12 Timer clock

The timer clock TIMPCLK is derived from PCLK (used for APB) as follows:

- If the APB prescaler is set to 1, TIMPCLK frequency is equal to PCLK frequency.
- Otherwise, the TIMPCLK frequency is set to twice the PCLK frequency.

For TIM1 and TIM15, PLLQCLK clock can also be selected. Its frequency must be set so as not to exceed 128 MHz.

2.13 Watchdog clock

If the Independent watchdog (IWDG) is started by either hardware option or software access, the LSI oscillator is forced ON and cannot be disabled. After the LSI oscillator temporization, the clock is provided to the IWDG.

2.14 Clock-out capability

MCO

The microcontroller clock output (MCO) capability allows the clock to be output onto the external MCO pin. One of the following can be selected as the MCO clock:

- LSI
- LSE
- SYSCLK
- HSI16
- HSE
- PLLRCLK

The selection is controlled by the MCOSEL[3:0] bits of the clock configuration register (RCC_CFGR). The selected clock can be divided with a factor programmable through the MCOPRE[2:0] field of clock configuration register (RCC_CFGR).

LSCO

The LSCO pin allows outputting on of low-speed clocks:

- LSI
- LSE

The selection is controlled by the LSCOSEL, and enabled with the LSCOEN in the RTC domain control register (RCC_BDCR). The configuration registers of the corresponding GPIO port must be programmed in alternate function mode.

This function remains available in Stop 0, Stop 1 and Standby modes.

2.15 Internal/external clock measurement with TIM14/TIM16/TIM17

It is possible to indirectly measure the frequency of all on-board clock sources with the TIM14, TIM16 and TIM17 channel 1 input capture, as represented in the figures below in each of the corresponding subsection.

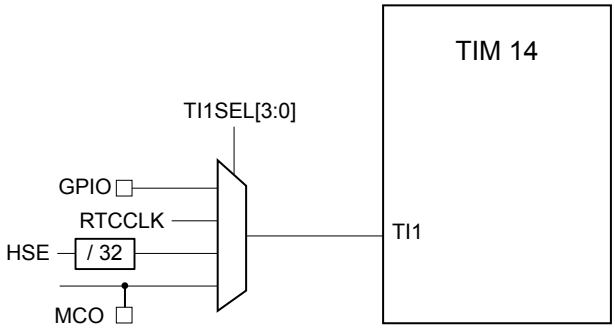
TIM14

By setting the TI1SEL[3:0] field of the TIM14_TISEL register, the clock selected for the input capture channel1 of TIM14 can be one of the following:

- GPIO (refer to the alternate function mapping in the device datasheets)
- RTC clock (RTCCLK)
- HSE clock divided by 32
- MCO (MCU clock output)

The last option is controlled by the MCOSEL[3:0] field of the clock configuration register (RCC_CFGR). All clock sources can be selected for the MCO pin.

Figure 8. Frequency measurement with TIM14 in capture mode



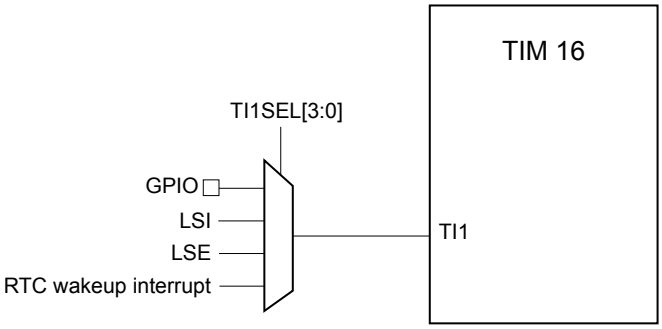
TIM16

By setting the TI1SEL[3:0] field of the TIM16_TISEL register, the clock selected for the input capture channel1 of TIM16 can be one of the following:

- GPIO (efer to the alternate function mapping in the device datasheets)
- LSI clock
- LSE clock
- RTC wakeup interrupt signal

The last option requires to enable the RTC interrupt.

Figure 9. Frequency measurement with TIM16 in capture mode



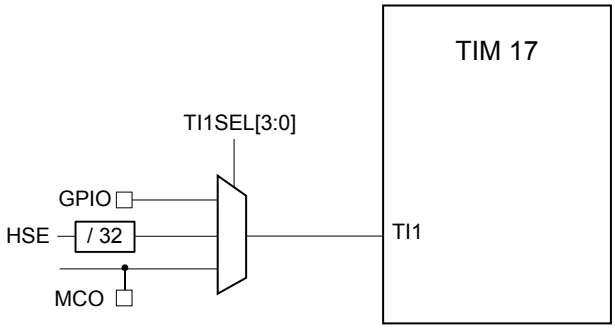
TIM17

By setting the TI1SEL[3:0] field of the TIM17_TISEL register, the clock selected for the input capture channel1 of TIM17 can be one of the following:

- GPIO (refer to the alternate function mapping in the device datasheets)
- HSE divided by 32
- MCO (MCU clock output)

The last option is controlled by the MCOSEL[3:0] field of the clock configuration register (RCC_CFGR). All clock sources can be selected for the MCO pin.

Figure 10. **Frequency measurement with TIM17 in capture mode**



Calibration of the HSI16 oscillator

For TIM14, TIM15 and TIM17, the primary purpose of connecting the LSE to the channel 1 input capture is to be able to precisely measure the HSISYS clock (derived from HSI16) selected as system clock. Counting HSISYS clock pulses between consecutive edges of the LSE clock (the time reference) allows measuring the HSISYS (and HSI16) clock period. Such measurement can determine the HSI16 oscillator frequency with nearly the same accuracy as the accuracy of the 32.768 kHz quartz crystal used with the LSE oscillator (typically a few tens of ppm). The HSI16 oscillator can then be trimmed to compensate for deviations from target frequency, due to manufacturing, process, temperature and/or voltage variation.

The HSI16 oscillator has dedicated user-accessible calibration bits for this purpose.

The basic concept consists in providing a relative measurement (for example, the HSISYS/LSE ratio): the measurement accuracy is therefore closely related to the ratio between the two clock sources. Increasing the ratio allows improving the measurement accuracy.

Generated by the HSE oscillator, the HSE clock (divided by 32) used as time reference is the second best method for reaching a good HSI16 frequency measurement accuracy. It is recommended in absence of the LSE clock.

In order to further improve the precision of the HSI16 oscillator calibration, it is advised to employ one or a combination of the following measures to increase the frequency measurement accuracy:

- set the HSISYS divider to 1 for HSISYS frequency to be equal to HSI16 frequency
- average the results of multiple consecutive measurements
- use the input capture prescaler of the timer (1 capture every up to 8 periods)
- use LSE clock for the RTC and the RTC wakeup interrupt signal as time reference

The last point significantly increases the reference period for HSI16 clock pulse counting, which improves the accuracy of a single measurement. For operation, the RTC wakeup interrupt must be enabled.

Calibration of the LSI oscillator

The calibration of the LSI oscillator uses the same principle as that for calibrating the HSI16 oscillator. TIM16 channel1 input capture must be used for LSI clock, and HSE selected as system clock source. The number of HSE clock pulses between consecutive edges of the LSI signal, counted by TIM16, is then representative of the LSI clock period.

2.16 Peripheral clock enable registers

Each peripheral clock can be enabled by the corresponding enable bit of the RCC_AHBENR or RCC_APBENRx registers.

When the peripheral clock is not active, the peripheral registers read or write accesses are not supported.

Note: The enable bit has a synchronization mechanism to create a glitch-free clock for the peripheral. After the enable bit is set, there is a 2-clock-cycle delay before the clock be active, which the software must take into account.

3 Boot configuration

In the STM32G0 Series, three different boot modes can be selected through the BOOT0 pin, BOOT_LOCK bit in FLASH_SECR register, and boot configuration bits nBOOT1, BOOT_SEL and nBOOT0 in the user option byte, as shown in the following table.

Table 3. Boot modes

Boot mode configuration					Selected boot area
BOOT_LOCK bit	nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit	nBOOT0 bit	
0	X	0	0	X	Main Flash memory
0	1	1	0	X	System memory
0	0	1	0	X	Embbeded SRAM
0	X	X	1	1	Main Flash memory
0	1	X	1	0	System memory
0	0	X	1	0	Embedded SRAM
1	X	X	X	X	Main Flash memory forced

The boot mode configuration is latched on the 4th rising edge of SYSCLK after a reset. It is up to the user to set boot mode configuration related to the required boot mode.

The boot mode configuration is also re-sampled when exiting from Standby mode. Consequently they must be kept in the required Boot mode configuration in Standby mode.

After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.

Depending on the selected boot mode, main Flash memory, system memory or SRAM is accessible as follows:

- Boot from main Flash memory: the main Flash memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space (0x0800 0000). In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from system memory: the system memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space 0x1FFF0000.
- Boot from the embedded SRAM: the SRAM is aliased in the boot memory space (0x0000 0000), but it is still accessible from its original memory space (0x2000 0000).

Forcing boot from user Flash memory

The BOOT_LOCK bit allows forcing a unique entry point in the main Flash memory for boot, regardless of the other boot mode configuration bits.

Empty check

Internal empty check flag (the EMPTY bit of the FLASH access control register (FLASH_ACR)) is implemented to allow easy programming of virgin devices by the boot loader. This flag is used when BOOT0 pin is defining Main Flash memory as the target boot area. When the flag is set, the device is considered as empty and System memory (boot loader) is selected instead of the Main Flash as a boot area to allow user to program the Flash memory.

This flag is updated only during Option bytes loading: it is set when the content of the address 0x08000 0000 is read as 0xFFFF FFFF, otherwise it is cleared. It means a power reset or setting of OBL_LAUNCH bit in FLASH_CR register is needed to clear this flag after programming of a virgin device to execute user code after System reset. The EMPTY bit can also directly be written by software.

Note: If the device is programmed for a first time but the Option bytes are not reloaded, the device still selects System memory as a boot area after a System reset.

Physical remap

Once the boot mode is selected, the application software can modify the memory accessible in the code area. This modification is performed by programming the MEM_MODE bits in the SYSCFG configuration register 1 (SYSCFG_CFGR1).

Embedded boot loader

The embedded boot loader is located in the System memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

- USART on pins PA2/PA3, PA9/PA10 or PC10/PC11
- I2C on pins PB6/PB7 or PB10/PB11
- SPI on pins PA4/PA5/PA6/PA7 or PB12/PB13/PB14/PB15

For further details, refer to application note *STM32 microcontroller system memory boot mode* (AN2606).

4 Debug management

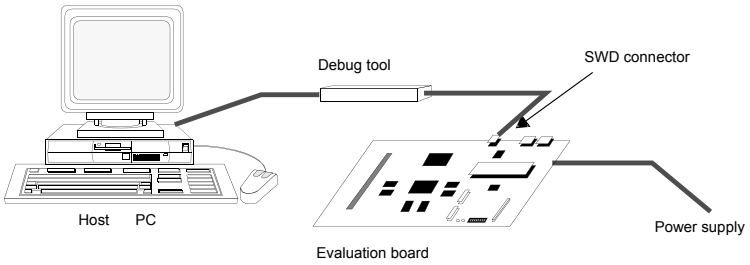
4.1 Debug management introduction

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, an SWD connector and a cable connecting the host to the debug tool.

The figure below shows the connection of the host to the evaluation board (STM32G081B_EVAL).

The STM32G081B_EVAL evaluation board embeds the debug tools (ST-LINK). Consequently, it can be directly connected to the PC through a USB cable.

Figure 11. Host-to-board connection



4.2 SWD port (serial wire debug)

The STM32G0 Series core integrates the serial wire debug port (SW-DP). It is an ARM® standard CoreSight™ debug port with a 2-pin (clock + data) interface to the debug access port.

4.3 Pinout and debug port pins

The STM32G0 Series devices are offered in various packages with varying numbers of available pins.

4.3.1 Serial wire debug (SWD) pin assignment

The same SWD pin assignment is available on all STM32G0 Series packages.

Table 4. SWD port pins

SWD pin name	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	serial wire clock	PA14

After reset (SYSRESETn or PORESETn), the pins used for the SWD are assigned as dedicated pins which are immediately usable by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for general-purpose I/O (GPIO) usage. For more details on how to disable SWD port, refer to the RM0444 section on I/O pin alternate function multiplexer and mapping.

4.3.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of these pins. The reset states of the GPIO control registers put the I/Os in the equivalent states:

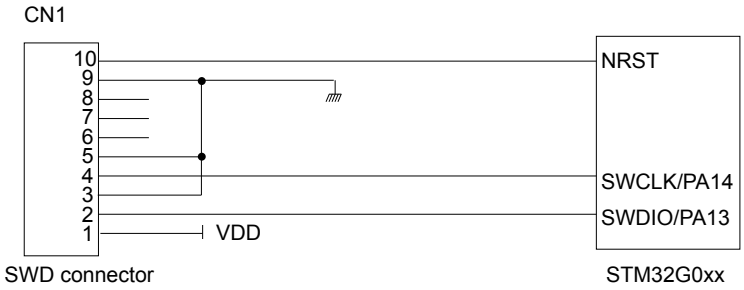
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

4.3.3 SWD port connection with standard SWD connector

Below figure shows the connection between the STM32G0 Series device and a standard SWD connector.

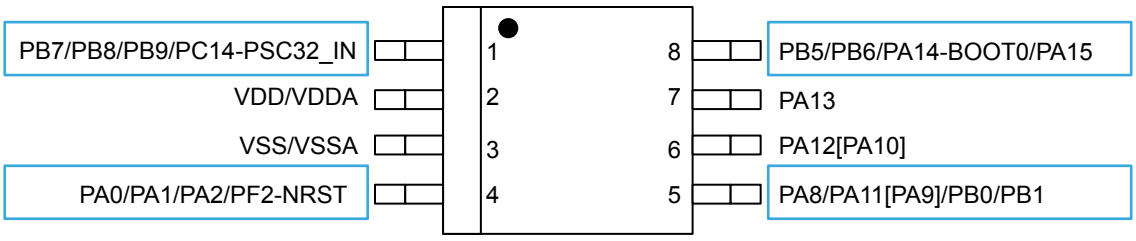
Figure 12. SWD port connection



4.3.4 Multi bonding on STM32G03xxx and STM32G04xxx small packages

A multi-bonding approach is used on the small packages in order to offer a maximum of alternate functions and analog inputs. This approach results in multiple die pads connected internally to a single package pin. See an example on the figure below.

Figure 13. Multi bonding example in small packages



The above figure shows that there are four device pad bonded to each of the pins 1, 4, 5 and 8 . Taking pin 1 as a concrete example; this multi bonding means that for this pin, each of the alternate functions (PB7, PB8, PB9 or PC14) are accessible on this pin if they are respectively configured at I/O port level.

The configuration state of each device pad must be done carefully as there are not any design protections present to avoid interferences from one pad to the other. By default, all GPIOs (except PA14 in this example) are configured in analog input; this must be taken into consideration before modifying the analog input configuration for another configuration state.

The multi bonding approach offers not only more versatility for the configuration of the product, but also offers an extended drive strength on the multi bonded pads. By configuring multiple devices pad in output mode (with the same output level), the transistor drive resistance is decreased and consequently the voltage drop at the device pin (Vol and Voh) is reduced. The transition from high to low level must be done with caution to guarantee that no short circuit are produced between the internal die pads.

5 Recommendations

5.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

5.2 Component position

A preliminary layout of the PCB must make separate circuits:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution. This reduces cross-coupling on the PCB that introduces noise.

5.3 Ground and power supply (V_{DD})

Every block (noisy, low-level sensitive or digital) should be grounded individually and all ground returns should be to a single point. Loops must be avoided or they should have a minimum area. In order to improve analog performance, the decoupling capacitors must be placed as close as possible to the device.

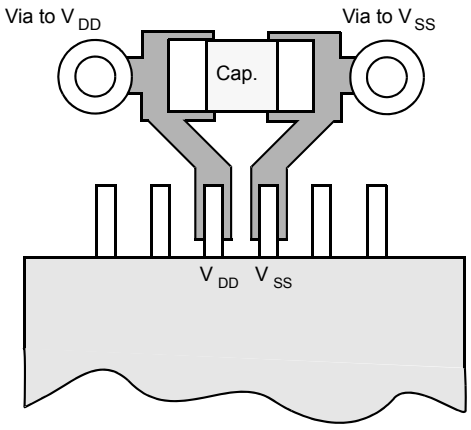
The power supply should be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and is therefore the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a shield (especially when using single-layer PCBs).

5.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections, including pads, tracks and vias should have as low an impedance as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, a power supply pair should be decoupled with 100 nF filtering ceramic capacitor and a chemical capacitor of about 4.7 µF connected between the supply pin of the STM32G0 Series device. These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. The figure below shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 14. Typical layout for VDD/VSS pair



5.5 Other signals

When designing an application, the EMC performance can be improved by closely studying:

- Signals for which a temporary disturbance affects the running process permanently (such as interrupts and handshaking strobe signals, but not LED commands). For these signals, a surrounding ground trace, shorter lengths and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
- Digital signals: the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (such as clock)
- Sensitive signals (such as high impedance)

5.6 Unused I/O and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

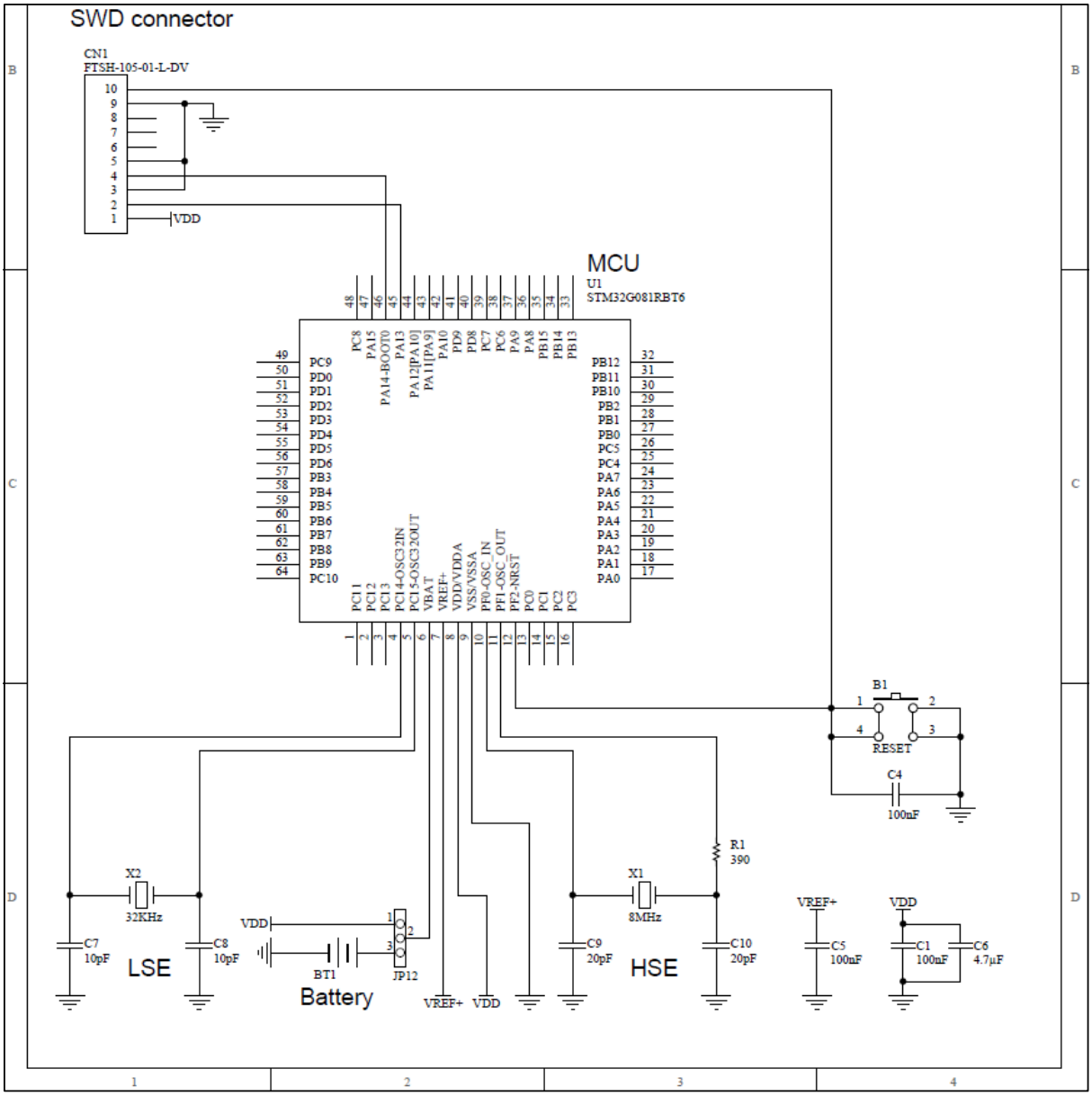
To increase EMC performance and avoid extra power consumption, unused clocks, counters or I/Os, should not be left free. I/Os should be connected to a fixed logic level of 0 or 1 by an external or internal pull-up or pull-down on the unused I/O pin. The other option is to configure GPIO as output mode using software. Unused features should be frozen or disabled, which is their default value.

6 Reference design

6.1 Description of reference design

The reference design shown in the figure below, introduces the STM32G081, a highly integrated microcontroller running at 64 MHz, that combines the Cortex®-M0+ 32-bit RISC CPU core with 128 Kbytes of embedded Flash memory and 36 Kbytes of SRAM.

Figure 15. STM32G0 Series reference schematic



Note: If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD}.

6.1.1 Clock

Two clock sources are used for the microcontroller:

- HSE: X1– 8 MHz crystal for the microcontroller
- LSE: X2– 32.768 kHz crystal for the embedded RTC

Refer to Section 2 Clocks.

6.1.2 Reset

The reset signal in Figure 15. STM32G0 Series reference schematic is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to Section 1.3 Reset on STM32G0 Series.

Note: By default the reset holder is activated on STM32G0 Series devices. Any internal reset results in pulling down NRST pin until it reaches its V_{IL} threshold, therefore giving the guarantee that capacity on this line is fully discharged.

6.1.3 Boot mode

The boot option is configured by default through option bytes. BOOT0 pin can be used if user want to have a physical control on boot entry point after reprogramming the option byte.

6.1.4 SWD interface

The reference design shows the connection between the STM32G0 Series device and a standard SWD connector. Refer to Section 4 Debug management.

Note: It is recommended to connect the reset pin in order to be able to reset the application from the tool.

6.1.5 Power supply

Refer to Section 1.1 Power supplies on STM32G0 Series.

6.1.6 Pinouts and pin description

Refer to the STM32G0 Series datasheets available at for the pinout information and pin description of each device.

6.2 Component references

Table 5. Mandatory components

Component	Reference	Value	Quantity	Comments
Microcontroller	U1	STM32G081RBT6	1	64-pin package
Capacitor	C1	100 nF	1	Ceramic capacitors (decoupling capacitors)
Capacitor	C6	4.7 µF	1	Used for VDD

Table 6. Optional components

Component	Reference	Value	Quantity	Comments
Resistor	R1	390 Ω	1	Used for HSE: the value depends on the crystal characteristics. This value is given only as a typical example
Capacitor	C4	100 nF	1	Ceramic capacitor for RESET button
Capacitor	C5	100 nF	1	Ceramic capacitor (decoupling capacitor)
Capacitor	C7/C8	10 pF	2	Used for LSE: the value depends on the crystal characteristics
Capacitor	C9/C10	20 pF	2	Used for HSE: the value depends on the crystal characteristics
Quartz	X1	8 MHz	1	Used for HSE
Quartz	X2	32 kHz	1	Used for LSE
Battery	BT1	3 V	1	If no external battery is used in the application, it is recommended to connect VBAT externally to VDD
Push-button	B1	-	1	Used as reset button
SWD connector	CN1	FTSH-105-01-L-DV	1	Used for program/debug of the MCU

Revision history

Table 7. **Document revision history**

Date	Version	Changes
07-Nov-2018	1	Initial release.
15-Jul-2019	2	Added Section 4.3.4 Multi bonding on STM32G03xxx and STM32G04xxx small packages

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