Migrating from STM32L4 and STM32L4+ to STM32L5 Series microcontrollers

Introduction

Designers of STM32 microcontroller applications must be able to easily replace one microcontroller type by another in the same product family or products from a different family.

Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate from an existing design based on the STM32L4 or STM32L4+ Series, to an application using the STM32L5 Series.

This document lists the full set of features available for the STM32L4 and STM32L4+ Series, and the equivalent features on the STM32L5 Series, and provides a guideline on both hardware and peripheral migration.

To fully benefit from this application note, the user must be familiar with the STM32 microcontroller family. For additional information, refer to the product datasheets and reference manuals.

AN5138 - Rev 2 - July 2020
For further information contact your local STMicroelectronics sales office.

www.st.com

1 STM32L5 Series overview

The STM32L5 devices reuse the STM32L4 and STM32L4+ Series technology, achieving excellence in ultra-low-power with more security.

The STM32L5 devices enhance efficiency and performance with up to 512 Kbytes of Flash memory and up to 256 Kbytes of RAM. These devices provide improved security features thanks to the ultra-low-power Arm® Cortex®-M33 32-bit core, with TrustZone® for Armv8-M, and to the ST instruction cache (ICACHE) that supports both internal and external memories.

The STM32L5 devices include a larger set of peripherals with more advanced features compared to the STM32L4 and STM32L4+ Series, such as the ones listed below:

- Security
    - TrustZone-aware and securable peripherals
    - RDP, active tamper, secure firmware upgrade support, secure hide protection
    - Up to eight configurable SAU regions
    - Octo-SPI memory encryption
    - Additional encryption accelerator engine (available only on STM32L562xx devices)
        - Advanced encryption hardware accelerator (AES)
        - Public key accelerator (PKA)
        - On-the-fly decryption engine on OCTOSPI (OTFDEC)
- Power consumption
    - Embedded regulator (LDO) with three configurable range outputs to supply the digital circuitry
    - SMPS step-down converter
    - External SMPS support
    - Optimized RTC consumption
- Performance
    - Cache for external memory
- New peripherals
    - USB Type-C™ connector/USB power delivery interface (UCPD)
    - FDCAN

Note: *This document only manages the differences between the STM32L4, STM32L4+ and STM32L5 Series for the common features. The new features in the STM32L5 Series, mainly linked to the TrustZone support, are not covered.*

The detailed list of available features and packages for each product is available in the respective product datasheet.

The table below summarizes the memory availability of the STM32L5 Series.

Table 1. Memory availability on STM32L5 Series

Products	Flash memory		RAM size (Kbytes)		Feature level
	Size (Kbytes)	Bank	SRAM1	SRAM2	
STM32L552xx	256/512	Dual	192	64	Without AES, PKA and OTFDEC
STM32L562xx	512				With AES, PKA, and OTFDEC

The STM32L4, STM32L4+ and STM32L5 Series are Arm®-based devices.

Note: *Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.*

arm

1.1 System architecture differences between STM32L4, STM32L4+ and STM32L5

The STM32L5 devices embed high-speed memories (512-Kbyte Flash memory and 256-Kbyte SRAM), a flexible external memory controller (FSMC) for static memories (for devices with packages of 100 pins and more), an Octo-SPI Flash memory interface (available on all packages), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

The following table illustrates the bus matrix differences between the STM32L4, STM32L4+ and STM32L5 Series.

Table 2. Bus matrix on STM32L4, STM32L4+ and STM32L5 Series

Bus type	STM32L4 Series	STM32L4+ Series	STM32L5 Series
AHB bus matrix masters	Five masters: CPU AHB, system, D-Code, I-Code, DMA1 and DMA2[1]	Up to nine masters: CPU AHB, system, D-Code, I-Code, DMA1 and DMA2, DMA2D, LCD-TFT controller DMA, SDMMC1, GFXMMU	Up to six masters: S-bus, Fast C-bus, Slow C-bus, DMA1 and DMA2, SDMMC1
AHB bus matrix slaves	Up to eight slaves: Internal Flash memory (on I-Code and D-Code bus), SRAM1, SRAM2, AHB1 (including APB1 and APB2), AHB2, FMC and QUADSPI	Up to eleven slaves: Internal Flash memory (on I-Code and D-Code bus), SRAM1, SRAM2, SRAM3, GFXMMU, AHB1 (including APB1 and APB2), AHB2, OCTOSPI1, OCTOSPI2 and FSMC	Up to seven slaves: Internal Flash memory, SRAM1, SRAM2, AHB1 (including APB1 and APB2), AHB2, OCTOSPI1 and FSMC

1. *Up to six masters with DMA2D only for STM32L496/4A6xx devices.*

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

The system architecture of the STM32L4, STM32L4+ and STM32L5 Series is shown in the figures below.

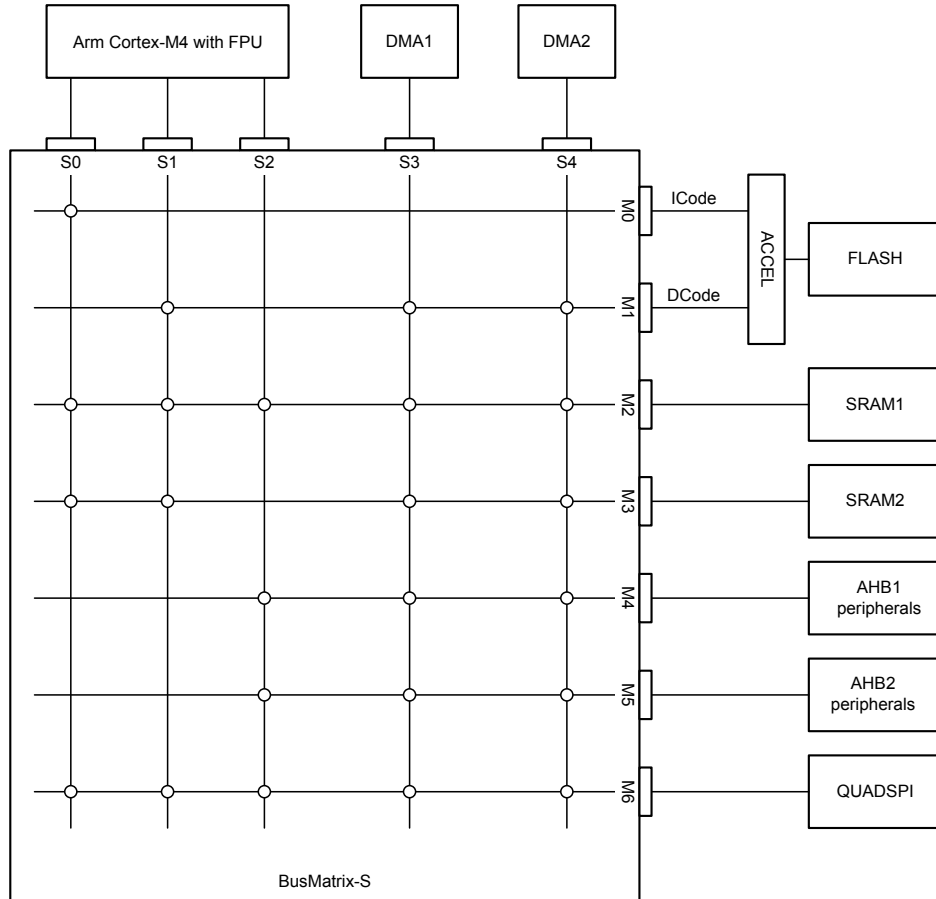**Figure 1. STM32L4 Series system architecture**
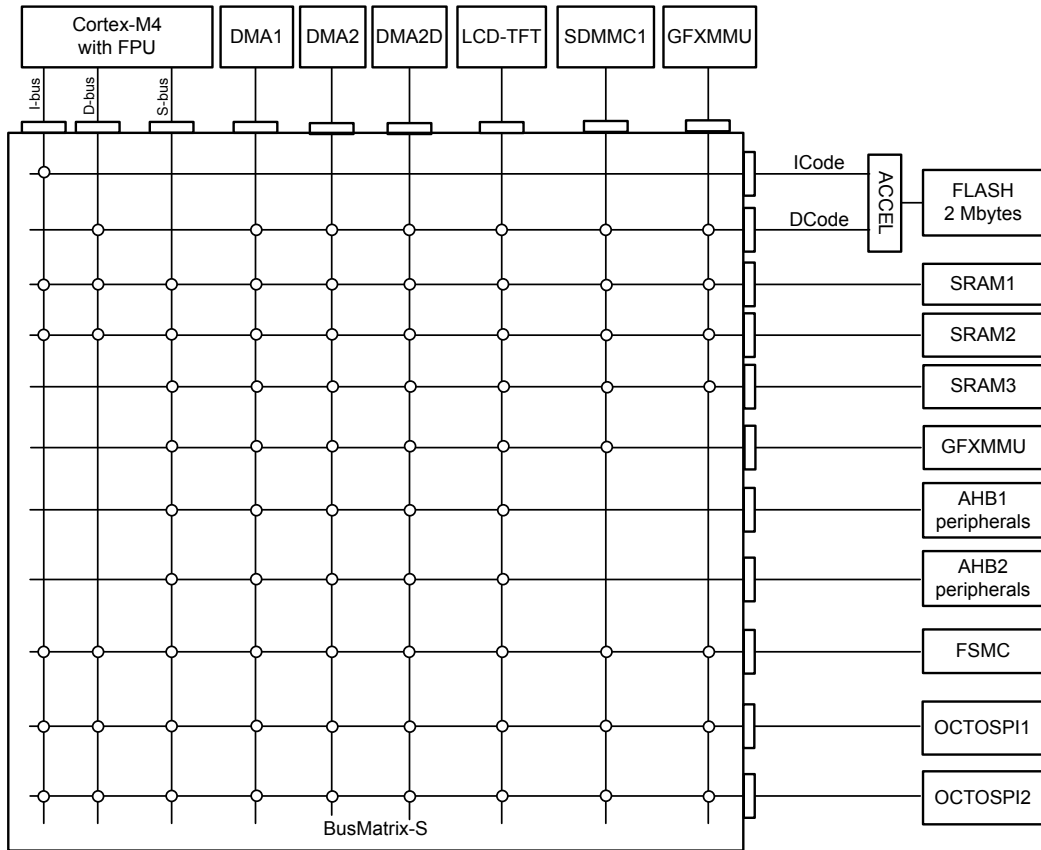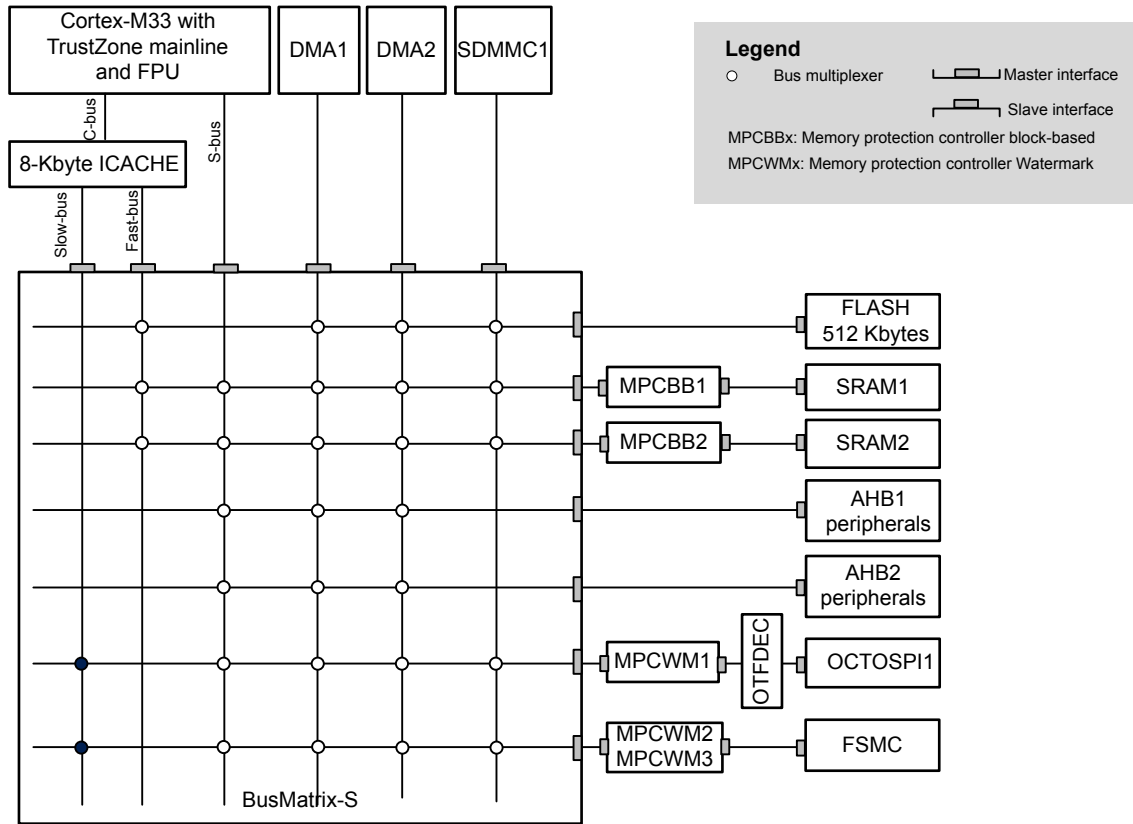
Figure 2. STM32L4+ Series system architecture

Figure 3. STM32L5 Series system architecture

When remapped by ICACHE

2 Hardware migration

2.1 Package availability

The STM32L5 devices offer seven packages from 48 to 144 pins, and three versions of pinout:

- without internal SMPS: fully compatible with the STM32L4 and STM32L4+ Series
- with internal SMPS: fully new packages that are not compatible with the STM32L4 and STM32L4+ Series
- with external SMPS: fully compatible with the STM32L4 and STM32L4+ Series (possible to externally supply the core voltage)

For the STM32L5 Series, the SMPS step-down converter and the external SMPS are available only on the following specific products (for more details on the pinout refer to the product datasheets.):

- STM32L5xxxxxQ = dedicated pinout supporting the SMPS step-down converter
- STM32L5xxxxxP = dedicated pinout supporting the external SMPS

The table below lists the available packages on the STM32L5 Series compared to the STM32L4 and STM32L4+ Series, as well as their compatibility.

Table 3. Packages available on STM32L4, STM32L4+ and STM32L5 Series

Package[1] (Size in mm x mm)	STM32L4 Series[2]	STM32L4+ Series[2]	STM32L5 Series (all except STM32L5xxxxxQ)[2]	STM32L5 Series (all except STM32L5xxxxxQ) compared to STM32L4/L4+ Series	STM32L5xxxxxQ (supporting SMPS step-down converter)
LQFP144 (20 x 20)	X[3]	X	X[4]	Compatible	
LQFP100 (14 x 14)	X[5]	X	X[4]	Compatible	
LQFP64 (10 x 10)	X	NA	X	Compatible	
UFBGA132 (7 x 7)	X[3]	X	X[4]	Not compatible	New pinout/ballout
WLCSP81 (4.36 x 4.07)[6]	X[7]	NA	X[8]	New ballout	
LQFP48 (7 x 7)[9][10]	X	NA	X	Not compatible	
UFQFPN48 (7 x 7)[10][11]	X	NA	X	Not compatible	

1. For more details about the available packages for STM32L4 and STM32L4+, refer to product datasheet.

2. X = available. NA = not available.

3. Available only for STM32L47/48/49/4Axxx devices.

4. Not available on STM32L5xxxxxP devices.

5. Not available for STM32L41/42xxx devices.

6. Size 4.4084 x 3.7594 for STM32L4 Series instead of 4.36 x 4.07 mm for STM32L5 Series.

7. Available only for STM32L476xx devices.

8. Available only STM32L5xxxxxP/Q devices.

9. Not available for STM32L45/46/47/48/49/4Axxx devices.

10. PIN 36 is a VDDUSB on STM32L4 Series and it is a VDD on STM32L5 Series.

11. Not available for STM32L47/48/49/4Axxx devices.

2.2 Pinout compatibility

The STM32L5 devices without embedded SMPS are pin-to-pin compatible with the STM32L4 and STM32L4+ devices.

Some devices of the STM32L4, STM32L4+ and STM32L5 Series offer a package option that allows the connection of an external SMPS. This is done through two VDD12 pins (only available on packages with the external SMPS supply option), that replace two existing pins in the package baseline.

The compatibility is kept between the STM32L4/L4+ and STM32L5 Series regarding those two pins: the pins replaced are different across the package types but are the same for all the derivatives on similar packages. Refer to the product datasheet for more details.

3 Boot mode compatibility

3.1 Boot mode selection

For the STM32L5 devices, the boot mode is selected with the BOOT0 pin or the nBOOT0 option bit, depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register.

In the STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx devices, the boot mode is selected with the nBOOT1 option bit and the BOOT0 pin or nBOOT0 option bit, depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register (see Table 6).

In the STM32L47/48xxx devices, the boot mode is selected with one BOOT0 pin and the nBOOT1 option bit located in the user option bytes, at memory address 0x1FFF 7800 (see Table 7).

The tables below detail the STM32L4, STM32L4+ and STM32L5 Series boot modes.

Table 4. Boot modes for STM32L5 Series when TrustZone is disabled (TZEN = 0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option byte selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Secure boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
-	1	1	NSBOOTADD1[24:0]	Secure boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000
1	-	0	NSBOOTADD0[24:0]	Secure boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Secure boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

Table 5. Boot modes for STM32L5 Series when TrustZone is enabled (TZEN = 1)

BOOT-LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address Option Byte selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash : 0x0C00 0000
	-	1	1		NA	RSS: 0x0FF8 0000	
	1	-	0	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash : 0x0C00 0000
	0	-	0	0	NA	RSS: 0x0FF8 0000	
	-	-	-	≠0	NA		
1	-	-	-	-	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash : 0x0C00 0000

Table 6. Boot modes for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx devices

nBOOT1 FLASH_OPTR[23] [1]	nBOOT0 FLASH_OPTR [27][1]	BOOT0 pin PH3[1]	nSWBOOT0 FLASH_OPTR [26][1]	Main Flash empty [1][2]	Boot memory space alias
X	X	0	1	0	Main Flash memory selected as boot area
X	X	0	1	1	System memory selected as boot area
X	1	X	0	X	Main Flash memory selected as boot area
0	X	1	1	X	Embedded SRAM1 selected as boot area
0	0	X	0	X	Embedded SRAM1 selected as boot area
1	X	1	1	X	System memory selected as boot area
1	0	X	0	X	System memory selected as boot area

1. X = equivalent to 0 or 1.
2. For STM32L41/42/43/44/45/46xxx devices, a Flash memory empty check mechanism is implemented to force the boot from system Flash memory if the first Flash memory location is not programmed (0xFFFF FFFF), and if the boot selection was configured to boot from the main Flash memory.

Table 7. Boot modes for STM32L47/48xxx devices

Selected boot area	BOOT1[1][2]	BOOT0
Main Flash memory	X	0
System Flash memory	0	1
Embedded SRAM1	1	1

1. X = equivalent to 0 or 1.
2. The BOOT1 value is the opposite of the nBOOT1 option bit.

3.2 Embedded bootloader

The bootloader, located in the system memory and programmed by ST during production, is used to reprogram the Flash memory through one of the serial interfaces listed in the table below. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details.

Table 8. Bootloader interface on STM32L4, STM32L4+ and STM32L5 Series

Peripheral	Pin	STM32L4 and STM32L4+ Series	STM32L5 Series
DFU	USB_DM (PA11)	X	X
	USB_DP (PA12)	X	X
USART1	USART1_TX (PA9)	X	X
	USART1_RX (PA10)	X	X
USART2	USART2_TX (PA2)	X	X
	USART2_RX (PA3)	X	X
USART3	USART3_TX (PC10)	X	X
	USART3_RX (PC11)	X	X
I2C1	I2C1_SCL (PB6)	X	X
	I2C1_SDA (PB7)	X	X
I2C2	I2C2_SCL (PB10)	X	X
	I2C2_SDA (PB11)	X	X
I2C3	I2C3_SCL (PC0)	X	X
	I2C3_SDA (PC1)	X	X
I2C4	I2C4_SCL (PD12)	X[1]	NA
	I2C4_SDA (PD13)	X[1]	NA
SPI1	SPI1_NSS (PA4)	X	X
	SPI1_SCK (PA5)	X	X
	SPI1_MISO (PA6)	X	X
	SPI1_MOSI (PA7)	X	X
SPI2	SPI2_NSS (PB12)	X	X
	SPI2_SCK (PB13)	X	X
	SPI2_MISO (PB14)	X	X
	SPI2_MOSI (PB15)	X	X
SPI3	SPI3_NSS (PG12)	NA	X
	SPI3_SCK (PG9)	NA	X
	SPI3_MISO (PG10)	NA	X
	SPI3_MOSI (PB5)	NA	X
CAN1	CAN1_RX (PB8)	X[2]	X[3]
	CAN1_TX (PB9)	X[2]	X[3]
CAN2	CAN2_RX (PB5)	X[4]	NA
	CAN2_TX (PB6)	X[4]	NA

1. *Only for STM32L45/46/49/4Axxx devices.*
2. *Not available on STM32L41/42xxx devices.*
3. *FDCAN1 is available for STM32L5 Series.*
4. *Only for STM32L49/4Axxx devices.*

4 Peripheral migration

4.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals that can be classified in three groups:

- Peripherals that are by definition common to all products

  These peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.

- Peripherals that are shared by all products but have only minor differences (in general to support new features)

  The migration from one product to another is very easy and does not need any significant new development effort.

- Peripherals that have considerable changes from one product to another (new architecture or new features for example)

  For this group of peripherals, the migration requires a new development at application level.

For the STM32L5 devices, each GPIO or peripheral, DMA channel, clock configuration register, ICACHE or small part of Flash memory or SRAM, can be configured as trusted or untrusted.

The following table summarizes the available peripherals in the STM32L4 and STM32L4+ Series compared to the STM32L5 Series, as well as their compatibility.

Table 9. STM32 peripheral compatibility between STM32L4, STM32L4+ and STM32L5 Series

Peripherals		STM32L4 Series	STM32L4+ Series	STM32L5 Series
Core		Cortex-M4		Cortex -M33
Power supply		1.71 V to 3.6 V with VBAT		
Flash memory	Size	1 Mbytes	2 Mbytes	512 Kbytes
	Bank	Dual		Dual or Single TrustZone
Maximum CPU frequency		Up to 80 MHz	120 MHz	110 MHz
SRAM (Kbytes)	SRAM1	Up to 256	192	
	SRAM2	Up to 64	64	
	SRAM3	NA	384	NA
DMA		DMA request line is connected directly to peripherals	DMA request line is connected to peripherals through DMAMUX	
		2		2 + TrustZone
DMAMUX1		NA	Yes	Yes + TrustZone
DMA2D		NA[1]	Yes	NA
FSMC (external memory controller for static memory)		Yes		
QUADSPI		Yes	NA	
OCTOSPI		NA	2	1
LCD		Yes	NA	
SWPMI		Yes	NA	
LTDC		NA	Yes	NA
DCMI		NA[2]	Yes	NA
Timers	Advanced control	2 (16-bit)		

Peripherals		STM32L4 Series	STM32L4+ Series	STM32L5 Series
Timers	General purpose	5 (16-bit) and 2 (32-bit)		
	Basic	2 (16-bit)		
	Low power	2 (16-bit)		3 (16-bit)
	SysTick	1		1 when TrustZone disabled 2 when TrustZone enabled
	IWDG	1		
	WWDG	1		
Communication interfaces	SPI	3[3]	3	
	I2C	3[4]	4	
	USART	3		3[5]
	UART	2		
	LPUART	1		
	SAI	2		
	CAN	1		1 x FDCAN
	USB	OTG_FS without clock recovery[6]	OTG_FS with clock recovery	-
		USB FS[7]	NA	USB FS with clock recovery
	UCPD	NA		Yes
	SDMMC	Yes		
RTC		Yes		
GFXMMU		NA	Yes	NA
Tamper pins		Up to 3		
RNG		Yes		
GPIOs[8]		Up to 114	Up to 140	Up to 115
Wakeup pins		Up to 5		
Number of I/Os down to 1.08 V		Up to 14		
Capacitive sensing		Up to 24		22
DFSDM (digital filters for sigma-delta modulators)		Yes		
12-bit ADC	Instance	3[9]	1	2
	Number of channels	Up to 19		Up to 16
12-bit DAC		2		
Internal voltage reference buffer		Yes		
Analog comparator		2		
Operational amplifiers (OPAMP)		2[10]	2	
Operating voltage		1.71 to 3.6 V		
EXTI		Yes		
PWR		Yes		
SYSCFG		Yes		
DSI		NA	Yes	NA
HASH		Yes[11]		Yes

Peripherals	STM32L4 Series	STM32L4+ Series	STM32L5 Series
AES	Yes[12]	Yes	Yes[13]
PKA	NA		Yes [13]
On-the-fly decryption (OTFDEC)	NA		Yes [13]

1. *Available only on STM32L496xx/4A6xx devices.*
2. *Available only on STM32L496/4A6xx devices.*
3. *Two SPIs for STM32L41/42xxx devices.*
4. *Four I2C for STM32L496/4A6xx/462xx /452xx devices.*
5. *USART3 not available on STM32L562CExxP devices.*
6. *Available only on STM32L4x5/4x6 devices.*
7. *USB FS available only on STM32L4x2/4x3xx devices.*
8. *If external SMPS package is used for STM32L4/L4+, two GPIOs are replaced by VDD12 pins to connect the SMPS power supplies, hence reducing the number of available GPIOs by two.*
9. *Three instances on STM32L47/48/49/4Axxx, two instances on STM32L41/42xxx, and one instance on STM32L43/44/45/46xxx.*
10. *One OPAMP1 on STM32L41/42/43/44/45/46xxx devices.*
11. *Available only on STM32L4+ and STM32L496/4A6xx devices.*
12. *Not available on STM32L476/486xx devices.*
13. *Available only on STM32L562xx devices.*

4.2 Memory mapping

The peripheral address mapping has been changed in the STM32L5 Series compared to the STM32L4 and STM32L4+ Series. The table below presents the peripherals register boundary addresses for the STM32L5 Series compared to the STM32L4 and STM32L4+ Series (for more details on the memory mapping, refer to the STM32L4, STM32L4+ and STM32L5 documentation).

Table 10. Peripheral address mapping differences between STM32L4, STM32L4+ and STM32L5 Series

Peripheral	STM32L4 STM32L4+ bus	STM32L4/L4+ bus address	STM32L5 bus	STM32L5 Series	
				Secure boundary address	Non-secure boundary address
RNG (1 Kbyte)	AHB2	0x5006 0800 - 0x5006 0BFF	AHB2	0x520C 0800 - 0x520C 0BFF	0x420C 0800 - 0x420C 0BFF
HASH (1 Kbyte) [1]		0x5006 0400 - 0x5006 07FF		0x520C 0400 - 0x520C 07FF	0x420C 0400 - 0x420C 07FF
AES (1 Kbyte) [2]		0x5006 0000 - 0x5006 03FF		0x520C 0000 - 0x520C 03FF	0x420C 0000 - 0x420C 03FF
OCTOSPIM (1 Kbyte)		0x5006 1C00- 0x5006 1FFF		NA	
PSSI (1 Kbyte) [3]		0x5005 0400 - 0x5005 07FF		NA	
PKA (8 Kbytes) [3]		0x5005 E000 - 0x5005 FFFF		0x520C 2000 - 0x520C 3FFF	0x420C 2000 - 0x420C 3FFF
DCMI (1 Kbyte) [1]		0x5005 0000 - 0x5005 03FF		NA	
ADC (1 Kbyte)		0x5004 0000 - 0x5004 03FF		0x5202 8000 - 0x5202 83FF	0x4202 8000 - 0x4202 83FF
OTG_FS (256 Kbytes/ STM32L4) (16 Kbytes/ STM32L4+) [4]		0x5000 0000 - 0x5003 FFFF		NA	
GPIOI (1 Kbyte)		0x4800 2000 - 0x4800 23FF		NA	
GPIOH (1 Kbyte)		0x4800 1C00 - 0x4800 1FFF		0x5202 1C00 - 0x5202 1FFF	0x4202 1C00 - 0x4202 1FFF
GPIOG (1 Kbyte)		0x4800 1800 - 0x4800 1BFF		0x5202 1800 - 0x5202 1BFF	0x4202 1800 - 0x4202 1BFF
GPIOF (1 Kbyte)		0x4800 1400 - 0x4800 17FF		0x5202 1400 - 0x5202 17FF	0x4202 1400 - 0x4202 17FF
GPIOE (1 Kbyte) [5]		0x4800 1000 - 0x4800 13FF		0x5202 1000 - 0x5202 13FF	0x4202 1000 - 0x4202 13FF
GPIOD (1 Kbyte) [5]		0x4800 0C00 - 0x4800 0FFF		0x5202 0C00 - 0x5202 0FFF	0x4202 0C00 - 0x4202 0FFF
GPIOC (1 Kbyte)		0x4800 0800 - 0x4800 0BFF		0x5202 0800 - 0x5202 0BFF	0x4202 0800 - 0x4202 0BFF
GPIOB (1 Kbyte)		0x4800 0400 - 0x4800 07FF		0x5202 0400 - 0x5202 07FF	0x4202 0400 - 0x4202 07FF
GPIOA (1 Kbyte)		0x4800 0000 - 0x4800 03FF		0x5202 0000 - 0x5202 03FF	0x4202 0000 - 0x4202 03FF
SDMMC1 (1 Kbyte) [5]		0x4001 2800 - 0x4001 2BFF (APB2 on STM32L4 Series) 0x5006 2400 - 0x5006 27FF (AHB2 on STM32L4+ Series)		0x520C 8000 - 0x520C 83FF	0x420C 8000 - 0x420C 83FF
SDMMC2 (1 Kbyte) [3]		0x5006 2800 - 0x5006 2BFF		NA	
OTFDEC1 (1 Kbyte)		NA		0x520C 5000 - 0x520C 53FF	0x420C 5000 - 0x420C 53FF
DMA2D (3 Kbytes) [1]	AHB1	0x4002 B000 - 0x4002 BBFF		NA	

Peripheral	STM32L4 STM32L4+ bus	STM32L4/L4+ bus address	STM32L5 bus	STM32L5 Series	
				Secure boundary address	Non-secure boundary address
GFXMMU (1 Kbyte)[6]	AHB1	0x4002 C000 - 0x4002 EFFF		NA	
TSC (1 Kbyte)		0x4002 4000 - 0x4002 43FF	AHB1	0x5002 4000 - 0x5002 43FF	0x4002 4000 - 0x4002 43FF
CRC (1 Kbyte)		0x4002 3000 - 0x4002 33FF		0x5002 3000 - 0x5002 33FF	0x4002 3000 - 0x4002 33FF
Flash registers (1 Kbyte)		0x4002 2000 - 0x4002 23FF		0x5002 2000 - 0x5002 23FF	0x4002 2000 - 0x4002 23FF
RCC (1 Kbyte)		0x4002 1000 - 0x4002 13FF		0X5002 1000 - 0x5002 13FF	0X4002 1000 - 0x4002 13FF
DMAMUX1 (1 Kbyte)[7]		0x4002 0800 - 0x4002 0BFF		0x5002 0800 - 0x5002 0BFF	0x4002 0800 - 0x4002 0BFF
DMA2 (1 Kbyte)		0x4002 0400 - 0x4002 07FF		0x5002 0400 - 0x5002 07FF	0x4002 0400 - 0x4002 07FF
DMA1 (1 Kbyte)		0x4002 0000 - 0x4002 03FF		0x5002 0000 - 0x5002 03FF	0x4002 0000 - 0x4002 03FF
GTZC (4 Kbytes)		NA		0x5003 2400 - 0x5003 33FF	0x4003 2400 - 0x4003 33FF
ICACHE (1 Kbyte)		NA		0x5003 0400 - 0x5003 07FF	0x4003 0400 - 0x4003 07FF
UCPD1 (1 Kbyte)		NA	APB1	0x5000 DC00 - 0x5000 DFFF	0x4000 DC00 - 0x4000 DFFF
LPTIM3 (1 Kbyte)		NA		0x5000 9800 - 0x5000 9BFF	0x4000 9800 - 0x4000 9BFF
LPTIM2 (1 Kbyte)	APB1	0x4000 9400 - 0x4000 97FF		0x5000 9400 - 0x5000 97FF	0x4000 9400 - 0x4000 97FF
I2C4 (1 Kbyte)		0x4000 8400 - 0x4000 87FF		0x5000 8400 - 0x5000 87FF	0x4000 8400 - 0x4000 87FF
LPUART1 (1 Kbyte)		0x4000 8000 - 0x4000 83FF		0x5000 8000 - 0x5000 83FF	0x4000 8000 - 0x4000 83FF
LPTIM1 (1 Kbyte)		0x4000 7C00 - 0x4000 7FFF		0x5000 7C00 - 0x5000 7FFF	0x4000 7C00 - 0x4000 7FFF
OPAMP (1 Kbyte)		0x4000 7800 - 0x4000 7BFF		0x5000 7800 - 0x5000 7BFF	0x4000 7800 - 0x4000 7BFF
DAC (1 Kbyte)		0x4000 7400 - 0x4000 77FF		0x5000 7400 - 0x5000 77FF	0x4000 7400 - 0x4000 77FF
PWR (1 Kbyte)		0x4000 7000 - 0x4000 73FF		0x5000 7000 - 0x5000 73FF	0x4000 7000 - 0x4000 73FF
USB FS (1 Kbyte)[8]		0x4000 6800 - 0x4000 6BFF		0x5000 D400 - 0x5000 D7FF	0x4000 D400 - 0x4000 D7FF
CAN1[13]/ FDCAN1 (1 Kbyte)[9]		0x4000 6400 - 0x4000 67FF		0x5000 A400 - 0x5000 A7FF	0x4000 A400 - 0x4000 A7FF
USB SRAM (1 Kbyte)[8]		0x4000 6C00 - 0x4000 6FFF		0x5000 D800 - 0x5000 DBFF	0x4000 D800 - 0x4000 DBFF
CRS (1 Kbyte)		0x4000 6000 - 0x4000 63FF		0x5000 6000 - 0x5000 63FF	0x4000 6000 - 0x4000 63FF
I2C3 (1 Kbyte)		0x4000 5C00- 0x4000 5FFF		0x5000 5C00 - 0x5000 5FFF	0x4000 5C00 - 0x4000 5FFF
I2C2 (1 Kbyte)		0x4000 5800 - 0x4000 5BFF		0x5000 5800 - 0x5000 5BFF	0x4000 5800 - 0x4000 5BFF
I2C1 (1 Kbyte)		0x4000 5400 - 0x4000 57FF		0x5000 5400 - 0x5000 57FF	0x4000 5400 - 0x4000 57FF

Peripheral	STM32L4 STM32L4+ bus	STM32L4/L4+ bus address	STM32L5 bus	STM32L5 Series	
				Secure boundary address	Non-secure boundary address
UART5 (1 Kbyte)	APB1	0x4000 5000 - 0x4000 53FF	APB1	0x5000 5000 - 0x5000 53FF	0x4000 5000 - 0x4000 53FF
UART4 (1 Kbyte)Section 4.2		0x4000 4C00 - 0x4000 4FFF		0x5000 4C00 - 0x5000 4FFF	0x4000 4C00 - 0x4000 4FFF
USART3 (1 Kbyte)		0x4000 4800 - 0x4000 4BFF		0x5000 4800 - 0x5000 4BFF	0x4000 4800 - 0x4000 4BFF
USART2 (1 Kbyte)		0x4000 4400 - 0x4000 47FF		0x5000 4400 - 0x5000 47FF	0x4000 4400 - 0x4000 47FF
SPI3 (1 Kbyte)[13]		0x4000 3C00 - 0x4000 3FFF		0x5000 3C00 - 0x5000 3FFF	0x4000 3C00 - 0x4000 3FFF
SPI2 (1 Kbyte)		0x4000 3800 - 0x4000 3BFF		0x5000 3800 - 0x5000 3BFF	0x4000 3800 - 0x4000 3BFF
IWDG (1 Kbyte)		0x4000 3000 - 0x4000 33FF		0x5000 3000 - 0x5000 33FF	0x4000 3000 - 0x4000 33FF
WWDG (1 Kbyte)		0x4000 2C00 - 0x4000 2FFF		0x5000 2C00 - 0x5000 2FFF	0x4000 2C00 - 0x4000 2FFF
RTC (1 Kbyte)		0x4000 2800 - 0x4000 2BFF		0x5000 2800 - 0x5000 2BFF	0x4000 2800 - 0x4000 2BFF
TIM7 (1 Kbyte)[10]		0x4000 1400 - 0x4000 17FF		0x5000 1400 - 0x5000 17FF	0x4000 1400 - 0x4000 17FF
TIM6 (1 Kbyte)		0x4000 1000 - 0x4000 13FF		0x5000 1000 - 0x5000 13FF	0x4000 1000 - 0x4000 13FF
TIM5 (1 KB)		0x4000 0C00- 0x4000 0FFF		0x5000 0C00 - 0x5000 0FFF	0x4000 0C00 - 0x4000 0FFF
TIM4 (1 Kbyte)		0x4000 0800 - 0x4000 0BFF		0x5000 0800 - 0x5000 0BFF	0x4000 0800 - 0x4000 0BFF
TIM3 (1 Kbyte)Section 4.2		0x4000 0400 - 0x4000 07FF		0x5000 0400 - 0x5000 07FF	0x4000 0400 - 0x4000 07FF
TIM2 (1 Kbyte)		0x4000 0000 - 0x4000 03FF		0x5000 0000 - 0x5000 03FF	0x4000 0000 - 0x4000 03FF
SWPMI1 (1 Kbyte)[11]		0x4000 8800 - 0x4000 8BFF		NA	
CAN2 (1 Kbyte)		0x4000 6800 - 0x4000 6BFF		NA	
LCD (1 Kbyte)		0x4000 2400 - 0x4000 27FF		NA	
LTDC (1 Kbyte)[7]	APB2	0x4001 6800 - 0x4001 6BFF		NA	
DSI (1 Kbyte)[12]		0x4001 6C00 - 0x4001 73FF		NA	
DFSDM1 (1 Kbyte/ STM32L4) (2 Kbytes/ STM32L4+ and STM32L5)		0x4001 6000 - 0x4001 63FF	APB2	0x5001 6000 - 0x5001 67FF	0x4001 6000 - 0x4001 67FF
SAI2 (1 Kbyte)		0x4001 5800 - 0x4001 5BFF		0x5001 5800 - 0x5001 5BFF	0x4001 5800 - 0x4001 5BFF
SAI1 (1 Kbyte)[13]		0x4001 5400 - 0x4001 57FF		0x5001 5400 - 0x5001 57FF	0x4001 5400 - 0x4001 57FF
TIM17 (1 Kbyte)		0x4001 4800 - 0x4001 4BFF		0x5001 4800 - 0x5001 4BFF	0x4001 4800 - 0x4001 4BFF
TIM16 (1 Kbyte)		0x4001 4400 - 0x4001 47FF		0x5001 4400 - 0x5001 47FF	0x4001 4400 - 0x4001 47FF
TIM15 (1 Kbyte)		0x4001 4000 - 0x4001 43FF		0x5001 4000 - 0x5001 43FF	0x4001 4000 - 0x4001 43FF
USART1 (1 Kbyte)		0x4001 3800 - 0x4001 3BFF		0x5001 3800 - 0x5001 3BFF	0x4001 3800 - 0x4001 3BFF
TIM8 (1 Kbyte)		0x4001 3400 - 0x4001 37FF		0x5001 3400 - 0x5001 37FF	0x4001 3400 - 0x4001 37FF

Peripheral	STM32L4 STM32L4+ bus	STM32L4/L4+ bus address	STM32L5 bus	STM32L5 Series	
				Secure boundary address	Non-secure boundary address
SPI1 (1 Kbyte)	APB2	0x4001 3000 - 0x4001 33FF	APB2	0x5001 3000 - 0x5001 33FF	0x4001 3000 - 0x4001 33FF
TIM1 (1 Kbyte)		0x4001 2C00 - 0x4001 2FFF		0x5001 2C00 - 0x5001 2FFF	0x4001 2C00 - 0x4001 2FFF
COMP (1 Kbyte)		0x4001 0200 - 0x4001 03FF		0x5001 0200 - 0x5001 03FF	0x4001 0200 - 0x4001 03FF
VREFBUF (1 Kbyte)[13]		0x4001 0030 - 0x4001 01FF		0x5001 0100 - 0x5001 01FF	0x4001 0100 - 0x4001 01FF
SYSCFG (1 Kbyte)		0x4001 0000 - 0x4001 002F		0x5001 0000 - 0x5001 002F	0x4001 0000 - 0x4001 002F
EXTI (1 Kbyte)		0x4001 0400 - 0x4001 07FF	AHB1	0x5002 F400 - 0x5002 F7FF	0x4002 F400 - 0x4002 F7FF
FIREWALL (1 Kbyte)		0x4001 1C00 - 0x4001 1FFF		NA	
QUADSPI (1 Kbyte)[11]	AHB4	0xA000 1000 - 0xA000 13FF		NA	
OCTOSPI2 (1 Kbyte)[7]	NA	0xA000 1400 - 0xA000 17FF		NA	
OCTOSPI1 (1 Kbyte)[7]	NA	0xA000 1000 - 0xA000 13FF	AHB3	0x5402 1000 - 0x5402 13FF	0x4402 1000 - 0x4402 13FF
FMC (1 Kbyte)	AHB3	0xA000 0000 - 0xA000 03FF		0x5402 0000 - 0x5402 03FF	0x4402 0000 - 0x4402 03FF

1. *Available only on STM32L49x/4Ax and STM32L4+ devices.*
2. *Available only on STM32L42/44/46/4A6xxx, STM32L486xx and STM32L4+ devices.*
3. *Available only on STM32L4P5/Q5xx devices.*
4. *Available only on STM32L4x5/L4x6xx and STM32L4+ devices.*
5. *Not available on STM32L41/42xxx and STM32L432/442xx devices.*
6. *Available only for STM32L4R/4Sxxx devices.*
7. *Available only on STM32L4+ devices.*
8. *Available only on STM32L4x2/4x3xx devices.*
9. *FDCAN1 available for STM32L5 devices.*
10. *TIM7 not available on STM32L41/42/45/46xxx devices.*
11. *Not available for STM32L4+ devices.*
12. *Available only on STM32L4R9/S9xx devices.*
13. *Not available on STM32L41/42xxx devices.*

4.3 Flexible static memory controller (FSMC)

The following table presents the FSMC interface differences between of the STM32L4, STM32L4+ and STM32L5 Series.

Table 11. FSMC interface differences between STM32L4, STM32L4+ and STM32L5 Series

FSMC		STM32L4 Series[1]	STM32L4+ Series	STM32L5 Series
External memory interfaces		• SRAM • NOR/NAND memories • PSRAM • NAND Flash memory with ECC hardware	• SRAM • NOR/NAND memories • PSRAM • NAND Flash memory with ECC hardware • FRAM (ferroelectric RAM)	• SRAM • NOR Flash memory/one NAND Flash memory • PSRAM • NAND Flash memory with ECC hardware to check up to 8 Kbytes of data • FRAM (ferroelectric RAM)
Features	Data bus width	8 or 16 bits		
	New timing	NA	• NBL setup timing • Data hold timing • Clock divider ratio 1	New PSRAM counter timing

1. FSMC is not available on STM32L41/42/43/44/45/46xxx devices.

For the STM32L5 Series, the FSMC registers can be configured as secure through the TZSC controller (refer to the STM32L5 Series reference manual for more details).

4.4 Direct memory access controller (DMA)

The STM32L4, STM32L4+ and STM32L5 devices embed the same DMA controllers:
- two DMAs with 7 + 7 channels for the STM32L4 and STM32L4+ Series
- two DMAs with to 8 + 8 channels for the STM32L5 Series

Each channel is dedicated to manage the memory access requests from one or more peripherals. The devices embed also an arbiter for handling the priorities among the DMA requests.

For the STM32L4+ and STM32L5 Series, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer. In the STM32L4 Series, the DMA request line is connected directly to the peripherals.

The table below presents the differences between the DMA requests in the STM32L4, STM32L4+ and STM32L5 Series.

Table 12. DMA differences between STM32L4, STM32L4+ and STM32L5 Series

DMA	STM32L4 and STM32L4+ Series	STM32L5 Series
Architecture	Two DMA controllers can access memory and peripherals.	
Channels	• 7 channels • 8 requests per channel	• 14 channels • 8 requests per channel
TrustZone security	NA	Yes
Privileged/unprivileged DMA		

4.5 DMA request multiplexer (DMAMUX)

The DMAMUX is available for the STM32L4+ and STM32L5 Series (not available on the STM32L4 Series). It enables routing a DMA request line between the peripherals and the DMA controllers of the product. The routing function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

The DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

The features and main characteristics of the DMAMUX in the STM32L4+ and STM32L5 Series, are specified in the table below.

Table 13. DMAMUX features and characteristics on STM32L4+ and STM32L5 Series

DMAMUX Feature	STM32L4+ Series	STM32L5 Series
Number of output request channels	14	16
Number of request generator channels	4	
Number of request trigger inputs	26	23
Number of peripheral request inputs	89	90
TrustZone support	NA	1

4.6 Interrupts

The table below presents the interrupt vector in the STM32L5 Series compared to the STM32L4 and STM32L4+ Series.

Table 14. **Interrupt vector differences between STM32L4, STM32L4+ and STM32L5 Series**

Position	STM32L4+ Series	STM32L4 Series	STM32L5 Series
2	RTC_TAMP_STAMP /CSS_LSE		RTC (EXTI17)
3	RTC_WKUP		RTC_S (EXTI18)
4	FLASH		TAMP (EXTI19)
5	RCC		TAMP_S (EXTI20)
6	EXTI0		FLASH
7	EXTI1		FLASH_S
8	EXTI2		GTZC
9	EXTI3		RCC
10	EXTI4		RCC_S
11	DMA1_CH1		EXTI0
12	DMA1_CH2		EXTI1
13	DMA1_CH3		EXTI2
14	DMA1_CH4		EXTI3
15	DMA1_CH5		EXTI4
16	DMA1_CH6		EXTI5
17	DMA1_CH7		EXTI6
18	ADC1_2	ADC1	EXTI7
19	CAN1_TX[1]		EXTI8
20	CAN1_RX0[1]		EXTI9
21	CAN1_RX1[1]		EXTI10
22	CAN1_SCE[1]		EXTI11
23	EXTI9_5		EXTI12
24	TIM1_BRK/TIM15		EXTI13
25	TIM1_UP/TIM16		EXTI14
26	TIM1_TRG_COM/TIM17	TIM1_TRG_COM	EXTI15
27	TIM1_CC		DMAMUX1_OVR
28	TIM2		DMAMUX1_OVR_S
29	TIM3[2]		DMA1_CH1
30	TIM4	NA	DMA1_CH2
31	NA	I2C1_EV	DMA1_CH3
32	NA	I2C1_ER	DMA1_CH4
33	I2C2_EV[3]		DMA1_CH5
34	I2C2_ER[3]		DMA1_CH6
35	SPI1		DMA1_CH7
36	SPI2[3]		DMA1_CH8

Position	STM32L4+ Series	STM32L4 Series	STM32L5 Series
37	USART1		ADC1_2
38	USART2		DAC
39	USART3[3]		FDCAN1_IT0
40	EXTI15_10		FDCAN1_IT1
41	RTC_ALARM		TIM1_BRK
42	DFSDM1_FLT3	NA	TIM1_UP
43	TIM8_BRK		TIM1_TRG_COM
44	TIM8_UP		TIM1_CC
45	TIM8_TRG_COM		TIM2
46	TIM8_CC		
47	Reserved		
48	FMC		
49	SDMMC1	SDMMC1[1][3]	
50	TIM5	NA	
51	SPI3	SPI3	TIM8_BRK
52	UART4	UART4[2]	TIM8_UP
53	UART5	NA	TIM8_TRG_COM
54	TIM6_DACUNDER	TIM6_DACUNDER	TIM8_CC
55	TIM7	TIM7[4]	I2C1_EV
56	DMA2_CH1		I2C1_ER
57	DMA2_CH2		I2C2_EV
58	DMA2_CH3		I2C2_ER
59	DMA2_CH4		SPI1
60	DMA2_CH5		SPI2
61	DFSDM1_FLT0[2]		USART1
62	DFSDM1_FLT1[2]		USART2
63	DFSDM1_FLT2	NA	USART3
64	COMP		UART4
65	LPTIM1		UART5
66	LPTIM2		LPUART1
67	OTG_FS[5]	USB_FS[6]	LPTIM1
68	DMA2_CH6		LPTIM2
69	DMA2_CH7		TIM15
70	LPUART1		TIM16
71	OCTOSPI1	QUADSPI	TIM17
72	I2C3_EV	I2C3_EV	COMP
73	I2C3_ER	I2C3_ER	USB_FS
74	SAI1[1]		CRS
75	SAI2	NA	FMC
76	OCTOSPI2	SWPMI1[4]	OCTOSPI1

Position	STM32L4+ Series	STM32L4 Series	STM32L5 Series
77	TSC		NA
78	DSIHSOT	LCD[7]	SDMMC1
79	AES[8]		NA
80	RNG		DMA2_CH1
81	FPU		DMA2_CH2
82	HASH and CRS[9]		DMA2_CH3
83	I2C4_EV[2]		DMA2_CH4
84	I2C4_ER[2]		DMA2_CH5
85	DCMI		DMA2_CH6
86	Reserved		DMA2_CH7
87	Reserved		DMA2_CH8
88	Reserved	NA	I2C3_EV
89	Reserved		I2C3_ER
90	DMA2D		SAI1
91	LCD-TFT		SAI2
92	LCD-TFT_ER		TSC
93	GFXMMU		AES[10]
94	DMAMUX1_OVR		RNG
95			FPU
96			HASH
97			PKA[10]
98			LPTIM3
99			SPI3
100			I2C4_ER
101	NA		I2C4_EV
102			DFSDM1_FLT0
103			DFSDM1_FLT1
104			DFSDM1_FLT2
105			DFSDM1_FLT3
106			UCPD1
107			ICACHE
108			OTFDEC1[10]

1. *Not available on STM32L41/42xxx devices.*
2. *Not available on STM32L41/42/43/44xxx devices.*
3. *Not available on STM32L432/442xx devices.*
4. *Not available on STM32L41/42/45/46xxx devices.*
5. *Available on STM32L4x5/4x6 and STM32L4+ devices.*
6. *Not available on STM32L431/451xx devices.*
7. *Available on STM32L4x3/4x5/4x6xx devices.*
8. *Not available on STM32L41/43/45xxx devices.*
9. *HASH available only on STM32L4+ and STM32L496/4A6xx devices.*
10. *Not available on STM32L552xx devices.*

4.7 Octo-SPI interface

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as Flash memory, PSRAM, HyperRAM™, HyperFlash™ and some specific circuits like FPGA or ASICs.

The Octo-SPI specialized communication interface targets single-, dual-, quad- or octal-SPI memories. It can be configured in three modes: Indirect, Status-polling and Memory-mapped modes.

The OCTOSPI peripheral is available on the STM32L5 Series as on the STM32L4+ Series, with several additional features.

Note: *The STM32L4 Series feature a QUADSPI peripheral (not an OCTOSPI). The OCTOSPI supports the same features than the QUADSPI and additionally supports Octo-SPI memories.*

The table below illustrates the OCTOSPI differences between the STM32L4+ and STM32L5 Series.

Table 15. OCTOSPI differences between STM32L4+ and STM32L5 Series

OCTOSPI features	STM32L4+ Series	STM32L5 Series
Number of instances	2	1
OCTOSPI I/O manager (OCTOSPIM)	Yes	NA
Single ended clock for 3V0 HyperBus™ mode	Yes	
Inverted clock for 1.8 V HyperBus™ mode	NA	Yes
Zero-wait-states-like performance execution	NA	Yes
Support of Quad- and Octo-SPI APmemory PSRAMs	NA	Yes
CS boundary and refresh	NA	Yes
Full support for HyperRAM memories	Yes	
OTFDEC protecting Flash code	NA	Yes
TrustZone security	NA	Yes

4.8 Reset and clock control (RCC)

The STM32L5 Series devices implement the same RCC features than the STM32L4 and STM32L4+ Series, but with some specification updates.

The table below details the RCC features for the STM32L5 Series compared to the STM32L4 and STM32L4+ Series.

Table 16. RCC features in STM32L4, STM32L4+ and STM32L5 Series

RCC	STM32L4 and STM32L4+ Series	STM32L5 Series
MSI	• Low power oscillator with programmable frequency up to 48 MHz • MSI can replace PPLs as system clock (faster wakeup, lower consumption). • MSI can be used as USB device clock (no need for external high-speed crystal oscillator). • Multi-speed RC factory and user trimmed 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz • Auto calibration from LSE	
HSI16	• 16 MHz RC factory and user trimmed	
LSI	• 32 kHz RC • LSI frequency prescaler (LSI/128) • Lower consumption, higher accuracy (refer to the electrical characteristics section of the datasheet)	
HSE	• 4 to 48 MHz	
LSE	• 32.768 kHz • Configurable drive/consumption	

RCC	STM32L4 and STM32L4+ Series	STM32L5 Series
	• Available in Backup domain (VBAT)	
HSI48	• 48 MHz RC (only for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx devices) • HSI48 can drive USB FS, SDMMC and RNG.	• 48 MHz RC • HSI48 can drive USB FS, SDMMC and RNG.

PLL	• Main PLL for system:
	  – Two PLLs for SAI1/2, ADC, RNG, SDMMC and OTG_FS clock. (for STM32L4+ and STM32L47/48/49/4Axxx devices)
	  – One PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (for STM32L43/44/45/46xxx devices)
	• Each PLL provides up to three independent outputs.
	• The PLL sources are MSI, HSI16, HSE.
		• Three PLLs: PLL, PLLSAI1 and PLLSAI2
		• Each PLL provides up to three independent outputs.
		• The internal PLLs can be used to multiply the HSI16, HSE or MSI output clock frequency.

System clock source	• MSI, HSI16, HSE or PLL	
System clock frequency	• Up to 80 MHz (or 120 for STM32L4+ Series) • 4 MHz after reset using MSI	• Up to 110 MHz • 4 MHz after reset using MSI
AHB frequency	• Up to 80 MHz (or 120 for STM32L4+ Series)	• Up to 110 MHz
APB1 frequency	• Up to 80 MHz (or 120 for STM32L4+ Series)	• Up to 110 MHz
APB2 frequency	• Up to 80 MHz (or 120 for STM32L4+ Series)	• Up to 110 MHz
RTC clock source	• LSI, LSE or HSE/32	
MCO clock source	• MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI or HSI48 (for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx devices) • With configurable prescaler 1, 2, 4, 8 or 16 for each output	• One of eight clock signals can be selected as MCO clock: LSI, LSE, SYSCLK, HSI16, HSI48, HSE, PLLCLK or MSI.
Clock security system (CSS)	• CSS on HSE • CSS on LSE	
Internal oscillator measurement / calibration	• LSE connected to TIM15 or TIM16 CH1: can measure HSI16 or MSI with respect to LSE clock high precision. • LSI connected to TIM16 CH1: can measure LSI with respect to HSI16 or HSE clock precision. • HSE/32 connected to TIM17 CH1: can measure HSE with respect to LSE/HSI16 clock. • MSI connected to TIM17 CH1: can measure MSI with respect to HSI16/HSE clock. • On STM32L41/42/43/44/45/46xxx devices, HSE/32 and MSI are connected to TIM16 CH1.	• LSE connected to TIM15/TIM16/TIM17 CH1 • LSI connected to TIM16 CH1: can measure LSI with respect to HSI16 or HSE clock precision. • HSE/32 connected to TIM17 CH1: can measure HSE with respect to LSE/HSI16 clock. • MSI connected to TIM17 CH1: can measure MSI with respect to HSI16/HSE clock. • HSE/32 and MSI connected to TIM16 CH1
Interrupt	• CSS (linked to NMI IRQ) • LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, PLLSAI1RDY, PLLSAI2RDY (only on STM32L4+ and STM32L47/48/49/4Axxx devices) (linked to RCC global IRQ)	• CSS (linked to NMI IRQ) • LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, PLLSAI1RDY, PLLSAI2RDY

4.8.1 Performance versus V_{CORE} ranges

In the STM32L5 devices, the maximum CPU clock frequency and the number of Flash memory wait states depend on the selected voltage range V_{CORE}.

The table below presents the different clock source frequencies, depending on different product voltage range for the STM32L4, STM32L4+ and the STM32L5 Series.

Table 17. Performance versus V_{CORE} ranges for STM32L4, STM32L4+ and STM32L5 Series

CPU performance	Power performance	V_{CORE} range	Typical value (V)	Max frequency[1]					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
STM32L4 Series									
High	Medium	1	1.2	-	80	64	48	32	16
Medium	High	2	1.0	-	26	26	18	12	6
STM32L4+ Series									
High	Medium	1 (boost mode)	1.28	120	100	80	60	40	20
		1 (normal mode)	1.2	-	-	80	60	40	20
Medium	High	2	1.0	-	-	-	26	16	8
STM32L5 Series									
High	Low	0	1.28	110	100	80	60	40	20
		1	1.2	-	-	80	60	40	20
Medium	High	2	1.0	-	-	-	26	16	8

1. WS = wait state.

4.8.2 Peripheral access configuration

Since the address mapping of some peripherals has been changed in the STM32L5 Series compared to the STM32L4 and STM32L4+ Series, different registers need to be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from Reset mode].

The table below shows the RCC registers used for peripheral access configuration for the STM32L4, STM32L4+ and the STM32L5 Series.

Table 18. RCC registers for STM32L4, STM32L4+ and STM32L5 Series

Bus	STM32L4 and STM32L4+ Series	STM32L5 Series	Comments
AHB	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2)	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2) RCC_AHB3RSTR (AHB3)	Used to [enter/exit] the AHB peripheral from reset
	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2)	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2) RCC_AHB3ENR (AHB3)	Used to [enable/disable] the AHB peripheral clock
	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3)		Used to [enable/disable] the AHB peripheral clock in Sleep mode
APB1	RCC_APB1RSTR1 RCC_APB1RSTR2		Used to [enter/exit] the APB1 peripheral from reset
	RCC_APB1ENR1 RCC_APB1ENR2		Used to [enable/disable] the APB1 peripheral clock

Bus	STM32L4 and STM32L4+ Series	STM32L5 Series	Comments
APB1	RCC_APB1SMENR1 RCC_APB1SMENR2		Used to [enable/disable] the APB1 peripheral clock in Sleep mode
APB2	RCC_APB2RSTR		Used to [enter/exit] the APB2 peripheral from reset
	RCC_APB2ENR		Used to [enable/disable] the APB2 peripheral clock
	RCC_APB2SMENR		Used to [enable/disable] the APB2 peripheral clock in Sleep mode

4.8.3 Peripheral clock configuration

The peripherals presented below have a dedicated clock source independent from the system clock, that is used to generate the clock required for their operation. This section presents the difference between the STM32L4, STM32L4+ and the STM32L5 Series, for the peripherals with different clock sources.

SAI

- In the STM32L4+ and STM32L47/48/49/4Axxx devices, the SAI clocks are derived from one of the following sources:
    - an external clock mapped on SAI1_EXTCLK or SAI2_EXTCLK
    - PLLSAI1 VCO (PLLSAI1CLK)
    - PLLSAI2 VCO (PLLSAI2CLK)
    - main PLL VCO (PLLSAI3CLK)
    - HSI16 clock
- In the STM32L43/44/45/46xxx devices, the SAI clocks are derived from one of the following sources:
    - An external clock mapped on SAI1_EXTCLK for SAI1
    - PLLSAI1 (P) divider output (PLLSAI1CLK)
    - main PLL (P) divider output (PLLSAI2CLK)
    - HSI16 clock
- In the STM32L5 Series, the SAI1 and SAI2 clocks are derived from one of the following sources (selected by software):
    - an external clock mapped on SAI1_EXTCLK for SAI1 and SAI2_EXTCLK for SAI2
    - PLLSAI1 VCO (PLLSAI1CLK)
    - PLLSAI2 VCO (PLLSAI2CLK)
    - main PLL VCO (PLLSAI3CLK)
    - HSI16 clock

DFSDM

- In the STM32L4 and STM32L4+ Series, the DFSDM clock is derived from one of the following sources (selected by software):
    - system clock (SYSCLK)
    - APB2 clock (PCLK2)
- In the STM32L5 Series, the DFSDM audio clock is derived from one of the following sources (selected by software):
    - SAI1 clock
    - HSI clock
    - MSI clock

OCTOSPI

- The STM32L4 Series do not support the OCTOSPI peripheral.

- In the STM32L4+ and STM32L5 Series, the OCTOSPI kernel clock is derived from one of the following sources (selected by software):
    - system clock
    - PLL48M1CLK
    - MSI clock

FDCAN

- The STM32L4 and STM32L4+ Series do not support the FDCAN peripheral.
- In the STM32L5 Series, the FDCAN kernel clock is derived from one of the following sources (selected by software):
    - PLL48M1CLK
    - PLLSAI1CLK
    - HSE clock

4.9 Power controller (PWR)

The STM32L5 devices implement the same PWR features than the STM32L4 and STM32L4+ Series, but with some specification updates and enhancements.

In the STM32L4, STM32L4+ and STM32L5 Series, several peripherals are supplied through independent power domains: VDDA, VDDIO2 and VDDUSB. These supplies must not be provided without a valid operating supply on the VDD pin.

Moreover, the STM32L5 devices integrate an optional SMPS step-down converter (power-efficient DC/DC voltage regulator) that can be enabled/disabled on the fly to optimize the energy.

In the STM32L5 Series, the SMPS power-supply pins are available only on specific packages with SMPS step-down converter option. If the selected package features the SMPS step-down converter option but this converter is never used by the application, it is recommended to set the SMPS power-supply pins as follows:

- VDDSMPS and VLXSMPS connected to VSS
- V15SMPS connected to VDD

In the STM32L5 devices, the I/Os, the embedded LDO regulator and the system analog peripherals (such as PLLs and reset block) are fed by V_{DD} supply source. The embedded linear voltage regulator is used to supply the internal digital power V_{CORE}, that is the power supply for digital peripherals and memories.

The table below presents the PWR controller features for the STM32L4, STM32L4+ and STM32L5 Series.

Table 19. PWR controller features for STM32L4, STM32L4+ and STM32L5 Series

PWR features	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Power supplies	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, Flash memory and internal regulator • Provided externally through VDD pins	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, the internal regulator or the SMPS step-down converter, and the system analog such as reset, power management and internal clocks • Provided externally through VDD pins
	• V_{CORE} = 1.0 to 1.28 V: power supply for digital peripherals, SRAM and Flash memory • Generated by an internal voltage regulator • Two V_{CORE} ranges can be selected by software depending on target frequency.	• V_{CORE} = 1.0 to 1.28 V: power supply for digital peripherals, SRAM and Flash memory • Generated by an internal voltage regulator • Three V_{CORE} power ranges (Range 0, Range 1 and Range 2) can be programmed by software depending on target frequency.

PWR features	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Power supplies	• V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present	
	• Independent power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}) allow a reduction of the power consumption by running MCU at lower supply voltage than analog and USB.	
	• V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DAC/OPAMPs) / 2.4 V (VREFBUF) to 3.6 V • V_{DDA} is the external analog power supply for A/D and D/A converters, voltage reference buffer, operational amplifiers and comparators. • The V_{DDA} voltage level is independent from the V_{DD} voltage.	
	• V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers • The V_{DDUSB} voltage level is independent from the V_{DD} voltage.	
	• V_{DDIO2} = 1.08 V to 3.6 V: external power supply for 14 I/Os (Port G[15:2]) This voltage is independent from the V_{DD} voltage (not applicable for STM32L41/42/43/44/45/46xxx devices).	
	NA	• V_{DDSMPS} from 2 to 3.6 V: external power supply for the SMPS step-down converter. It must be connected to VDD. • V_{LXSMPS} is the switched SMPS step-down converter output. • V_{15SMPS} is the power supply for the system regulator. It is provided externally through the SMPS step-down converter VLXSMPS output. • An external coil with typical value of 4.7 μH must be connected between the dedicated VLXSMPS pin to VSSSMPS, via a capacitor of 4.7 μF. • V_{SSSMPS} is an isolated supply ground.
	• V_{LCD} = 2.5 to 3.6 V	NA
	• Available only on SM32L4R9/4S9xx devices • V_{DDDSI} is an independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY. • It must be connected to VDD.	
	• Available only on SM32L4R9/4S9xx devices • V_{CAPDSI} is the output of the DSI regulator (1.2 V), that must be connected externally to VDD12DSI.	
	• Available only on SM32L4R9/4S9xx devices • $V_{DD12DSI}$ is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. • An external capacitor of 2.2 μF must be connected on the VDD12DSI pin.	
Battery Backup domain	• RTC with backup registers (128 bytes) • LSE • PC13 to PC15 I/Os	
Power supply supervisor	• Integrated POR/PDR circuitry • Programmable voltage detector (PVD)	
	• Brownout reset (BOR) • BOR is always enabled, except in Shutdown mode.	

PWR features	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Power supply supervisor	Four peripheral voltage monitoring (PVM): • PVM1 for VDDUSB (~1.2 V) • PVM2 for VDDIO2 (~0.9 V) • PVM3/PVM4 for VDDA (~1.65 V/ ~2.2 V)	Four peripheral voltage monitoring (PVM): • PVM1 for VDDUSB (1.2 V) • PVM2 for VDDIO2 (0.9 V) • PVM3/PVM4 for VDDA (~1.65 V/ ~1.8 V)
	NA	Upper VDD and temperature monitoring
Low-power modes	• Sleep mode	
	• Low-power run mode (up to 2 MHz)	
	• Low-power sleep mode (up to 2 MHz) • System clock limited to 2 MHz • I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz. • Consumption is reduced at lower frequency thanks to the low-power regulator.	
	• Stop 0 • Stop1	
	• Stop 2 (for STM32L4 Series) • Stop 2: SRAM3 enabled (RRSTP = 1) and disabled (RRSTP = 0) within PWR_CR1 register (for STM32L4+ Series)	• Stop 2
	• Standby mode (VCORE domain powered off) • Optional SRAM2 retention • Optional I/O pull-up or pull-down configuration	• Standby mode (VCORE domain powered off) • Full SRAM2 content or only 4 Kbytes • Optional I/O pull-up or pull-down configuration
	• Shutdown mode (VCORE domain powered off and power monitoring off)	
External SMPS	• Support for external SMPS for high-power efficiency • Refer to the application note *Design recommendations for STM32L4xxxx with external SMPS* (AN4978) for STM32L4 Series	
Wakeup sources	• Sleep mode: – any peripheral interrupt/wakeup event	

	• Stop 0, Stop 1 and Stop 2 modes:
	  – any EXTI line event/interrupt
	  – BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
		• Stop 0, Stop 1 and Stop 2 modes:
		  – any EXTI line event/interrupt
		  – BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, LPTIM

	• Standby mode:
	  – five WKUP pins rising or falling edge
	  – RTC event
	  – external reset in NRST pin
	  – IWDG reset	

Wakeup clocks	• Wakeup from Stop: HSI16 (16 MHz) or MSI (all ranges up to 48 MHz) allowing 5 µs wakeup at high speed, without waiting for PLL startup time	
	• Wakeup from Standby: MSI (ranges from 1 to 8 MHz)	
	• Wakeup from Shutdown: MSI (4 MHz)	
Configuration	• 23 registers: 4 control registers, 2 status registers, 1 status clear register, 2 registers per GPIO port (A, B,..H) for controlling pull-up and pull-down (16 registers)	

1. *Blue cells = Same feature but with a specification change or enhancement. Green cells= new feature or new architecture.*

The following figures present the power supply for the STM32L4, STM32L4+ and STM32L5 Series. The differences are summarized in the previous table.

Figure 4. STM32L4 Series power supply overview
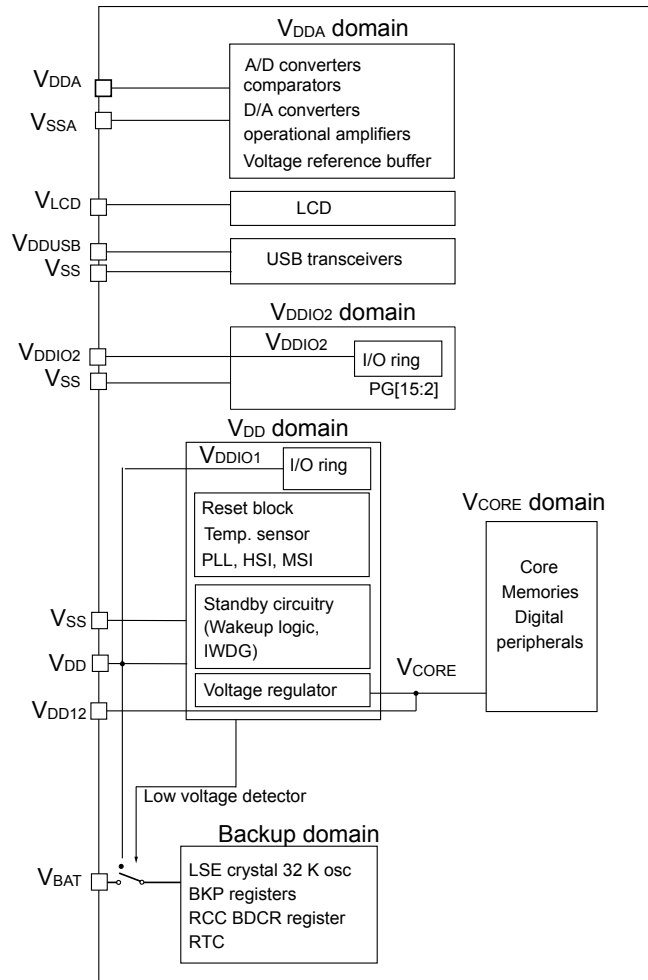
Figure 5. STM32L4R5/R7/S5/S7xx power supply overview
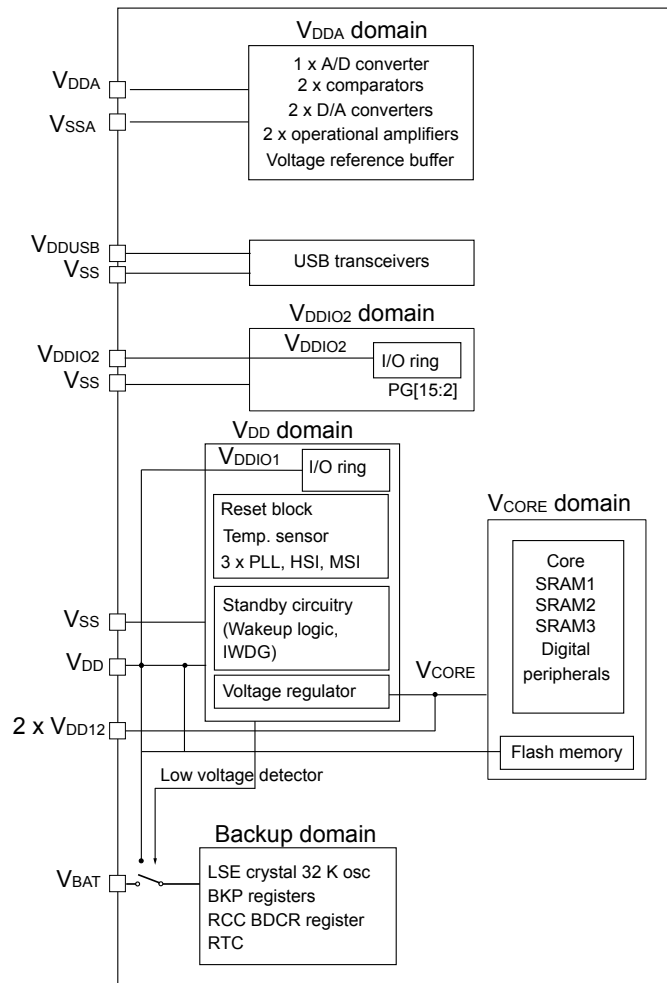
Figure 6. STM32L4R9/S9xx power supply overview
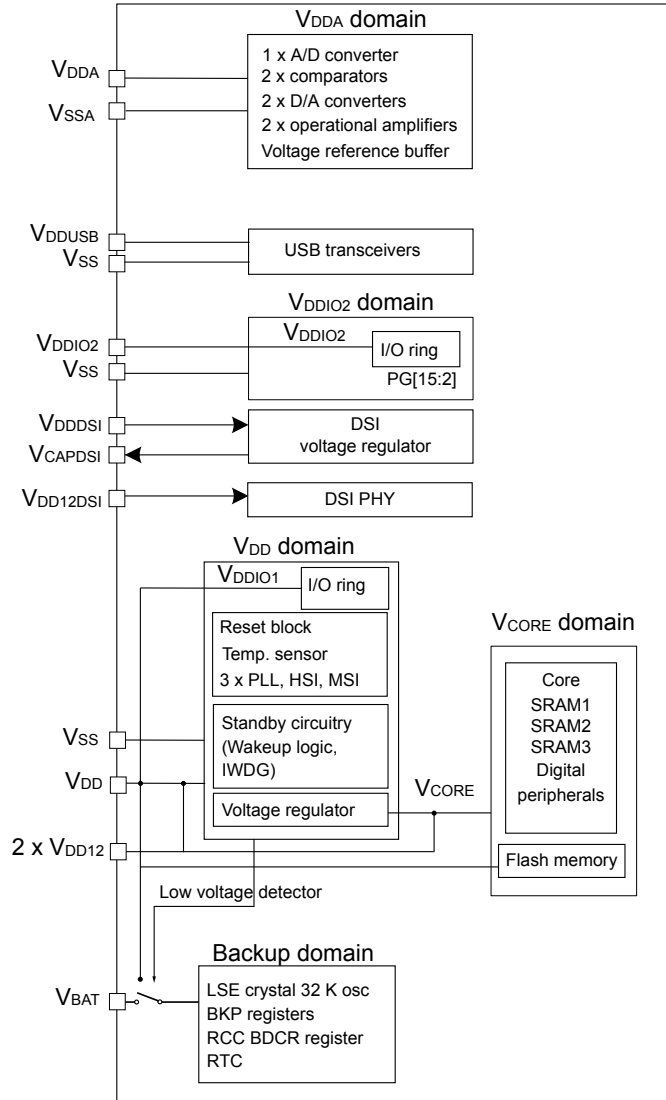
Figure 7. STM32L5 Series power supply overview (without SMPS)
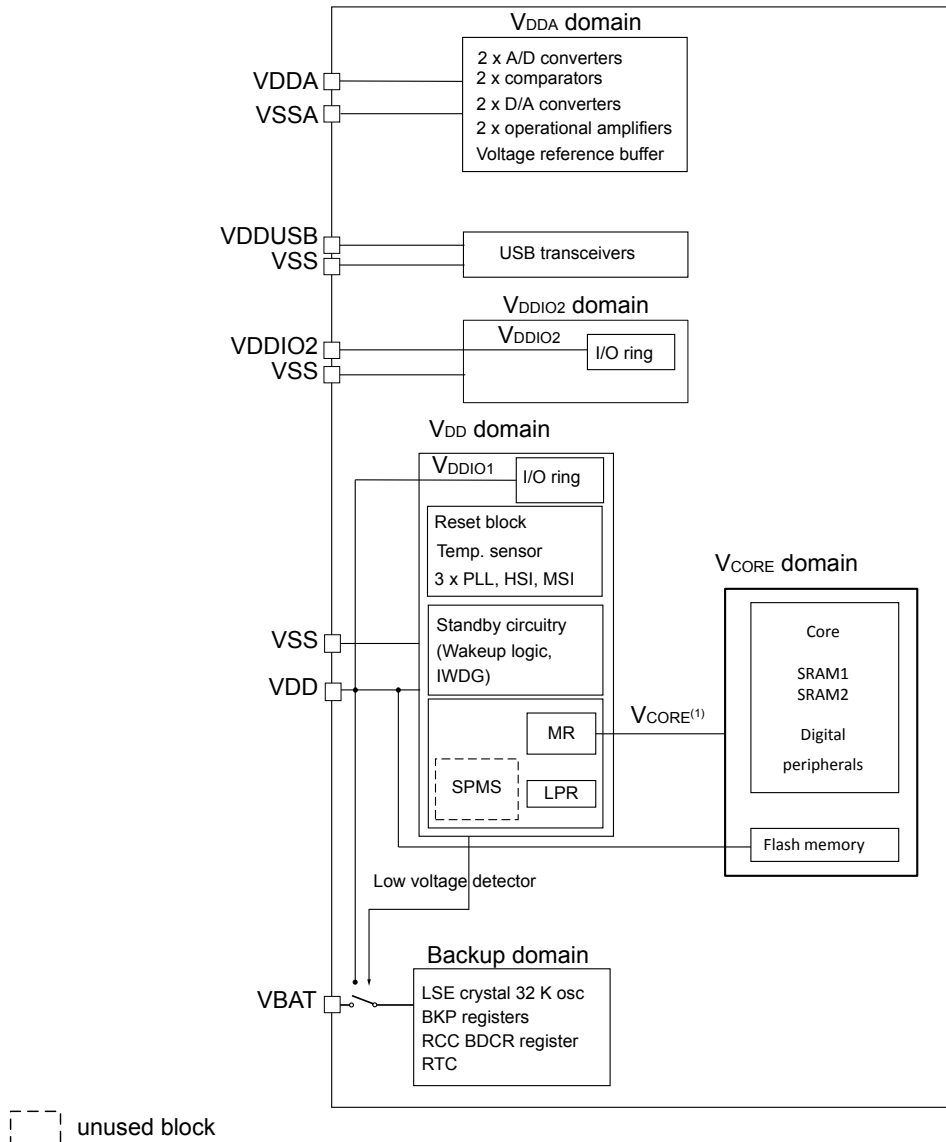
4.10 Real-time clock (RTC)/TAMP

The STM32L5 devices implement the same RTC features than the STM32L4 and STM32L4+ Series but with some specification updates and enhancements. The main differences are stated in the table below. For more information about RTC, refer to the RTC section of the product reference manual.

Note: *For the STM32L5 Series, the TAMP peripheral is separately present.*

Table 20. RTC differences between STM32L4, STM32L4+ and STM32L5 Series

RTC	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Features	• 3 tamper pins (available in VBAT)	• Up to 8 external tampers • Up to 5 internal tampers
	NA	• RTC and TAMP TrustZone support

1. Green cells = new feature.

4.11 General-purpose I/O interface (GPIO)

The STM32L5 devices implement the same GPIO features than the STM32L4 and STM32L4+ Series but with additional TrustZone security support.

For the STM32L5 Series, each general-purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR) and one 32-bit set/reset register (GPIOx_BSRR).

In addition, all GPIOs in the STM32L5 Series have a 32-bit locking register (GPIOx_LCKR), two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL) and a secure configuration register (GPIOx_SECCFGR).

Each general-purpose I/O pin of GPIO port in the STM32L5 Series can be individually configured as secure/non-secure in the GPIOx_SECCFGR register.

After reset, all general-purpose I/O of GPIO ports are secure.

All GPIO registers can be read and written by privileged and unprivileged accesses, whatever the security state secure or non-secure

For more information about the STM32L5 Series GPIO programming and usage, as well as TrustZone security, refer to the General-purpose I/Os (GPIO) section of the STM32L5 Series references manual and to the product datasheet for detailed description of the pinout and alternate function mapping.

4.12 System configuration controller (SYSCFG)

The SYSCFG differences between the STM32L4, STM32L4+ and STM32L5 Series are shown in the table below.

Table 21. SYSCFG differences between STM32L4, STM32L4+ and STM32L5 Series

SYSCFG	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Features	• Remapping memory areas • Managing the external interrupt line connection to the GPIOs • Managing robustness feature • Setting SRAM2 write protection and software erase • Configuring FPU interrupts • Enabling the firewall • Enabling/disabling the I2C Fast-mode plus driving capability on some I/Os and voltage booster for I/Os analog switches	• Managing robustness feature • Setting SRMA2 write protection and software erase • Configuring FPU interrupts • Enabling/disabling the I2C fast-mode plus driving capability on some I/Os and voltage booster for I/Os analog switches • Configuring TrustZone security register access

1. Blue cells = same feature but with a specification change or enhancement.

4.13 Extended interrupt and event controller (EXTI)

The STM32L5 devices implement almost the same EXTI features than the STM32L4 and STM32L4+ Series, with one exception: the STM32L5 Series feature TrustZone security support and privileged/unprivileged mode selection.

The table below illustrates the EXTI differences between the STM32L4, STM32L4+ and STM32L5 Series.

Table 22. EXTI differences between STM32L4, STM32L4+ and STM32L5 Series

EXTI	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Features	Up to 41 lines: • 12 direct, 26 configurable on STM324R/4Sxxx • 15 direct, 26 configurable on STM32L49/4Axxx • 14 direct, 26 configurable on STM32L47/48xxx • 12 direct, 25 configurable on STM32L41/42/43/44xxx	• 42 lines: 20 direct, 22 configurable • TrustZone support

1. Blue cells = same feature but with a specification change or enhancement.

The table below presents the EXTI line differences between the STM32L4, STM32L4+ and STM32L5 Series.

Table 23. EXTI line differences between STM32L4, STM32L4+ and STM32L5 Series

EXTI line	STM32L4+ Series	STM32L4 Series	STM32L5 Series
17	OTG FS wakeup event (OTG_FS_WKUP)[1][2]		RTC
18	RTC alarms		RTC secure
19	RTC tamper or timestamp or CSS_LSE		TAMP
20	RTC wakeup timer		TAMP secure
30	UART5 wakeup[2]	NA	USART5 wakeup
34	Reserved	SWPMI1 wakeup[2][3]	USB FS wakeup
36	PVM2 wakeup	NA	PVM2 wakeup
39	Reserved	LCD wakeup[4]	Reserved
40	I2C4 wakeup	I2C4 wakeup[5]	I2C4 wakeup
41	NA		UCPD1 wakeup
42	NA		LPTIM3 wakeup

1. Available on STM32L4x5/L4x6xx and STM32L4+ devices.
2. This line source cannot wake up from the Stop 2 mode.
3. Not available on STM32L41/42/45/46xxx devices.
4. Available on STM32L4x3/4x5/4x6xx devices.
5. Not available on STM32L41/42/43/44xxx devices.

4.14 Flash memory

The following table compares the Flash memory interface on the STM32L4, STM32L4+ and STM32L5 Series.

Table 24. Flash memory comparison between to STM32L4, STM32L4+ and STM32L5 Series

Flash memory		STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Main/program memory		For **STM32L4+** Series: • Up to 2 Mbytes • Split in two banks • When dual bank is enabled, each bank = 256 pages of 4 Kbytes. • When dual bank is disabled, memory block contains 256 pages of 8 Kbytes. For **STM32L47/48/49/4Axxx**: • Up to 1 Mbyte • Split in two banks where each bank = 256 pages of 2 Kbytes For **STM32L45/46xxx**: • Up to 512 Kbytes • One bank = 256 pages of 2 Kbytes For **STM32L43/44xxx**: • Up to 256 Kbytes • One bank = 128 pages of 2 Kbytes For **STM32L41/42xxx**: • Up to 128 Kbytes • One bank = 64 pages of 2 Kbytes	Up to 512 Kbytes • Single bank page size is 4 Kbytes. • Dual bank page size is 2 Kbytes.
Specific features		• Read while write (RWW) on dual-bank devices • Dual bank boot (only for STM32L4+ Series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx)	• Read while write (RWW)
ECC		Yes	
Read access		• Read access of 64 bits	• Single bank mode (DBANK = 0): read access of 128 bits • Dual-bank mode (DBANK = 1): read access of 64 bits
Wait states		• Up to 4 WS (depending on the supply voltage and the frequency)	
One time programmable (OTP)		• 1 Kbyte	• 512 bytes
Read protection (RDP)	Level 0	• No protection – RDP = 0xAA	
	Level 0.5	NA	When TrustZone is enabled, the device is partially closed • Non-secure debug only • NS-Flash access allowed (with debug connection) • Boot @ must target secure user Flash memory. • Boot on SRAM not allowed
	Level 1	Memory protection – RDP ≠ {0xAA, 0xCC}	
	Level 2	RDP = 0xCC[2]	

Flash memory	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Write protection (WRP)	• Single bank: 4 areas • Dual bank: 2 areas per bank	

User option bytes	• RDP:
	   – 0xAA: Level 0
	   – 0xCC: Level 2
	   – Others: Level 1
		• RDP:
		   – 0xAA: Level 0
		   – 0x55: Level 0.5
		   – 0xCC: Level 2
		   – Others: Level 1

	• nRST_STOP • nRST_STDBY • nRST_SHDW • IWDG_SW • IWDG_STOP, IWDG_STDBY • WWDG_SW • BOR_LEV[2:0]	
	• BFB2 (except for STM32L45xxx/46xxx, STM32L43xxx/44xxx and STM32L41xxx/42xxx)	• SWAP_BANK
	• DUALBANK (except for STM32L4+ and STM32L41/42/43/44/45/46xxx)	NA
	• DB1M (for STM32L4+ Series)	• DB256K
	• DBANK (for STM32L4+ Series)	• DBANK
	• SRAM2_RST, SRAM2_PE	
	• nSWBOOT0 (only for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx)	• nSWBOOT0
	• nBOOT0 (only for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx)	• nBOOT0
	NA	• SECBOOTADD0[24:0]
		• NSBOOTADD0[24:0] • NSBOOTADD1[24:0]
		• BOOT_LOCK
		• HDPx_PEND[6:0] • HDPxEN
		• SECWMx_PSTRT[6:0] • SECWMx_PEND[6:0]
		• PA15_PUPEN
		• TZEN
Protections	PCROP protection: one PCROP area per bank	NA
	NA	Two secure hide-protection areas (only when TrustZone is enabled)
Security	NA	• TrustZone • One secure area per bank including a secure HDP area • Block-based security attribution (volatile)

1.   Blue cells = Same feature but with a specification change or enhancement. Green cells = new feature or new architecture.

2.   Memory read protection level 2 is an irreversible operation. When level 2 is activated, the level of protection cannot be decreased to level 0 or level 1.

4.15 Universal synchronous/asynchronous receiver transmitter (U(S)ART)

The STM32L5 devices implement the same U(S)ART features than the STM32L4 and STM32L4+ Series but with some specification updates and enhancements. The main differences are stated in the table below.

Table 25. U(S)ART differences between STM32L4, STM32L4+ and STM32L5 Series

U(S)ART	STM32L4 Series	STM32L4+ and STM32L5Series
Instances	• 3 USARTs • 2 UARTs for STM32L4+ and STM32L47/48/49/4Axxx • 1 UART for STM32L45/46xxx • 1 LPUART	• 3 USARTs • 2 UARTs • 1 LPUART • 2 USARTs for STM32L552CExxP

Clock	• Dual clock domain allowing:
	  – UART functionality and wakeup from Stop mode
	  – Convenient baudrate programming independent from the PCLK reprogramming	

Data	• Word length: programmable (7, 8 or 9 bits) • Programmable data order with MSB-first or LSB-first shifting	
Interrupt	• 14 interrupt sources with flags	• 23 interrupt sources with flags
Features	• RS232 hardware flow control (CTS/RTS) • Continuous communication using DMA • Multiprocessor communication • Single-wire half-duplex communication • IrDA SIR ENDEC block • LIN mode • SPI master	
	• Wakeup from Stop mode (Start bit, Received byte, Address match) • Support for ModBus communication: timeout feature CR/LF character recognition	• Wakeup from Stop mode (Start bit, Received byte, Address match) • ModBus communication: timeout feature CR/LF character recognition • Two internal FIFOs for transmit and receive data • SPI slave
	• Receiver timeout interrupt • Auto baud rate detection • Driver enable • Swappable TX/RX pin configuration *LPUART does not support Synchronous mode (SPI master), Smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt and auto baud rate detection.*	
	• Smartcard mode T = 0, T = 1 supported • Number of stop bits: 1, 1.5, 2	

4.16 Controller area network

The main differences related to CAN (controller area network) between the STM32L4, STM32L4+ and STM32L5 Series are presented in the table below.

Table 26. CAN differences between STM32L4, STM32L4+ and STM32L5 Series

CAN	STM32L4 and STM32L4+ Series[1]	STM32L5 Series
Instances	• x1 bxCAN on STM32L4+ and STM32L43/44/45/46/47/48xxx • x2 bxCANs on STM32L49/4Axxx	• x1 FDCAN

Features	• Supports CAN protocol version 2.0 A, B Active
	• Bit rates up to 1 Mbit/s
	• Supports the time triggered communication option
	• Tx: 3 transmit mailboxes, configurable priority, time stamp on SOF transmission
	• Rx: 2 receive FIFOs with 3 stages, scalable filter banks, identifier list, configurable FIFO overrun, time stamp on SOF reception
	• Time-triggered communication option: Disable automatic retransmission mode 16-bit free running timer Time Stamp sent in last two data bytes
	• Management
	   – Maskable interrupts
	   – Software-efficient mailbox mapping at a unique address space
		• Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015, -4
		• CAN FD with maximum 64 data bytes supported
		• CAN error logging
		• AUTOSAR and J1939 support
		• Improved acceptance filtering
		• Rx: 2 receive FIFOs of three payloads each (up to 64 Bytes per payload)
		• Separate signaling on reception of High priority messages
		• Configurable transmit FIFO / queue of three payloads (up to 64 bytes per payload)
		• Transmit event FIFO
		• Programmable loop-back test mode
		• Maskable module interrupts
		• Two clock domains: APB bus interface and CAN core kernel clock
		• Power down support
		• Dual interrupt lines

1. Not available on STM32L41/42xxx devices.

4.17 Universal serial bus interface (USB)

The STM32L4, STM32L4+ and STM32L5 Series have different USB peripherals:
- The STM32L5 and STM32L41/42/43/44/45/46xxx devices implement an USB FS only instead of an USB OTG FS.
- The STM32L4+ and STM32L4x5/L4x6xx devices implement a USB OTG FS.

On the STM32L5, STM32L4+ and STM32L41/42/46/44/45/46/49/4Axxx devices, a clock recovery system (CRS) block is included. The CRS can provide a precise clock to the USB peripheral:
- When using USB device mode, the CRS allows crystal-less USB operation.
- When using USB host mode, the CRS allows low frequency crystal (32.768 kHz) USB operation.

Most features supported by the STM32L4 and STM32L4+ Series are also supported by the STM32L5 Series. The main USB differences between the STM32L4, STM32L4+ and STM32L5 Series are listed in the table below.

Table 27. USB differences between STM32L4, STM32L4+ and STM32L5 Series

USB	STM32L4 and STM32L4+ Series	STM32L5 Series[1]
Features	• Full support for the USB on-the-go (USB OTG FS) (for STM32L4+, STM32L49/4Axxx and STM32L476/486xx devices) • USB FS (available on STM32L4x2xx/4x3xx devices only)	• USB FS with clock recovery
	FS mode:	• Up to 8 bidirectional endpoints

USB	STM32L4 and STM32L4+ Series	STM32L5 Series[(1)]

Features	• For STM32L4+ and STM32L47/48/49/4Axxx devices:
	  – 1 bidirectional control endpoint
	  – 5 IN endpoints (Bulk, Interrupt, Isochronous)
	  – 5 OUT endpoints (Bulk, Interrupt, Isochronous)
	• For STM32L43/44/45/46xxx devices:
	  – 1 bidirectional control endpoint
	  – 7 IN endpoints (Bulk, Interrupt, Isochronous)
	  – 7 OUT endpoints (Bulk, Interrupt, Isochronous)
		• 4 IN endpoints (Bulk, Interrupt, Isochronous)
		• 4 OUT endpoints (Bulk, Interrupt, Isochronous)

	• Configurable number of endpoints from 1 to 8 • Cyclic redundancy check (CRC) generation/checking, Non-return-to-zero Inverted (NRZI) encoding/decoding and bit-stuffing • Isochronous transfers support • Double-buffered bulk/isochronous endpoint support • USB Suspend/Resume operations • Frame locked clock pulse generation	
	• Attach detection protocol (ADP) (only on STM32L4+ and STM32L47/48/49/4A devices) • Battery charging detection (BCD)	
	• Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB	
	• USB internal connect/disconnect feature with an internal pull-up resistor on the USB D+ (USB_DP) line	
Mapping	• APB1 for STM32L4+ and STM32L47/48/49/4Axxx • AHB2 for STM32L41/42/43/44/45/46xxx	• APB1
Buffer memory	• 1.25-Kbyte data FIFOs management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO (for STM32L4+ and STM32L47/48/49/4Axxx) • 1024 bytes of dedicated packet buffer memory SRAM (for STM32L41/42/43/44/45/46xxx)	• 1024 bytes of dedicated packet buffer memory SRAM
Low-power modes	• USB suspend and resume • USB revision 2.0 including link power management (LPM) support	

1. Blue cells = Same feature but with a specification change or enhancement.

4.18 Secure digital input/output MultiMediaCard interface (SDMMC)

The STM32L5 devices implement the same SDMMC features than the STM32L4 and STM32L4+ Series but with some specification updates. The following table presents the differences between the SDMMC interface on the STM32L4, STM32L4+ and STM32L5 Series.

Table 28. SDMMC main differences between STM32L4, STM32L4+ and STM32L5 Series

SDMMC	STM32L4 Series[(1)]	STM32L4+ Series	STM32L5 Series
Bus	• APB2	• APB2	• AHB
Clock source	• MSI clock • PLL /Q • PLLSAI1/Q • HSI48[(2)]	• MSI clock • PLL /Q • PLLSAI1 /Q • HSI48	• Main PLL VCO (PLL48M1CLK) • PLLSAI1 VCO (PLL48M2CLK) • MSI clock • HSI48
Features	• Full compliance with MultiMediaCard system specification version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	• Full compliance with MultiMediaCard system specification version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	

SDMMC	STM32L4 Series[1]	STM32L4+ Series	STM32L5 Series
Features	• Full compliance with SD memory card specification version 2.0	• Full compliance with SD memory card specifications version 4.1	
	• Full compliance with SD I/O card specification version 2.0. Card support for two different databus modes: 1-bit (default) and 4-bit	• Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit	
	• Data transfer up to 50 MHz for the 8-bit mode	• Data transfer up to 104 Mbyte/s for the 8-bit mode	
	NA	• SDDMC IDMA is used to provide high speed transfer between the SDMMC FIFO and the memory. • The AHB master optimizes the bandwidth of the system bus. The SDMMC internal DMA (IDMA) provides one channel to be used either for transmit or receive.	

1. *SDMMC is not available on STM32L41/42xxx and STM32L432/442xx devices.*

2. *Available only on STM32L43/44/45/46/49/4Axxx devices).*

4.19 Comparators (COMP)

Comparators for the STM32L4, STM32L4+ and STM32L5 Series have identical electrical parameters and configuration options. There is only one difference in the new blanking sources for the STM32L5 Series:

• TIM3 OC3 is added as blanking source in COMP1.
• TIM3 OC4/TIM8 OC5/TIM15 OC1 are added as blanking sources in COMP2.

4.20 Digital filter for sigma delta modulators (DFSDM)

The STM32L5 devices implement the same DFSDM features than the STM32L4 and STM32L4+ Series but with different implementation as stated in the table below.

Table 29. DFSDM main features implementation in STM32L4, STM32L4+ and STM32L5 Series

DFSDM features	STM32L4 and STM32L4+ Series	STM32L5 Series
Number of channels	Up to 8	4
Number of filters	Up to 8	4
Input from internal ADC	X[1]	X
Supported trigger sources	11/ 12[2]	32[3]
Pulses skipper	X[1]	X

1. *Not available for STM32L476/486xx devices.*

2. *The LPTIM1 is the new trigger source for the STM32L4+ Series.*

3. *For available trigger sources, refer to the 'DFSDM triggers connection' table in the product reference manual.*

5 Software migration

5.1 Reference documents

- Definitive guide to Arm Cortex-M33 and Cortex-M4 processors
- *STM32 Cortex-M4 MCUs and MPUs programming manual* (PM0214)
- CortexM4 Processor Technical Reference Manual, available on http://infocenter.arm.com
- CortexM33 Processor Technical Reference Manual, available on http://infocenter.arm.com

5.2 Cortex-M4 and Cortex-M33 overview

5.2.1 STM32 Cortex-M4 processor and core peripherals

The Cortex-M4 processor is a high-performance 32-bit processor designed for the microcontroller market. It offers significant benefits to the developers, including :

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultra-low power consumption with integrated sleep modes
- Platform security robustness, with integrated memory protection unit (MPU).

The Cortex-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers an exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754- compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, a saturating arithmetic and dedicated hardware division.

The STM32 Cortex-M4 implementation is illustrated in the figure below.

Figure 8. STM32 Cortex-M4 implementation
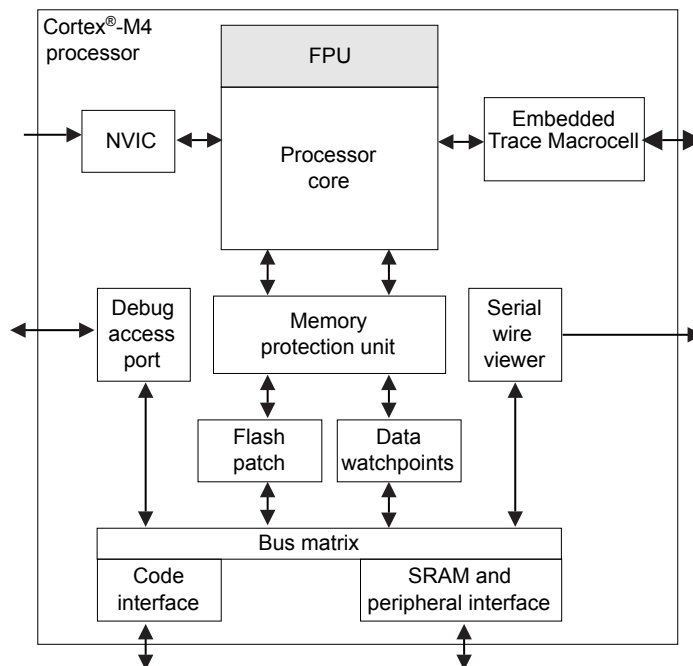
Cortex-M4 key features

- Architecture 32 bits RISC Armv7E-M
- 3-stage pipeline with branch speculation
- Instruction set:
    – Thumb, Thumb-2
    – Hardware multiply, hardware divide, saturated arithmetic
    – DSP extensions:
        . Single-cycle 16-/32-bit MAC
        . Single-cycle dual 16-bit MAC
        . 8-/16-bit SIMD arithmetic
- FPU (VFPv4-SP)

5.2.2 STM32 Cortex-M33 processor and core peripherals

The Cortex-M33 processor is excellence in ultra-low-power, performance and security.

The processor is based on the Armv8-M architecture for use in environments requiring more security implementation. The Cortex-M33 core implements a full set of DSP (digital signal processing) instructions, TrustZone aware support and a memory protection unit (MPU) that enhances the application security.

The Cortex-M33 core also features a single-precision floating-point unit (FPU), that supports all the Arm single-precision data-processing instructions and all the data types.

STM32 Cortex-M33 implementation is illustrated in the figure below.

Figure 9. STM32 Cortex-M33 implementation
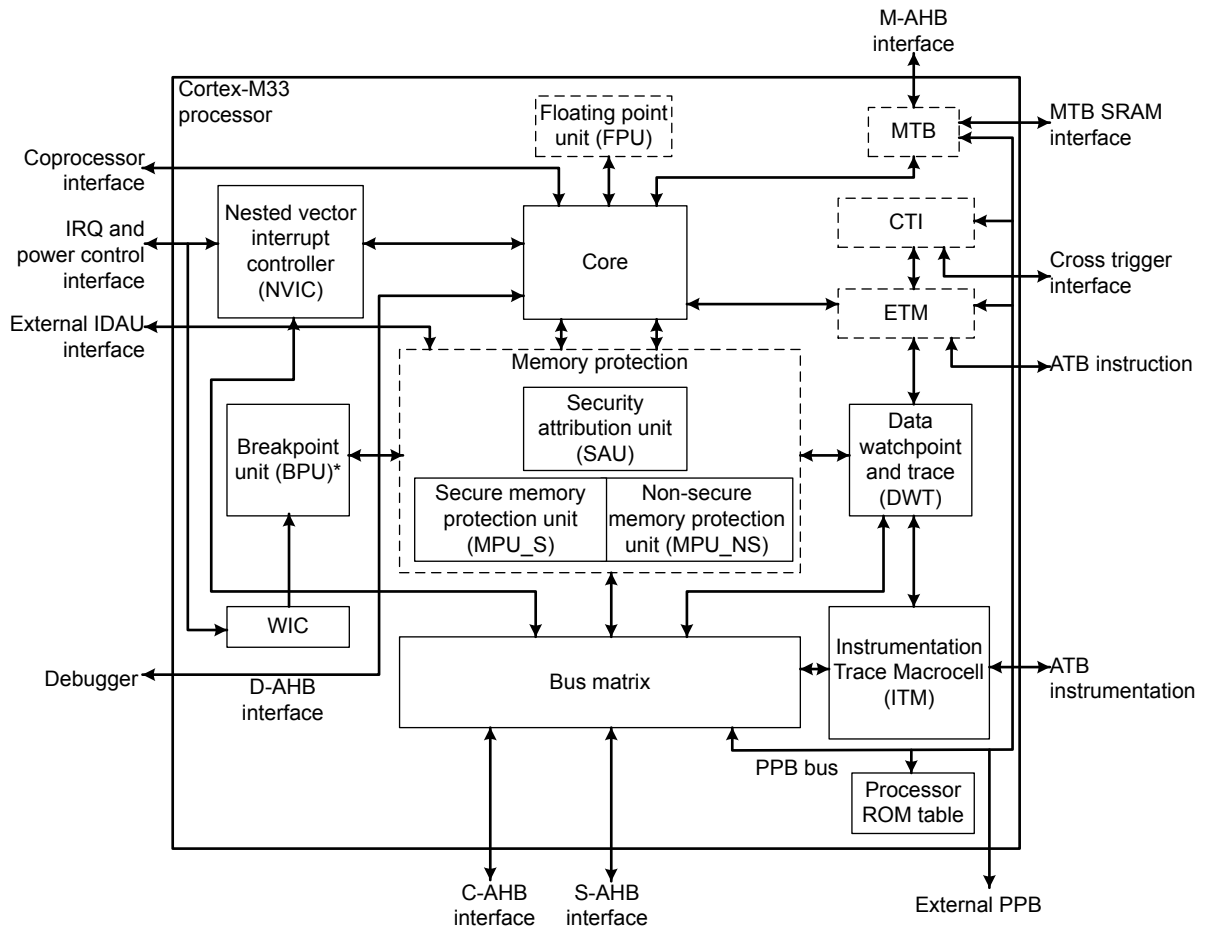
* Flash patching is not supported in the Cortex-M33 processor.

Cortex-M33 key features

- Arm-v8M Architecture with 2-/3-stage pipeline, Harvard, 1,4 DMIPS/MHz
- Single-cycle branch, no branch prediction
- Hardware divide instruction
- Debug (CoreSight™ compliant)
- Memory exclusive instructions
- NVIC without interrupts increased up to 480 max (256 priority levels)
- Enhanced MPU, more flexible (32 bytes) up to 16 regions (for each one of the secure and non-secure states)
- New AMBA® 5 AHB interface, support of security state extension to the system
- Support of external implementation defined attribution unit
- Fully compatible with TrustZone system

The differences between Cortex-M4 and Cortex-M33 are presented in the table below.

Table 30. Comparison of Cortex-M4 and Cortex-M33

Feature	Cortex-M4	Cortex-M33
Instruction set architecture	Armv7-M	Armv8-M mainline
	Thumb, Thumb-2	
Pipeline	Three-stages	
Performance efficiency (CoreMark™/ MHz)	3.40	4.02
DMIPS/MHz	1.25	1.50
Memory protection	Yes	
Maximum MPU regions	8	8 for secure and 8 for non-secure
Trace (ETM or MTB)	ETMv3	MTB and/or ETMv4
DSP	Yes	
Floating point hardware	Yes	
Bus protocol	AHB Lite, APB	AHB5
Max. number of external interrupts	240	480
CMSIS support	Yes	
TrustZone for Armv8-M	No	Yes
Coprocessor interface	No	Yes

5.2.3 Software point of view

The Cortex-M33 has the same features than the Cortex-M4, but includes also the following features:

- Armv8-M architecture
- Latest floating-point unit (FPU) specification (based on Arm FPv5 architecture) that adds more instructions than the Cortex-M4 has
- AHB5 specification used for the system and memory interface to extend security across the whole system
- Latest version of the memory protection unit (MPU) specification used to simply the setup of regions
- Extends the number of maximum interrupts to 480
- Optional execution trace using MTB or ETM
- Enhanced debug components to make simplify usage
- Coprocessor interface supporting up to eight coprocessors units
- Hardware stack limit checking
- TrustZone security features adding efficient security features

The Cortex-M33 enhancements compared to Cortex-M4 are illustrated in the figure below.

Figure 10. Cortex-M33 enhancements versus Cortex-M4
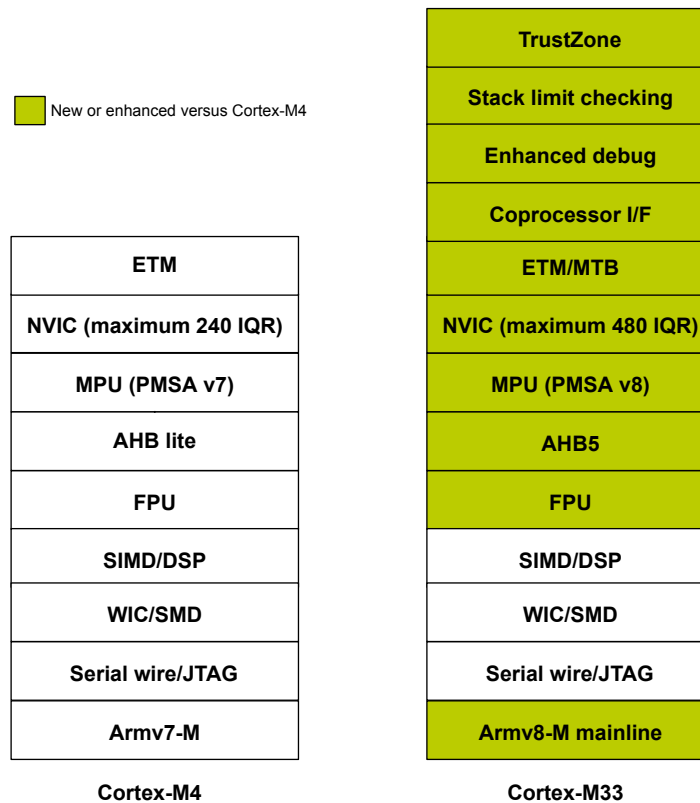
5.3 Cortex mapping overview

The mapping is different on the Cortex-M4 and the Cortex-M33, as shown in the table below.

Table 31. Cortex overview mapping for STM32L4, STM32L4+ and STM32L5 Series

-		STM32L4 and STM32L4+ Series	STM32L5 Series
Core	Architecture	Cortex-M4	Cortex-M33
	NVIC	• Maskable interrupt channel: – 94 (STM32L4+) – 91(STM32L49/4Axxx) – 82 (STM32L47/48xxx) – 67 (STM32L41/42/43/44/45/46xxx)	109 maskable interrupt channels (not including the 16 Cortex-M33 with FPU interrupt lines)
	EXTI	• Up to 41 event/interrupt (STM32L4+ and STM32L49/4Axxx) • Up to 40 event/interrupt (STM32L47/48xxx) • Up to 37 event/interrupt (STM32L41/42/43/44/45/46xxx)	• 42 event/interrupt
Mapping	System timer	0xE000 E010 to 0xE000 E01F	0xE000 E010 to 0xE000 E0FF
	NVIC	0xE000 E100 to 0xE000 E4EF	0xE000 E100 to 0xE000 ECFF
	MPU	0xE000 ED90 to 0xE000 EDB8	0xE000 ED90 to 0xE000 EDB8
	FPU	0xE000 EF30 to 0xE000 EF44	0xE000 EF30 to 0xE000 EF44

6 Conclusion

This application note is a complement to the STM32L4, STM32L4+ and STM32L5 Series datasheets and reference manuals.

This document provides a simple guideline to migrate an existing application based on the STM32L4 Series and STM32L4+ Series, to the STM32L5 Series.

Revision history

Table 32. Document revision history

Date	Version	Changes
7-Oct-2019	1	Initial release.
21-Jul-2020	2	Updated: • Title and Introduction • Table 3. Packages available on STM32L4, STM32L4+ and STM32L5 Series • Section 2.2 Pinout compatibility (table removed) • Table 9. STM32 peripheral compatibility between STM32L4, STM32L4+ and STM32L5 Series • Table 10. Peripheral address mapping differences between STM32L4, STM32L4+ and STM32L5 Series • Table 14. Interrupt vector differences between STM32L4, STM32L4+ and STM32L5 Series • Table 19. PWR controller features for STM32L4, STM32L4+ and STM32L5 Series • Figure 7. STM32L5 Series power supply overview (without SMPS) • Section 4.13 Extended interrupt and event controller (EXTI) • Table 24. Flash memory comparison between to STM32L4, STM32L4+ and STM32L5 Series • Table 25. U(S)ART differences between STM32L4, STM32L4+ and STM32L5 Series • Table 27. USB differences between STM32L4, STM32L4+ and STM32L5 Series

Contents

List of tables

List of figures

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.