
LIS25BA: low-noise, high-bandwidth 3-axis digital output accelerometer with TDM interface

Introduction

This document is intended to provide usage information and application hints related to ST's LIS25BA motion sensor.

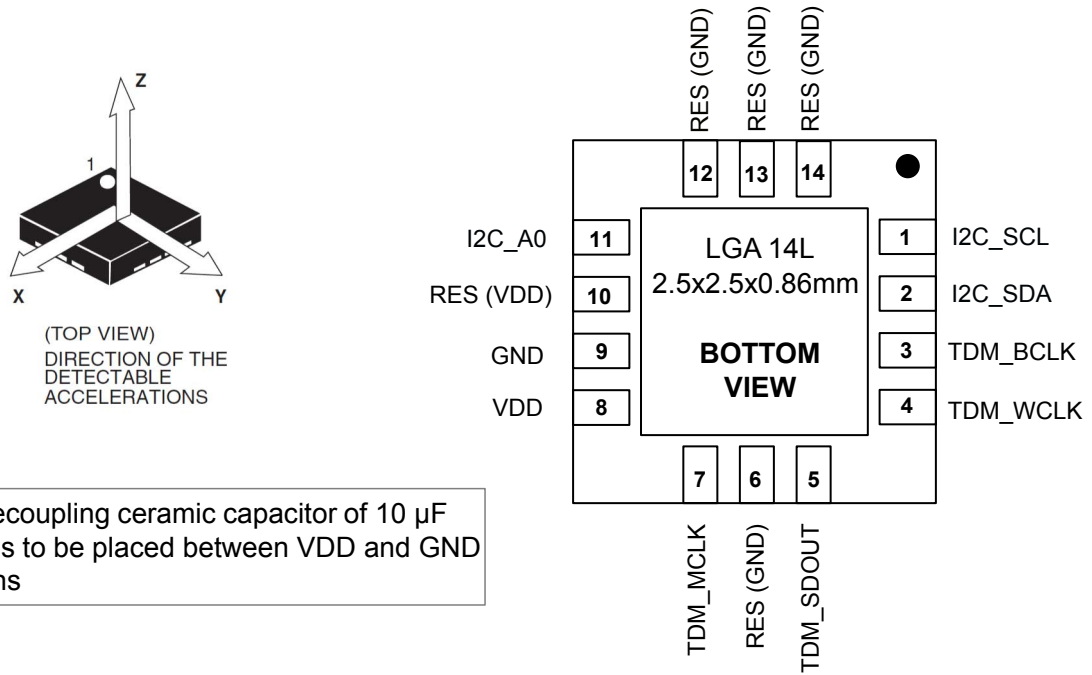
The LIS25BA is a high-performance 3-axis MEMS accelerometers with low-noise, high and flat bandwidth and a Time-Division Multiplexing (TDM) interface.

The device has a full-scale acceleration range of $\pm 3.85 g$, a 16-bit data output and is capable of measuring accelerations with a signal bandwidth of 2400 Hz.

Thanks to its high bandwidth, the LIS25BA is particularly suitable for hearables or smart headphones, where it can significantly improve the audio quality, especially in systems using ST MEMS microphones to implement noise-canceling functions. The device key applications are bone vibration detection, beam forming enhancement and voice detection enhancement.

The LIS25BA is available in a small thin plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

1 Pin description

Figure 1. Pin connections


Decoupling ceramic capacitor of 10 μ F has to be placed between VDD and GND pins

Pin #	Name	Function	Pin status
1	I2C_SCL	I ² C serial clock - SCL	Default: input open-drain
2	I2C_SDA	I ² C serial data - SDA	Default: input open-drain
3	TDM_BCLK	TDM bit clock	Default: input open-drain
4	TDM_WCLK	TDM word clock	Default: input open drain
5	TDM_SDOUT	TDM serial data output	Default: input open-drain
6	RES (GND)	Connect to GND	Connect to GND
7	TDM_MCLK	TDM master clock	Default: input open-drain
8	VDD	Power supply	Power supply
9	GND	0 V power supply	0 V power supply
10	RES (VDD)	Connect to VDD	Connect to VDD
11	I2C_A0	I ² C slave address selection	Default: input with pull-down
12	RES (GND)	Connect to GND	Connect to GND
13	RES (GND)	Connect to GND	Connect to GND
14	RES (GND)	Connect to GND	Connect to GND

2 Registers

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TEST_REG	0Bh	0	0	0	0	ST	0	0	0
WHO_AM_I	0Fh	0	0	1	0	0	0	0	0
TDM_cmax	24h	0	0	0	0	TDM_cmax11	TDM_cmax10	TDM_cmax9	TDM_cmax8
TDM_cmax	25h	TDM_cmax7	TDM_cmax6	TDM_cmax5	TDM_cmax4	TDM_cmax3	TDM_cmax2	TDM_cmax1	TDM_cmax0
CTRL_REG	26h	0	0	PD	0	0	0	0	0
TDM_CTRL_REG	2Eh	TDM_pd	Delayed	data_valid	mapping	0	WCLK_fq1	WCLK_fq0	0
AXES_CTRL_REG	2Fh	AXISZ_EN	AXISY_EN	AXISX_EN	0	0	0	0	ODR_AUTO_EN

3 Operating modes

The LIS25BA provides two operating modes:

- Disabled mode;
- Normal mode.

After the power supply is applied, the LIS25BA performs a 5.5 ms boot procedure to load the trimming parameters. After the boot is completed, the accelerometer is automatically configured in Disabled mode.

The LIS25BA provides two interfaces:

- I²C digital interface, which is used to configure the device;
- TDM interface, which is used to retrieve acceleration data.

When the sensor is in Disabled mode, almost all the internal blocks of the device are switched off. The I²C digital interface remains active to allow the communication with the device.

The LIS25BA can be configured in Normal mode by setting the PD bit of CTRL_REG register to 0: in Normal mode, the sensing chain is active.

In order to gather acceleration output data, the TDM interface must be enabled. It is recommended to set all TDM interface clocks (MCLK, BCLK and WCLK) before enabling the interface itself. The TDM interface can be enabled by setting the TDM_pd bit of TDM_CTRL_REG register to 0.

3.1 TDM interface configuration

The TDM interface can be configured through the TDM_CTRL_REG register.

Table 1. TDM_CTRL_REG (2Eh)

b7	b6	b5	b4	b3	b2	b1	b0
TDM_pd	Delayed	data_valid	mapping	0	WCLK_fq1	WCLK_fq0	0

- TDM_pd: TDM enable. If the TDM_pd bit is set to 0, the TDM interface is enabled, otherwise it is disabled.
- Delayed: TDM delayed configuration. If the Delayed bit is set to 0, TDM works with 'no-delayed' configuration, otherwise it works with 'delayed' configuration. Selecting 'no delayed' configuration, SLOT0 data is sampled on the first rising/falling edge (based on the value of the data_valid bit, as described below) after the rising edge of WCLK, otherwise selecting 'delayed' configuration, SLOT0 data is sampled on the second rising/falling edge after the rising edge of WCLK.
- data_valid: TDM data valid configuration. If the data_valid bit is set to 0, the data is sampled on the rising edge of the bit clock (BCLK), otherwise it is sampled on the falling edge.
- mapping: TDM mapping configuration. If the mapping bit is set to 0, accelerometer X-Y-Z data are mapped respectively in SLOT0, SLOT1, SLOT2, otherwise they are mapped in SLOT4, SLOT5, SLOT6. During the transfer of non-active slots, the TDM_SDOOUT pin is configured in high-impedance.
- WCLK_fq: TDM clock frequencies, described in the following section.

The LIS25BA offers four possible configurations for the TDM interface: the following table summarizes Delayed and data_valid configuration associated to each TDM configuration supported.

Table 2. TDM configuration

Delayed	data_valid	TDM configuration
0	0	SLOT0 on first rising edge of BCLK after rising edge of WCLK
0	1	SLOT0 on first falling edge of BCLK after rising edge of WCLK
1	0	SLOT0 on second rising edge of BCLK after rising edge of WCLK
1	1	SLOT0 on second falling edge of BCLK after rising edge of WCLK

3.2 TDM clock frequency

The function of the WCLK signal is simply to identify the beginning of a frame; in particular the frame starts at the rising edge of the WCLK signal. The supported WCLK widths are:

- 16-slot width (1024 BCLK periods, 50% duty cycle);
- One-slot width (16 BCLK periods);
- One BCLK period.

In TDM mode, the LIS25BA can output accelerometer data on the TDM_SDOOUT pin at the following sampling rates:

- WCLK = 8 kHz;
- WCLK = 16 kHz;
- WCLK = 24 kHz.

TDM clock frequency can be selected in two different ways:

- Using WCLK_fq[1:0] bits of TDM_CTRL_REG register. In this case the ODR_AUTO_EN bit of the AXES_CTRL_REG register must be set to 0. Available configurations for WCLK_fq bits are:
 - 00b: sampling rate equal to 8 kHz;
 - 01b: sampling rate equal to 16 kHz;
 - 10b: sampling rate equal to 24 kHz.
- Using the output of the ODR_auto block (described in the LIS25BA datasheet) which receives as inputs both MCLK and the WCLK and computes the current sampling frequency as a ratio between MCLK and WCLK. The ODR_auto block can be enabled by setting to 1 the ODR_AUTO_EN bit of the AXES_CTRL_REG register. Depending on the ratio between the MCLK and WCLK signals, the possible outputs of the ODR_auto block are:
 - sampling rate equal to 8 kHz (MCLK/WCLK = 1536);
 - sampling rate equal to 16 kHz (MCLK/WCLK = 768);
 - sampling rate equal to 24 kHz (MCLK/WCLK = 512).

Note: if the ratio between MCLK and WCLK differs from 1536, 768 and 512, the sampling is automatically forced to 8 kHz.

The sole purpose of the serial clock BCLK is to shift the data out of the serial TDM_SDOOUT port. For this purpose, the TDM interface uses an internal counter that is set to one when the rising edge of the WCLK is detected, and it is reset to zero when the maximum number of BCLK in a WCLK period is reached.

The maximum number of BCLK contained in a WCLK period, called c_{max} , can be expressed as a function of both the BCLK and WCLK frequencies, and can be computed using the following equation:

$$c_{max} = \frac{BCLK}{WCLK} - 1$$

In order to support a serial clock BCLK variable in the range [1024 MHz, 12.288 MHz], and consequently to compute the correct maximum value of the internal TDM counter, two possible solutions can be selected:

- The c_{max} value at the input of the TDM interface can be computed automatically by the device. This functionality by default is enabled, and can be disabled by setting the ODR_AUTO_EN bit of the AXES_CTRL_REG to 0.
- The TDM c_{max} can be programmed through the register TDM_cmax.

3.3 Axis disable

In TDM mode, the host processor can power down each axis of the LIS25BA accelerometer selectively by deasserting the AXISX_EN, AXISY_EN, AXISZ_EN bits of the AXES_CTRL_REG register in order to reduce power consumption during operation. When an axis is powered down, the corresponding TDM slot will be put in high-impedance.

The datasheet provides typical and maximum current consumption for each mode (mono-axial, bi-axial or tri-axial mode).

3.4 Configuration switches

The TDM interface must be activated explicitly from the I²C interface. The first 3 samples after enabling the TDM interface must be discarded: this is due to the interface synchronization on the external WCLK. Moreover, TDM protocol can be reconfigured on the fly, but also in this case the first 3 samples after the TDM configuration change will be invalid.

4 Reading output data

4.1 Startup sequence

Once the device is powered up, it automatically downloads the calibration coefficients from the embedded flash to the internal registers. When the boot procedure is completed, the accelerometer automatically enters Disabled mode.

To turn on the accelerometer and gather acceleration data through the TDM interface, it is necessary to select the operating Normal mode through the PD bit of CTRL_REG register and enable the TDM interface through the TDM_pd bit of TDM_CTRL_REG.

The following general-purpose sequence can be used to configure the accelerometer:

```
1. Write CTRL_REG = 00h // Normal mode
2. Provide MCLK, BCLK and WCLK to TDM interface
3. Write TDM_CTRL_REG = 0xxx0000b // TDM enable and configuration selection
4. Wait 4.5 ms // Wait the duration of the turn-on time
5. Start gathering acceleration data from TDM interface
```

4.2 Understanding output data

The measured acceleration data are sent to the TDM interface slots configured through the mapping bit of the TDM_CTRL_REG register.

Acceleration output data are represented as 16-bit numbers in two's complement format.

Once retrieved from the active slots of the TDM interface, acceleration data must be converted to mg by multiplying the sensitivity value indicated in the datasheet: 0.122 mg / LSB (typ.).

4.2.1 Examples of output data

The following table provides a few basic examples of the accelerometer data that is read from the TDM output slots when the device is subjected to a given acceleration.

The values listed in the following tables are given under the hypothesis of perfect device calibration (i.e. no offset, no gain error, ...).

Acceleration value [mg]	LSB (hexadecimal)	LSB (signed decimal)
0	0000h	0
350 mg	0B34h	2868
1000 mg	2004h	8196
-350 mg	F44Ch	-2868
-1000 mg	DFFCh	-8196

5 Self-test

The embedded self-test functions allows checking the device functionality without moving it.

When the self-test is enabled, an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels which are related to the full scale through the sensitivity value.

The accelerometer self-test function can be configured through the ST bit of the TEST_REG register: it is off when the ST bit is set to 0; it is enabled when the ST bit is set to 1.

When the accelerometer self-test is activated, the sensor output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force.

The procedure consists of:

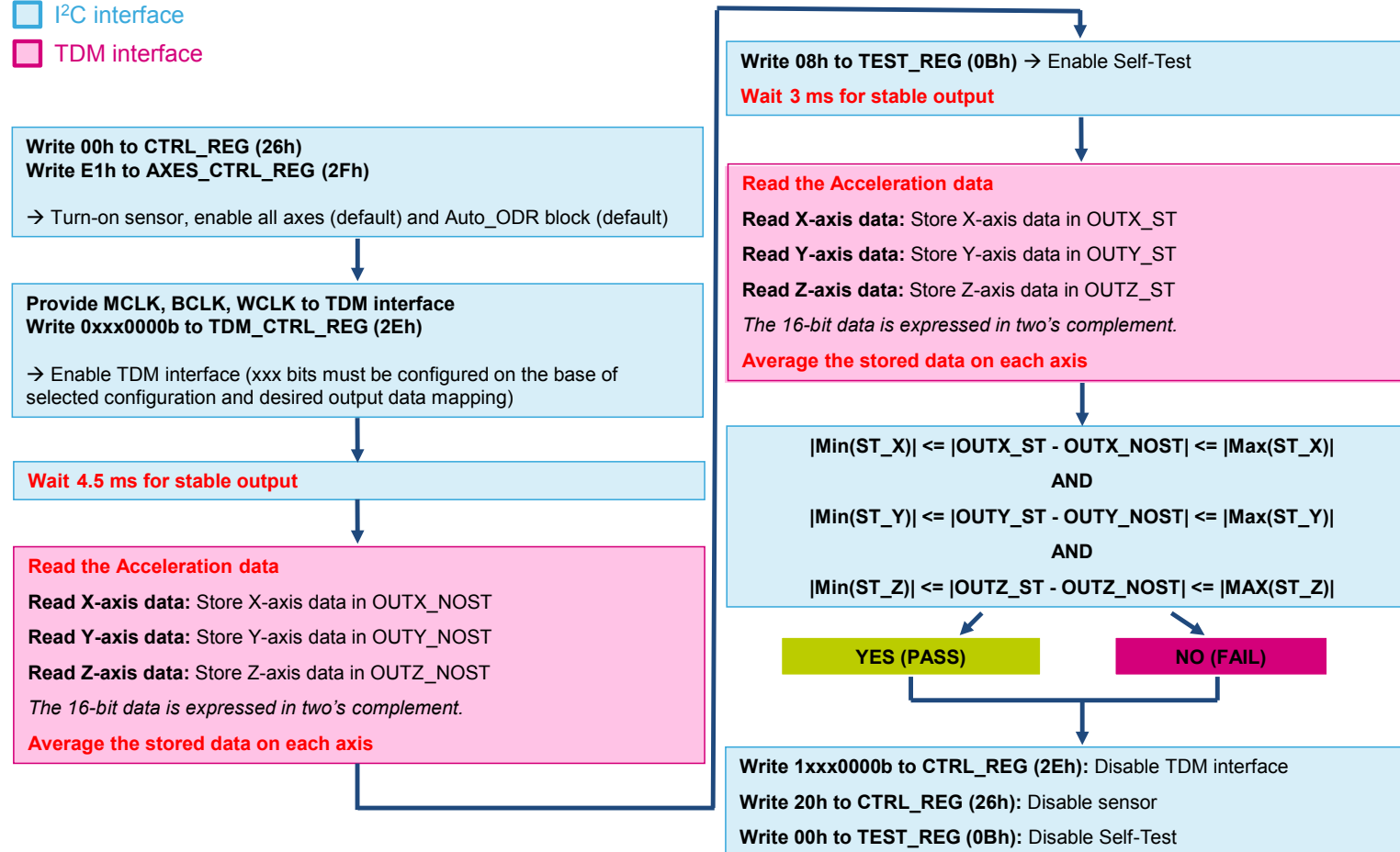
1. enabling the accelerometer and TDM interface;
2. averaging 5 samples before enabling the self-test;
3. averaging 5 samples after enabling the self-test;
4. computing the difference in absolute value for each axis and verifying that it falls within a given range. The minimum and maximum values are provided in the datasheet.

The complete self-test procedure is indicated in [Figure 2. Accelerometer self-test procedure](#).

Figure 2. Accelerometer self-test procedure

Note: keep the device still during self-test procedure

- I²C interface
- TDM interface



Revision history

Table 3. Document revision history

Date	Version	Changes
24-May-2018	1	Initial release
14-Jan-2020	2	Update concerning ODR_auto block in Section 3.2 TDM clock frequency

Contents

1	Pin description	2
2	Registers	3
3	Operating modes	4
3.1	TDM interface configuration	4
3.2	TDM clock frequency	4
3.3	Axis disable	5
3.4	Configuration switches	5
4	Reading output data	7
4.1	Startup sequence	7
4.2	Understanding output data	7
4.2.1	Examples of output data	7
5	Self-test	8
	Revision history	10

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