Application note

Using STM32L5 Series cache to optimize performance and power efficiency

Introduction

This application note describes the instruction cache (ICACHE), the first cache developed by STMicroelectronics.

Embedded in the STM32L5 Series microcontroller, the ICACHE introduced on the C-AHB bus of the Arm® Cortex®-M33 processor, allows the users to improve their application performance when fetching instruction and data, from both internal and external memories.

This document gives some typical examples in order to highlight the ICACHE features and facilitate its configuration.

1 Overview of the ICACHE in the STM32L5 Series

This section provides an overview of the ICACHE interface embedded in the STM32L5 Series Arm® Cortex® core-based microcontrollers.

This section details the ICACHE multiple features and its integration in the system architecture.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

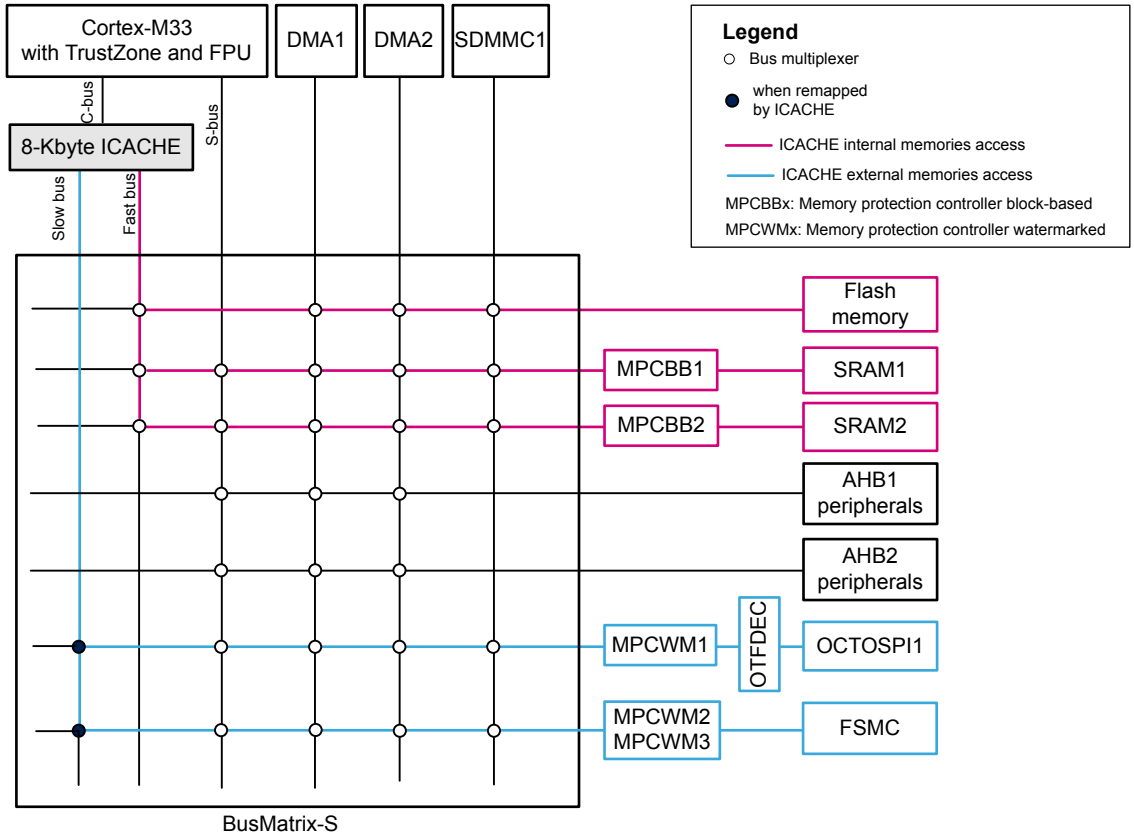
arm

1.1 STM32L5 Series smart architecture

The STM32L5 Series smart architecture is based on a bus matrix allowing multiple masters (Cortex-M33, ICACHE, DMA1/2 and SDMMC1) to access multiple slaves (such as Flash memory, SRAM1/2, OCTOSPI1 or FSMC).

The figure below describes the STM32L5 Series smart architecture.

Figure 1. STM32L5 Series smart architecture

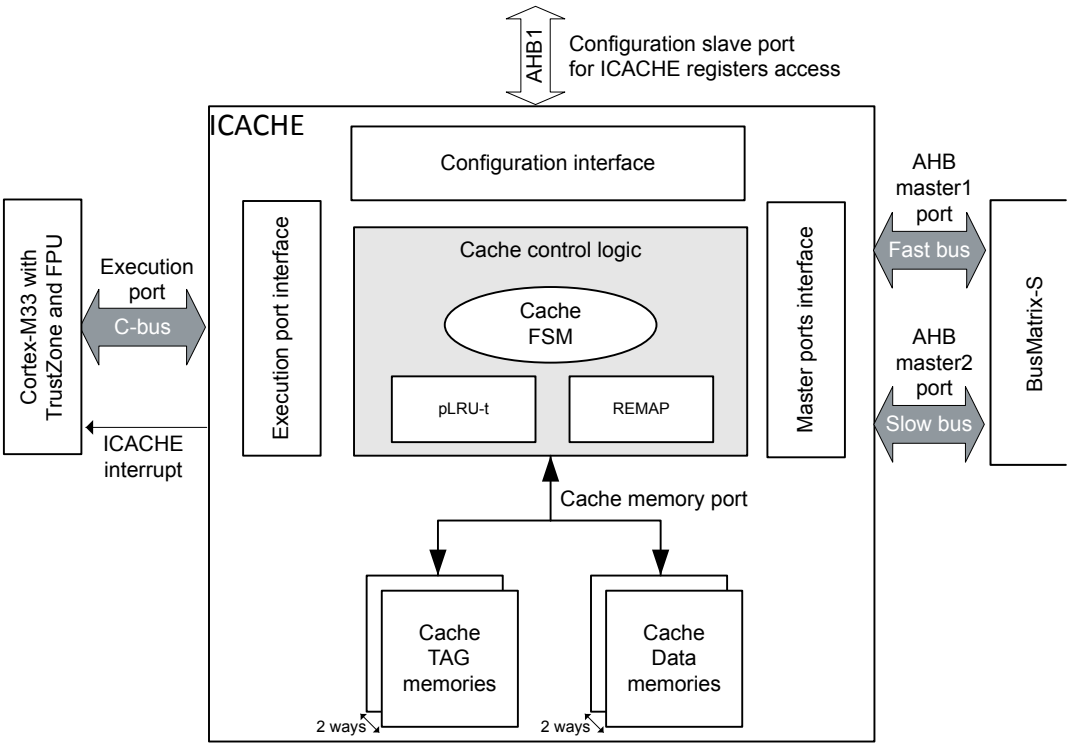


Thanks to the ICACHE interface introduced to its C-AHB bus, the Cortex-M33 performance is improved when fetching code or data from the internal memories (Flash memory, SRAM1 or SRAM2) via the Fast bus, and also from the external memories (OCTOSPI1 or FSMC) via the Slow bus.

1.2 ICACHE block diagram

The ICACHE block diagram is given in the figure below.

Figure 2. ICACHE block diagram



The ICACHE memory includes:

- the TAG memory with:
  - the address tags that indicate which data are contained in the cache Data memory
  - the validity bits
- the Data memory, that contains the cached data

1.3 STM32L5 Series ICACHE features

1.3.1 Dual masters

The ICACHE accesses the AHB bus matrix over two AHB master ports: master1 (Fast bus) and master2 (Slow bus). This feature allows the traffic to be decoupled when accessing different memory regions (such as internal Flash memory, internal SRAM and external memories), in order to reduce the CPU stalls on cache misses.

The following table summarizes the STM32L5 Series memory regions and their addresses.

Table 1. Regions of the STM32L5 Series memories

Peripheral		Cacheable memory access		Not cacheable memory access	
Type	Name	Bus name	Region address	Bus name	Region address
Internal	FLASH	ICACHE Fast bus	[0x0800 0000 to 0x0807 FFFF]	N/A	N/A
	SRAM1		[0x0A00 0000 to 0x0A02 FFFF]	S-bus	[0x2000 0000 to 0x2002 FFFF]
	SRAM2		[0x0A03 0000] to [0x0A03 FFFF]		[0x2003 0000 to 0x2FFF FFFF]
External	OCTOSPI1	ICACHE Slow bus (1)	Alias address in the range of [0x0000 0000 to 0x07FF FFFF] or [0x1000 0000:0x1FFF FFFF] defined by means of remapping feature		[0x9000 0000 to 0x9FFF FFFF]
	FSMC				Bank 1: [0x6000 0000 to 0x6FFF FFFF] Bank 3: [0x8000 0000 to 0x8FFF FFFF]

1. *To be selected when remapping such regions.*

1.3.2 1-way versus 2-way cache

By default, the ICACHE is configured in associative operating mode (two ways enabled), but it is possible to configure the ICACHE in direct mapped mode (one way enabled), for applications requiring a very-low power consumption. The ICACHE configuration is done with the WAYSEL bit in the ICACHE_CR register as follows:

- WAYSEL = 0: direct mapped operating mode (1-way)
- WAYSEL = 1 (default): associative operating mode (2-way)

Table 2. 1-way versus 2-way cache

Parameter	1-way cache	2-way cache
Cache size (Kbytes)	8	
Cache number of ways	1	2
Cache line size	128 bits (16 bytes)	
Number of cache lines	512	256 per way

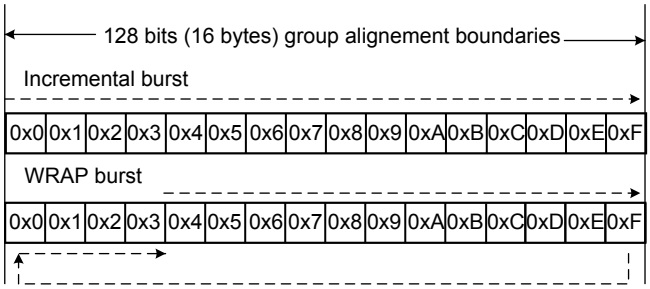
1.3.3 Burst type

Some Octo-SPI memories support the WRAP burst, that provides the benefit of critical-word-first feature performance. The ICACHE burst type of the AHB memory transaction for remapped regions is configurable. It implements incremental burst or WRAP burst, selected with the HBURST bit in the ICACHE_CRRx register.

The differences between the WRAP and the incremental bursts are given below (see also the figure):

- WRAP burst:
  - cache line size = 128 bits
  - burst starting address = word address of the first data requested by the CPU
- Incremental burst:
  - cache line size = 128 bits
  - burst starting address = address aligned on the boundary of the cache line containing the requested word

Figure 3. Incremental versus WRAP burst



1.3.4 Cacheable regions and remapping feature

The ICACHE is connected to the Cortex-M33 via the C-AHB bus, and caches the code region from addresses [0x0000 0000 to 0x1FFF FFFF].

Since the external memories are mapped at an address in the range [0x6000 0000 to 0x9FFF FFFF], the ICACHE supports a remap feature that allows any external memory region to be remapped at an address in the range of [0x0000 0000 to 0x07FF FFFF] or [0x1000 0000 to 0x1FFF FFFF], and to become accessible through the Slow bus.

Up to four external memory regions can be remapped with this feature.

Once a region is remapped, the remap operation occurs even if the ICACHE is disabled or if the transaction is not cacheable.

The cacheable memory regions can be defined and programmed by the user in the memory protection unit (MPU). The table below summarizes the configurations of the STM32L5 Series memories.

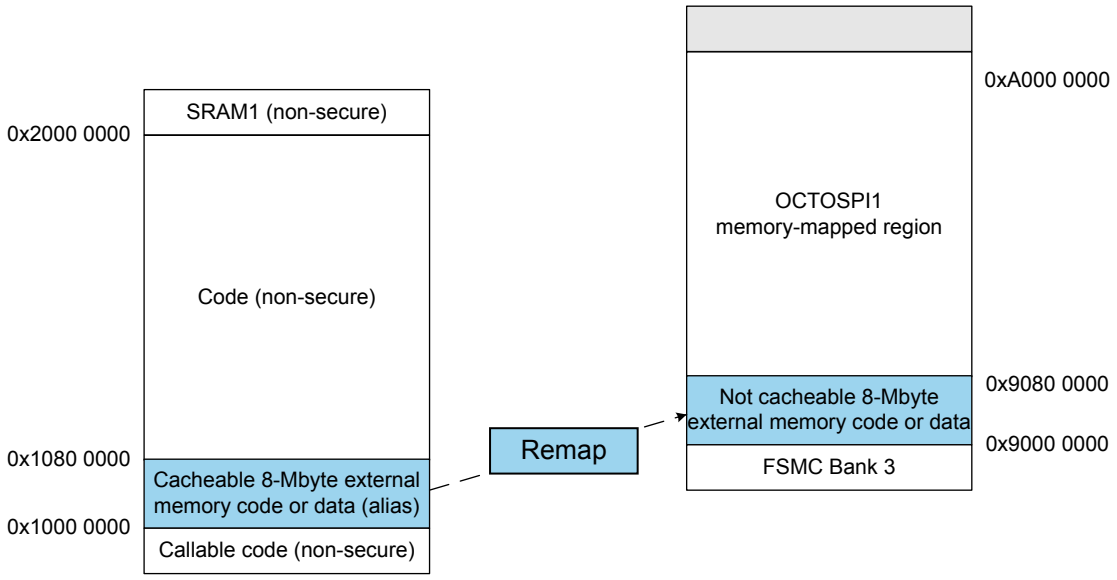
Table 3. Configuration of STM32L5 Series memories

Product memory	Cacheable (MPU programming)	Remapped in ICACHE (ICACHE_CRRx programming)
Flash memory	Yes or No	Not required
SRAM	Not recommended	
External memories (OCTOSPI or FSMC)	Yes or No	Required if the user wants external code fetching on C-AHB bus (else on S-AHB bus)

1.3.5 Benefit of ICACHE external memory remapping

The example in the figure below, shows how to benefit from the ICACHE enhanced performance during code execution or data read when accessing an external 8-Mbyte external Octo-SPI memory (such as external Flash memory or RAM).

Figure 4. Octo-SPI memory remap example



The following steps are needed to remap this external memory:

1. OCTOSPI configuration for the external memory

   Configure the OCTOSPI interface in order to access the external memory in Memory mapped mode (the external memory is seen as an internal memory mapped in the [0x9000 0000 to 0x9FFF FFFF] region). Since the external memory size is 8 Mbytes, it is seen at the region [0x9000 0000 to 0x907F FFFF]. The external memory at this region is accessed via the S-bus and is not cacheable. The next step shows the ICACHE configuration in order to remap this region.

Note: For the OCTOSPI configuration in memory-mapped mode, refer to the application note Octo-SPI interface on STM32 microcontrollers (AN5050).

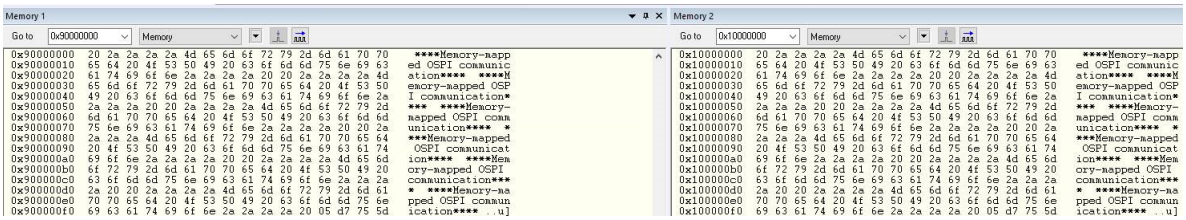
2. ICACHE configuration to remap the external memory mapped region

   The 8 Mbytes placed in the [0x9000 0000 to 0x907F FFFF] region are remapped to the [0x1000 0000 to 0x107F FFFF] region. It can then be accessed through the Slow bus (ICACHE master2 bus).

   – ICACHE_CR register configuration
     a. Disable ICACHE with EN = 0.
     b. Select 1-way or 2-ways (depending on the application needs) with WAYSEL = 1 or 0.
   – ICACHE_CRRx register configuration (up to four regions, x = 0 to 3)
     a. Select the 0x1000 0000 base address (remap address) with BASEADDR [28:21] = 0x80.
     b. Select the 8-Mbyte region size to remap with RSIZE[2:0] = 0x3.
     c. Select the 0x9000 0000 remapped address REMAPADDR[31:21] = 0x480.
     d. Select the ICACHE AHB master2 port for external memories with MSTSEL = 1.
     e. Select the WRAP burst type with HBURST = 0.
     f. Enable the remapping for region x with REN = 1.

   The following figure shows how the memory regions are seen with IAR after enabling the remap.

Figure 5. Memory regions remapping example



   The 8-Mbyte external memory is now remapped and can be accessed over the [0x1000 0000 to 0x107F FFFF] region.

3. ICACHE enable

   – ICACHE_CR register configuration

     Enable the ICACHE with EN = 1.

1.3.6 Hit and miss monitors

The ICACHE implements two monitors for cache performance analysis:

- a 32-bit **hit monitor**: counts the number of time the CPU fetches for data in the cache memory without generating a transaction on ICACHE master ports (fetched data already available in the cache).

  The hit monitor counter is available in the ICACHE_HMONR register.
- a 16-bit **miss monitor**: counts the number of time the CPU fetches for data in the cache memory and generates a transaction on ICACHE master ports, in order to load the data from the memory region (fetched data not already available in the cache).

  The miss monitor counter is available in the ICACHE_MMONR register.

Note: These two monitors do not wrap over when reaching their maximum values.

These monitors are managed from the following bits in the ICACHE_CR register:

- HITMEN bit (respectively MISSMEN bit) to enable/stop the hit (respectively miss) monitor
- HITMRST bit (respectively MISSMRST bit) to reset the hit (respectively miss) monitor

By default, theses monitors are disabled in order to reduce power consumption.

1.3.7 Maintenance

The software can invalidate the ICACHE by setting the CACHEINV bit in the ICACHE_CR register. This action invalidates the whole cache, making it empty. Meanwhile, if some remapped regions are enabled, the remap feature is still active, even when the ICACHE is disabled.

As the ICACHE only manages read transactions and does not manage write transactions, it does not ensure coherency in case of writes. Consequently, the software must invalidate the ICACHE after programming a region.

1.3.8 Security

ICACHE is a securable peripheral. It can be configured as secure through the GTZC TZSC secure configuration register. When it is configured as secure, only secure accesses are allowed to the ICACHE registers.

ICACHE can also be configured as privileged through the GTZC TZSC privilege configuration register. When ICACHE is configured as privileged, only privileged accesses are allowed to the ICACHE registers.

By default, the ICACHE is non-secure and non- privileged through the GTZC TZSC.

1.3.9 Events and interrupt management

The ICACHE manages the functional errors when detected, by setting the ERRF flag in ICACHE_SR. An interrupt can also be generated if the ERRIE bit is set in ICACHE_IER.

In case of ICACHE invalidation, when the cache busy state finished, the BSYENDF flag is set in ICACHE_SR. An interrupt can also be generated if the BSYENDIE bit is set in ICACHE_IER.

The table below lists the ICACHE interrupts and events flags.

Table 4. ICACHE Interrupt and events management bits

Register	Bit name	Bit description	Bit access type
ICACHE_SR	BUSYF	Cache executing a full invalidate operation	Read-only
	BSYENDF	Cache invalidation operation finished	
	ERRF	An error occurred during caching operation	
ICACHE_IER	ERRIE	Enable interrupt for cache error	Read/write
	BSYENDIE	Enable interrupt in case of invalidation operation finished	
ICACHE_FCR	CERRF	Clears ERRF in ICACHE_SR	Write-only
	CBSYENDF	Clears BSYENDF in ICACHE_SR	

2 Conclusion

The STM32L5 Series MCUs provide the first cache developed by STMicroelectronics, ICACHE, able to cache internal and external memories, offering performance enhancement for data and instruction fetches. This application note shows the different features supported by the ICACHE, its configuration simplicity and flexibility allowing lower development cost and faster time to market.

Revision history

Table 5. **Document revision history**

Date	Version	Changes
10-Oct-2019	1	Initial release.
27-Feb-2020	2	Updated: • Table 1. Regions of the STM32L5 Series memories • Section 1.3.7 Maintenance • Section 1.3.8 Security

Contents

List of tables

List of figures