Low-voltage Power MOSFET switching behavior and performance evaluation in motor control application topologies

Introduction

During the last years, some applications based on electrical power conversion are gaining more and more space in the civil and industrial fields.

The constant development of microprocessors and the improvement of modulation techniques, which are useful for the control of power devices, have led to a more accurate control of the converted power as well as of the power dissipation, thus increasing the efficiency of the motor control applications.

Nowdays, frequency modulation techniques are used to control the torque and the speed of brushless motors in several high- and low-voltage applications and in different circuit topologies using power switches in different technologies such as MOSFETs and IGBTs.

Therefore, the devices have to guarantee the best electrical efficiency and the least possible impact in terms of emissions.

The aim of this application note is to provide a description of the most important parameters which are useful for choosing a low-voltage Power MOSFET device for a motor control application.

Three different motor control applications and topology cases are deeply analyzed to offer to motor drive designers the guidelines required for an efficient and reliable design when using the MOSFET technology in hard-switch applications:

- BLDC motor in a 3-phase inverter topology
- DC motor in H-bridge configuration
- DC motor in single-switch configuration

1 Control techniques and brushless DC (BLDC) motors

During the last years, servomotors have evolved from mostly brush to brushless type. This choice has been driven by the lower maintenance required and the higher reliability of brushless motors.

As brushless motors have become more prevalent, the circuit and system techniques used to drive them have evolved as well.

Most of the high-performance servo systems employ an inner control loop that regulates torque. The torque produced by a brush motor is fairly easy to control because the motor commutates itself. Torque is proportional to the DC current in the two terminals of the motor, regardless of the speed. Torque control can therefore be implemented through a P-I feedback loop which adjusts the voltage applied to the motor in order to minimize the error between the motor current requested and the one measured.

Given that brushless motors are not self-commutating, they are more complicated to control.

A BLDC motor has a rotor with permanent magnets and a stator with windings; the brushes and the commutator have been eliminated, and the windings are connected to the electronic control which replaces the function of the commutator and properly energize them. The windings are energized in a pattern which rotates around the stator; its winding leads the rotor magnet and switches just as the rotor aligns with the stator. The system needs 3 sensors to determine the position of the rotor (Hall sensor or encoder).

Whenever the rotor magnetic poles pass near the Hall sensors, they give a high or a low signal, indicating that the N or S pole passes near the sensors. Torque is produced because of the interaction between the magnetic field generated by the stator coils and the permanent magnets. Ideally, the peak torque occurs when these two fields are at 90° to each other and falls off as the fields move together. Speed and torque are linked by relations similar to those found on DC motors.

Therefore, the electronics required to drive brushless motors is substantially more complex than the one used for brush motors.

The most common control modes, for brushless motors, are trapezoidal, sinusoidal or field-oriented control (FOC).

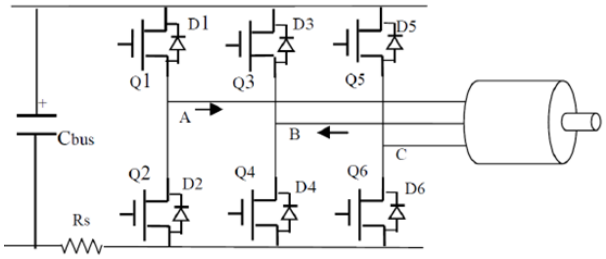
Trapezoidal commutation can be relatively efficient at high speeds, but causes torque ripple at slow speeds. Sinusoidal commutation produces smooth motion at slow speeds, but it is inefficient at high speeds. The FOC provides a smooth motion at slow speeds as well as an efficient operation at high speeds. Field-orriented control provides the best of both worlds.

2 BLDC motor in a 3-phase inverter topology

This is the most common circuit topology for applications that use a three-phase brushless motor with a full-bridge circuit controlled with the PWM technique, by means of drivers.

The following figure shows the equivalent circuit diagram with the three legs (one for each phase) made up of two Power MOSFET devices for each leg.

Figure 1. BLDC three-phase inverter



In the PWM modulation technique only a high-side device can be closed to allow current to circulate in the respective motor winding. Current flows on one or two low-side devices (not on the same leg to avoid short-circuits).

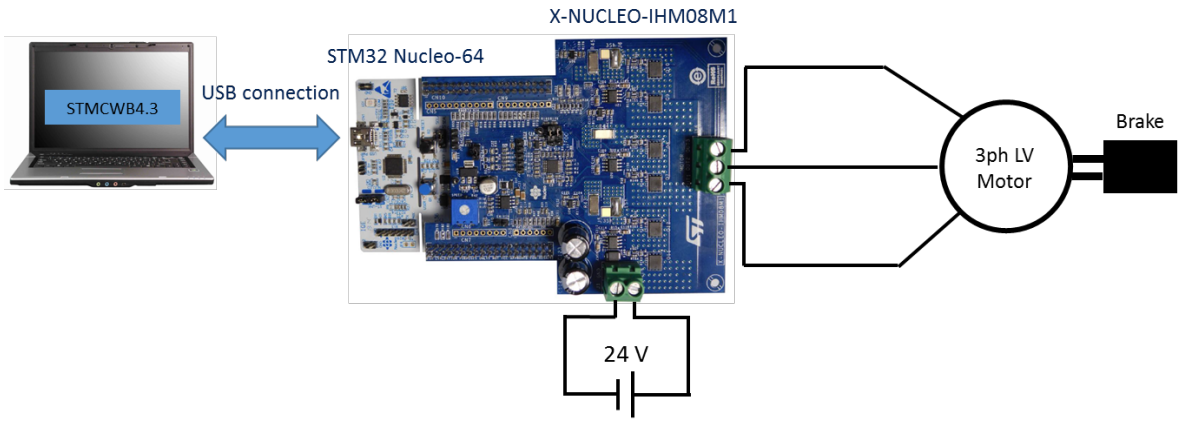
An important event occurs during the recovery phase when the switching off of a device would change the current direction of the motor winding. In this case the current continues to flow in the same direction, recirculating through the free-wheeling diodes. The amplitude as well as the duration of the recovery current must be reduced in order to reduce losses during the device switching phases. For this reason, the performance of the antiparallel diode determines the selection of the proper device.

To study a system of this type and the most important parameters involved, an application with a FOC-type motor control was chosen, and a power board equipped with a low-voltage MOSFET, a control board and a firmware have been used, all owned by STMicroelectronics. In particular:

- X-NUCLEO-IHM08M1
- STM32 Nucleo-64

The following figure shows a schematic diagram of the entire system used, including the instrumentation for the electrical analysis and the calculation of the efficiency.

Figure 2. Bench setup



2.1 System efficiency

The system efficiency is impacted by the losses produced during conduction and during the switching phases of the power devices.

Conduction losses are strictly related to the R_{DSon} resistance which is intrinsic to the device and measures the resistance offered to the current flow, when it is in the ON state, between drain and source. This resistance is proportional to temperature and increases with it.

One way of limiting losses is to keep the device temperature as low as possible with the use of appropriate heatsinks.

The drain-source on-state resistance (R_{DSon} per transistor active area) has been gradually reduced in the latest MOSFET generations, allowing the use of power transistors with smaller die sizes without provoking any negative impact on current capability and on-state losses. Smaller device die sizes and improved gate oxide structures reduce the total gate charge (Q_G) with significant enhancement in the dynamic performance of the device.

Thus, the MOSFET's figure of merit ($FoM = R_{DSon} \cdot Q_G$) becomes lower and lower offering a significant efficiency gain in high-switching frequency applications.

However, especially in synchronous rectification and in bridge configuration, the R_{DSon} and the Q_G are not the only important parameters for Power MOSFETs. The dynamic behavior of the intrinsic body-drain diode also plays an important role in the overall MOSFET performance.

The forward voltage drop (V_F) of the body-drain diode impacts the device losses during freewheeling periods (the device is in off-state and current flows from source to drain through the intrinsic diode); the reverse recovery charge (Q_{RR}) affects not only the device losses during the reverse recovery process, but also the switching behavior as the voltage spike across the MOSFET increases with Q_{RR}. So, low V_{FD} and Q_{RR} diodes can improve the overall device performance especially at high-switching frequencies.

Figure 3. Typical turn-off waveform and relevant power losses and Figure 4. Typical turn-on waveform and relevant power losses below show the typical behaviors during the turning off and on of a MOSFET device in a three-phase bridge for a motor control application. The two figures show the V_{DS} (drain-source) and the V_{GS} (gate-source) voltages of the low-side device as well as the current affecting the device under analysis (with the positive direction from drain to source).

Losses can be calculated during a single switching, multiplying the V_{DS} and I_{DS} in order to have an idea of the possible efficiency of the system or a comparison between different designs. The maximum power involved during the switching on and off of the device can be checked in order to avoid a possible thermal leakage.

Figure 3. Typical turn-off waveform and relevant power losses

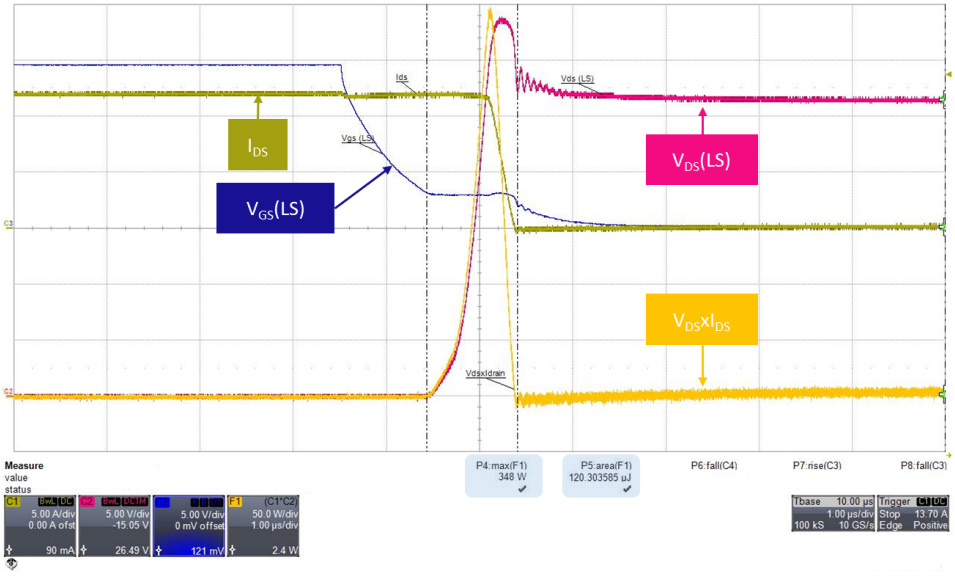
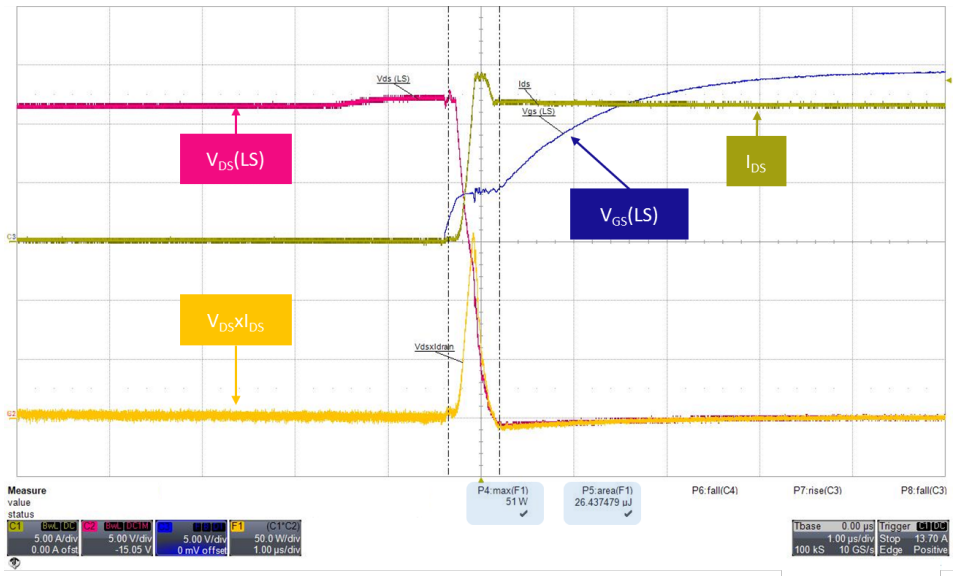


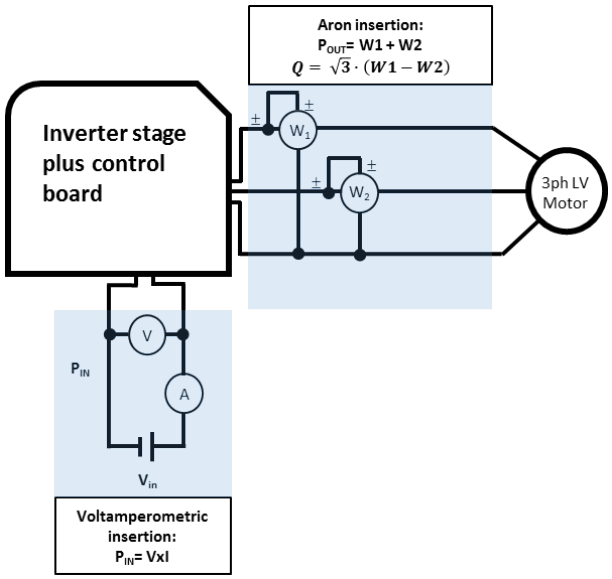
Figure 4. Typical turn-on waveform and relevant power losses



The energy efficiency of the system can be calculated based on the ratio between output power and input power.

The input power can be measured with the product voltage x the current obtained by means of a voltamperometric measurement on the system input. The output power can be calculated as the sum of the two power values obtained with measurements using the Aron insertion.

Figure 5. Bench setup for efficiency measurement with the Aron insertion



The system efficiency can be obtained using the following formula:

$$\eta = \frac{P_{OUT}}{P_{IN}}$$

The input power is calculated through a voltamperometric measurement on the system input. The power absorbed by the system is given by the sum of the power of the two wattmeters in the Aron insertion:

$$P_{OUT(Aron)} = W_1 + W_2$$

For these systems, which present ohmic-inductive load, it is often necessary also to calculate the power factor of the system as well as the reactive power absorbed by it; in this case, for systems considered as balanced, the reactive power of the system can be calculated using the power measured by the two wattmeters:

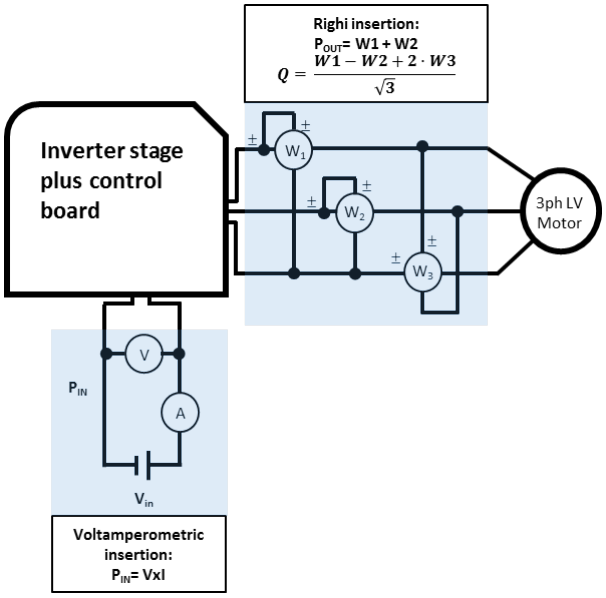
$$Q_{OUT(Aron)} = \sqrt{3} \cdot (W_1 - W_2)$$

The system power factor can be calculated:

$$cos\varphi = \text{cosarctg}\frac{Q_{OUT(Aron)}}{P_{OUT}}$$

If the load is considered unbalanced, a third wattmeter can be used, inserted in the quadrature on the wire left free, as shown in the following figure (Righi insertion).

Figure 6. Bench setup for efficiency measurement with the Righi insertion



In this case, the system efficiency will be calculated with the Aron insertion while the reactive power will be calculated using the following formula:

$$Q_{OUT(Righi)} = \frac{W_1 - W_2 + 2 \cdot W_3}{\sqrt{3}}$$

And the power factor:

$$cos\varphi = \text{cosarctg}\frac{Q_{OUT(Righi)}}{P_{OUT}}$$

The following table shows the main parameters to be taken in consideration for the calculation of the energy lost during the switching and conduction operation of two MOSFETs, used in a three-phase bridge configuration with FOC control, with the scope of estimating its efficiency.

Table 1. Device main parameters

Device	R_{on} (mΩ)	Total gate charge Q_G (nC)	Reverse recovery charge Q_{RR} (nC)
Device 1	1	67	110
Device 2	0.78	88	105

The parameters listed above contribute to the calculation of the energy lost during the switching phase, the conduction phase, the diode recirculation phase and the one due to driving, according to the following formulas:

$$P_{sw} = \frac{1}{6} \cdot 0{,}5 \cdot V_{IN} \cdot I_{IN} \cdot f_{sw} \cdot \left(t_{rise} + t_{fall}\right)$$

$$P_{con} = D \cdot R_{DSon} \cdot \left(I_{ph}\right)^2$$

$$P_{Diode} = f_{sw} \cdot Q_{RR} \cdot V_{IN}$$

$$P_{gate\ driving} = f_{sw} \cdot Q_G \cdot V_{GS}$$

D represents the control duty cycle used.

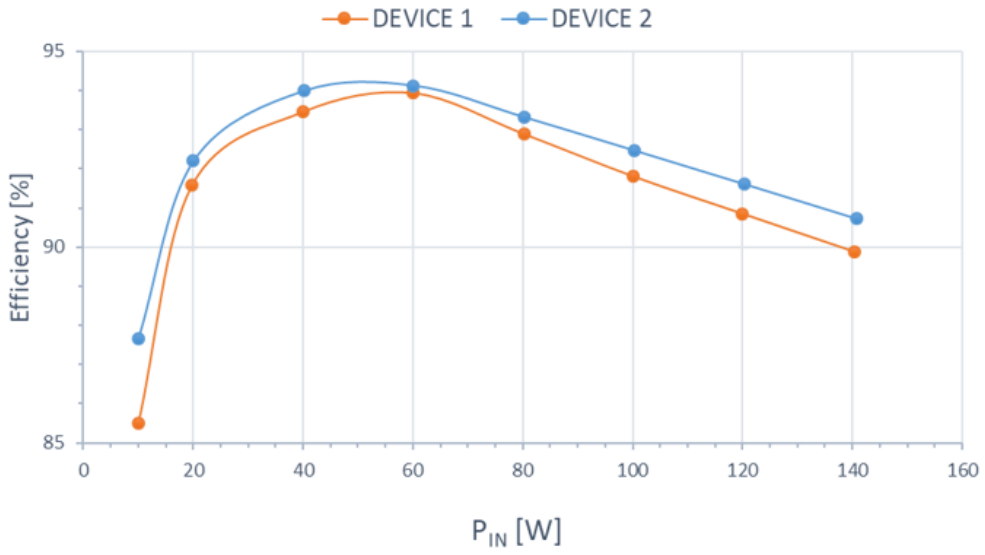
Figure 7. Efficiency measurement with the Aron insertion below shows the comparison of the results obtained in terms of efficiency between the two devices as a function of the input power used.

The device 2, although having a gate charge greater than device 1 and a slightly higher recovery charge, has a higher efficiency in the whole input power range. This gate charge, as mentioned, affects the switching losses of the devices.

On the other hand, the device 2 has a lower R_{DSon} than the other device, which affects the losses during the conduction phases and allows it to bridge the gap and overcome it in efficiency.

In this kind of applications, where the switching frequencies are lower than 20 kHz, the conduction losses can assume a significant weight, making the device with lower R_{DSon} the best one in terms of efficiency.

Figure 7. Efficiency measurement with the Aron insertion



A way to increase the system's efficiency is, as already described, to optimize the turning on and off losses of the device.

The board design also includes the correct selection of the drive resistors to be inserted in series to the device's gate pin.

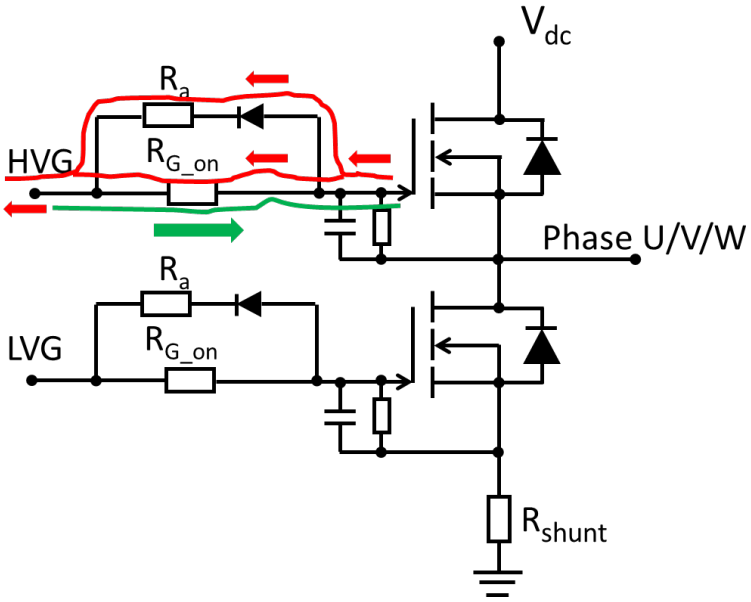
The switch-on and switch-off paths can be designed differently so that the turn on resistance is different from the switching off one.

Increasing the switching speed can allow you to reduce the losses, but will simultaneously worsen the emissions due to the device switching and therefore the system's noise.

Starting from the driver, the turn-on and turn-off paths are different; during the turn-on, the sink current flows through a resistive path given by the R_{G_ON} resistance which is appropriately selected so as to give an appropriate d_V/d_t on the device.

During the turn-off phase, the source current flows through the resistive path made by the parallel of R_{G_ON} and R_A.

Figure 8. **Typical gate driving network suggested**



2.2 V_{GS} and related parameters

Table 2. Device 1 switching parameters and Table 3. Device 2 switching parameters are the switching time tables of two STMicroelectronics' 40 V Power MOSFETs "ST285N4F7AG" and "STL260N4LF7" with different turn-on threshold: standard and low threshold. The same technology shows different switching on and off times.

Table 2. Device 1 switching parameters

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay	V_{DD} = 20 V, I_D = 48 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	30	-	ns
t_r	Rise time		-	21	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
t_r	Fall time		-	13	-	ns

Table 3. Device 2 switching parameters

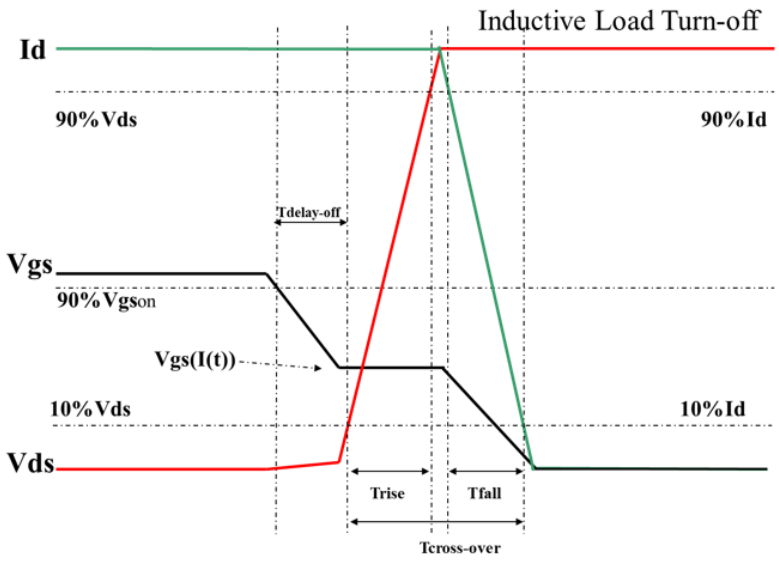
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay	V_{DD} = 20 V, I_D = 25 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	44	-	ns
t_r	Rise time		-	42	-	ns
$t_{d(off)}$	Turn-off delay time		-	171	-	ns
t_r	Fall time		-	39	-	ns

Figure 9. Ideal inductive turn-off time sequence shows the V_{GS} and V_{DS} behavior during a turn-off phase for an inductive load.

In particular, the delay off time is the time required to discharge the gate-source capacitance from the 90% V_{GSon} applied to the V_{GSth} (90%I_d). It is directly proportional to C_{GS}+C_{GD} and to R_{GOFF}.

The fall time is the time required to discharge the gate-source capacitance from the V_{GSth} (90%Id) to the V_{GSth} ($10\%I_d$) and, considering a resistive load, the V_{DS} rises from 10% to 90% of V_{DD}. It is proportional to Miller equivalent capacitance and to R_{GOFF}.

Figure 9. Ideal inductive turn-off time sequence



Considering the turn-on of a MOSFET device, it is necessary to take into account the delay-on time and the rise-time.

The first one is the time needed to charge the gate-source capacitance from V_{GS}= 0 V to V_{GSth} ($10\%I_d$). It is directly proportional to C_{GS}, R_{GON} and V_{GSON} applied.

The rise-time is the time needed to charge the gate-source capacitance from V_{GSth} ($10\%I_d$) to V_{GSth}($90\%I_d$); in the meantime, considering the resistive load the V_{DS} falls from 90% to 10% of V_{DD}. It is directly proportional to Miller equivalent capacitance and to R_{GON}.

From an application point of view, in a three-phase controlled-bridge system it is necessary that the turning on of a device starts once the device of the same leg has been already turned off and vice versa.

The speed with which a device can be switched on and off can be changed by modifying, during the project, the driving network through the gate resistance path.

However, it is also necessary to refer to another known problem with the name of the "Miller effect" (see Section 2.2.1 Miller effect).

The threshold voltage of the device can also affect the operation of a three-phase topology application due to the interaction of several devices.

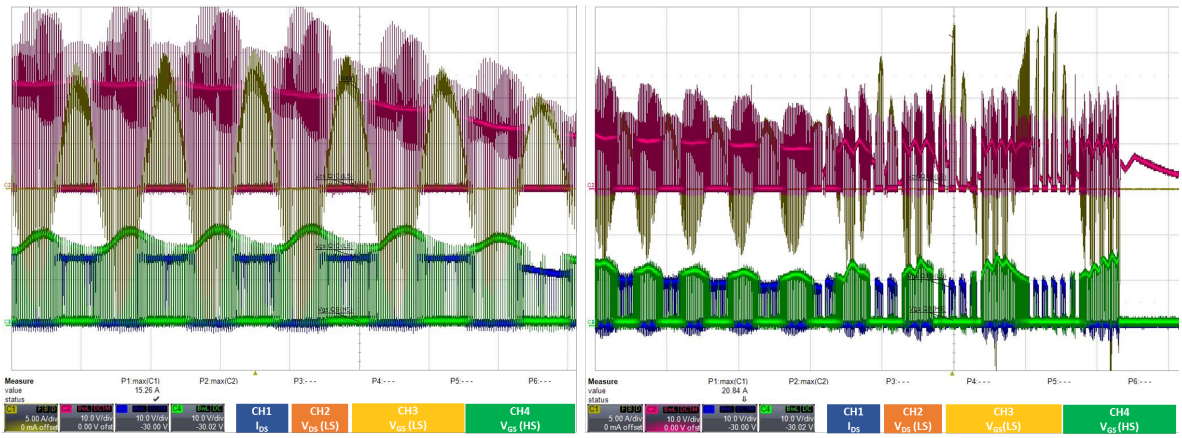
Figure 10. System behavior waveforms of different V_{th} devices shows the system behavior during the locked rotor condition, which represents a critical condition in this kind of applications, with an effect similar to the short-circuit of the motor phases. During normal operation (at rated speed) the rotor is locked by a dynamometric brake in a short-time interval.

The devices analyzed have a different threshold voltage.

The left graph shows excessive noises, during the analyzed time window, in terms of current peaks, noise on the gate and drain voltages of the devices compared to the one in the right. The cause of this behavior is certainly due to the different threshold voltage. The application equipped with lower threshold devices (at the left) shows some cross-conduction events due to the undesired turn-on of the same leg devices; the LS switch could, due to V_{GS} bouncing over its V_{th}, turn on when the HS is turns on (Miller effect).

If such condition is permanent, the relevant increase in temperature can cause the failure of the device.

Figure 10. **System behavior waveforms of different V_{th} devices**



2.2.1 Miller effect

The following figure shows a simplified MOSFET model which can help to describe the induced turn-on problem. R_G is the internal gate resistance of the MOSFET while C_{GS}, C_{GD}, and C_{DS} are the gate-to-source capacitance, the gate-to-drain Miller capacitance and the output capacitance, respectively.

Figure 11. **Equivalent circuit of inner structure**

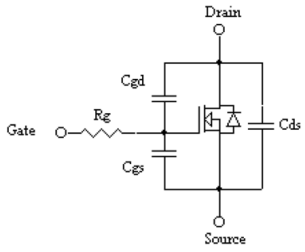


Figure 12. Switching waveform in a motor control inverter shows the shutdown of the high-side MOSFET (*Q9*) and the subsequent power-on of the low-side MOSFET (*Q10*) in one phase of a three-phase bridge.

#1: start-off phase of the high-side MOSFET (*Q9*): once the gate voltage of the MOSFET drops below the switch-off threshold, there is an increase in the drain voltage on the MOSFET's low-side (*Q10*) due to the recirculation phase current on its diode (area #2).

#3: the low-side MOSFET (*Q10*) starts the turn-on phase while the high-side MOSFET (Q9) has been turned off. The current has a peak due to the recovery phase of the high-side MOSFET diode (Q9) once it is completed, which, after some oscillations, stabilizes.

#4: the low-side MOSFET (*Q10*) is finally turned on and the V_{DS} voltage reaches a value close to zero (R_{DSON} x I_{DS}).

#5: there is a voltage spike on the high-side MOSFET which, in case it overcomes its threshold voltage, could lead to an unwanted re-ignition, just when the low-side MOSFET of the same leg is already on and shorting the leg.

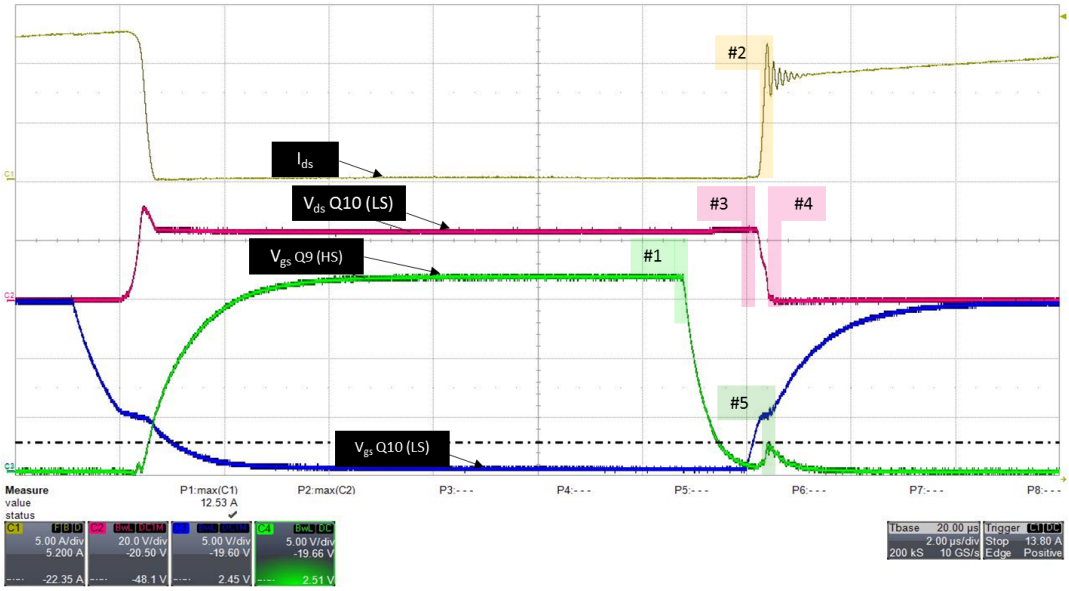
This voltage increase is due to the charge accumulated during the recirculation phase of the diode which leads to the charging of the capacitive divider formed by the intrinsic capacitances of the device, C_{GD} and C_{GS}, through the driving resistance R_G and the upstream driving network. Therefore, the voltage spike V_{GS} on the high-side device (*Q9*) will depend on $C \cdot \frac{dV}{dt}$, on the capacitive divider values and on the total gate resistance.

To prevent the turn-on induced by the $C \cdot \frac{dV}{dt}$, the gate voltage must not exceed its turn-on threshold voltage.

A higher threshold voltage can help to prevent this condition, but this can lead to an increase in the R_{DSON} resistance. Another way could be to have a lower Miller's capacitance (Q_{GD}) and/or increase the C_{GS} gate-source capacitance in order to prolong the charge time and reduce the voltage peak on the gate.

In general, the reduction of the ratio, the increase of the threshold voltage and the reduction of the gate resistance will contribute to the reduction of the Miller effect.

Figure 12. Switching waveform in a motor control inverter



2.3 Dead time and f_{sw}

In a three-phase bridge “dead time" variable (which is usually possible to modify within the firmware that drives the system) indicates the time that must elapse between a shutdown command given to a device of a leg (HIGH/LOW side) and the turn-on of the device of the same leg (LOW/HIGH side) to avoid time intervals in which both devices of the same leg are switched at the same time causing cross-conduction phases with increasing temperatures, increasing losses and consequent failures.

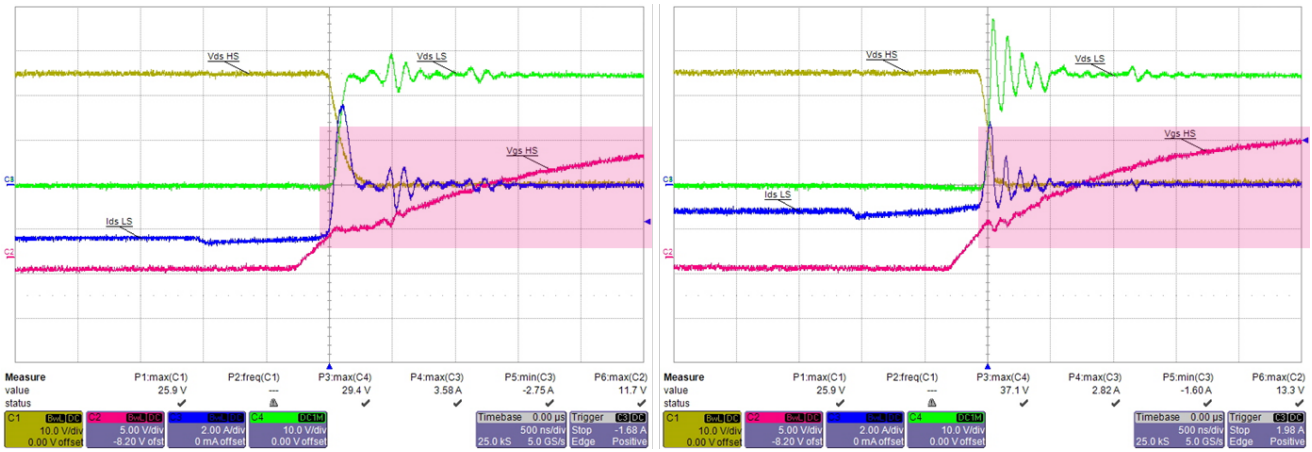
Excluding any delays due to the external network (control board/driver vs gate of the power device), this dead time must take into account the intrinsic on and off times of the device used.

On the other hand, the choice must also take into account that an excessive waiting time between one switching and another leads to a less efficient use of the PWM system, increasing the modulation index of the system and making the voltage/current output characteristics of the system noisier.

When choosing the device, it will be necessary to focus on the characteristics related to the t_{on} and t_{off} that could also vary considerably from one device to another.

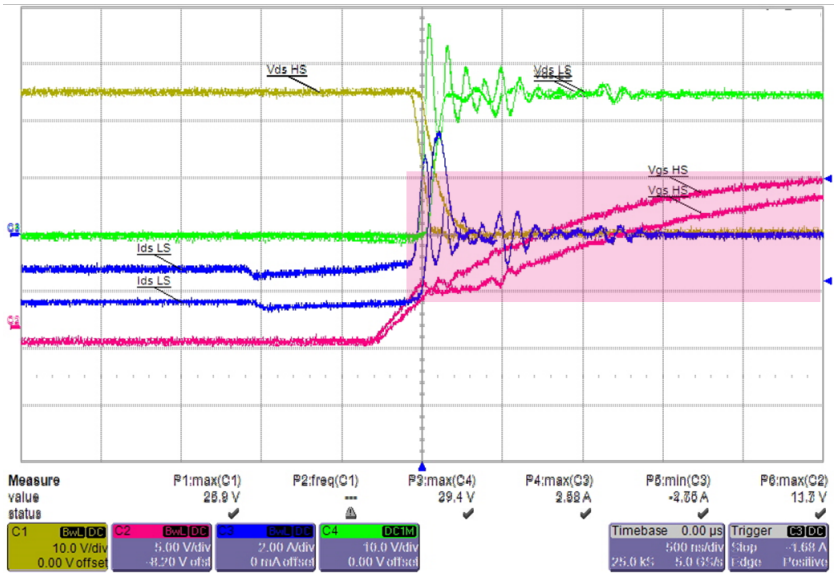
Figure 13. Turn-on waveforms of different switching behavior devices shows a typical example of the turning on of two different devices, used in the same motor control application, with different turn-on times.

Figure 13. Turn-on waveforms of different switching behavior devices



Both devices are the high side of the same leg of a three-phase bridge. The different duration of the switch-on time is shown in Figure 14. Turn-on comparison in which the same overlapping figures are shown maintaining the same time scales.

Figure 14. Turn-on comparison



The device 1 reaches full turn-on in about 2.5 µs while the device 2 reaches the same voltage in almost 3 µs.

In general, as discussed, the turn-on and turn-off times depend on the device and on the driving network.

Higher times lead to higher losses, but lower emission values during switching. In any case, during the design phase of the firmware these times need to be taken into account to choose the dead time.

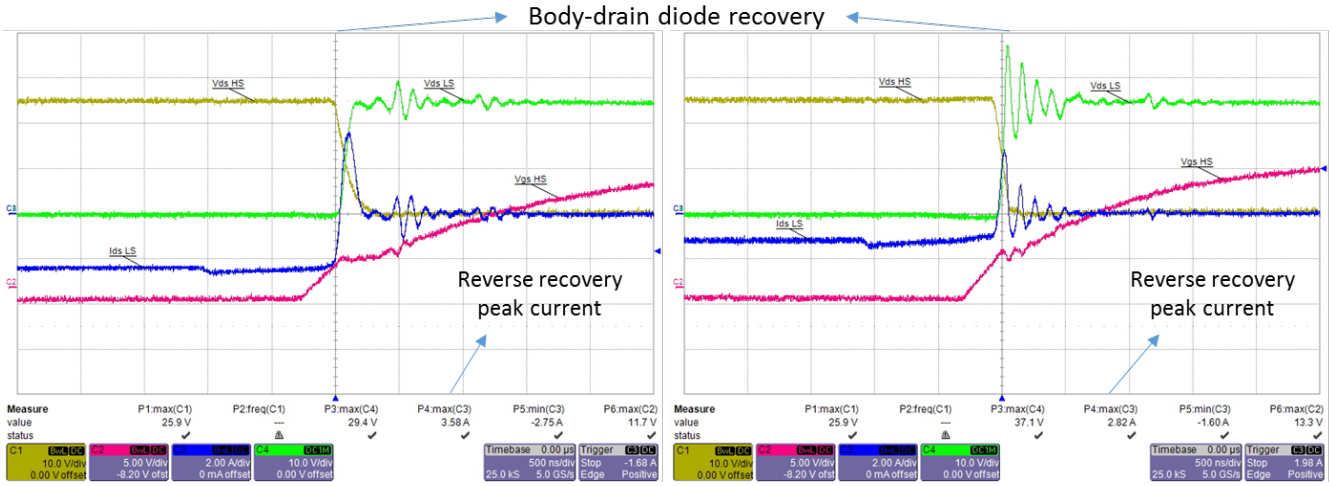
2.4 Current behavior

Figure 15. Hard-switch turn-on and body drain diode Q_{RR} impact shows the turn-on of two different devices placed in the low side of a leg of a three-phase bridge system in the same motor control application.

The comparison shows the different behavior of the drain-source current during the turn-on phase. The current has a first peak due to the recirculation phase of the diode which, at the end, reaches the real value required by the load after some oscillations.

The trend of the I_{ds} current on the left graph has a more pronounced peak than the other one, reaching 3.58 A vs 2.82 A.

Figure 15. Hard-switch turn-on and body drain diode Q_{RR} impact



This current peak and the relative oscillations contribute to the decrease of the efficiency during the switching phases, increase the temperature and have an impact in terms of emissions so the characteristics of the MOSFET body-drain diode are very relevant.

In bridge topologies, the reverse recovery process occurs at the end of the freewheeling period of the low-side device before the high side starts conducting. The recovery current adds to the high-side current. Together with the extra-current on the high-side device, low-side reverse recovery and its commutation from $V_{DS} \approx 0$ V to V_{DC} can produce spurious bouncing on the low-side gate-source voltage, due to induced charging of the low-side C_{ISS} (input capacitance) via C_{RSS} (Miller capacitance). As a consequence, the induced voltage on the Q2 gate could turn on the device, thus worsening the system's robustness and efficiency. The low-side device, in bridge configuration, should have soft commutation without dangerous voltage spikes and high-frequency ringing across the drain and source. This switching behavior can be achieved using a Power MOSFET with lower reverse recovery charge (Q_{RR}) which has a direct impact on the overshoot value. The higher the Q_{RR} is, the higher is the overshoot. Lower values for V_{DS} overshoot and ringing reduce the spurious voltage bouncing on the low-side gate, limiting the potential risk for a shoot-through event.

Furthermore, soft recovery enhances the overall EMI performance as the switching noise is reduced.

2.4.1 BLDC 3-phase power bridge operating conditions

This section presents the waveforms related to a motor control application with the FOC algorithm in PWM control.

The arrows in Figure 16. Current path setup definition show the conventional direction of the current, considered as positive, according to the current probe set up.

The dashed arrows, in the following examples, show the closing paths of the current in the other phases of the bridge.

Figure 16. Current path setup definition

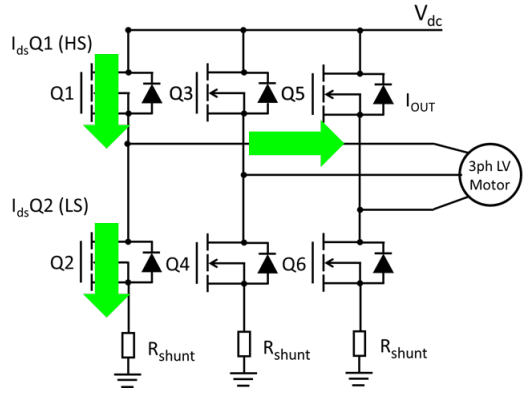


Figure 17. High-side turn-on waveforms and relevant current path on the inverter block diagram shows the drain current waveforms for two devices of the same leg during the turning on of the high-side power device.

In particular, the figure below shows the currents and their direction before switching on the device (section *#1* on the graph); during the switching on of the HS device, the current on this leg has some oscillations, which are also reflected on the LS device, due to the recirculation current in the free-wheeling diode. At this stage the phase current will not change the direction.

Once the device has finally switched on (section *#2*), the current on the LS has already completed the free-wheeling stage while the HS current grows to the loading maximum value.

Figure 17. High-side turn-on waveforms and relevant current path on the inverter block diagram

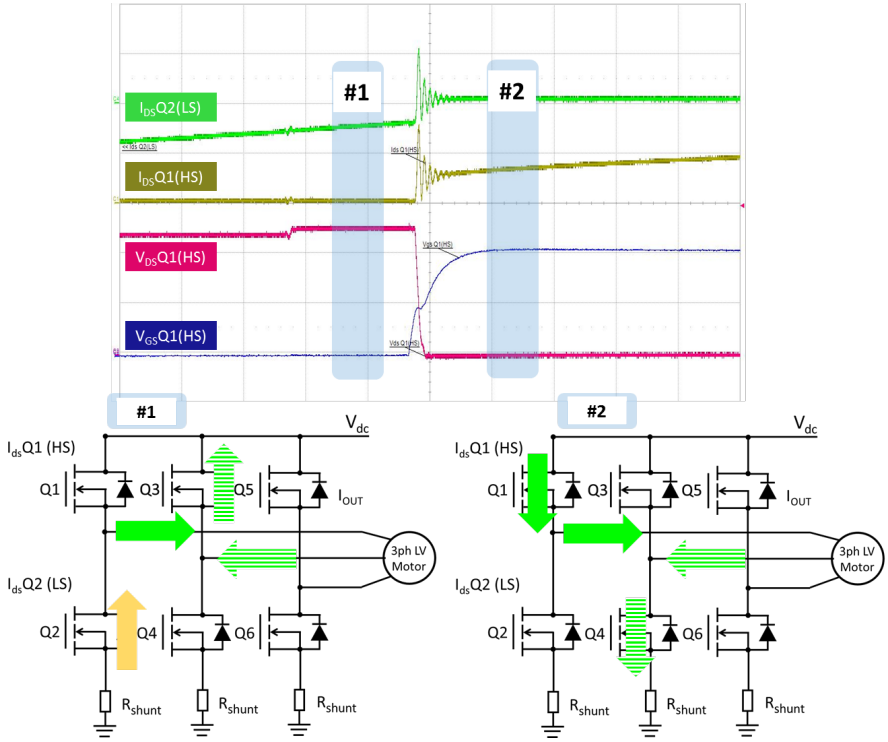


Figure 18. Active free-wheeling waveforms and relevant current path on the inverter block diagram shows the drain current curves for two devices of the same leg during the switching off of the high-side power device.

During the HS switching off, the current on this leg has some oscillations due to the recirculation current on the LS device. The dashed arrows show the loop paths of the current of the other legs in the power bridge.

Once the HS device has definitively turned off (#2), its current goes back to zero while the LS one is negative (circulation in the diode of the other legs and on the FET channel belonging to the same leg of the bridge: active free-wheeling).

Figure 18. Active free-wheeling waveforms and relevant current path on the inverter block diagram

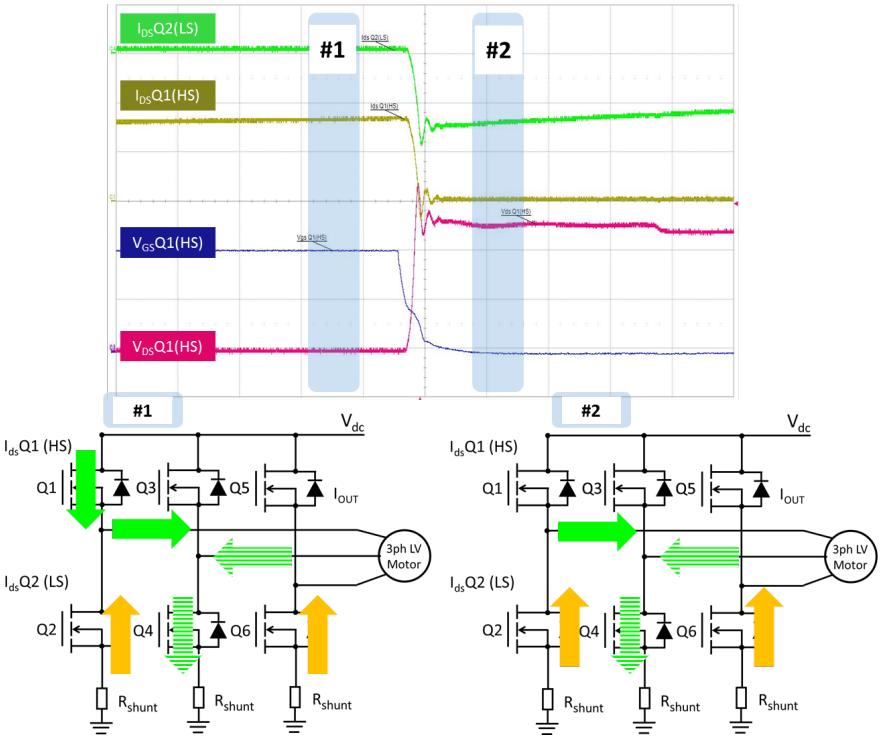


Figure 19. High-side power losses at turn-off and Figure 20. High-side power losses at turn-on show the maximum power and the energy managed by the high-side device during the turn-off and turn-on phases.

Figure 19. High-side power losses at turn-off

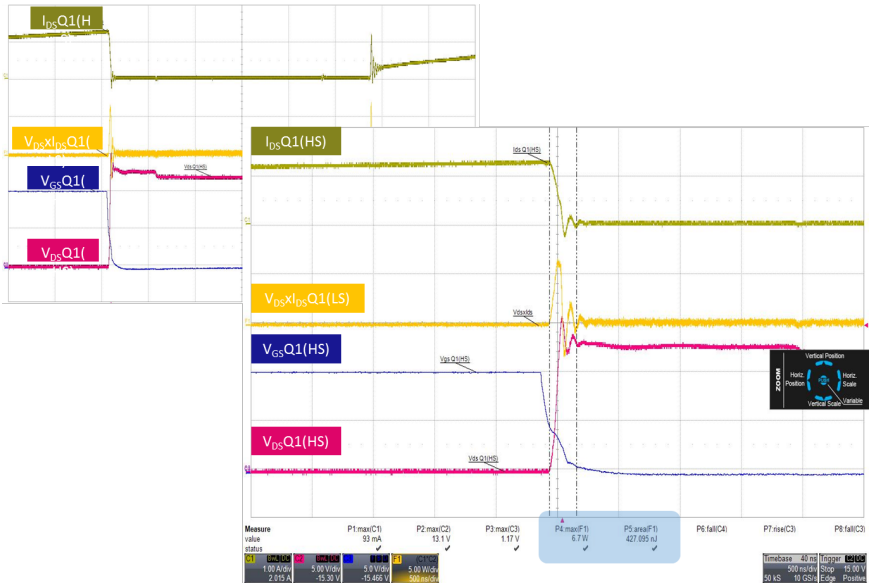


Figure 20. **High-side power losses at turn-on**

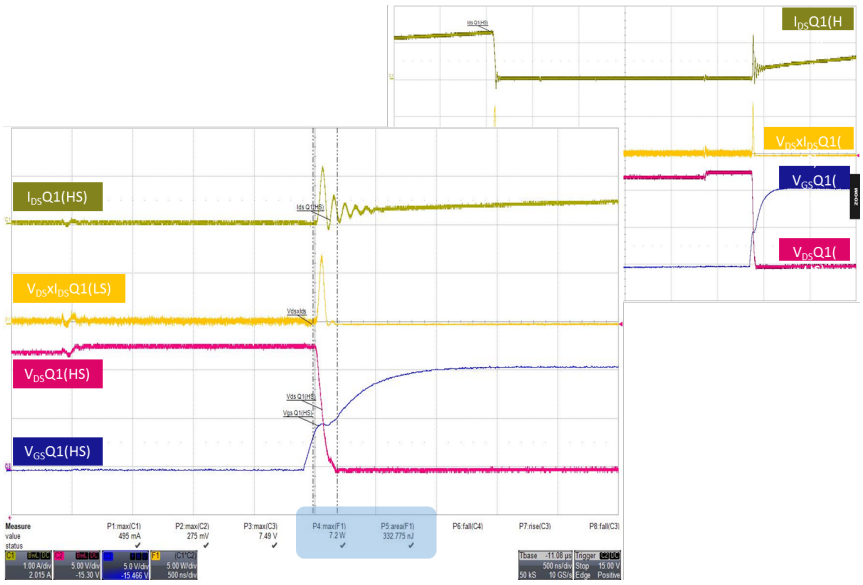


Figure 21. Circuit diagram and relevant switching waveforms including the load current shows the switching off and the switching on of the power device placed in the high side of the three-phase bridge. In this case the three system currents were simultaneously monitored. On top of that, the phase motor current (I_{OUT}) was also considered.

#1: the high-side MOSFET is turned on and the current is positive and increasing; no current flows on the low side while the phase current of the motor follows the trend of the high-side current, also flowing, to close the loop, through the low-side device of the other leg of the bridge.

#2: the high-side device starts to switch off and then the current through it goes to zero. I_{out} cannot suddenly drop to zero and cannot change direction; it will find a free-wheeling path through the body–drain diode at the beginning and then in the channel of the same leg's low-side MOSFET.

#3: the high-side device is turned on again, the current reaches a peak due to the LS free-wheeling current and then flows on the high side. I_{OUT} current starts to rise again.

Figure 21. Circuit diagram and relevant switching waveforms including the load current

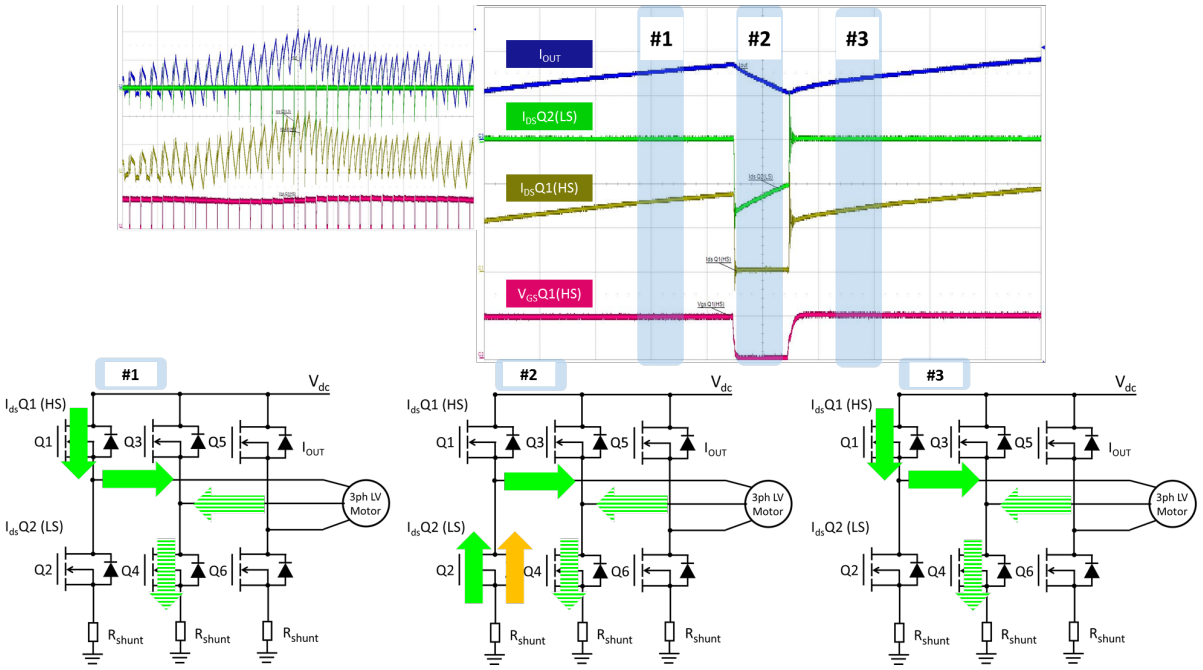


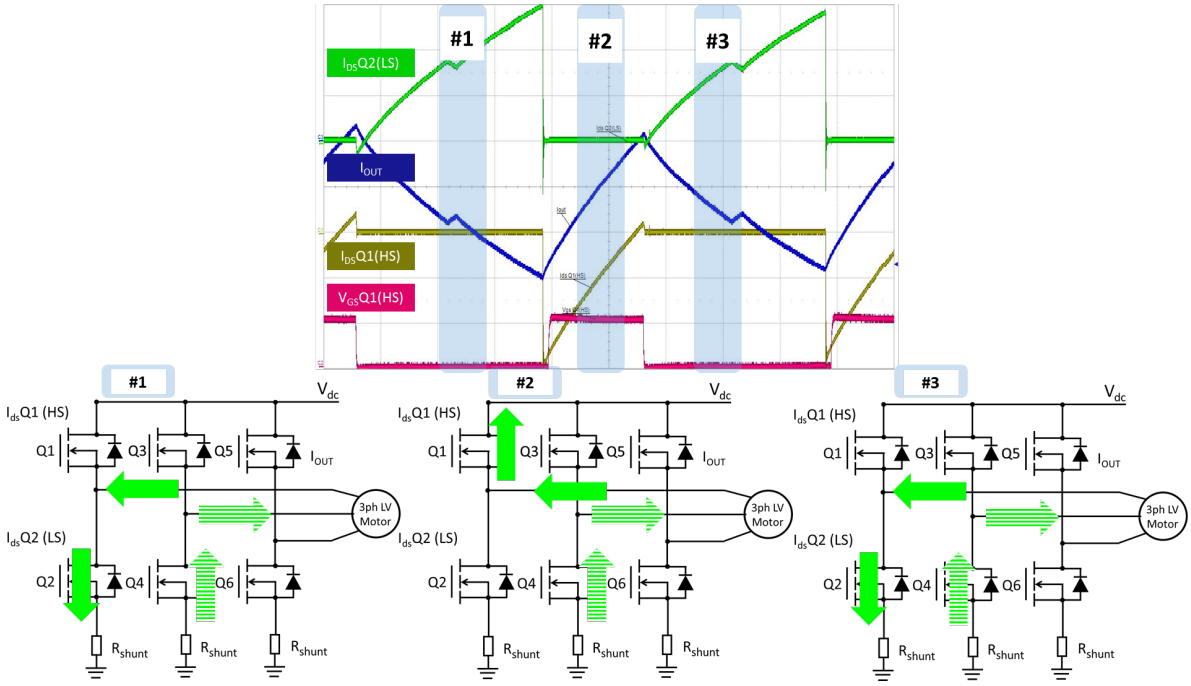
Figure 22. Circuit diagram and relevant switching waveforms including the load current with high-side active free-wheeling shows the turn-on and the turn-off of the same device as in the previous case.

#1: the high-side MOSFET is turned off and the I_{DS} current on the device is zero. The current I_{OUT} is negative and therefore flows in the low-side MOSFET.

#2: the high-side MOSFET is turned on and the I_{DS} current flows on the device in the opposite direction (from source to drain). The I_{OUT} current direction has not changed while the current on the low-side MOSFET is still zero. In this operating condition the free-wheeling is operated by the HS FET.

#3: the high-side MOSFET was turned off again.

Figure 22. Circuit diagram and relevant switching waveforms including the load current with high-side active free-wheeling



2.5 Turn-off V_{DS} voltage spike and ringing effect

The V_{DS} of the device must be able to sustain, at least, the nominal voltage of the system. The analysis of the behavior of this voltage across the two terminals of the device shows that, in some phases, it can exceed the system voltage.

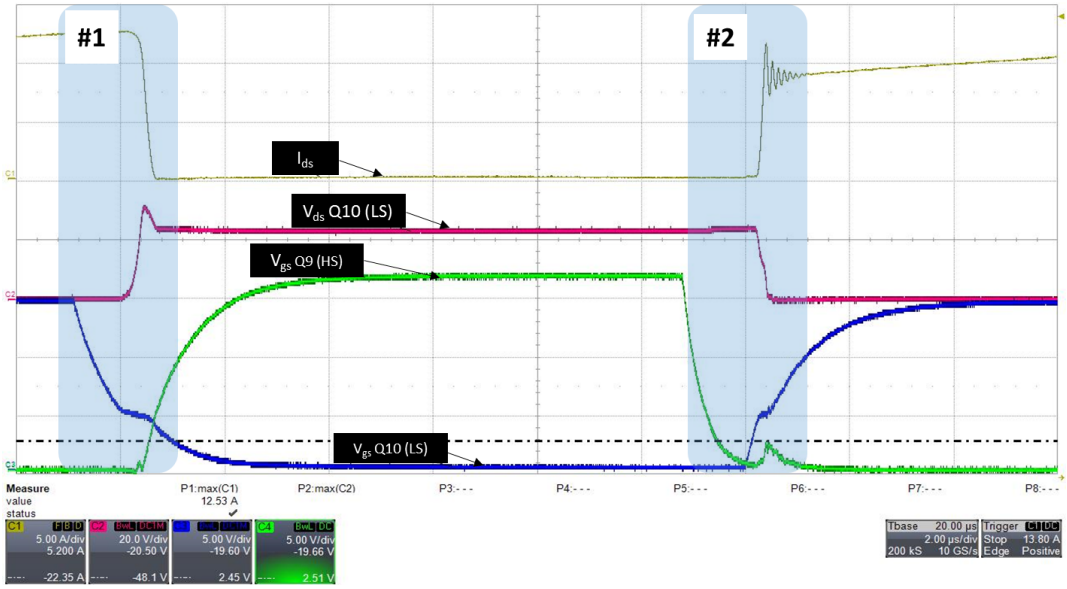
Considering Figure 23. Typical switch-off with V_{DS} extra voltage spike, during the switch-off phase (*#1*), due to parasitic inductances present in the device switch-off network, the drain pin can go beyond the nominal value of the device.

During the turn-off, the current (I_{DS}) decreases until it is canceled. The voltage at the ends of the device begins to rise and at some point, over a certain period of time, exceeds the value of the bus voltage and then levels off at its steady state value.

The peak value of the voltage reached in this phase can exceed the maximum voltage limit of the device.

During the ignition phase (*#2*) the current of the monitored phase (I_{DS}) rises exceeding the nominal value due to the recirculation phase of the exceeded diode which shows a change in slope in the V_{DS} voltage. As already mentioned in the previous paragraphs, the reduction of the Q_{GD}/Q_{GS} ratio and a lower Q_{RR} of the recirculation diode, leads also in this case to a reduction of the voltage ringing and overshoot during the extinguishing phase.

Figure 23. **Typical switch-off with V_{DS} extra voltage spike**



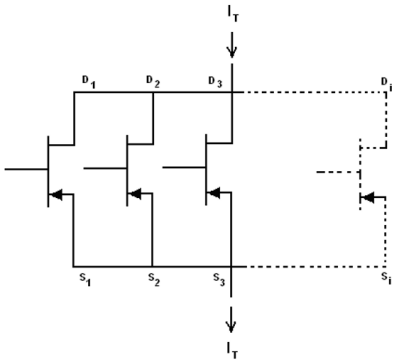
2.6 Paralleled MOSFETs

In power applications, when the current in the single phase is too high to be managed by a single device, it is frequent to use many devices in parallel with the same characteristics so that the total current is divided between them.

The current sharing between the devices depends on the R_{DSon} of the device and on the voltage between drain and source.

All the devices should sustain the same V_{DSon} voltage:

Figure 24. **Parallel connection of different devices**

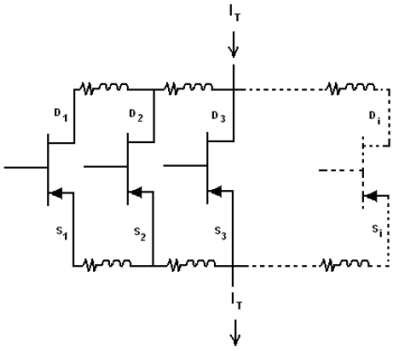


The condition is:

$$V_{DS1} = V_{DS2} = \cdots\cdots\cdots\cdots V_{DSi}$$

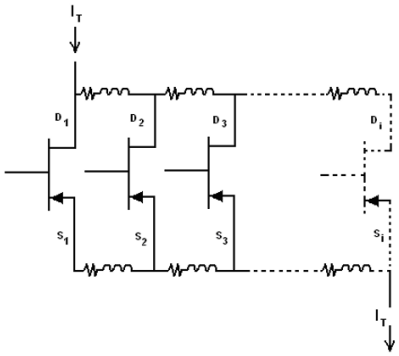
Where V_{DSi} are the single voltages between the drain and source pins of the devices, considering irrelevant the resistances and the inductances due to the connections and the tracks in the PCB which, depending on the layout of the schematic, make the parallel condition more complicated.

Figure 25. Equivalence stray inductances and resistive path of PCB tracks



In general, however, if for each device the resistance R_{DSON} is much larger than the parasitic resistances, the distribution of the current will be less influenced by these differences. A good compromise will be:

Figure 26. Equivalence stray inductances and resistive path of PCB tracks when applying a well-balanced solution



In this case the current flowing through each device meets, approximately, the same resistance and if they have the same R_{DSON} the current distribution will be balanced.

Other important parameters that influence the current sharing of several devices in parallel are the V_{GS} thresholds. In general, the device having a higher current gain and a lower threshold voltage, if used in parallel, is the first one to turn on and the last one to go off.

So, the current sharing is influenced by the following parameters:

- driving resistances of single devices
- track lengths
- parasite inductors
- distance of the driving resistances from the gate pad
- current gain of devices
- turn-on/-off threshold

It is important to underline that devices with the same part number, may have some different electrical parameters that can cause a different current sharing during the switching phases of the devices.

Gate resistors can help, because they allow to separate the on and off behavior and must be positioned close to the gate pins.

Another phenomenon is the oscillation that can occur between gate-source during the switching operation. In general, it happens when the device has low R_{DSON}, low BV_{DSS} and high V_{GS}, high G_{FS}, and parasitic inductances of the tracks.

Generally, the oscillations involve all Power MOSFET pins and could be very dangerous, especially between gate and source, because the voltage spikes can exceed the maximum V_{GS} rating. If the devices are put in parallel,

the electric tank of all parasitic inductances can amplify the oscillations. In general, this behavior is reduced by properly choosing the gate resistors that could help in smoothing the oscillation due to the resonant RLC stray path.

Thermal runaway is called a quick rise of the device junction temperature, caused by power dissipation, and is usually linked to the on-resistance itself and the threshold voltage. The on-resistance increases as junction temperature rises and consequently power dissipation increases, too. Moreover, the temperature increase produces a V_{th} reduction and a higher current capability. The junction temperature increases until the device achieves the thermal equilibrium in the system by the heat-sink, the fan etc.

If the heat removal system is inadequate the junction temperature increases more and more till the device's failure. This phenomenon could be more evident if the devices are put in parallel, because the sudden temperature increase and consequently the on-resistance increase could produce the device's failure without any compensation of other devices. This kind of failure produces the so-called hotspot with the burning of a small silicon area where locally this kind of positive feedback is more focalized.

In conclusion the use of Power MOSFETs in parallel is necessary in applications that manage high-power load, because the total current can be shared between many devices and maintain a uniform operating temperature.

A good device paralleling can be obtained if the following conditions are satisfied:

- devices with similar parameters
- asymmetric driving (different turning on and off)
- symmetrical board layout
- good thermal coupling by same heatsink
- low parasitic oscillations

These conditions are not easy to achieve, but are strongly recommended if the devices are used in parallel working, in any case sorting by threshold voltage and G_{fs} allows to reduce current unbalance.

2.6.1 On-bench analysis

This section shows the results of some tests performed on a board, designed for low-voltage and high-current inverter applications, which uses 100 V MOSFET devices controlled by means of an STM32 microcontroller.

The system has been designed to meet the following requirements:

- Supply voltage: up to 60 V
- Switching frequency: 15-20 kHz
- P_{OUT} = 5 kW

The following figure shows the complete system of the driver board, power board and bulk capacitors board.

Figure 27. **5 kW inverter board view**

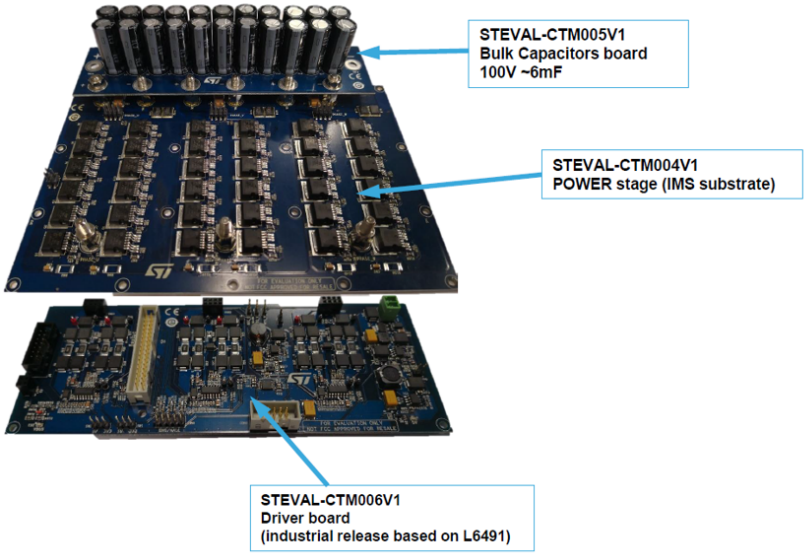


Figure 28. 5 kW inverter turn-on current sharing detail shows the current trends on the six MOSFETs of the same leg during the turn on-phase in nominal condition load. The current sharing is not perfect. Some measurements of the V_{GS} have evidenced a higher value of the V_{GS} of the MOSFET Q2 which leads it to a later turn-on and consequently is crossed by a lower current. Vice versa, the devices with the highest current value (Q5 and Q6) were with a lower V_{GS} threshold of.

Figure 28. **5 kW inverter turn-on current sharing detail**

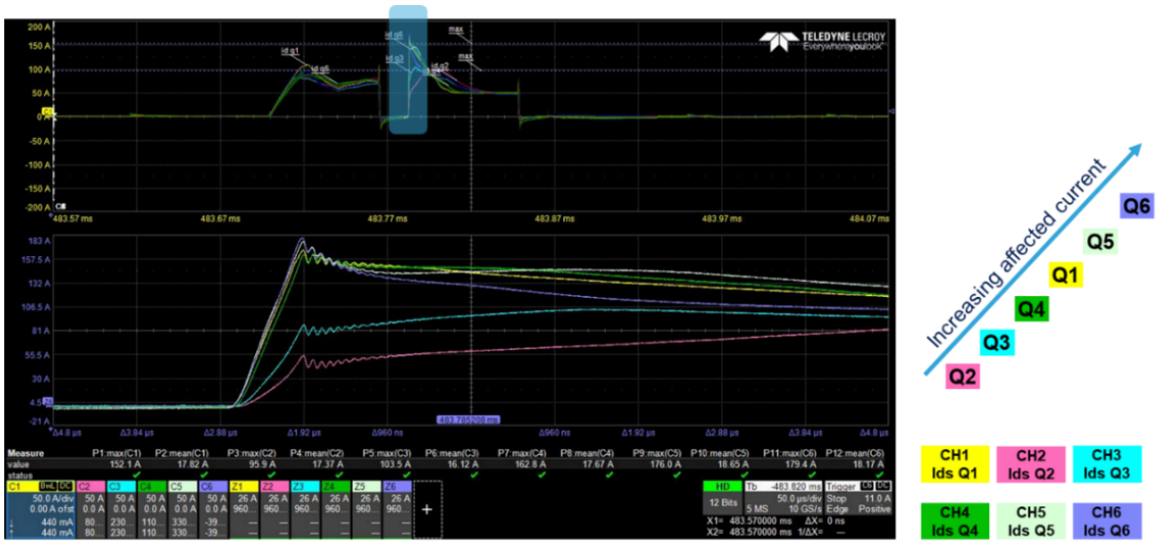


Figure 29. 5 kW inverter turn-off current sharing detail shows the current sharing of the six MOSFETs during the turn-off phase. In this case the MOSFET Q1 is the device with the higher current probably due to a lower value of the C_{RSS} which increases the speed of the device during the turn-off.

Figure 29. **5 kW inverter turn-off current sharing detail**

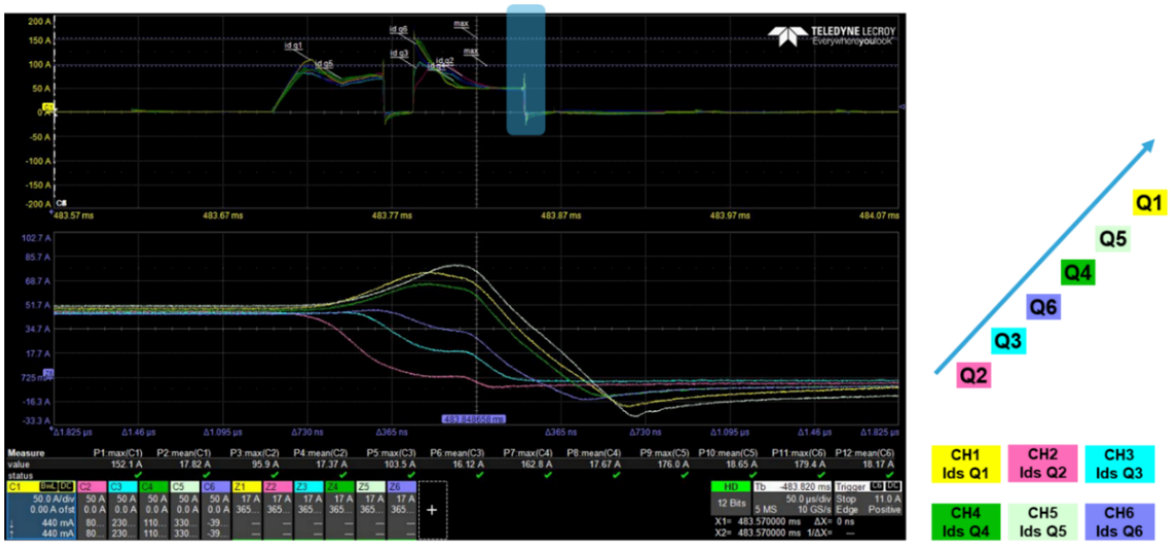
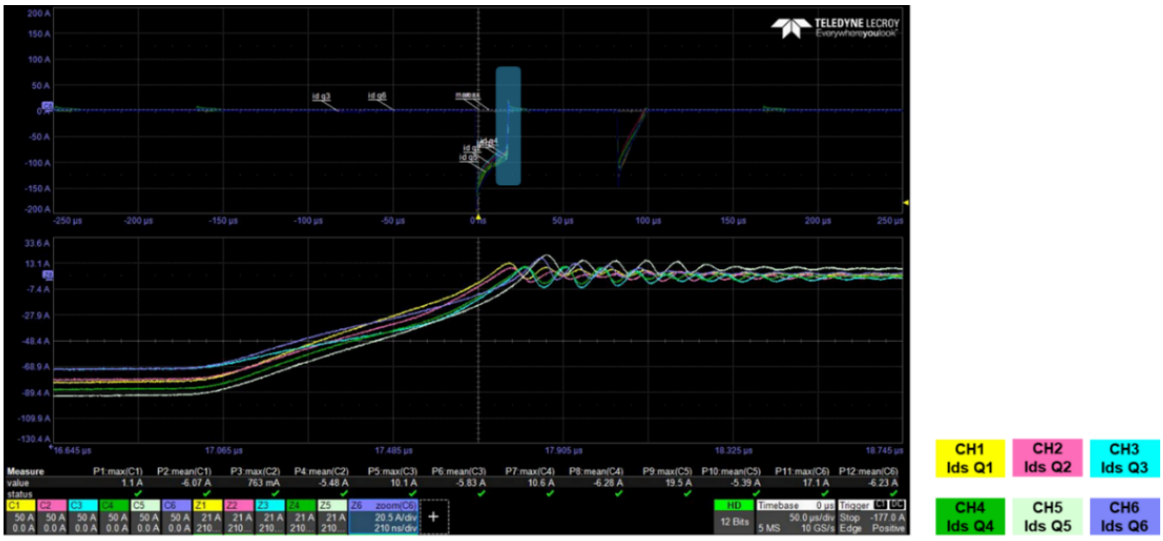


Figure 30. 5 kW inverter active free-wheeling and body drain diode involvement shows another important part to take into account for an in-depth analysis of such applications.

The recovery phase of the freewheeling diode, which may lead to an increase in losses, has already been discussed. In this case, thanks to the fairly close parameters of the body drain diodes, the diode recovery currents are fairly balanced in the 6 parallel MOSFETs.

Figure 30. **5 kW inverter active free-wheeling and body drain diode involvement**



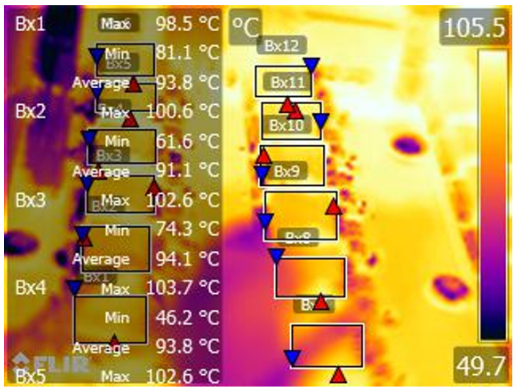
The temperature of the devices during the operating conditions plays a fundamental role when using some MOSFETs in parallel conditions.

This temperature is closely linked to the losses of the devices and to their heat dissipation capacity; the losses are strictly linked to the conduction and the switching phases, to the electrical parameters, the driving network and the board design. A heatsink must be positioned in order to guarantee a uniform heat dissipation of the devices.

Figure 31. 5 kW inverter thermal picture shows the temperatures, measured by means of a thermo-camera, of the 12 devices (6x low side and 6x high side) of the same phase.

The balance of power will be better if all the devices have a balanced temperature.

Figure 31. 5 kW inverter thermal picture



During the on-bench tests, the driving resistances of the MOSFETs on board were changed. Originally, these resistances were:

R_{ON} = 4.7 + 3.3 = 8 Ω

R_{OFF} = (3.3 // 1.5) Ω

The resistance of the turn-on path of the MOSFETs has been increased while keeping the turn-off one unchanged:

$R_{ON(new)}$= 2.2 + 8.2 = 10.4 Ω

Figure 32. 5 kW inverter turn-on current sharing detail (original design) and Figure 33. 5 kW inverter turn-on current sharing detail with improved solution show the current sharing during a generic conduction phase between two MOSFETs of the same leg.

The comparison shows a better sharing, along the gate circuit, thanks to the new solution with the modified resistance values which allow to lower the peak current compared to the original design.

Figure 32. 5 kW inverter turn-on current sharing detail (original design)

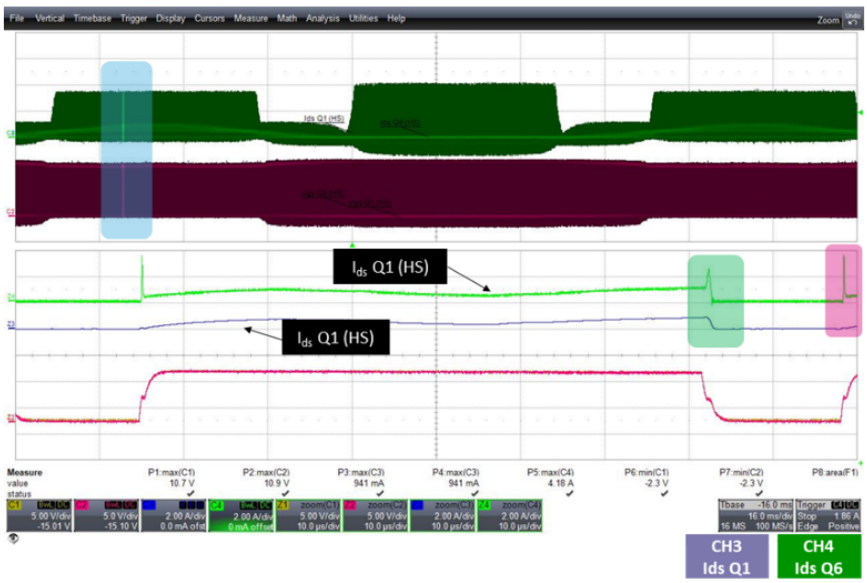
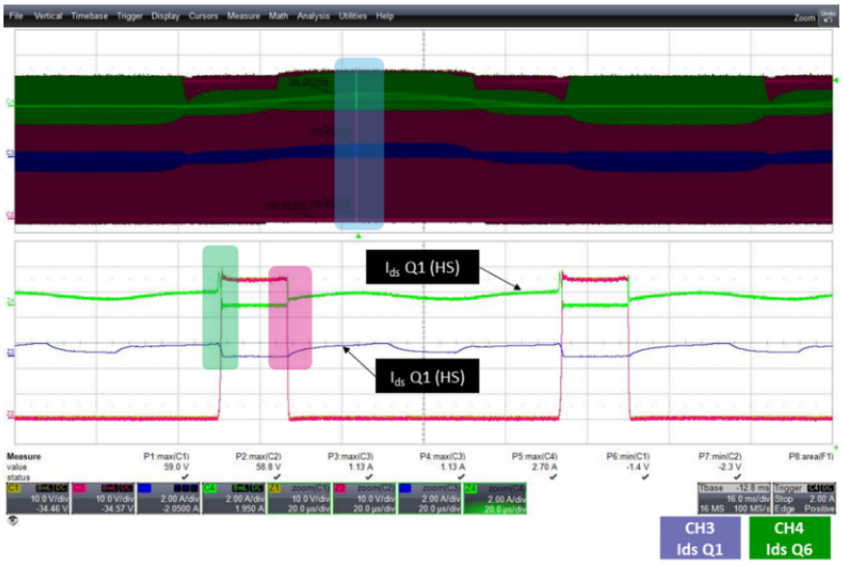


Figure 33. 5 kW inverter turn-on current sharing detail with improved solution



These modifications also have highlighted improvements, which are visible even during the devices turn-on and turn-off phases in terms of voltage spikes and current peaks.

Figure 34. 5 kW inverter switching behavior with original design and Figure 35. 5 kW inverter switching behavior with modified driving details show a comparison of the voltages V_{GS}, V_{DS} and the current of two devices of the same leg between the original and new design.

The new driving shows a better behavior during the turning off of the V_{DS} voltage, compared to the original gate driving setup and shows a lower current spike.

The current spike is also lower.

Figure 34. 5 kW inverter switching behavior with original design

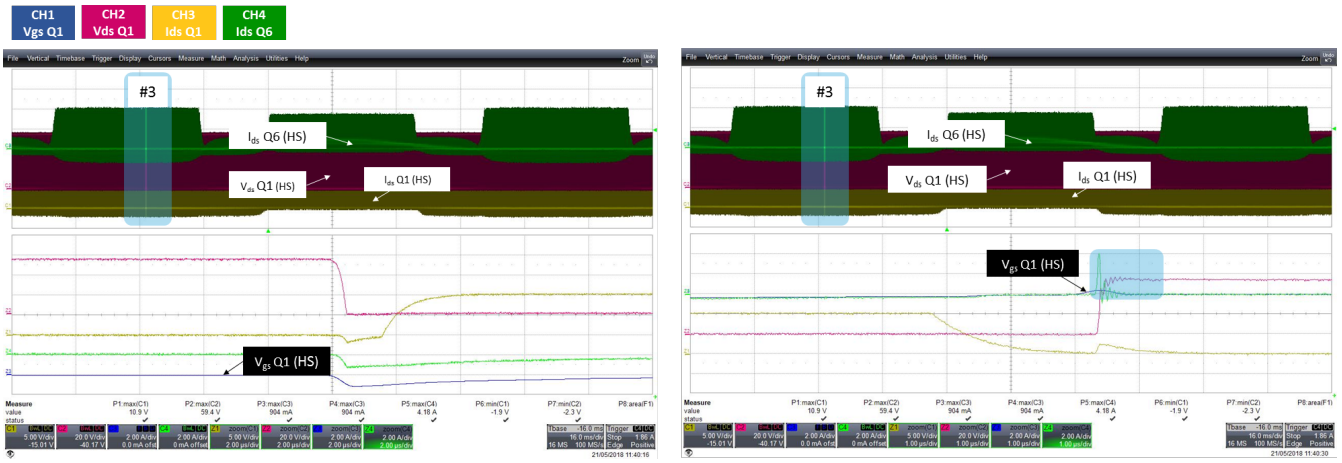


Figure 35. 5 kW inverter switching behavior with modified driving details

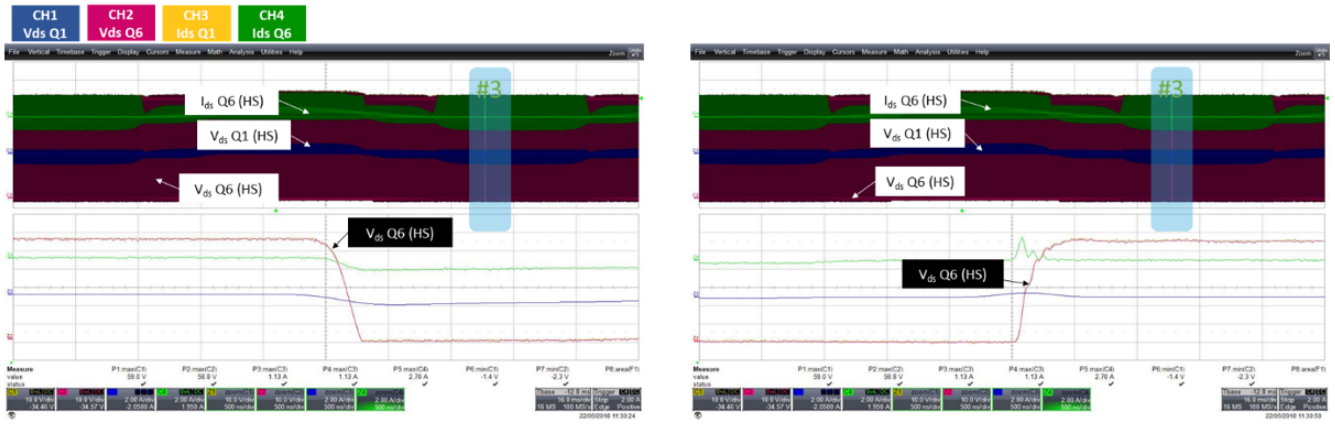


Figure 36. 5 kW inverter original design with voltage oscillations and Figure 37. 5 kW inverter updated design with improved voltage oscillations also show an improvement regarding the voltage ringing during the turn-on and turn-off phases, of the same devices, between the original setup and the modified one.

Figure 36. 5 kW inverter original design with voltage oscillations

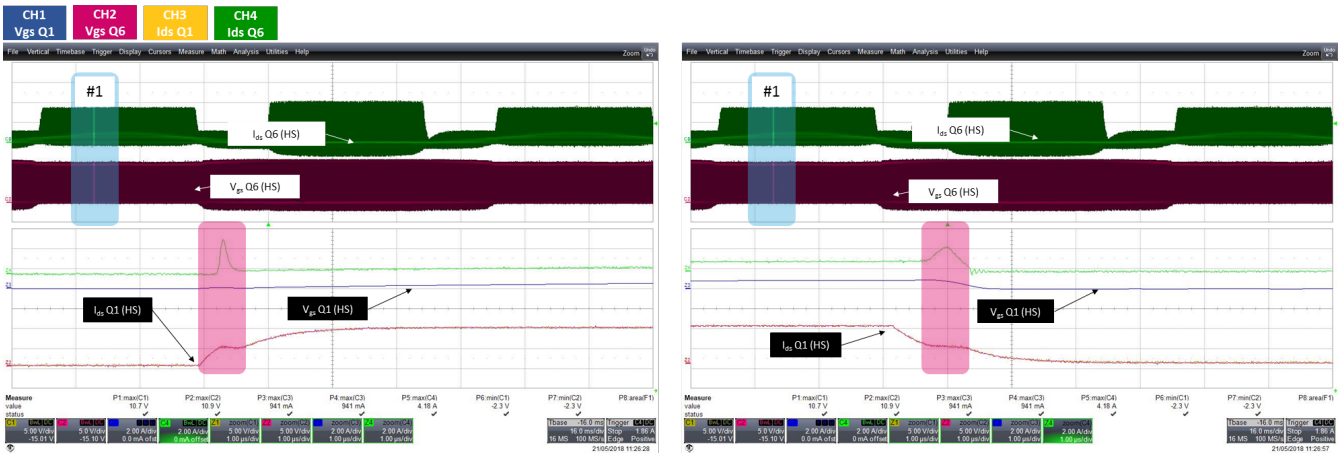
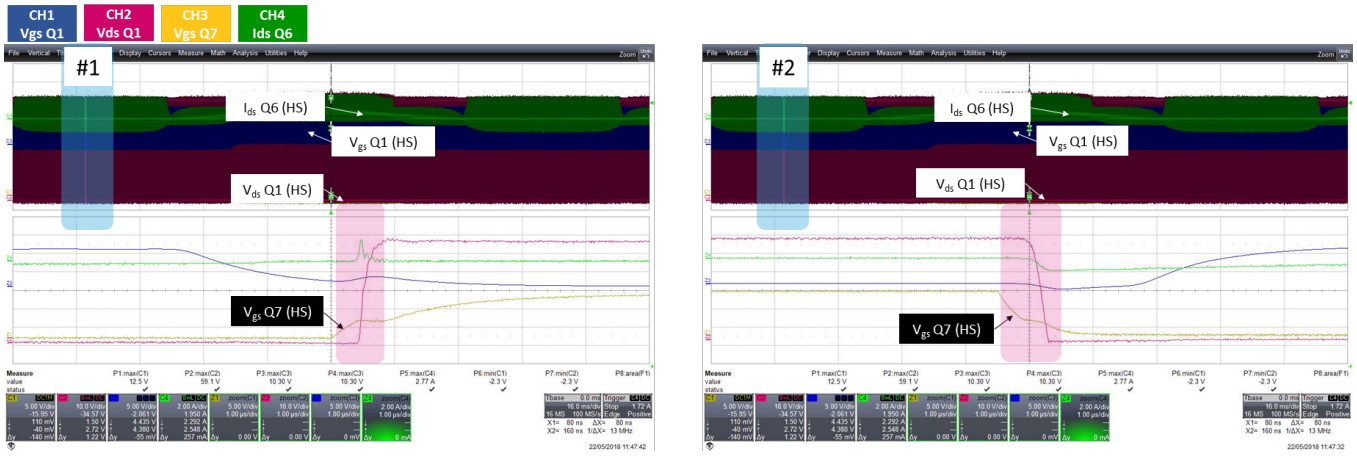


Figure 37. **5 kW inverter updated design with improved voltage oscillations**



2.7 Kelvin pin improvements

A way to improve the gate voltage control path of a MOSFET is to use a package with an additional pin (3S) (see Figure 38. Device inner connections for Kelvin pin implementation), which is a Kelvin source that is used as a return path for gate driving. Figure 39. Device inner connections for standard three pin connections shows the same device in a standard package (with 3 pins).

Figure 38. **Device inner connections for Kelvin pin implementation**

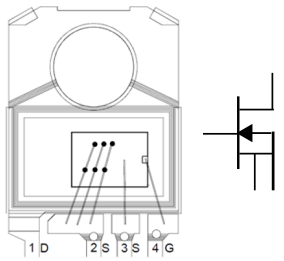
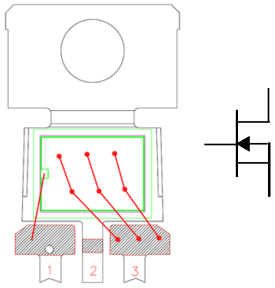


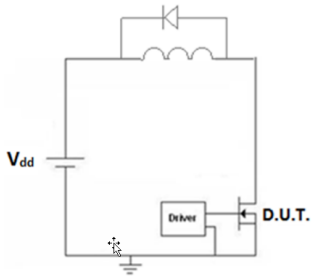
Figure 39. **Device inner connections for standard three pin connections**



The Kelvin source pin has the advantage, given that it is not flown by I_{ds} current, to have a low voltage drop in the G_S path driving controller during the switching operation.

A bench comparison was made between two identical devices (STx310N10F7) assembled in the two different packages. The same electrical scheme has been used as shown in Figure 40. Block diagram for switching behavior characterization to check if the additional Kelvin source allows to have a benefit in terms of power dissipation.

Figure 40. Block diagram for switching behavior characterization

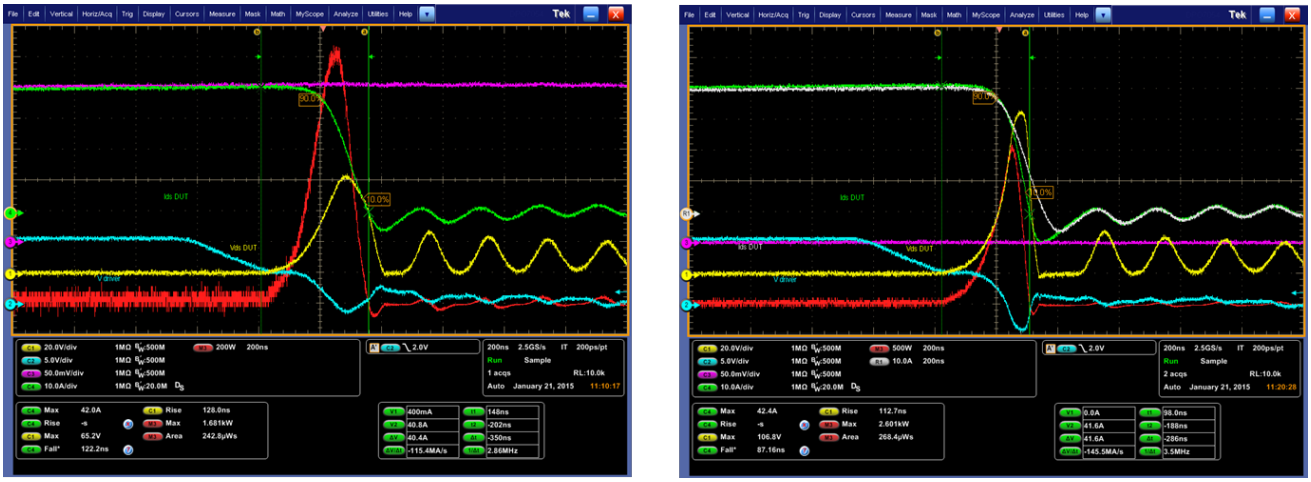


The testing electrical scheme is a simple UIS circuit with a freewheeling diode. The test performed on the bench was monitoring the turn-on/off switching at various V_{DD} and I_{DS}.

By monitoring the turn-off switching at the same I_{DS} current values, it was shown (see Figure 41. Turn-off comparison among the three (left) and 4 (right) leads solutions and Figure 42. Turn-on comparison among the three (left) and 4 (right) leads solutions) that the the device with 4 leads is faster than the other ones and the turn-off time is 286 ns instead of 350 ns. The higher switching speed induces higher voltage and consequently higher peak power dissipation.

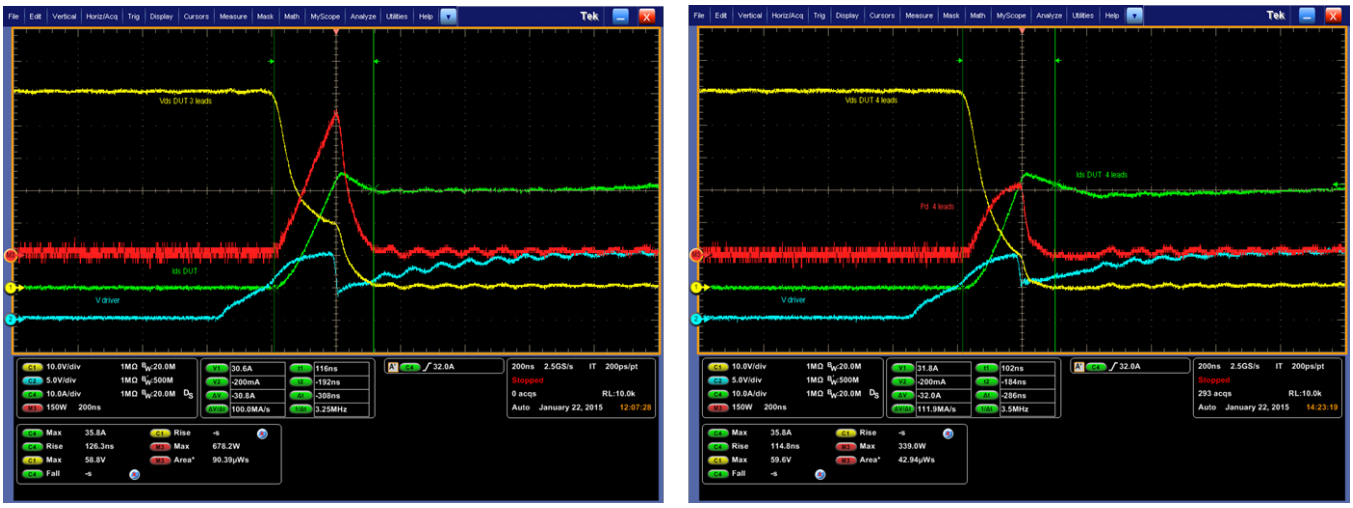
The E_{OFF} energy is slightly higher: 268 µJ vs 242 µJ (around 10%).

Figure 41. Turn-off comparison among the three (left) and 4 (right) leads solutions



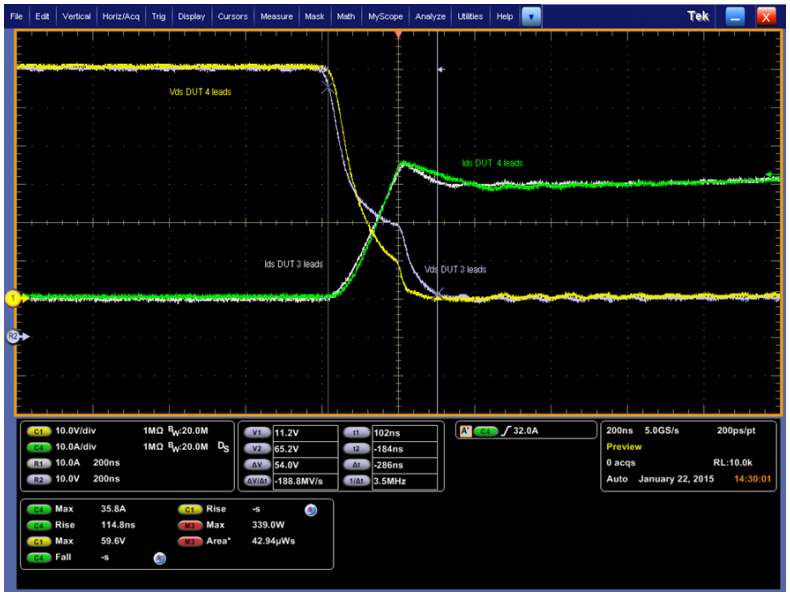
By monitoring the turn-on switching at the same V_{DS}/I_{DS} values, the main results were that the device with 4 leads had a lower E_{on} energy: 42.9 µJ vs 90.3 µJ (52% less) as shown in Figure 42. Turn-on comparison among the three (left) and 4 (right) leads solutions. This difference becomes interesting when V_{DD}/I_{DS} are getting increased.

Figure 42. Turn-on comparison among the three (left) and 4 (right) leads solutions



A zoom detail is shown in Figure 43. Turn-off gate-source comparison among the three (left) and four (right) leads solutions. The graph shows the comparison of the V_{DS} vs I_{DS} curves for the two devices.

Figure 43. Turn-off gate-source comparison among the three (left) and four (right) leads solutions



The main difference is the shape of the V_{DS} slopes (instead the I_{ds} current and di/dt are almost alike). At the beginning, the V_{DS} slope of the 3-lead device is similar to the 4-lead one, but when the current starts reaching its half value, a sort of smoothing occurs resulting in an additional loss of the switching energy. The reason is that the k-source of the leads is used also as a return path for gate driving. The K-source is not interested by the I_{DS} current so that the external V_{GS} (coming from the gate driver) is almost the same as the intrinsic V_{GS} device during the turning on. Instead, in the 3-lead device, the source pin is used also as return path for gate driving. This solution implies that during turning ON external V_{GS} is lower than intrinsic V_{GS} device, because the external V_{GS} is affected by a voltage drop occurring in the source pin due to parasitic components.

During the turning on, the main parasitic voltage drops can be resumed as follows:

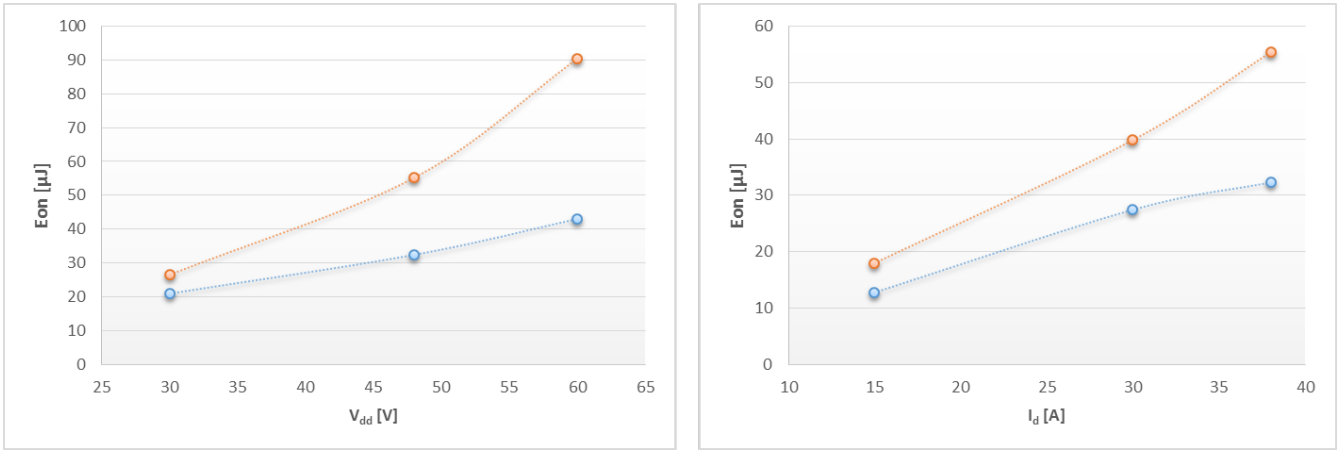
- Parasitic inductance voltage drops depending on the parasitic inductance value and di/dt

- Parasitic resistance voltage drops depending on the electric resistance of source wires and lead. The voltage drop is linear to the current I_{DS}.

The 3-lead intrinsic V_{GS} gets lower linearly with the increase of the I_{ds} current, this affects the R_{DSON} modulation and, consequently, its V_{DS} slope shape.

Finally, Figure 44. Turn-on (left) and turn-off (right) energy wasting shows the energy losses during the device start-up phase. The two graphs below show a lower energy loss during the turn-on of the device with k-source. This is more evident at higher V_{DD} and I_{DS} values.

Figure 44. Turn-on (left) and turn-off (right) energy wasting



3 DC motor in H-bridge configuration

The following figure shows a typical H-bridge schematic used in all those applications where a brushed motor rotates in both directions.

Figure 45. Full-bridge topology for DC brushed motor driving

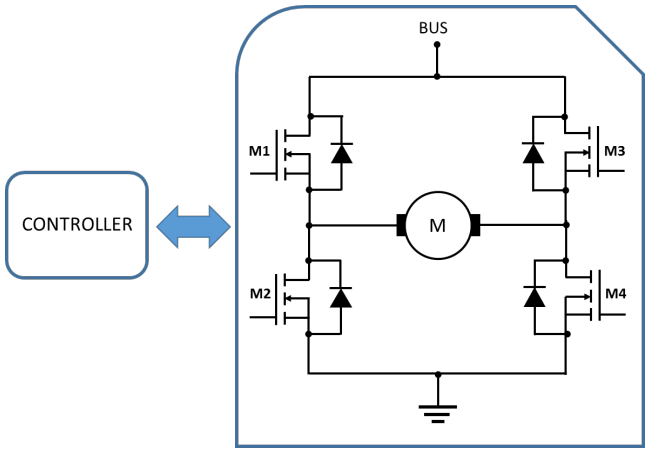


Figure 46. Steady state full-bridge switching waveforms shows the M2, M3 and M4 V_{gs} voltages (voltage drop between gate and source) during the forward operation. The M2 (LS) is always on and M3 (HS) switches; M4 is in off state while the M3 is on, and in on state while the M3 is off (freewheeling phase) in order to reduce power dissipation.

The waveforms do not show any voltage oscillations or spurious voltage spikes.

Figure 46. Steady state full-bridge switching waveforms

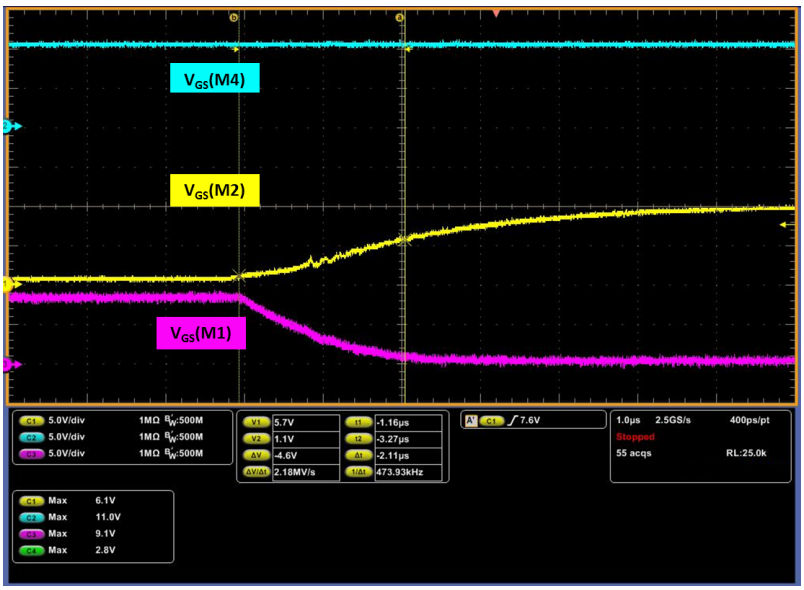
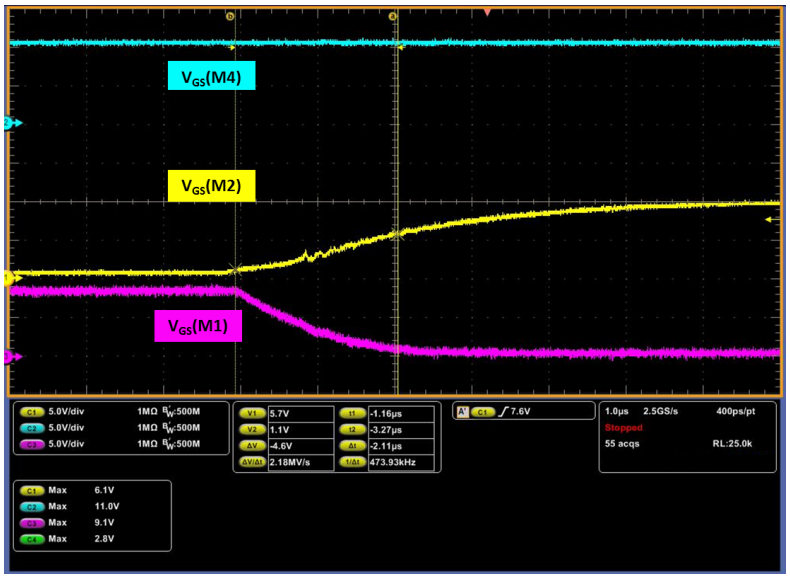


Figure 47. High-side turn-off detail shows the M4, M2 and M1 V_{gs} voltages during the down operation. The M4 (LS) is always on and M1 (HS) switches, M26 is in off state while the M1 is on, and in on state while the M1 is off (freewheeling phase).

The waveforms show the turn-off phase, M1 is off and M2 is on (freewheeling phase), and there are not any voltage oscillations or spurious voltage spikes.

Figure 47. High-side turn-off detail

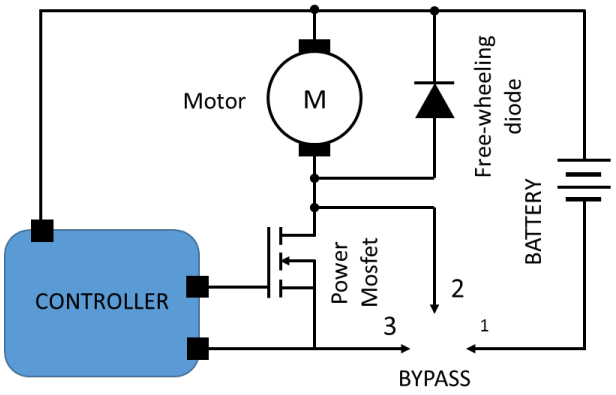


All considerations made in the previous paragraphs concerning the noise, the electrical efficiency and the emissions are also applicable for this circuit topology.

4 DC motor in single-switch configuration

The following figure shows a typical power tools application schematic.

Figure 48. Single-switch topology for DC brushed motor driving



Bypass Position	
1-2	Controller disabled; total battery voltage applied to the motor.
1-3	Controller enabled; battery voltage applied is proportional to the load.

The bypass could stand for the trigger of a drill; in fully activated position *1-2* the control is opened and the battery provides full power to the device. In position *1-3* the power is managed by the control that changes the duty cycle of the MOSFET polarization period in proportion to the applied load.

The TO-220 package, positioned so as to connect a copper or aluminum plate with a heatsink function on its drain, helps to dispose of the high temperature during normal operation conditions.

The phases to be analyzed are those occuring during the switching of the device with focus on the current during the turn-on, to the drain-source voltage during the turn-off and to the losses in these phases.

Figure 49. Locked rotor turn-off avalanche event shows the steady state waveform and its zoom during the power off phase.

When the gate-source voltage (V_{GS}) reaches the switch-off threshold of the device (section *#1* on the graph), the current starts to decrease (section *#2*) with a time dependent on the RLC parasites of the circuit. At the same time the drain-source voltage (V_{DS}) starts to rise exceeding the voltage value of the BUS and reaching a peak of 43.1 V (section *#3*). This voltage peak is due to the energy stored by the inductances of the circuit.

At this point the avalanche phenomenon takes place; in this time period, the most important part of the energy will be disposed of and the temperature of the device will increase.

As soon as the stored energy is disposed of, the V_{DS} voltage, after some oscillations, reaches the voltage battery.

The avalanche phenomenon, in addition to increasing the energy to be disposed of by the device during the shutdown phase, is also involved in reliability problems of the device's oxide, thus increasing the risk of failure if it occurs repeatedly in an application.

Figure 49. Locked rotor turn-off avalanche event

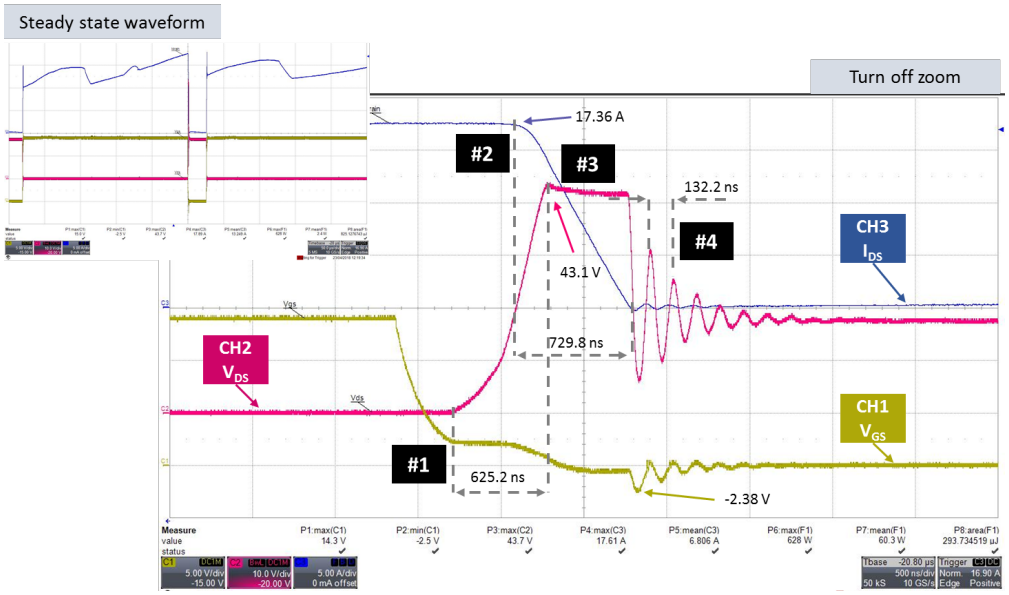


Figure 50. Locked rotor turn-off avalanche event with relevant energy measurement shows the same turn-off with the addition of the V_{DS} vs I_{DS} waveform which provides the power peak and, through the area, the energy managed during this phase.

Figure 50. Locked rotor turn-off avalanche event with relevant energy measurement

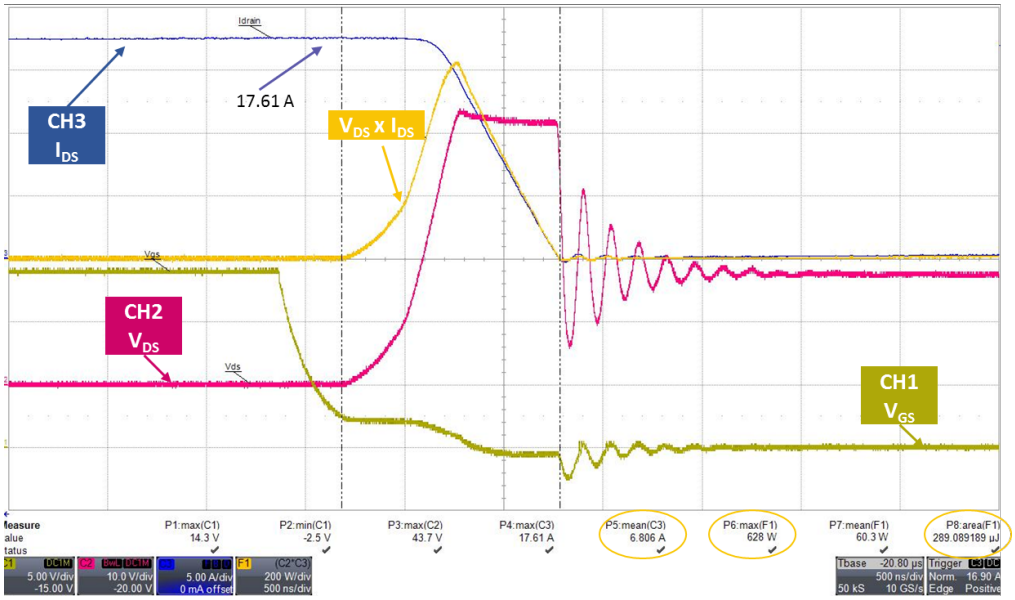


Figure 51. Locked rotor turn-on shows the steady state waveform and its zoom during the power on phase.

When the gate-source (V_{GS}) reaches the switch-on threshold of the device (section *#1*), the current starts to increase and the drain-source voltage (V_{DS}) reaches a value equal to R_{DSON} x I_{DS} during the device conduction.

The I_{DS} current increases by exceeding the steady state value (section #2) and reaching the peak, shown in the figure, due to the current flowing in the anti-parallel diode of the motor, during the free-wheeling phase, that it is added to the current required by the load.

Once the recovery energy is finished, the current is stabilized at the value required by the load.

During the diode recovery phase, there are some noises both on the V_{DS} voltage and on the V_{GS} which however, in this case, are not able to create excessive problems to the application.

Figure 51. Locked rotor turn-on

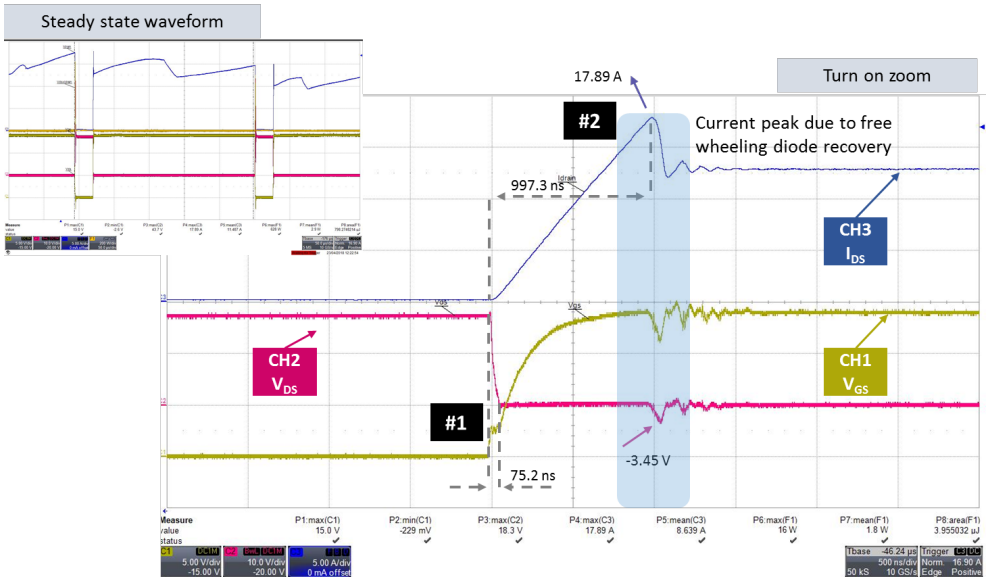
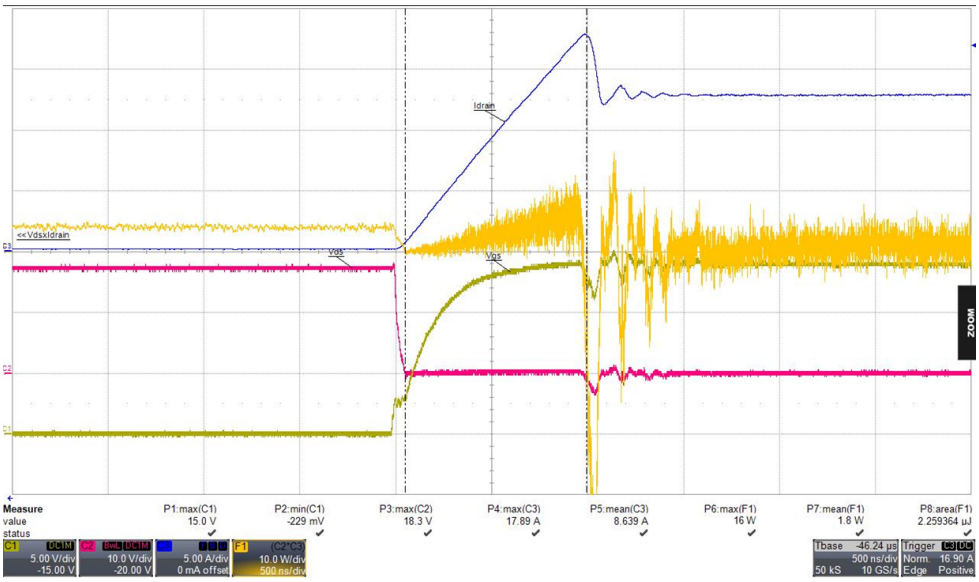


Figure 52. Locked rotor turn-on with relevant energy measurement shows the same turn-on (as in the previous figure) with the addition of the V_{DS} vs I_{DS} waveform which provides the power peak and, through the area, the energy managed during this phase.

Figure 52. Locked rotor turn-on with relevant energy measurement



5 EMI investigation

For applications that manage high current and voltage values in hard switching, the board layout could be critical regarding the track lengths and widths, the circuit areas as well as the proper routing of the traces and the optimized reciprocal arrangement of the various system elements and power sources in the PCB area.

For a better driving of the MOSFETs it will be necessary, for example, to ensure that the signal tracks, such as the one for driving the gate of the devices, are not surrounded by the ground power track.

The parasitic inductances due to PCB traces could have an impact on the EMI issues and on the over-voltage spikes.

As discussed in the previous sections, the softness of the freewheeling diode plays a fundamental role on the power system emissions and efficiency.

The low-side device should have soft switching without dangerous voltage spikes and high ringing frequencies between the drain and the source. This behavior can be achieved by using a Power MOSFET with a low reverse recovery charge (Q_{RR}) that has a direct impact on the value of the overshoot.

A higher Q_{RR} value means higher overshoots. Lower V_{DS} overshoot and ringing reduce the potential risk of a shoot-through event. Furthermore, soft recovery enhances the overall EMI performance, as the switching noise is reduced.

Another factor that influences the current and the output voltage behavior, during the tur- on and turn-off phases of the devices, is their output impedance consisting of C_{OSS} and R_{OSS}. The higher this impedance is, the higher is the ability to dampen the oscillations.

Figure 53. Turn-off voltage spike and dumpling details shows the turning off of two 100 V devices with different technological characteristics. The voltage and the current ringing of the device 2 is lower than the other one thanks to the output resistance characteristic (shown in Figure 54. R_{OSS} vs V_{DS} measurement detail). The device 2 has an output resistance higher than the device 1, which also has a less stable pattern compared to device 2. This instability leads to greater voltage ringing during the shutdown.

Figure 53. Turn-off voltage spike and dumpling details

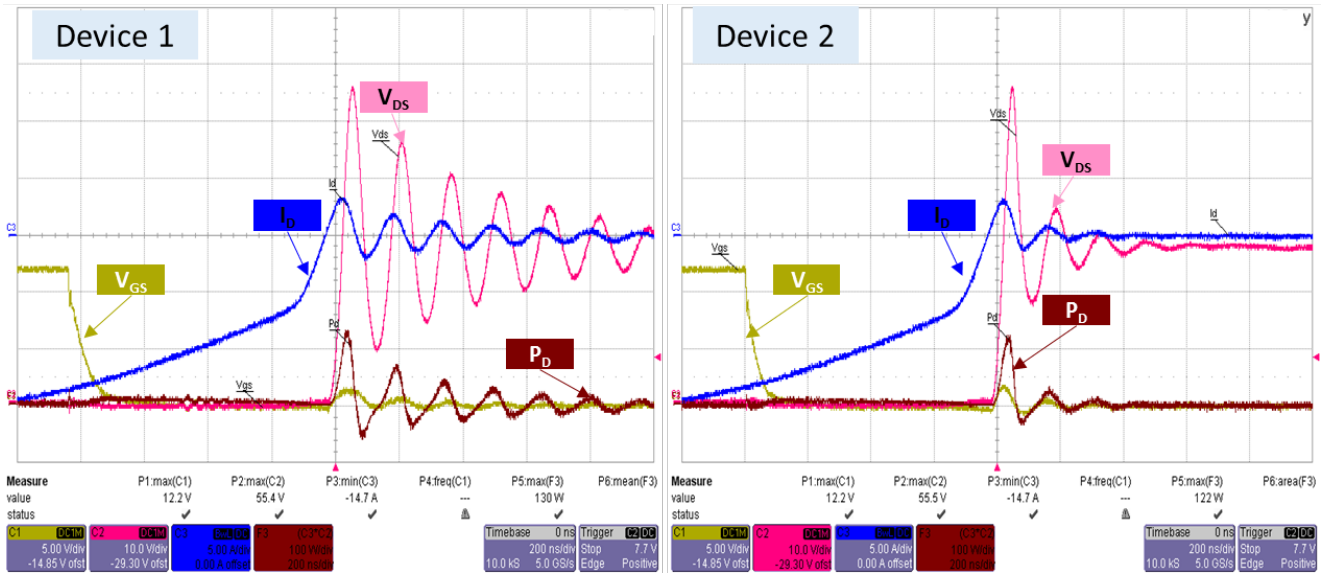
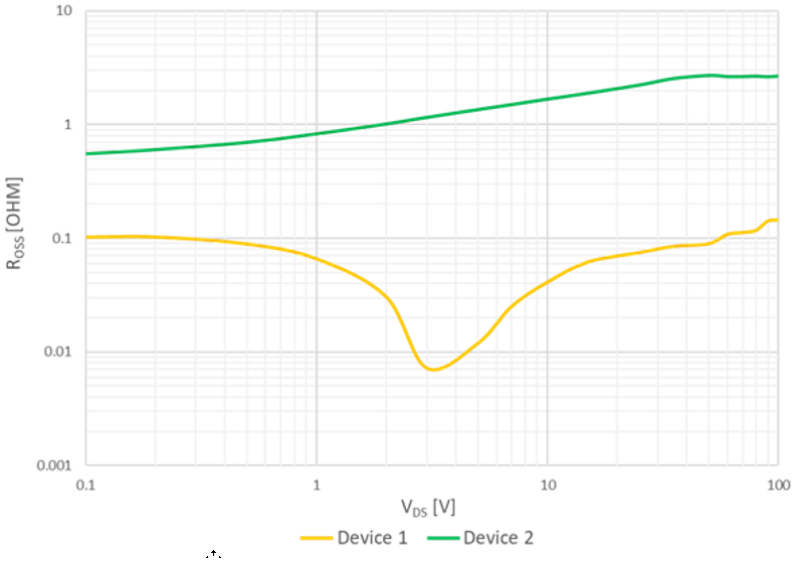


Figure 54. R_{OSS} vs V_{DS} measurement detail



5.1 Technology comparison

A significant reduction of the swithcing emissions can be achieved using the trench gate field-stop technology.

Figure 55. Body drain diode recovery process shows a comparison between the MOSFET current on the freewheeling diode in the "old" planar technology and the one got on a diode in a device with two different trench technologies.

The traditional trench improves the Q_{RR} needed to reduce the power loss during the turn off phase. The advanced trench technology is an improvement of the previous one enhancing the softness of the diode.

The energy lost during the turn-off phase will be lower, and the recirculation current and its oscillations, which are the cause of the frequency emissions, will end faster.

Figure 55. Body drain diode recovery process

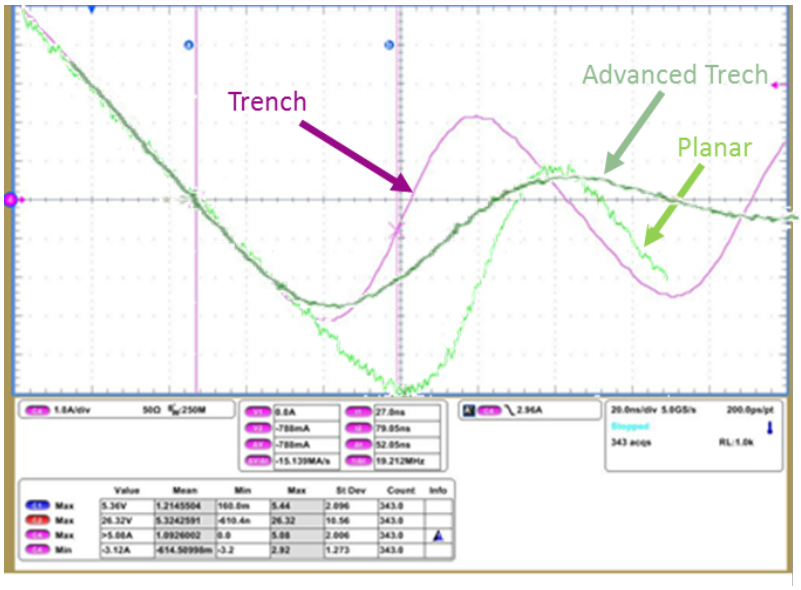
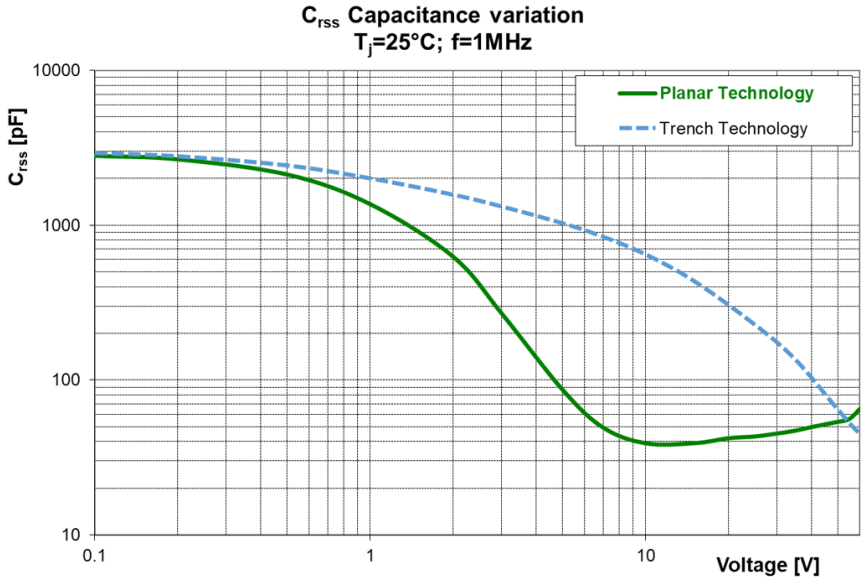


Figure 56. Planar vs trench C_{RSS} comparison shows the trend of the reverse transfer capacitance relative to the two devices, with different technology, with the recovery current previously shown. The device in planar technology has a capacity variation with the voltage much more pronounced than the one in trench technology.

Figure 56. Planar vs trench C_{RSS} comparison

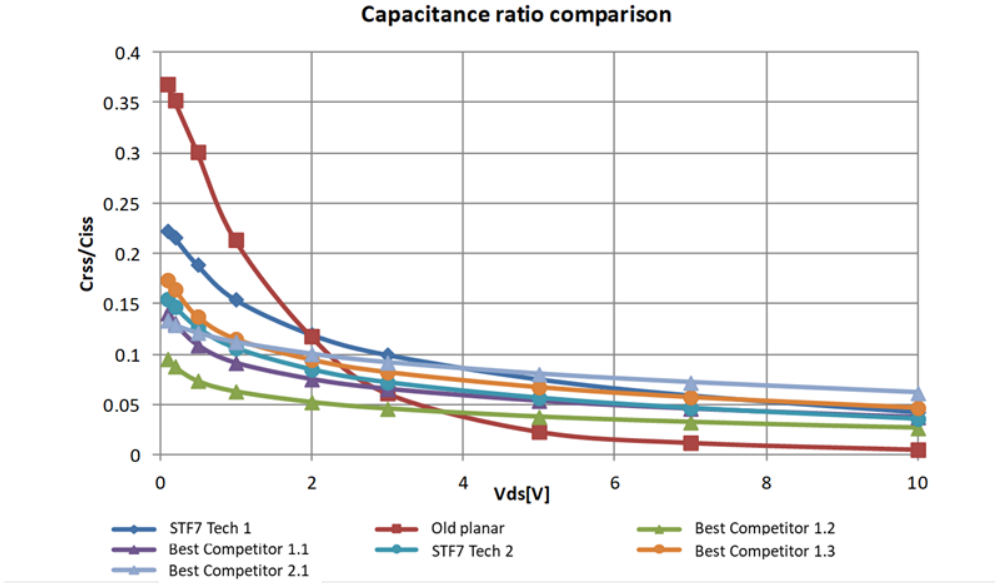


Beside a single Miller transfer cap, another important parameter to be considered to minimize the sensitivity to EMI is the C_{rss}/C_{iss} ratio in terms of maximum amplitude at V_{DS} = 0 V and it decreases the trend at higher V_{DS}.

This ratio is a good indicator of how the MOSFET can control the di/dt and the dv/dt during the transient phases. Moreover, this ratio determines the under threshold current conduction effect in the MOSFET impacting the Miller effect minimization as well, as reported in previous paragraphs. Due to this phenomena, the low current going to the stray inductances of the PCB contributes to the EMI/EMC emissions of the system.

The following figure shows the cap ratio curves of the trench technology devices (vs the old ST planar technology) by main suppliers.

Figure 57. Capacitance ratio curves



5.1.1 Application example (1)

This example will show how to limit the device emissions by fine-tuning the board's passives in order to reduce the noise impact of the turning on and off phases.

The benchmark analysis of a motor control application in an H-bridge topology is used as an example.

The figures below show the V_{GS} voltages of the four devices of the H bridge during switching. Both the turn-on and the turn-off switching are affected by noise and oscillations.

As shown in Figure 58. High-side turn-on waveforms with relevant high-frequency oscillations, which is a zoom during the oscillations, the frequency of such oscillation is around 277 MHz matching the EMI frequency. The voltage oscillations are in general caused by:

- Power MOSFET intrinsic capacitance, which value depends on V_{DS}
- Miller effect on the MOSFET
- Parasitic capacitance-inductance of the schematic tracks in the layout.

In order to reduce voltage oscillations, some components have been replaced.

Figure 58. High-side turn-on waveforms with relevant high-frequency oscillations

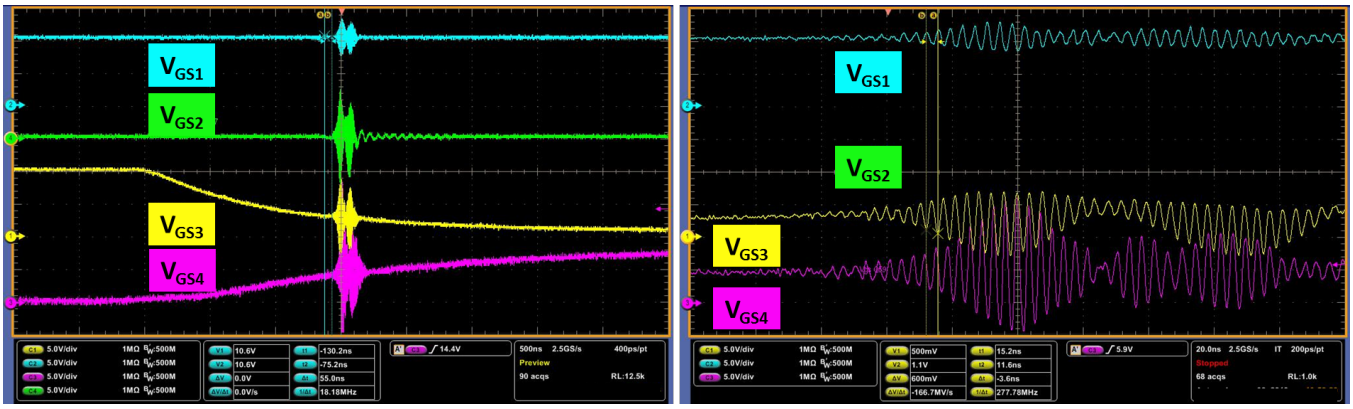


Figure 59. High-side turn-on and turn-off waveforms after modifications shows the turn-on and the turn-off of the same devices after some modifications. The voltage ringing is disappeared and the operation of the motor controller is good.

This condition was obtained with the following modifications:

- R_{GOFF} resistance of device 2 (LS) replaced with a shortcut, therefore set at 0 Ohm
- C_{GS} capacitance of device 2 (LS) reduced from 10 nF to 2 nF
- C_{GS} capacitance of device 4 (HS) removed (open circuit)

Figure 59. High-side turn-on and turn-off waveforms after modifications

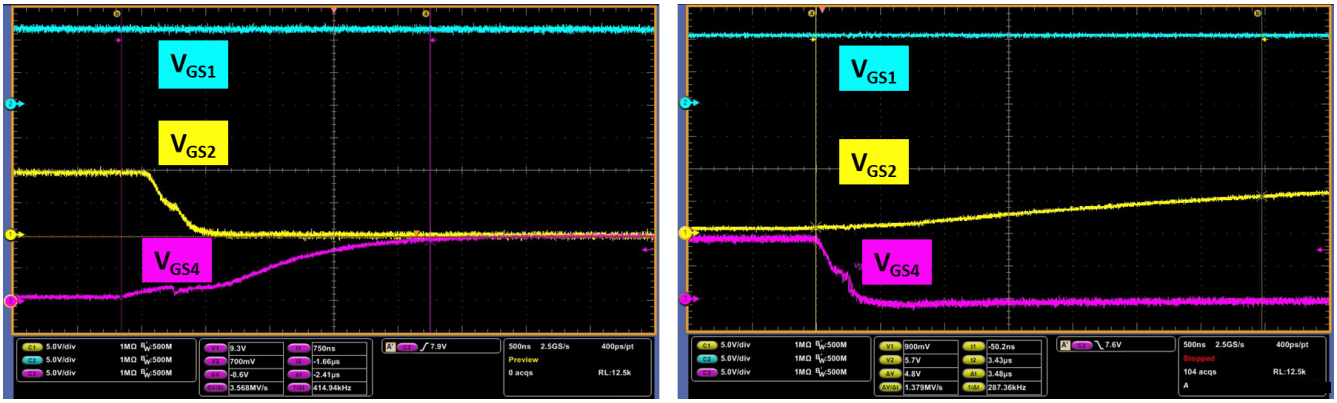


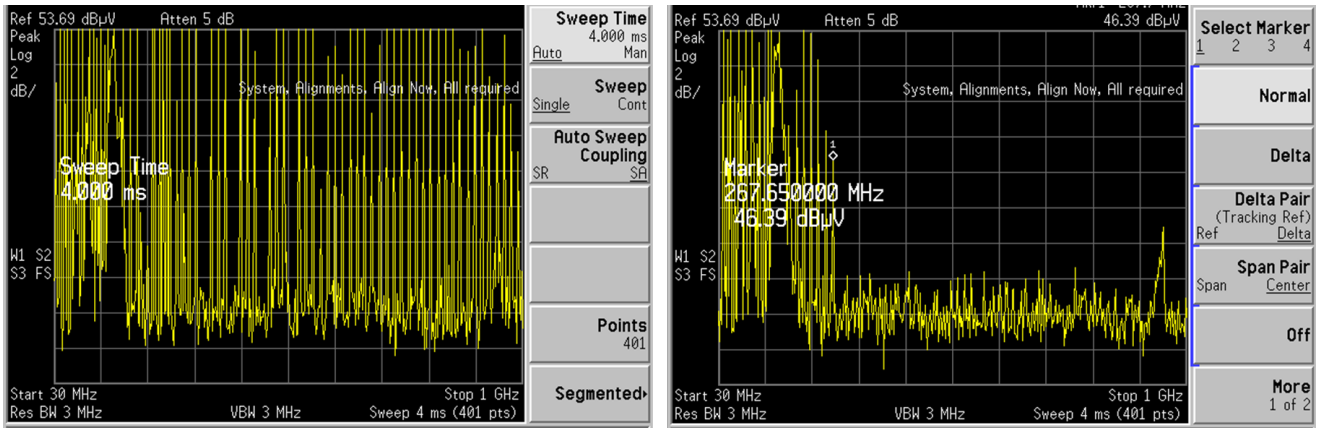
Figure 60. Comparison of radiated emissions before (left) and after (right) hardware modifications shows the EMI measurements and comparisons performed on the board in the same application area before and after the fine tuning.

The measurements were performed using the following equipment:

- RSH 400-1 probe SET HZ-15 (0÷3GHz) - 20 dB attenuation (ROHDE SCHWARZ)
- AGILENT E4402B 100 Hz - 3 GHz spectrum analyzer

The graph on the left shows that the application has emissions which flatten in the right graph where there are only peaks due to power supply except for 43.9 dBuV at 255.5 MHz.

Figure 60. Comparison of radiated emissions before (left) and after (right) hardware modifications



5.1.1.1 *Theoretical explanation*

Figure 61. Turn-off current path for the explanation of the Miller effect shows a typical current path during the device turn-off.

The upgrading performed in the board was addressed to minimize the Miller effect. The R_{G_OFF} minimization and the insertion of the 2 nF gate–source capacitance in the low side minimizes one step more the capacitive ratio already discussed in the previous sections.

A lower C_{GD} and a higher C_{GS} will minimize the residual V_{GS} (capacitive divider) when the device is off.

Considering the V_{GS} bouncing:

$$V_{GS} = R_{G\_TOT} \cdot C_{GD} \cdot {}^{dV}/_{dt}$$

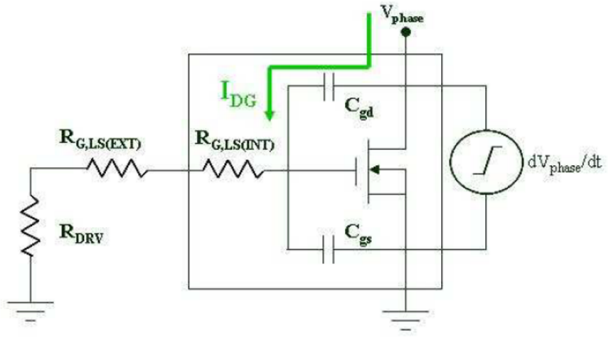
When R_{G_TOT} is the sum of the intrinsic R_G plus the external gate resistor R_{GOFF} plus the output driver resistance R_{DRV}.

If the V_{GS} value is close or above the FET V_{th}, it can produce a sub-threshold conduction of the FET which is the root of the noise.

Therefore, the gate-source capacitive finetuning and the R_{G_OFF} reduction are addressed to minimize the bouncing on the gate. The layout has an impact (behavior of different bridges) because the PCB tracks have spurious inductances that affect the di/dt and therefore the oscillation as well (RCL resonant circuit).

R_{G_EXT} and the IC driver next to the gate pin can improve the switching of the FET. This leads to L stray minimization and smoothing of oscillations which are the sources of EMI.

Figure 61. Turn-off current path for the explanation of the Miller effect



5.1.2 Application example (2)

Another example of radiated emission investigation can come from the application shown in Section 2.6.1 On-bench analysis which concerns a tri-phase bridge topology with 6 paralleled MOSFETs for each leg.

In this second application case both the radiated and the conducted emissions were analyzed.

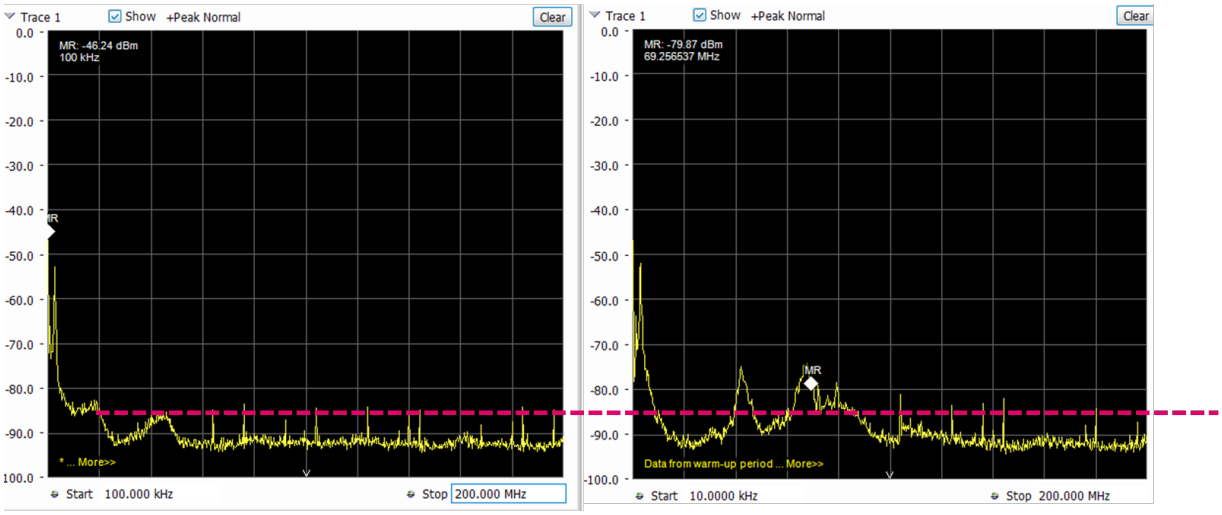
A Tektronics spectrum analyzer (RSA3026B) was used for the radiated emissions. The RSA306B uses the PC and Tektronix SignalVu-PC™ RF signal analysis software to provide real time spectrum analysis, streaming capture and deep signal analysis capabilities for signals from 9 kHz to 6.2 GHz for field, factory or academic use.

Figure 62. Comparison of radiated emissions between two different MOSFET technologies on the same board shows two different captures taken using a probe, which was put on a single MOSFET, during the nominal operation condition of the board.

The two captures show different results, in terms of emissions, for two boards equipped with different MOSFETs which were used under the same operating conditions.

The left graph shows lower emissions thanks to a better capacitive ratio and diode softness.

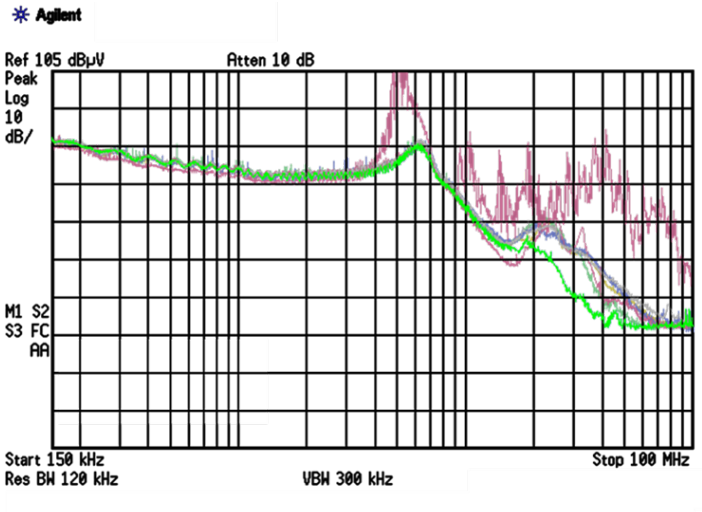
Figure 62. Comparison of radiated emissions between two different MOSFET technologies on the same board



For the conducted emissions, the Agilent E7402A EMI test receiver was used with LISN 150 kHz - 100 MHz.

Also for this kind of emissions, the device with a better capacitive ratio and diode softness shows lower conducted emissions (green waveform in the following figure).

Figure 63. Comparison of conducted emissions for several MOSFET devices



Revision history

Table 4. **Document revision history**

Date	Version	Changes
26-Nov-2018	1	First release.

Contents

List of tables

List of figures