AN5265

VIPower VNHD7xxAY H-Bridges drivers

Introduction

The VIPower VNHD7008AY and VNHD7012AY H-bridges drivers are newcomer-devices belonging to the state-of-the-art M0-7 H-bridges family and targeting brushed 12 V DC Motor Control applications with power in the range 80 W to 150 W typically (medium to high power Automotive DC motors).

The majority of their embedded features are common with the rest of the family so this document is to be considered as a complement of the AN5026 available on www.st.com.

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1 General Items

The worldwide revenue for electric motors in automotive applications is expected to increase dramatically in the next years with about 68% of DC Brushed motors in automotive applications and remaining part formed by brushless and stepper motors. In 2021 each car should have in average 28 DC motors reaching up to 70 DC motors in premium segment. On top of traditional applications like door lock, windows lift, sunroof many emerging application, which target mostly Advance Driver Assistance Systems, Safety, Body Computer and Exhaust gas treatment, are leading the growth:

- Power lift gate
- Tow hitch
- Safety belt pretensioner
- Spoiler adjustment
- Active grill shutter
- Seat vibration
- Port flap for the on board charger
- Exhaust recirculation flap
- Exhaust noise damper flap
- Camera adjustment

Some common applications with DC motors with a rated current higher than 5 A are shown in the following table:

Table 1. Typical medium and high power Automotive DC motors applications

Application	Peak current (A)	Load continuous current (A)
Dual washer pump	35	8
Windows lift	27	6
Sun blind	18	6
String column	25	8
Power lift gate	43	9
Seat belt pretensioning	20	8
Tow ball	30	20

In order to drive those applications low Ohmic PowerMOS should be used. VNHD7008AY and VNHD7012AY (typical $R_{DS(on)}$ of High Side is 8 mΩ and 12 mΩ respectively), in PowerSSO-36 package represent a suitable solution and are integrated chips for the driving and protection of a full H-bridge; the gates of the two external Power MOS acting as Low Side can be driven directly by VNHDxxAY.

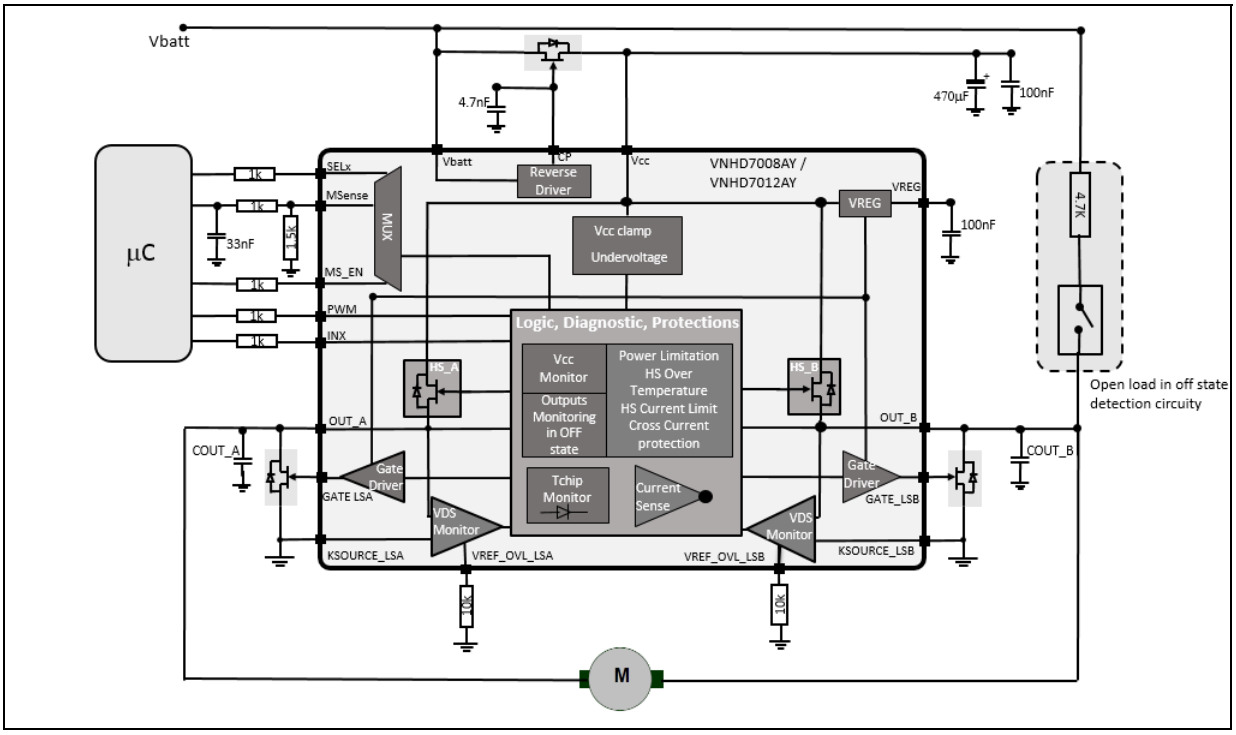
2 Suggested application schematic and PCB layout

2.1 Typical application schematic and block diagram

The M0-7 VNHDxxAY are a set of devices particularly suitable for driving two direction loads like DC brushed motors in 12 V car systems, featuring many state of the art features which give benefit to the whole application.

The *Figure 1* shows the functional block diagram and typical application schematic with main external connections and components for VNHD7008AY and VNHD7012AY.

Figure 1. VNHD7008AY and VNHD7012AY functional block diagram of and typical application schematic.



2.2 Block description

In the following table the internal functional blocks of VNHD7xxAY are described.

Table 2. Main Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table and avoid cross Current.
Undervoltage (UV)	Shuts down the device for battery voltage below 4 V.
Vcc clamp	Protects the device against the high voltage on the battery line.

Table 2. Main Block description (continued)

Name	Description
LS Gate driver	Drives the gates of the two external Power Mos acting as bridge Low Side to allow a proper Ron.
HS Current limitation	Limits the motor current in case of short circuit.
Power limitation	Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.
High-side over-temperature protection	In case of short-circuit or overload, when junction temperature exceeds a certain threshold it shuts down the concerned Power Mos driver to prevent degradation and to protect the chip.
Tchip Monitor	Provides a signal linked to the Chip temperature by a feedback on the MultiSense according to the setting of the MUX.
Vcc Monitor	Provides a signal linked to the Vcc voltage by a feedback on the MultiSense according to the setting of the MUX.
V_{DS}_MONITORING	Protection of external Low Side Power MOS against short to battery failure.
Outputs monitoring in OFF state	Signalize, in combination with an external resistor, an open-load when the switches are off by a feedback on the MultiSense.
Reverse Driver	Charge pump designed to drive the external N-MOSFET used on the battery track for the reverse battery protection.
VREG	Internal voltage regulator that provides the supply for the gates of the external low-side switches.
Current Sense	The current sense provides a signal linked to the OUT current on the MultiSense according to the setting of the MUX.

2.3 Pin description

The M0-7 VNHD7008AY and VNHD7012AY are designed to be housed in 36-lead PowerSSO-36 package with one exposed pad on the surface in order to increase thermal conductivity to the PCB.

- **VBAT:** Battery supply, connection to the source of the external PowerMOS used for the reverse battery protection.
- **V_{cc}:** Supply voltage. Drain of the high-side switches and connection to the drain of the external PowerMOS; In combination with VBAT pin it acts as reverse battery protection.
- **CP**: Drives the gate of external Power-MOSFET for the reverse battery protection.
- **INA, INB:** voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level on INA turns high side A (HSA) on; logic high level on INB turns high side B (HSB) on.
- **PWM:** voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level turns one or both the low side drivers on, depending on the state of INA, INB pins. A square wave signal with frequency up to 20 kHz can be used on this pin for motor speed control.
- **OUTA, OUTB**: these output power pins are connected to the external load. The OUTA leads are internally shorted to the sources of the HSA PowerMOS and must be externally connected to the drain of the LSA PowerMOS; likewise for OUTB. All OUTA

and OUTB leads must be connected together to corresponding leads to ensure uniform distribution of the load current in the device.

- **GATE_LSA, GATE_LSB:** Gate driver of the external PowerMOS LSA and LSB respectively.
- **KSOURCE_LSA, KSOURCE_LSB**: sources of External MOS to the LSA. Ground connection.
- **VREF_OVL_LSA, VREF_OVL_LSB:** Sets the threshold for V_{DS}_MONITORING feature of the external PowerMOS LSA and LSB.
- **VREG**: Pin for the Internal voltage regulator that provides the supply for the gates of the external low-side switches, a capacitor of 100nF has to be connected between this pin and Ground.
- **MultiSense:** the multiplexed analog sense output pin:
  - delivers a current proportional to the HSA or HSB output current according to the settings SEL0 = high or low and SEL1= low.
  - in combination with SEL1 = low and SEL0 = high or low settings, it develops a voltage flag in case of failure on the relevant output in the ON state as well as the OFF state.
  - In combination with SEL1= high and SEL0= high or low settings, it develops a voltage signal proportional to the high side chip temperature or Vcc pin voltage or Chip temperature.
- **SEL0, SEL1:** voltage controlled input pins with hysteresis, compatible with 3 V and 5 V CMOS outputs. They act as Multiplexer input pins thus:
  - In the ON state: when SEL1 is low and SEL0 is high, they allow sensing the current flowing in the HSA or a fault relevant to the Output A through the MultiSense output; likewise for SEL0 low, HSB and Output B.
  - In the OFF state: When SEL1 is low and SEL0 is high, they allow monitoring of the voltage level of DRAIN_LSA, SOURCE_HSA to detect and signal an open load or an output stuck to Vcc through the MultiSense output; likewise for SEL0 low, DRAIN_LSB, SOURCE_HSB.
  - Both in ON or OFF state: two combinations allow the MultiSense pin to develop a signal proportional to the high side driver chip temperature (SEL0=low, SEL1=high) or to the Vcc voltage (SEL0=SEL1=high).
- **MultiSense_EN:** voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. A logic high level enables the MultiSense output reading. A logic low level sets the MultiSense output to high impedance.

2.4 Standby mode

When INA = INB = PWM = SEL0 = SEL1 = MultiSense_EN = 0 device enters standby after T_{D_STBY} (this parameter is given in the datasheet). In standby mode also the CP for reverse battery protection is turned off.

To power on the device from standby it is recommended to toggle INA or INB or SEL0 or SEL1 or Multisense_EN from 0 to 1 first; then toggle PWM from 0 to 1 with a delay equal or larger than 20 µs (this parameter is present in the datasheet and it is named tstby_ovl_lsd) to avoid any overstress on the device in case of an existing short-to-battery.

2.5 Basic External components to drive and protect

The typical application schematic (see the *Figure 1: VNHD7008AY and VNHD7012AY functional block diagram of and typical application schematic.*) shows some basic external components to protect the device itself and other electronic device (i.e. microcontroller) connected to the device.

For general description of basic external components, (see chapter 1.5 of the VIPower M0-7 H-bridges Application note - AN5026).

Specific features of the VNHD7008AY and VNHD7012AY family that require dedicated external components are:

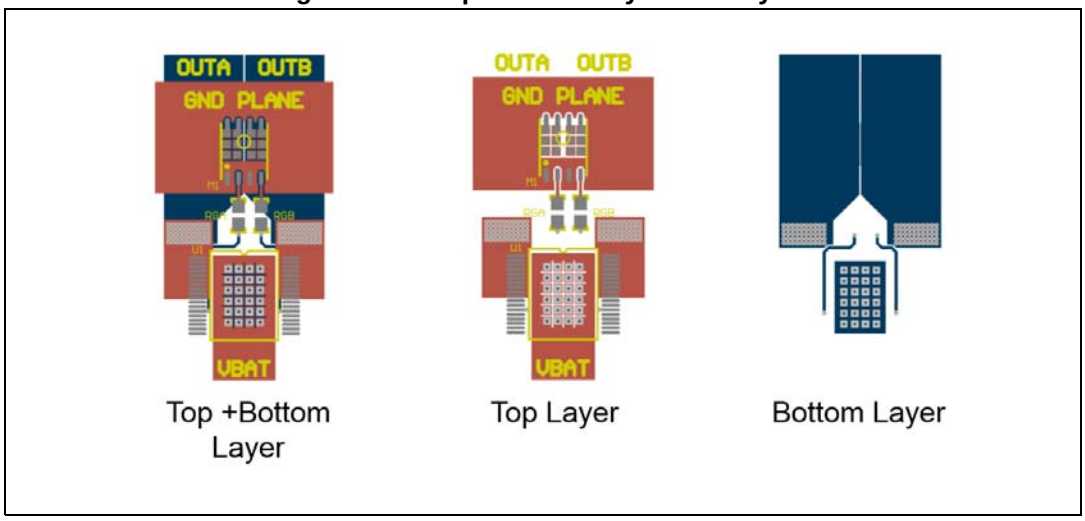
- N-MOSFET on the battery line: it acts as a reverse battery protection switch and it is driven directly by the embedded charge pump (see *Chapter 6: Protection against reverse battery with the embedded CP* for detailed description and dimensioning of the external Power MOSFET).
- Resistor for external Power MOSFET (used as Low Side of the H-bridge) protection: this resistor must be connected between VREF_OVL_LSx device pin and PowerMOS source pin. It is necessary for the V_{DS}_monitoring function that protects the external PowerMOS in case of short circuit OUT to battery. Dimensioning of this component is fully described in *Chapter 4.1: Principle of external MOSFET switching behavior* (Protection against short of Output to battery).

2.6 PCB general layout suggestions

In order to avoid ground shift between KSOURCE_LSx pins, and consequently to ensure the right V_{DS} protection intervention, it is fundamental to have the most symmetrical layout.

An example of symmetric and balanced layout with a two layer PCB is the following:

Figure 2. Example of two Layer PCB layout



The previous picture shows the simplified layout connections of a VNHD7008AY/ VNHD7012AY device with two Power MOSFETs housed in a PowerFLAT™ 5x6 Double Island (only the two R_{GATE} are placed between GATE_LSx pin and the relevant gate of the Power MOSFETs).

Best performance in terms of parasitic inductance and EMC can be reached with a 3 or 4-layer PCB with a dedicated GND plane that improves filtering efficiency.

All filtering capacitors must be placed as close as possible to the device terminals to keep the parasitic inductors of the PCB-wires as low as possible.

To keep the RF noise from the DC motor low and reach good immunity from ESD, the capacitors C(OUT) and C(Vbatt) must be placed on the board connector and directly soldered to the module GND usually in star connection with all possible ground signals (Digital GND, Analog GND and Power GND).

For a more detailed description on ESD, EMC, component placements, see *Chapter 7: Rejection of Electro Magnetic Interference*.

3 Considerations for External Power MOS dimensioning

In order to fulfill all the application requirement for the full bridge configuration, it is very important to perform the right selection of the two external Power MOSFETs that act as Low Side drivers in the full bridge configuration.

This selection depends on various factors:

- Application battery Voltage range.
- Load (Motor or other) features such as: inrush current, stall current.

The VNHD7xxAY family devices have embedded all circuitry necessary to drive and to protect the external Power MOSFETs.

In this chapter it will be described the right way to select the external power MOSFET basing on the application constraints, while in *Chapter 5: Protection against Output short to battery* will describe the behavior of VNHD7xxAY and external MOSFETs in case of overload or short circuit to battery.

3.1 Applicative Battery range

The internal Low Side Driver Stage is designed to drive the external MOSFET gate in all the battery condition within the V_{cc} Operating Supply Range (from 4 V to 28 V).

In particular, the internal low drop voltage regulator (VREG) is designed to guarantee a driver voltage of about 10 V if Vbattery > 10 V, and a voltage equal to battery voltage if Vbattery < 10 V (until V_{cc} is bigger than 4 V). This should allow a proper MOS transition.

Moreover, if the application requires to correctly drive the load also in case of very low battery conditions (i.e. in case of voltage drop during engine cold start), the right external MOSFET has to be chosen in order to guarantee its correct activation also at very low battery voltage.

In particular, the MOSFET parameter to take into account is its threshold voltage $V_{GS(th)}$, that is the minimum gate voltage that initiates drain current flow.

This is especially valid in case of MOSFET PWM operation in order to reduce the total power dissipation.

In this condition a logic level gate-source threshold voltage device is suggested.

An example could be the STL76DN4LF7AG an Automotive-grade dual N-channel 40 V, 5 mΩ Power MOSFET housed in a Power FLAT 6x6 Double Island.

This selected device guarantees a typical $R_{DS(on)}$ of 7 mΩ with a V_{GS} = 4.5 V (see *Figure 3*)

Figure 3. Extract of STL76DN4LF7AG datasheet

Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 40 V			10	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 10 A		5	6	mΩ
		V_{GS} = 4.5 V, I_D= 10 A		7	12	

If the compatibility with very low battery voltage is not requested, also a “standard level gate-source threshold voltage ($V_{GS(th)}$) device could be chosen.

A typical example could be the STL15DN4F5: an Automotive-grade dual N-channel 40 V,

8 mΩ Power MOSFET housed in a Power FLAT 6x6 Double Island.

In this last case, as you can see in *Figure 4* the typical $R_{DS(on)}$ is guaranteed with a V_{GS}=10 V.

Figure 4. Extract of STL15DN4F5 Datasheet

Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
		V_{GS} = 0 V, V_{DS} = 40 V, T_C= 125 °C (1)			10	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 7.5 A		8	9	mΩ

Both part numbers (Standard or Logic level threshold) are Designed for automotive applications and AEC-Q101 qualified and guarantee in a single package the complete solution for the full bridge configuration.

Another important parameter linked to the application battery range is the so-called Drain-source breakdown voltage ($V_{(BR)DSS}$).

This value must be compatible with the VNHD7xxAY absolute maximum voltage that can be applied on Vcc/Vbatt pin.

This value is reported on the Table **Absolute maximum ratings** of the relevant datasheet and it has a value of 38 V for all devices belonging to VNHD7xxAY family.

So in this case, both Power MOSFET part number suggested above can be considered suitable because they have a minimum $V_{(BR)DSS}$ = 40 V.

3.2 Power dissipation

Power loss in a MOSFET comes from two sources. Every MOSFET has a resistive element, so it dissipates power as soon as current flows through the device. The resistive parameter is described as on-resistance, or $R_{DS(on)}$.

The other source of power loss is through switching losses. As the MOSFET switches on and off, its own intrinsic parasitic capacitance stores and then dissipates energy during each switching transition. The losses are proportional to the switching frequency and the values of the parasitic capacitances.

In case of PWM application, even if lower $R_{DS(on)}$ is able significantly reduce the conduction loss, the switching loss can have a not negligible role in the total power dissipation (especially in high frequency PWM application like motor drivers).

Before going deeply in power dissipation analysis, a very important parameter to take into account for the right external Power MOSFET dimensioning is the motor current profile. In general, there are three phases of motor current demand.

- **Inrush phase**: during motor starting phase, in order to provide peak torque, the current goes above nominal current for a short time.
- **Movement phase:** the moving motor draws less current; in general it is desired motor operation phase.
- **Stall phase:** the motor loses its movement speed and current becomes maximal; the current is limited by the armature winding resistance only.

In order to proper set the external Power MOSFET to connect as low side driver it is necessary to calculate the value of the maximum allowable drain current that avoids the activation of V_{DS} monitoring protection feature.(**see** *Chapter 5: Protection against Output short to battery* for a dedicated description).

When the power MOSFET is in ON state, the V_{DS} is given by the product of $R_{DS(on)}$ and the drain current ($I_{D)}$.

So, considering the maximum motor current (inrush or stall current), this relation must be satisfied:

Equation 1:

$$R_{DS(on)} < \frac{I_{REF\_OVL\_LSx\_MIN} * R_{OVL}}{I_{D\_MAX}}$$

Where:

I_{D_MAX} is the maximum motor current (inrush or stall current).

$I_{REF\_OVL\_LSx\_MIN}$ is the minimum Low-side drain-current overload reference current.

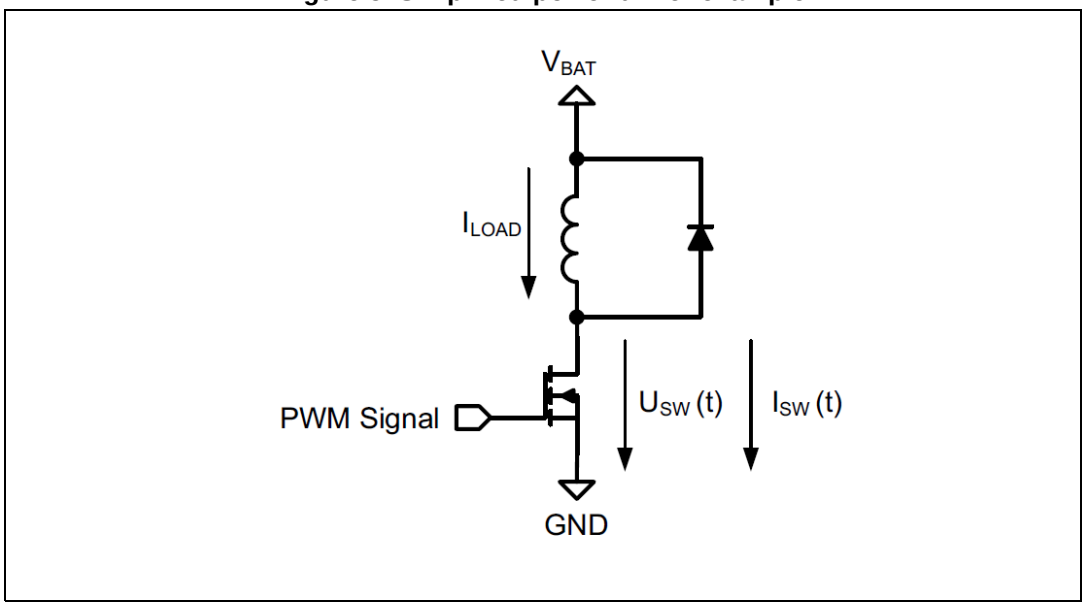
R_{OVL} is the external resistor (connected between $V_{REF\_OVL\_LSx}$ pin and GND) that sets the overload voltage threshold. This ensures no protection intervention in case the typical load is applied to the output (a detailed description of V_{DS} protection is given in (*Chapter 5:*

Protection against Output short to battery).

In order to calculate the power dissipated inside the power switch, configured as low side driver in a full bridge configuration, the simplified schematic in *Figure 5: Simplified power driver example* can be considered. In the picture the diode in parallel to the inductive load represents the parasitic body diode of the VNHD7xxAY device. This diode conducts as soon as the Low Side Power MOS switches off. For the VNHDxxAY devices the power dissipation due to reverse recovery time of the HSD is negligible.

The two main power dissipation sources will be considered individually.

Figure 5. Simplified power driver example



3.3 Conduction Losses

The Main source of power dissipated inside the Power MOSFET is the power dissipated in the its own ON resistance or $R_{DS(on)}$.

ON state power dissipation (W):

Equation 2:

$P_{0N} = R_{DS(on)} * I^2_{out,RMS}$

ON state energy loss:

Equation 3:

$E_{0N} = P_{0N} * T_{0N}$

Where TON is the ON state duration.

The $R_{DS(on)}$ parameter depends on both: temperature and V_{GS}. Relevant graphs are reported in the Power MOSFET datasheet in order to extract the $R_{DS(on)}$ value derating from the typical one (given at a specific IDRAIN / V_{GS}).

Note: Note that $R_{DS(on)}$ increases with temperature; so as the device heats, the power dissipation increases. This must be considered calculating the total device power dissipation.

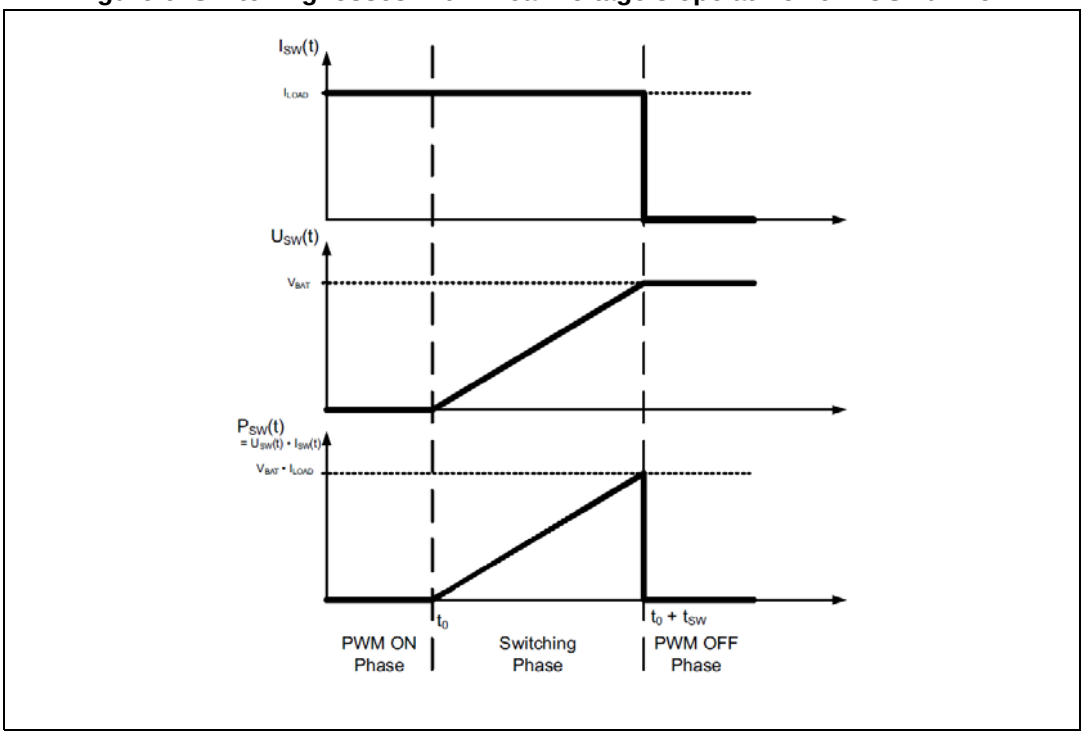
3.4 Switching Losses

The switching losses are important especially in PWM operation. Compared to conduction losses, the calculation depends on many factors like: the load characteristic (resistive, capacitive or inductive), the device characteristics (switching times) and the environmental conditions (ambient, temperature, battery voltage). This section deals with an inductive load (such as a motor).

To simplify the calculation of the switching losses for an inductive load, it can be assumed that the voltage over the switch will change linearly and the current is constant (as shown in *Figure 6: Switching losses with linear voltage slope at PowerMOS Turn-off*).

The instantaneous power dissipation during the switching phase is equal to drain to source voltage (V_{DS}) multiplied by the output current (I_{OUT}). Assuming linear switching times, the instantaneous power dissipation can be approximated by triangular waveform.

Figure 6. Switching losses with linear voltage slope at PowerMOS Turn-off



Under this condition, the energy loss during one PWM period is given by:

Equation 4:

$$E_{SW} = \int_{t_{0'}}^{t_{0'}+t_{swon}} U_{SW} * I_{SW}\, dt + \int_{t_0}^{t_0+t_{swoff}} U_{SW} * I_{SW}\, dt = \frac{1}{2} V_{BAT} * I_{LOAD} * t_{SW}$$

Considering an entire PWM period:

Equation 5:

$$t_{SW} = t_{SW_{ON}} + t_{SW_{OFF}}$$

Where t_{SWon} and t_{SWoff} are the external power MOSFET and off switching times.
So, the total switching power dissipation is:

Equation 6:

$$P_{SW} = \frac{1}{2} V_{BAT} * I_{LOAD} * t_{SW} * f$$

Where (f) is the PWM switching frequency.

3.5 Total power dissipation

In the total power dissipation calculate two cases must be considered:

- The power dissipated during the motor inrush phase that can last about 10-20ms. For the sake of simplicity, the device can be considered DC driven during this phase. So the power dissipated is:

Equation 7:

$$P_{inrush} = R_{DS(ON)} \times I^2_{Inrush}$$

- The power dissipated in steady state when the motor is driven in PWM. So the power dissipated is:

Equation 8:

$$P_{PWM} = P_{ON} + P_{SW} = \mathrm{R_{DS(ON)}} * \mathrm{I^2_{LOAD}} * DC + \frac{1}{2} V_{BAT} * I_{LOAD} * t_{SW} * f$$

Where DC is the PWM duty cycle.

It is important to check for both cases if the device is able to handle the power in order to avoid overheating/overload.

Considering the two separated phase (inrush and PWM steady sate), it is important to check that the maximum MOSFET junction temperature does not exceed the maximum operating device's temperature. So, considering the maximum ambient temperature for the specific application, the maximum device junction temperature could be calculated as follow:

Equation 9:

$$T_{J,max} = T_{AMB} + \Delta T$$

Where ΔT depends on thermal impedance and power dissipated as follow:

- For the Inrush phase it is important to check if the power dissipated during inrush phase inside the MOSFET:

Equation 10:

$$\Delta T = Zth_{j-a} * P_{inrush}$$

Where $Z_{thj\text{-}a}$ is the single pulse impedance related to the pulse duration.

- For the PWM steady state phase.

Equation 11:

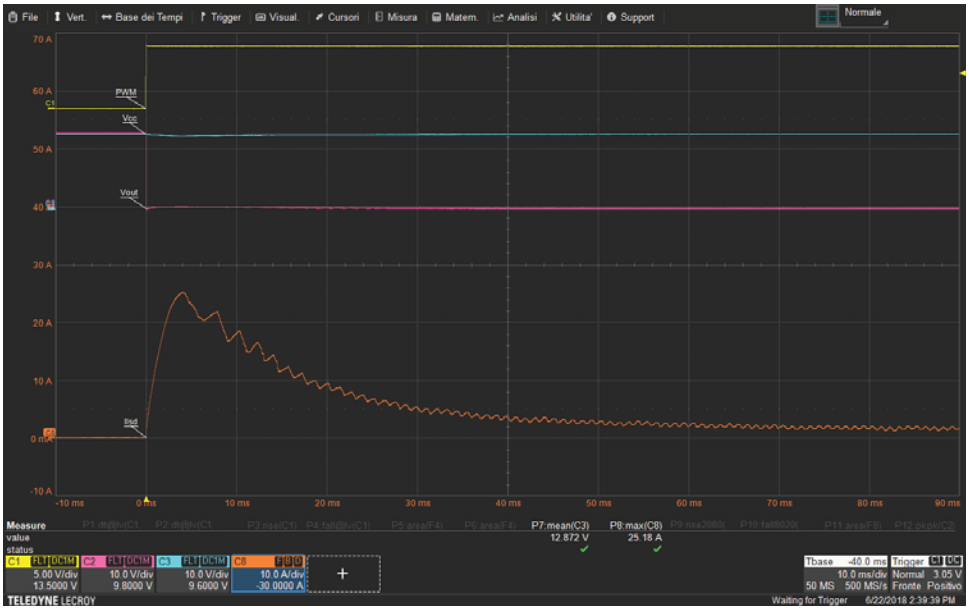
$$\Delta T = R_{Thj-a} \times P_{PWM}$$

3.6 Example

The following example shows a standard configuration of VNHD7008AY with STL76DN4LF7AG.

Next plot shows the behavior of the external PowerMOSFET during a motor inrush. The external Low side is driven in DC mode through VNHD7008AY PWM pin.

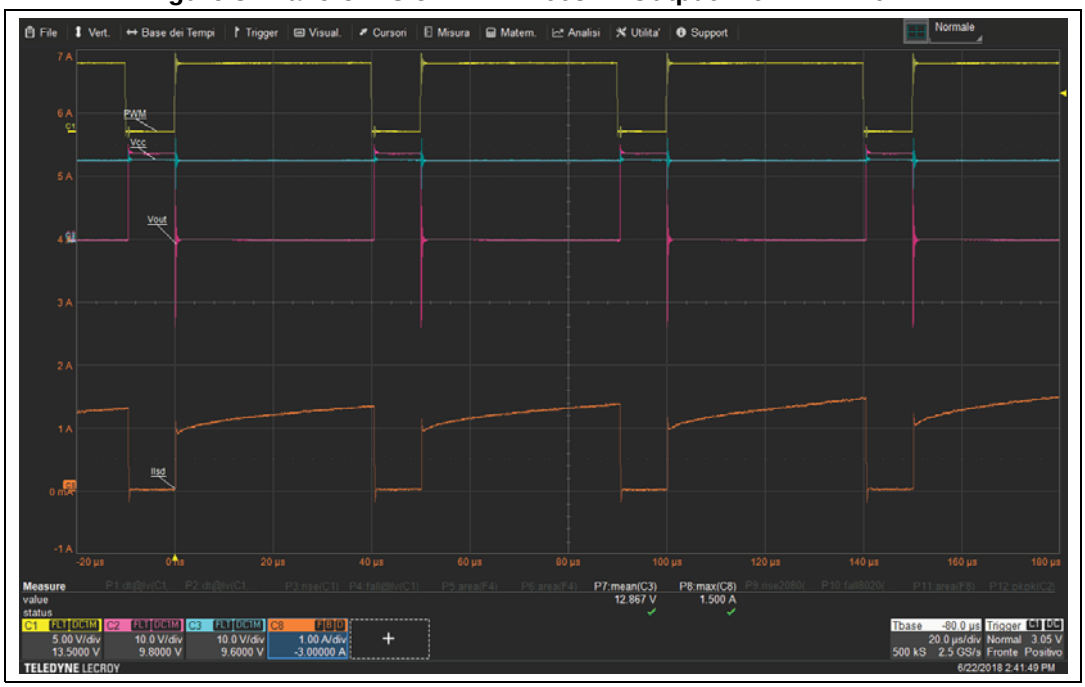
Figure 7. PowerMOSFET behavior during a motor inrush



In the picture, the current is the external PowerMOSFET current (not the motor current) and its peak value is about 25 A with a duration of about 10 ms.

Next *Figure 5*, *Figure 6* and *Figure 7* show an example of PWM 20 kHz 80% driving of VNHD7xxAY with the details of switch ON/OFF phase of the external PowerMOSFET. The ringing of the output voltage is due to a inductive-capacitive effect on PowerMOS.

Figure 8. Waveforms on VNHD7008AY Output with PWM 20 kHz

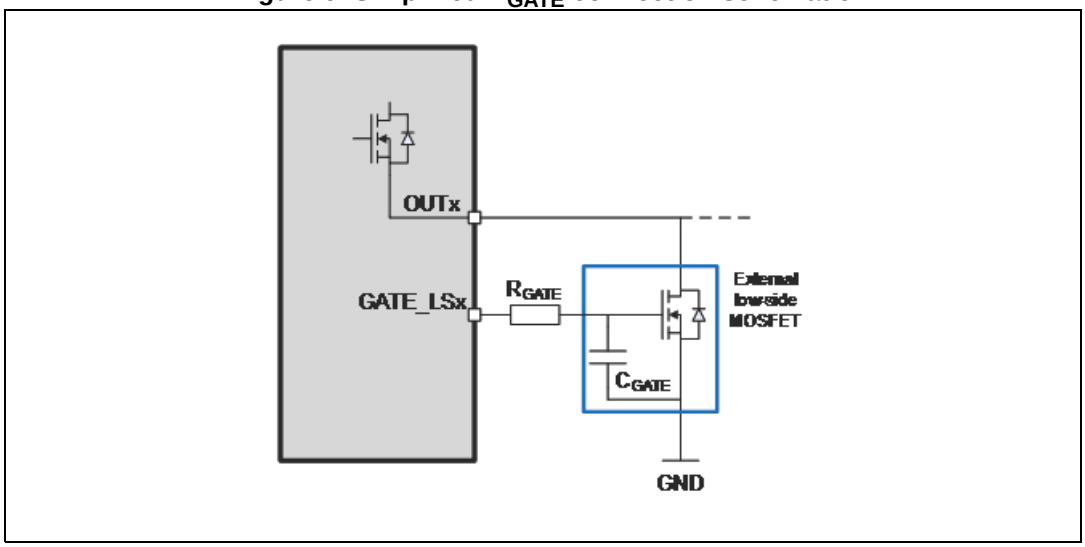


4 Adjustable low side flanks

The VNHD7xxAY embeds a dedicated pre-driver for control of external low-side power MOSFETs. Such circuitry preserves correct operation driving the internal High side and the external MOSFET Low-side, and avoiding shoot-through effect (High Side and Low Side belonging to the same leg both activated).

Switching behavior of external low-side Power MOSFETs is determined by its gate capacitance charge. The process of gate charge can be controlled by interconnecting the external component R_{GATE} (applied between external MOSFETs and H-bridge controller). See (*Figure 1: VNHD7008AY and VNHD7012AY functional block diagram of and typical application schematic.*)

Figure 9. Simplified R_{GATE} connection schematic



MOSFET gate capacitance in combination with gate resistor influence the overall Low-side switching time, switching losses, and also other aspects (e.g. EMI, dV/dt, dI/dt).

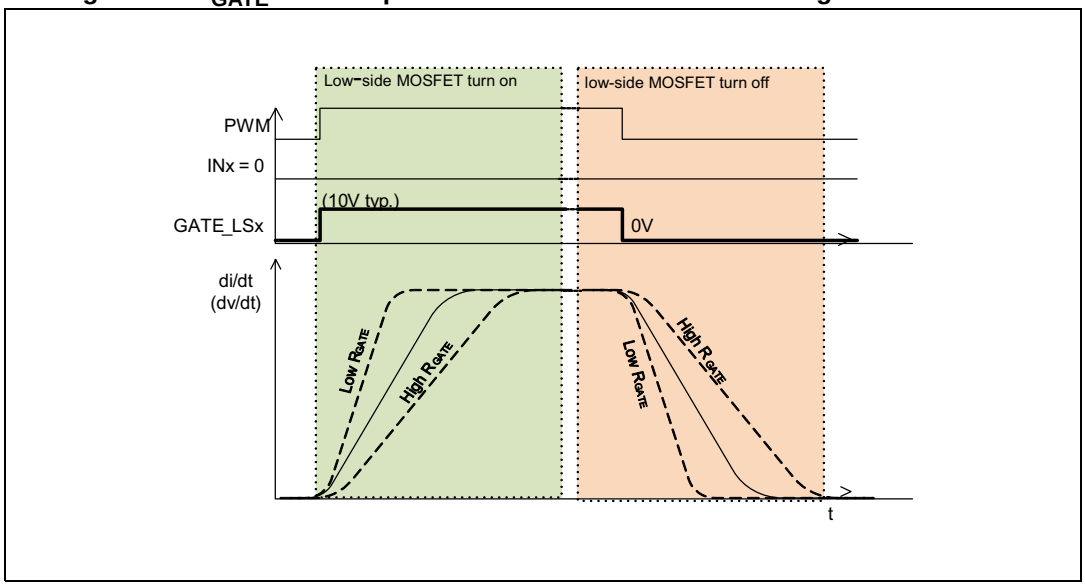
Selection of Low-side MOSFETs is usually linked with application case (current capability, switching time). External components are then adjusted to fit application needs, e.g. switching frequency, switching losses, inductance, EMI.

4.1 Principle of external MOSFET switching behavior

During the switching phases the VNHD7xxAY pre-driver (gate controller) injects current into the gate of external MOSFET during the low-side activation (source capability), while it sinks the current during low-side deactivation (sink capability). In these phases the MOSFET gate acts as variable capacitor; the applied Resistor fixes the current flowing from pre-driver to external MOSFET gate. Therefore, according to the resistor value, the slope of the switching MOSFET can be adjusted.

Applying the lower R_{GATE} value, the transient switching time of MOSFET activation and deactivation gets reduced, consequently the switching losses are less. (please see *Figure 10: RGATE value impact to low-side MOSFET switching characteristics*).

Figure 10. R_{GATE} value impact to low-side MOSFET switching characteristics



Following two examples depict switching characteristics of STL15DN4F5 MOSFET applying different R_{GATE} values, during low-side turn-on and turn-off:

Note: Measurement points are applied according the following schematic.

Figure 11. VNHD7xxAY simplified schematic

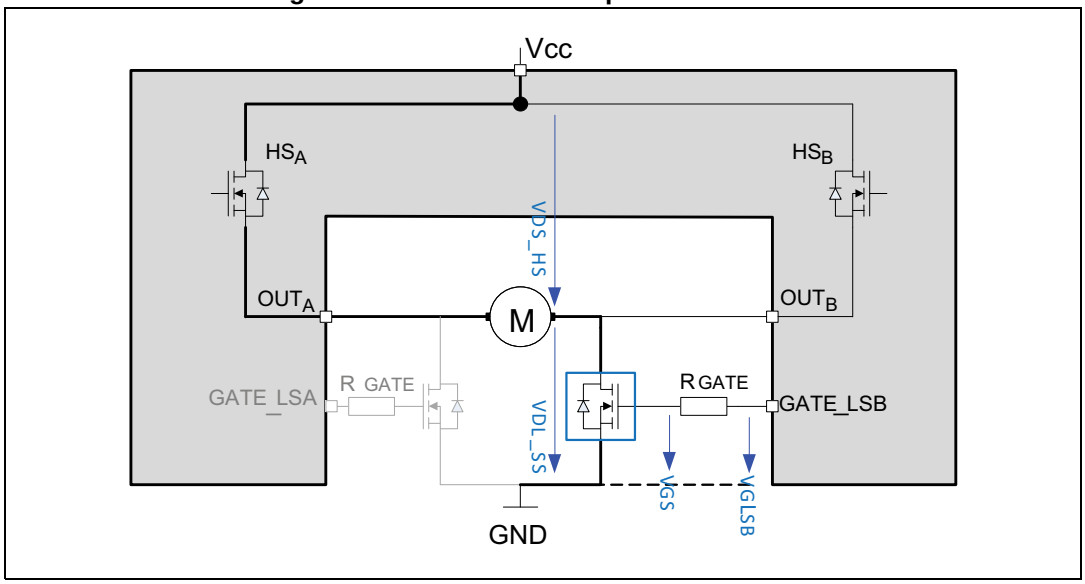
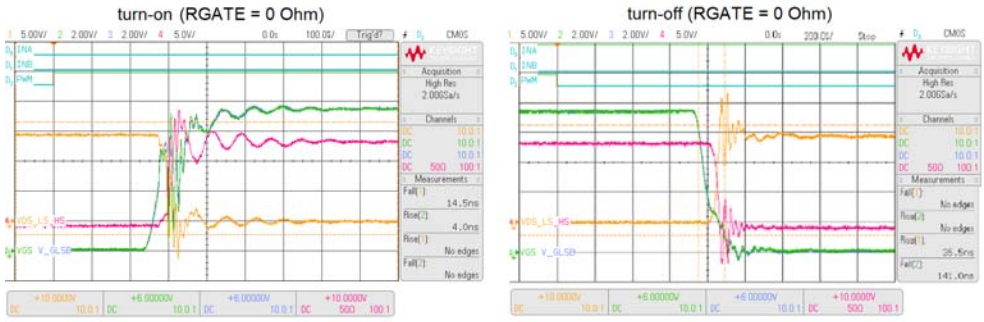


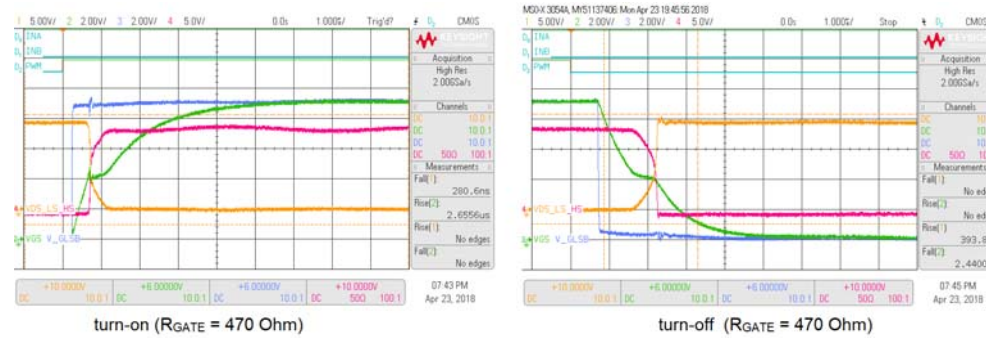
Figure 12. Example 1 motor load switching with STL15DN4F5 applying R_{GATE} = 0 Ohm



Example shows:

- Fast switching response time (turn-on = 15 ns; turn-off = 35 ns)
- High EMI noise (spikes on V_{DS})

Figure 13. Example 2 motor load switching with STL15DN4F5 applying R_{GATE} = 470 Ω



Example shows:

- Slow switching response time (turn-on = 281 ns; turn-off = 393 ns)
- Limited EMI noise (spikes on V_{DS} almost filtered)

As a general rule increasing R_{GATE}, following parameters are influenced:

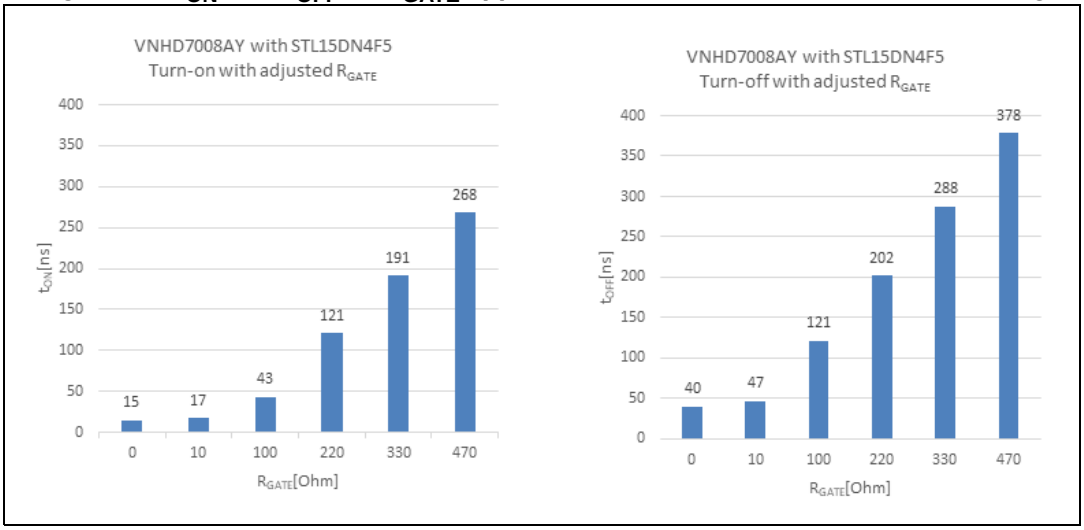
- Turn-on, turn-off times increase (slower MOSFET switching)
- Switching losses increase
- Turn on, turn off peak current decrease
- Slew rate dv/dt, di/dt decrease
- EMI noise decreases

Equivalent opposite effect is valid when R_{GATE} is decreased:

- Turn-on, turn-off times decrease (faster MOSFET switching)
- Switching losses decrease
- Turn on, turn off peak current increase
- Slew rate dv/dt, di/dt increase
- EMI noise increases

Figure 15 shows dependency of switching time to different R_{GATE} values applied:

Figure 14. T_{ON} and T_{OFF} vs R_{GATE} applied on STL15DN4F5 motor load switching

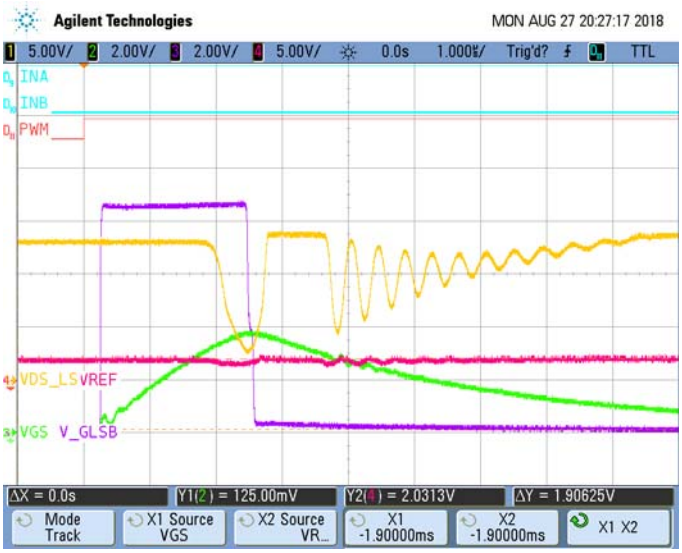


When Adjusting the switching slope through external R_{GATE}, special attention must be paid in order to not activate the $V_{DS\_}$ monitor protection.

The $V_{DS_}$monitoring function senses the low side Power Mos drain-source voltage and compares it with a predetermined threshold. In case of fault condition the low-side is automatically turned-off and the fault state is reported by MultiSense pin (VSENSEH).

To avoid unwanted activations during PWM transitions (LS PowerMos gate not fully charged) the $V_{DS_}$monitoring Protection is activated after a blanking time ($T_{DEL\_OVL\_LSD}$ typ 2.2 µs). If the R_{GATE} value exceeds certain levels, the external MOSFET will be not fully turned on within V_{DS} Monitor blanking time ($T_{DEL\_OVL\_LSD}$). In this case V_{DS} diagnostic applies Overload Error Detection, deactivating the output and setting the fault condition.

Figure 15. Example with V_{DS} diagnostic intervention before output activated (due to high R_{GATE} value)



General assumptions for gate resistor dimensioning:

A gate resistor must be chosen with respect to optimize switching in order to lower losses, parasitic MOSFET drain-source output oscillation and limiting EMI through V_{DS} slope variation and ringing.

Higher load current as well higher switching frequency imply to use lower gate resistance providing faster switching transients (vice versa small loads may apply higher gate resistances).

The minimum value of gate resistance might be selected in range indicated in the MOSFET datasheet. Since R_{GATE} leads to increase switching losses, the minimum R_{GATE} tends to be applied, the drawback is the possible increase of voltage ringing on drain-source during fast switching. Ringing might lead to difficulties maintain required electromagnetic interferences specifications. Due to this fact, the usual external gate resistance can be assumed roughly 2 or 3 times higher compared to minimum one. Such value could be used as starting point for most of the brush motor applications. The way to ensure a proper R_{GATE} value is to test and measure the final application.

5 Protection against Output short to battery

VNHD7008AY and VNHD7012AY integrate advanced functions for short circuit protection able to preserve the embedded high side power stage, the external MOSFETs and the connected load.

In case of short circuit of Output vs GND the protection strategy is identical to the one described in the document AN5026 “VIPower M0-7 H-bridges”.

Short circuit between outputs and battery is detected by the “V_{DS}_MONITORING” feature. In this case the voltage between drain and source of the Low Side PowerMOS (V_{DS}) increases: the current flowing is limited by $R_{DS(on)}$ and the short circuit impedance.

The Drain-Source voltage of external MOSFET is steadily compared to the voltage threshold specified by the VREF_OVL_LSx Pin. If V_{DS} voltage exceeds the reference level, the low-side MOSFET is automatically deactivated. In order to guarantee the low-side MOSFET is fully activated the V_{DS}_MONITORING protection is activated after a blanking time $T_{DEL\_OVL\_LSD}$ (typical 2.2 µs).

The V_{DS} threshold of intervention can be set in a range between 0.4 V and 2 V (indicated in the datasheet with VREF_OVL_LSD_MIN and VREF_OVL_LSD_MAX respectively).

The level of reference voltage for overload detection is programmable by external resistor connected to VREF_OVL_LSx pin, supplied by internal reference current $I_{REF\_OVL\_LSD}$ = 50 µA (typ.). For each low-side MOSFET, separate reference is applied.

The resistor has to be selected so that the VDS threshold for the short to battery protection lies in between VREF_OVL_LSD_MIN and VREF_OVL_LSD_MAX (given in the datasheet). Resistor values out of this range are not granted.

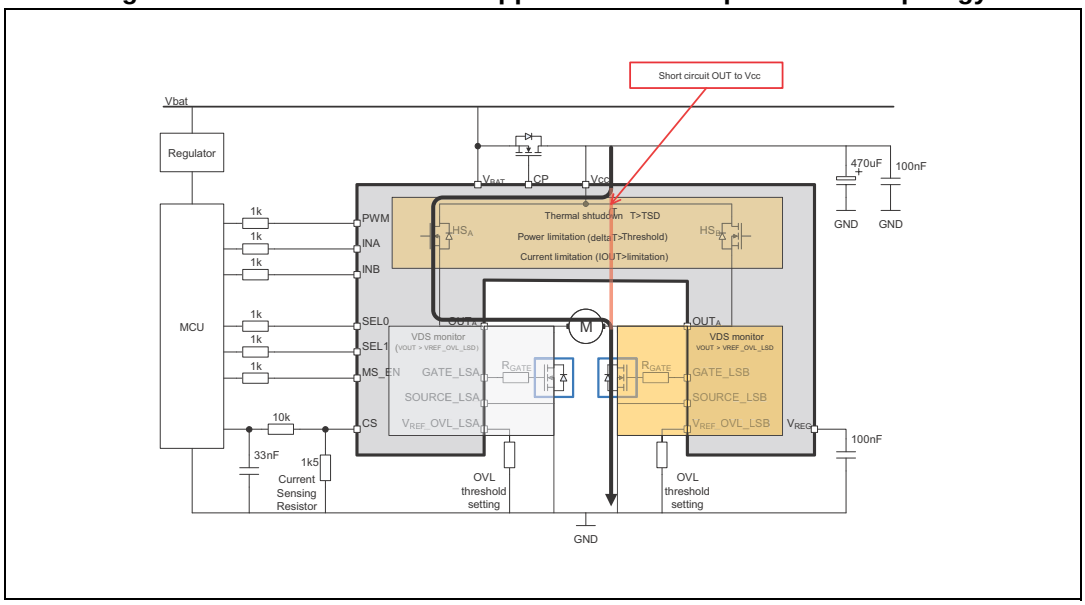
Equation 12:

$$V_{REF\ OVL\ LSx} = R_{REF} * I_{REF\ OVL\ LSD}$$

Where X = A, B

The fault is indicated by the MultiSense pin (when Multisense mux is set to low-side activated output), internally switched to voltage source level VsenseH (applied by the off - state diagnostic, where open-load threshold voltage is exceeded due to short to Vcc).

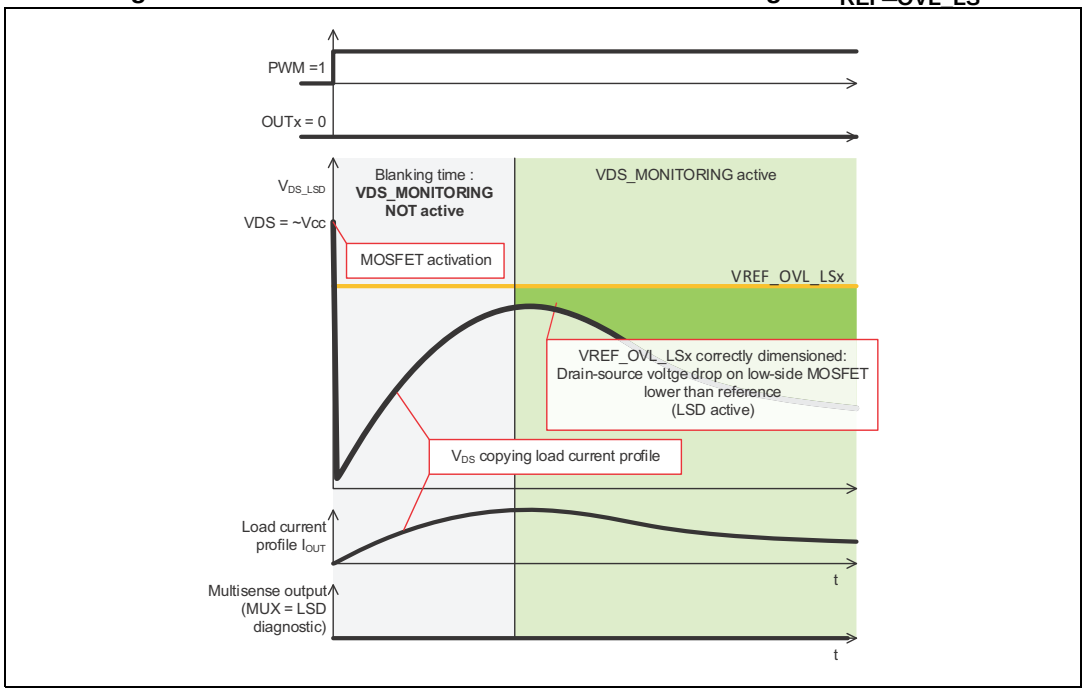
Figure 16. Short circuit to Vcc applied on OUTB - protections topology



Following images depict two cases of $V_{REF\_OVL\_LSx}$ configurations:

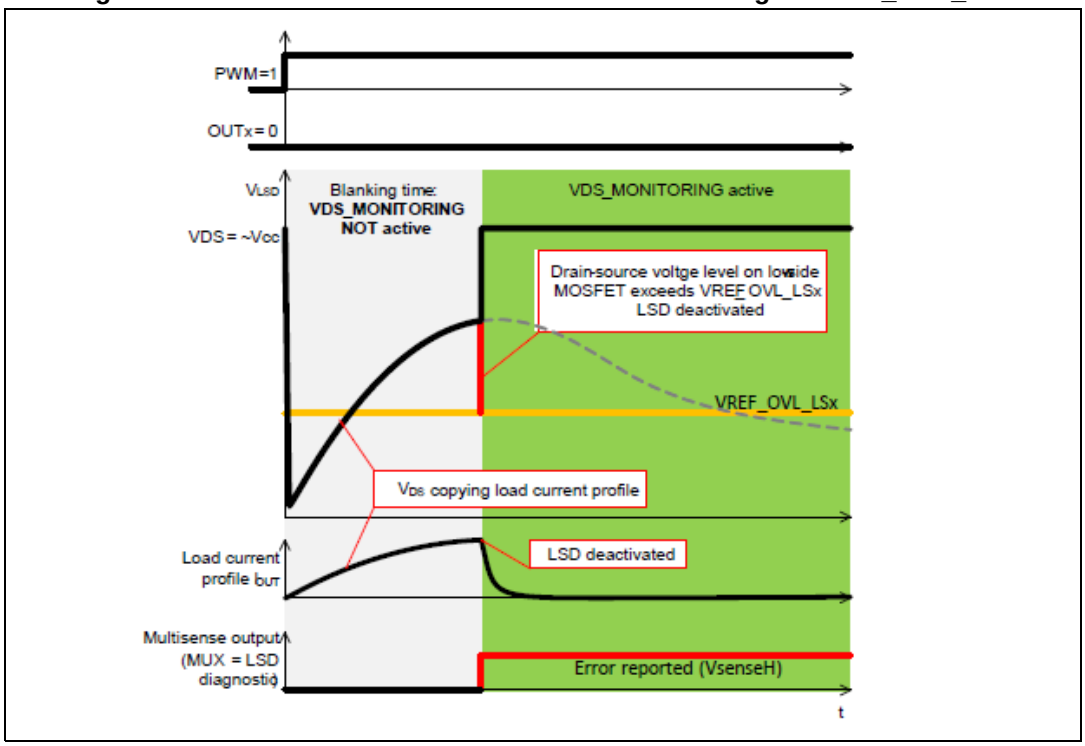
- The first case shows the low-side activation, with no protection activation. Drain-source voltage on low-side MOSFET doesn't exceed the reference voltage $V_{REF\_OVL\_LSx}$ dedicated to driven low-side output.

Figure 17. Low-side activation - correct dimensioning of $V_{REF\_OVL\_LS}$



- The Second case shows the attempt to low-side activation, where protection on external MOSFET is activated. Drain-source voltage on low-side exceeds the reference voltage, which triggers protection after blanking time expiration and consequently external MOSFET is deactivated (fault reported through the MultiSense).

Figure 18. Low-side activation - incorrect dimensioning of VREF_OVL_LSx



It is mandatory to correctly set overload threshold, in order to prevent false error triggering during the normal activation of the load.

Following steps should be applied:

- Characterize controlled load profile current (inrush current, stall current level, IMAX)
- Calculate maximum voltage drop on used low-side MOSFET during active state (considering its $R_{DS(on)}$) which can typically increase up to two times at maximal junction temperatures

Equation 13:

$$V_{DS\,MAX} = I_{MAX} * R_{ON}(@high\ temperature)$$

- Out of the voltage drop on the MOSFET, the minimum reference voltage for short circuit detection has to be calculated (by applying the minimum reference current IREF_OVL_LSD given in the datasheet)

Equation 14:

$$V_{REF\ OVL\ LSD} > V_{DS\ MAX}$$

Equation 15:

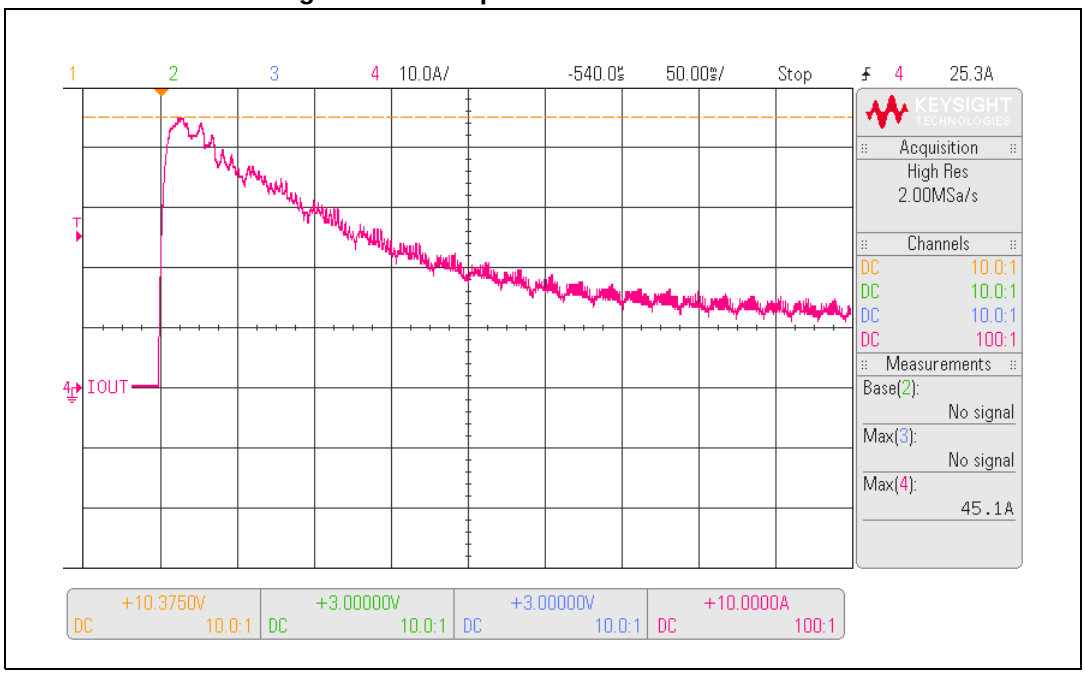
$$R_{REF\ OVL\ LSD} > \frac{V_{REF\ OVL\ LSD}}{I_{REF\ OVL\ LSD\ (MIN)}}$$

The calculated resistance should preserve correct operation (when IOUT doesn't exceed its maximum threshold given by load characterization). Verification by measurement in real application should be applied, to confirm standard use-case limits.

Example 1- calculation of $R_{REF\_OVL\_LSD}$ for motor load:

- Step 1 - I_{OUT} load profile characterization (motor activation)

Figure 19. Example – motor inrush current



- Step 2 - Maximum drain-source voltage during IMAX
- RON_MAX specification

Selecting the MOSFET - STL76DN4LF7AG is selected as Low side, the RON@25oC = 6 mOhm.

Considering that at high temperature RON maximum is typically doubled, RON_MAX@175°C = 12 mOhm

The maximum voltage drop over the fully activated low-side MOSFET is

Equation 16:

$$V_{DS\ MAX} = I_{MAX} * R_{ON}(@high\ temperature) = 45A * 12\ mOhm = 540mV$$

- Step 3 - $R_{REF\_OVL\_LSD}$ calculation

Using IREF_OVL_LSD_MIN = 40 µA, calculated RREF_OVL_LSD is

Equation 17:

$$R_{REF\_OVL\_LSD} > \frac{R_{REF\_OVL\_LSD}}{I_{REF\_OVL\_LSD\_MIN}} = \frac{540mV}{40\mu A} = 13.3kOhm$$

There is used the $R_{REF\_OVL\_LSD}$ = 14 kOhm.

The resistance should be in the allowed range of 8 KOhm to 40 KOhm corresponding to $V_{REF\_OVL\_LSD\_MIN}$ and $V_{REF\_OVL\_LSD\_MAX}$ window

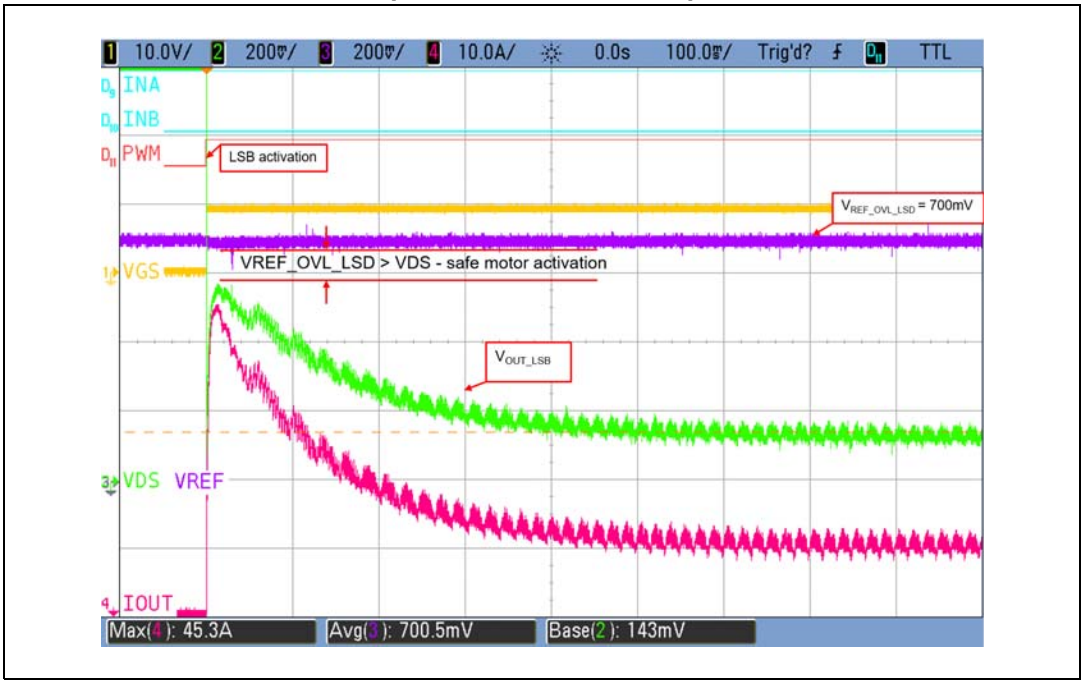
- Step4 - verification by real test

Activation process with correctly dimensioned $R_{REF\_OVL\_LSD}$ is shown on following figure:

Equation 18:

$$V_{REF\_OVL\_LSD} = I_{REF\_OVL\_LSD\_TYP} \cdot R_{REF\_OVL\_LSD} = 50\mu A \cdot 14k = 700mV$$

Figure 20. Load activation with correct VREF_OVL_LSD dimensioning (RREF_OVL_LSD = 14 k)

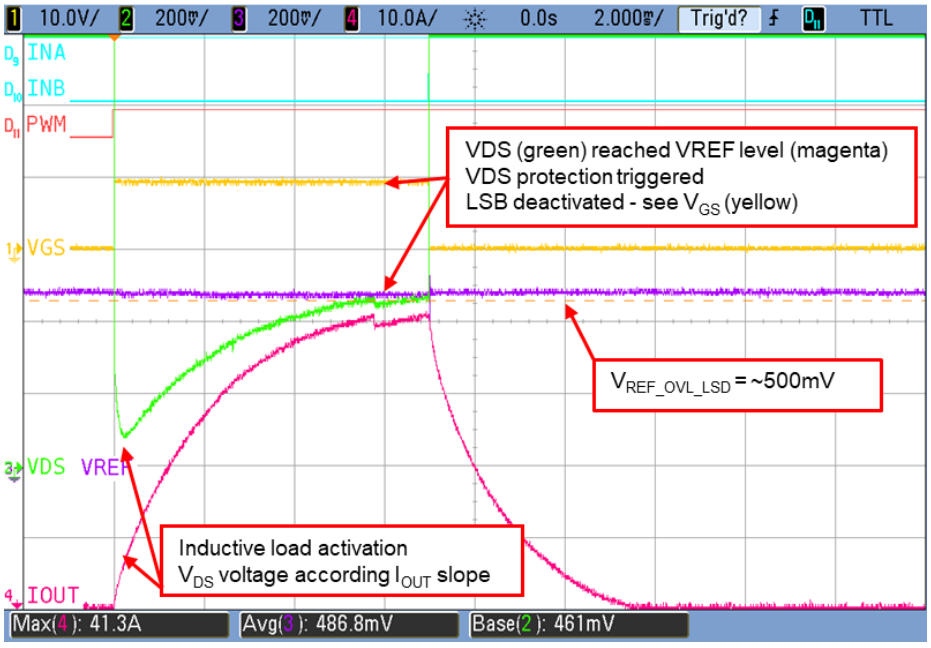


Example 2 - applied too low $R_{REF\_OVL\_LSD}$

The following example depicts an improper selection (too low) $R_{REF\_OVL\_LSD}$ = 10 kΩ, implying $V_{REF\_OVL\_LS}$ ~ 500 mV.

During load activation, V_{DS_ON} low-side exceeds after certain time (on depicted example it is ~7 ms after low-side activation) the error detection threshold, the low-side MOSFET since (LSB) (green slope on figure) is deactivated. This means that motor cannot be properly started.

Figure 21. Load activation with too low $V_{REF\_OVL\_LSD}$ ($R_{REF\_OVL\_LSD}$ = 10 k)



Example 3 - too high $R_{REF\_OVL\_LSD}$

Applying too high value of $R_{REF\_OVL\_LSD}$ leads to impossibility trigger V_{DS} protection during failure.

Following example describes possible effect:

Resistive **short circuit to Vcc** happen on activated low side MOSFET STL52DN4LF7AG.

Assuming a resistive short circuit R_{SHORT} ~ 150 mOhm (assumption confirmed by the example below) between MOSFET drain and Vcc, current flowing through MOSFET can be calculated as follows:

Equation 19:

$$I = \frac{V_{CC}}{R_{SHORT} + R_{DS\_ON}}$$

Applying

- Vcc = 13 V
- MOSFET $R_{DS(on)}$ at high temperature (175 °C) ~ 12 mOhm

Equation 20:

$$I = \frac{13}{0.15 + 0.012} = 80A$$

Maximum drain source voltage across MOSFET is in equation below.

Equation 21:

$$V_{DS\_MAX} = I \cdot R_{DS\_ON@175°C} = 80 \cdot 0.012 = 960mV$$

If reference $V_{REF\_OVL\_LSD}$ is applied higher than V_{DS_MAX}, the V_{DS} protection is not activated during assumed short circuit. A wrong $R_{REF\_OVL\_LSD}$ value corresponding to $V_{REF\_OVL\_LSD}$ level is: µ

Equation 22:

$$R_{REF\_OVL\_LSD} > \frac{V_{DS\_MAX}}{I_{REF\_OVL\_LSD\_MAX}} = \frac{0.96V}{60\mu A} = 16kOhm$$

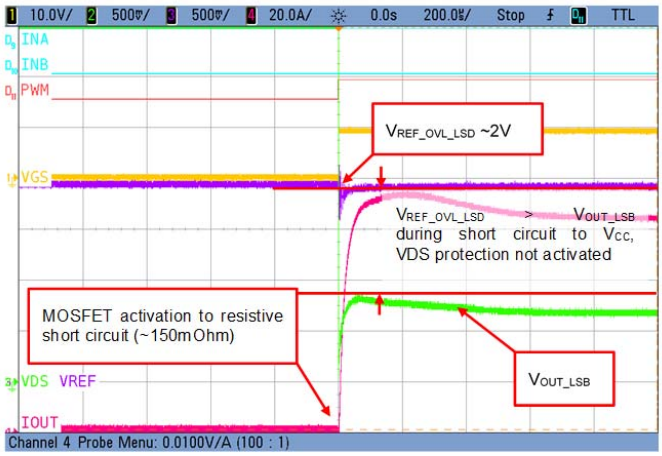
Since the protection will never be activated, current flowing continuously during short circuit cause power dissipation on the MOSFET.

Equation 23:

$$P_{DISSIPATED} = R_{DS\_ON@175°C} \cdot I^2 = 0.012 \cdot 80^2 = 77W$$

Total power dissipation exceeds maximum MOSFET ratings and consequently MOSFET is damaged due to over-temperature. (The current keeps on flowing in the Power MOSFET even if PWM is deactivated).

Figure 22. Experimental measurement result with resistive short circuit ~150 mΩ



Consequently MOSFET got damaged by over-temperature I_{OUT} still flows even PWM already deactivated (V_{GS} = 0 V), until MOSFET burned.

6 Protection against reverse battery with the embedded CP

The embedded charge pump circuit of VNHD7xxAY devices is designed to protect the device against reverse battery condition. The CP Pin is intended to drive the gate of an external N channel Power MOSFET connected as shown in the typical application circuit (please refer to *Figure 1: VNHD7008AY and VNHD7012AY functional block diagram of and typical application schematic.*).

Normal operative conditions: VBATT voltage is higher than GND voltage. The Charge pump is turned on as soon as the device goes out form Stand-by mode, setting one the input High (toggle INA or INB or SEL0 or SEL1 or Multisense_EN from 0 to 1). The embedded CP block will provide a voltage VCP-VBATT able to turn on the external Power MOS. So that the Pin VCC (the internal power supply of the device) will be polarized at VBATT.

Reverse battery condition: VBATT voltage is lower than GND voltage. In this case the voltage VCP-VBATT is less than PowerMOS gate threshold and the external PowerMOS is turned off. The reverse current is blocked by the body diode.

Basing on above consideration the external N-channel Power MOSFET used for the reverse battery protection should have the following characteristics:

- B_{VDSS} > 20 V (for a reverse battery of -16 V)
- $R_{DS(on)}$ < 1/3 of H-bridge total $R_{DS(on)}$
- Standard Level Gate Driving

The N-channel Power MOSFET $R_{DS(on)}$ must be dimensioned in order to handle the whole load current so that power dissipation is kept low enough to keep the junction temperature below the rated maximum (150 °C).

Equation 24:

$$\Delta Tj = T_{JNMOS\_max} - T_{amb\_max}$$

Equation 25:

$$\Delta Tj = P_{max} * R_{thJ\text{-}A,n\ ch} = (R_{DS(on)} * I^2 motor\_RMS\_max) * RThj\text{-}A,\ n\ ch$$

So, fixing the package and the related PCB, the Power MOSFET thermal resistance junction-to-ambient Rthj-A can be considered as fixed.

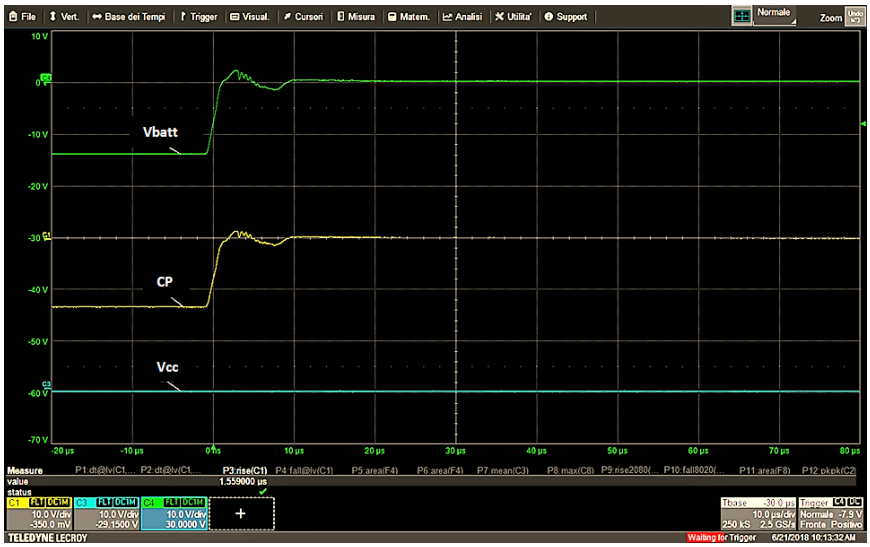
Then the $R_{DS(on)}$ can be chosen accordingly to the following equation:

Equation 26:

$$R_{DSon} = \left(\frac{T_{NMOS-max} - T_{amb-max(A,NMos)}}{I^2_{motor\_RMS\_max} \times R_{Thj-(A,NMOS)}} \right)$$

The Gate capacitance of the N-channel MOSFET also determines the turn-on and turn-off time when exposed to fast negative transients or abrupt reverse polarity according to LV 124: 2013-06 standard.

Figure 23. Vbatt transition from 0 to -14 V



The protection works also in case of dynamic reverse battery based on LV124 Normative (E15 test case 2).

During this test the device is switched ON with a resistive load (while Vbatt = 10.8 V), then the voltage goes negative (Vbatt = -4 V) for 60 sec.

The test result is shown in *Figure 24: Dynamic reverse polarity* where Icc represents the current flowing through Vcc device pin.

Figure 24. Dynamic reverse polarity

If the embedded CP is not used for reverse battery protection we recommend to short VBAT pin to V_{CC}.

7 Rejection of Electro Magnetic Interference

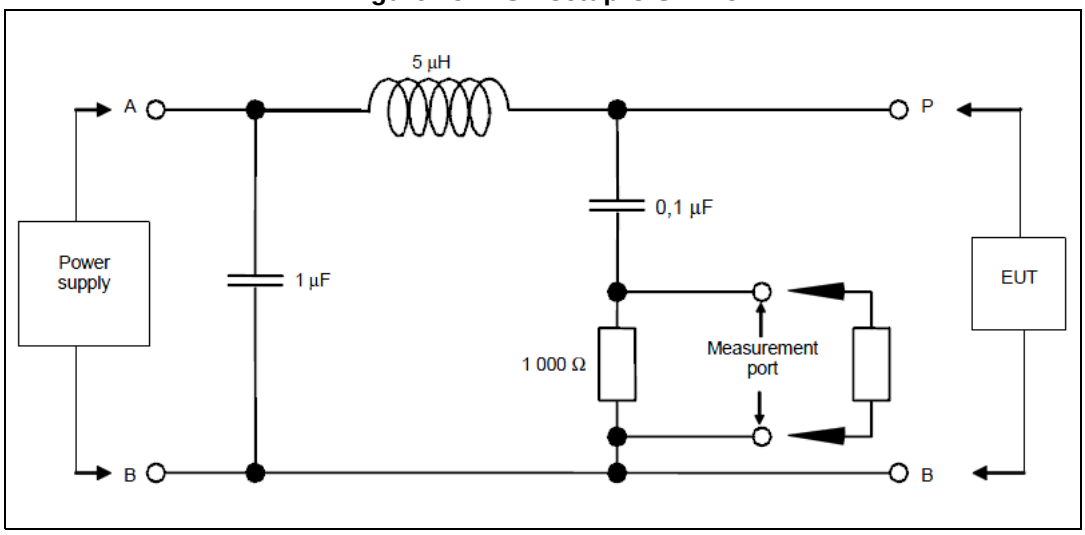
A device or system generates noise which is injected into connection lines or radiated, potentially affecting the performance of other devices or systems connected to the same lines and placed close to it.

To limit the effect of this noise, its amplitude must be lower than EMC limits contained in specific technical reference documentation.

- Standard reference CISPR25 (conducted emissions on Vbatt, radiated emissions at system level)
- Standard reference IEC 61967/4 (conducted emissions on Outputs using 1 Ω/150 Ω method)
- Standard reference IEC 61967/2 (radiated emissions using TEM-Cell method and wideband TEM-cell method -150 KHz to 8 GHz)

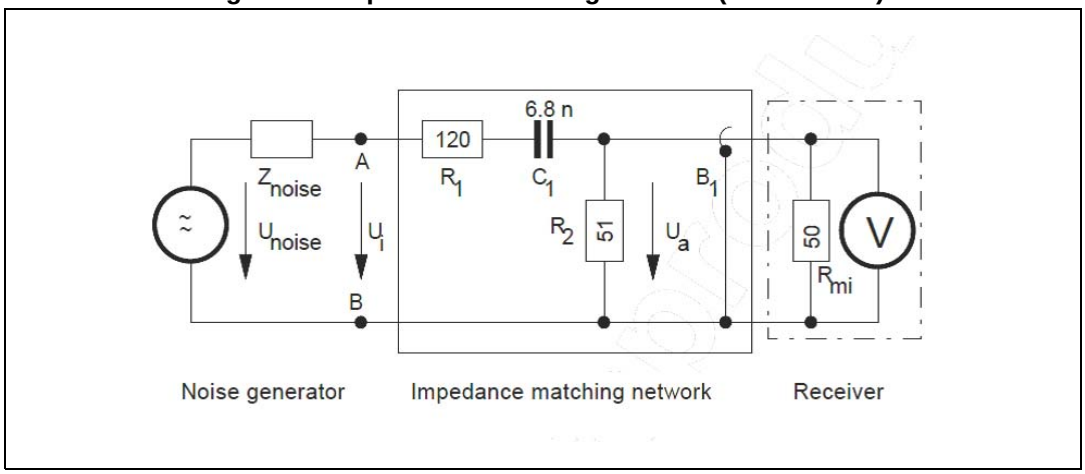
For conducted emissions on Vbatt, a specific artificial network (AN) called line impedance stabilizing network (LISN), is used to couple the measurement instrument (spectrum analyzer).

Figure 25. LISN setup-CISPR25



For conducted emissions on system outputs (e.g., V_{CC} line or VNH7XX outputs), the 150 Ω measurement method (IEC 61967/4) is commonly used. To perform measurements, the impedance matching network figured below is required.

Figure 26. Impedance matching network (IEC 61000-4)



One or multiple configurations can be chosen for input signals, PWM frequency, duty cycle percentage and output loads. The final configuration is usually the one closer to the common operating condition of the DUT. The type (shielded or unshielded) and length of wire may affect performance of the DUT either with respect to the CISPR25/IEC 61967/4 standard (conducted emissions) or the IEC 61967/2 standard (radiated emissions).

7.1 Pi-filter dimensioning

Conducted emission measurements may reveal levels of RF noise injected into the battery line above the required limits. The best solution in this case is to add a Pi filter in series with the dedicated battery line.

$C1_{(Vcc)}$ can be considered as part of the normally used Pi filter and its capacitance is calculated with formulas explained in previous chapters.

The resonance frequency of the $L_{(Vcc)}$ and $C_{(Vbatt)}$ filter is:

Equation 27:

$$f_r = \frac{1}{2 \cdot \Pi \cdot \sqrt{L_{(Vcc)} \cdot C_{(Vbatt)}}}$$

The equation for the $L_{(Vcc)}$, $C_{(Vbatt)}$ filter transfer function V_{out}/V_{in}:

Equation 28:

$$\frac{V_{out}}{V_{in}} = \frac{\frac{1}{J\omega C(V_{batt})}}{J\omega L_{(Vcc)} + \frac{1}{J\omega C_{(Vbatt)}}}$$

Where V_{IN} is the device $V_{CC,}$ while V_{out} is the V_{batt} as the filter is intended to cut the noise generated by the H-bridge while operating in PWM. Artificial network (LISN to couple spectrum analyzer with DUT) impedance and internal resistance of Vbatt are considered negligible.

According to transfer function given above, $L_{(Vcc)}$ $C_{(Vbatt)}$ filter attenuation in dB can be expressed as follows:

Equation 29:

$$Att._{dB} = 20 * log\left|\frac{Vout}{Vin}\right| = 20 * log\left|\frac{\frac{1}{j\omega C(Vbatt)}}{j\omega L(Vcc) + \frac{1}{j\omega C(Vbatt)}}\right|$$
$$= 20 * log\left|\frac{1}{1 - 4 * \pi^2 * f^2 * L(Vcc) * C(Vbatt)}\right|$$
$$\cong 20 * log\left|\frac{1}{4 * \pi^2 * f^2 * L(Vcc) * C(Vbatt)}\right|$$

Where, considering frequencies whose attenuation values, in absolute value, are generally higher or equal to 40dB, we can suppose:

Equation 30:

$$1 \ll 4 * \pi 2 * f 2 * (Vcc) * (Vbatt)$$

Selection criteria for the input power inductor $L_{(Vcc)}$ include inductance value, rated current, series resistance, power rating (internal temperature rise) and size.

The power dissipated inside the inductor depends on the typical DC resistance RDCR and worst case input RMS current.

Equation 31:

(Vcc) = RDCR * (Vcc)2

Taking the criteria into account, $L_{(Vcc)}$ is generally in the range of 1 µH to 30 µH.

Particular attention has to be paid to maximum current which the inductor can handle without changing its properties. In-fact, if the current is too close to saturation limit reported in the datasheet, filtering capability of the component may result compromised. It is good practice to choose inductors being sure that current will pass through them is about 20~40% of their saturation current.

According to general conducted EMC rules or specific customer requirements, minimum noise attenuation in dB can be chosen at a given frequency (generally the lower value in the measurement frequency range).

Starting from the selected $L_{(Vcc)}$ value and required noise attenuation level, we can express $C_{(Vbatt)}$ as:

Equation 32:

$$C_{(Vbatt)} = \frac{1}{L_{(Vcc)}} \bullet \left(\frac{10 = \frac{A_{tt-dtt}}{40}}{2 \cdot \Pi \cdot f} \right)^2 = \frac{1}{L_{(Vcc)}} \bullet \left(\frac{10 = \frac{A_{tt-dtt}}{40}}{2 \cdot \Pi \cdot f} \right)$$

The real attenuation of the PI filter made of the $L_{(Vcc)}$ and $C_{(Vbatt)}$ components just dimensioned is actually lower than the value calculated in *Equation 29*. This is mainly due to the equivalent series resistance (ESR) of $C_{(Vbatt)}$, called ESR.

To determine the attenuation of the real filter, given that

Equation 33:

$1 \ll 4 * \pi 2 * f 2 * (Vcc) * (Vbatt)$

we use the formula:

Equation 34:

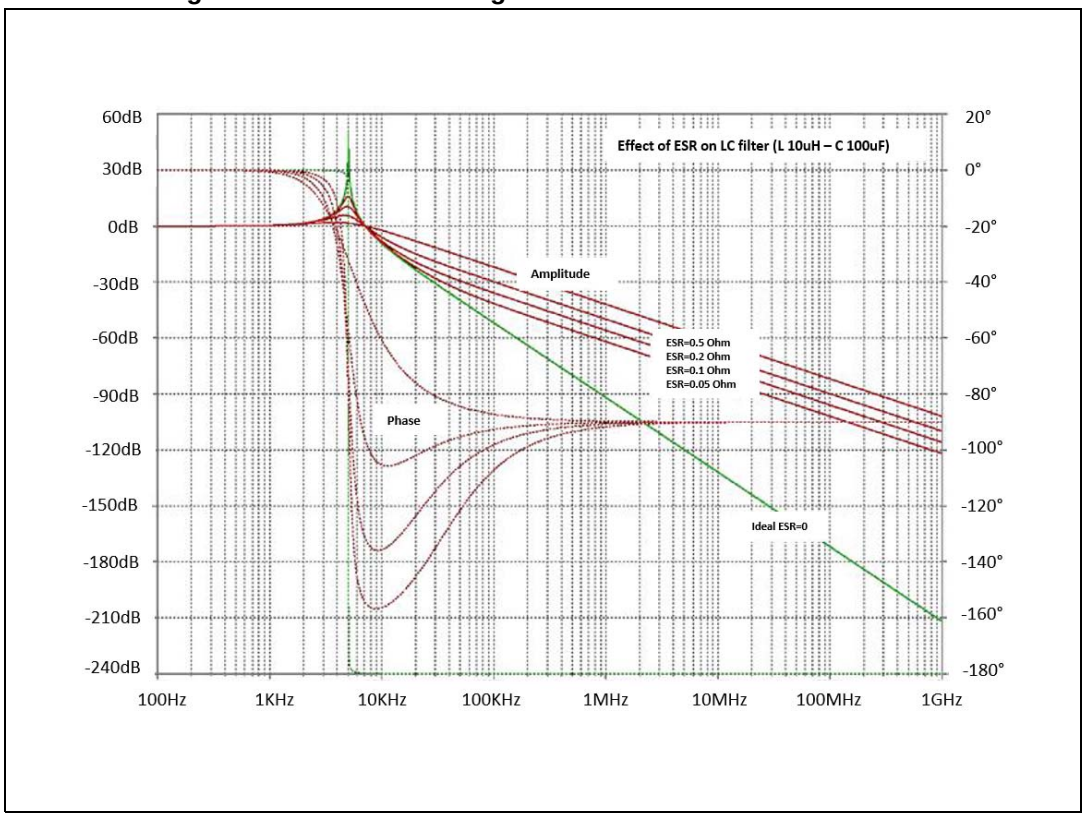
$$Att_{dB} = 20 \cdot log \sqrt{\frac{1}{1 + w^2 \cdot L \cdot C \cdot \frac{w^2 \cdot L \cdot C - 2}{1 + w^2 \cdot ESR^2 \cdot C^2}}}$$

Where

- $\omega = 2*\Pi*f$
- $L = L_{(Vcc)}$
- $C = C_{(Vbatt)}$
- $ESR = ESRC_{(Vbatt)}$

The figure below illustrates the effect of rising ESR and compares the ideal and real cases for a filter where $L_{(Vcc)}$ = 10 µH and $C_{(Vbatt)}$ = 100 µF. The ESR acts as a damping resistor which partially compensates the resonance effect.

Figure 27. Attenuation diagram of Pi-filter with different ESR



Below we can see an example regarding the benefit we can obtain introducing PI filter on the Vbatt line. Without a filter the CISPR25 spectrum (compared to customer limits TL965EN VW) is above class4 limit mask in almost all frequency ranges; by adding a PI filter, dimensioned as written in *Equation 32*, emissions on battery line decrease significantly. The filter is dimensioned considering that a real attenuation of -50dB minimum at 150 kHz frequency is required, bearing in mind that the theoretical and real attenuation are different because of the ESR.

A simplified schematic and component values are shown in *Figure 31: Conducted emission spectra according CISPR25 with and without C(OUT)*.

By setting for example L(Vcc) = 6 µH inductance and taking into account *Equation 29* where we considered the theoretical Attenuation of -70 dB, we calculated a capacitance value of 593 µF for C(Vbat) capacitor. Using a commercial capacitor with a capacitance of 470 µF, we obtain through *Equation 34* about -68 dB attenuation instead of -70 dB theoretical.

Figure 28. Simplified schematic and component values

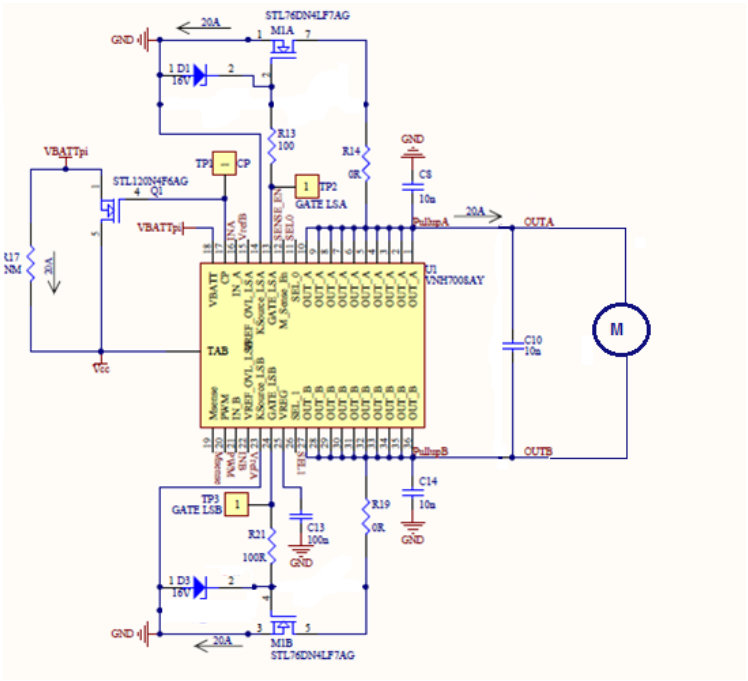
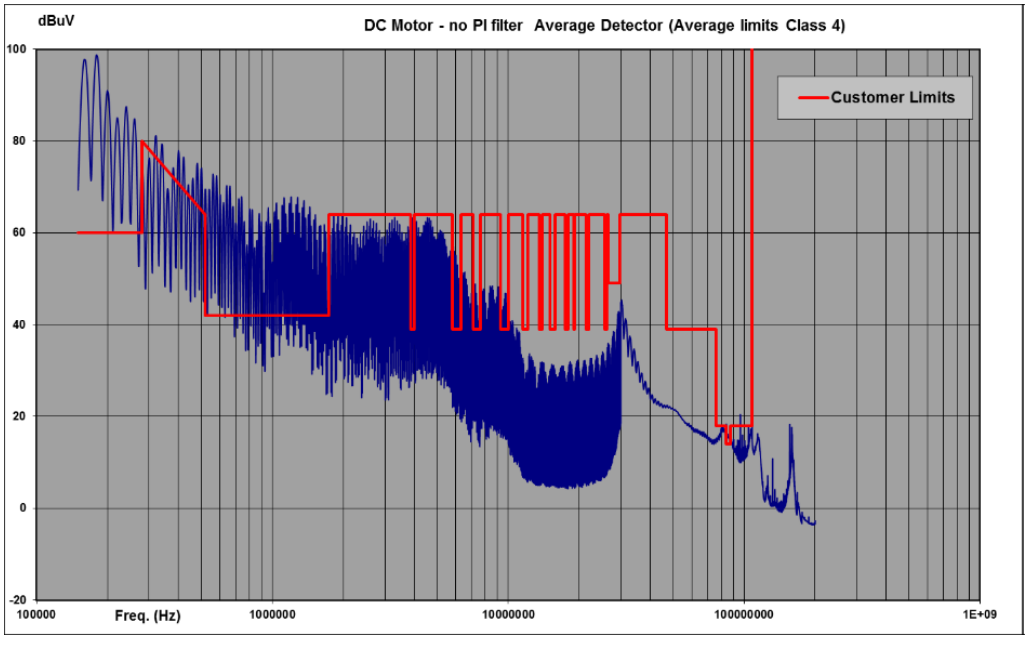


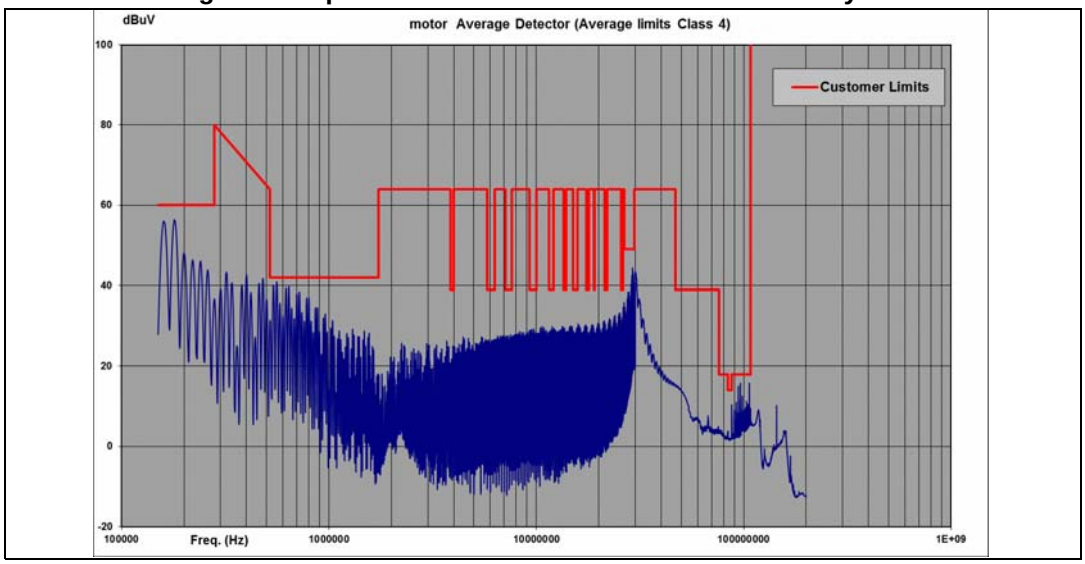
Figure 29. Spectrum measured without PI filter on battery line



The above figure shows the spectrum measured without putting the filter on battery line, while the figure below shows the spectrum with a PI filter on the battery line.

We can see emissions are about 50 dB lower at low frequency range. This allows the spectrum to be below the class4 limit mask.

Figure 30. Spectrum measured with PI filter on battery line



As shown in the two figures, the real attenuation as the absolute value, is 20 dB lower than the theoretical one due to ESR of C(Vbat), about 50 mΩ in this case.

In case the real filter does not fulfill the attenuation specification, we can dimension the filter by assigning a higher theoretical attenuation in **Equation 6**, in order to compensate the ESR value and repeating the verification through **Equation 7.**

7.2 Capacitors on Outputs (C(OUT)) and on Vcc (C2(Vcc))

Ceramic capacitors on the outputs help to improve application EMI and ESD performance. Their values depend on the PWM frequency, on the inductive energy in place and on the motor wires.

During motor control in PWM, EM disturbance is injected into the VNHD7xxAY output pins either due to the antenna effect in car wiring or due to motor brushes. Capacitors on outputs create a path to GND for those disturbances, thus avoiding their return to Vbatt.

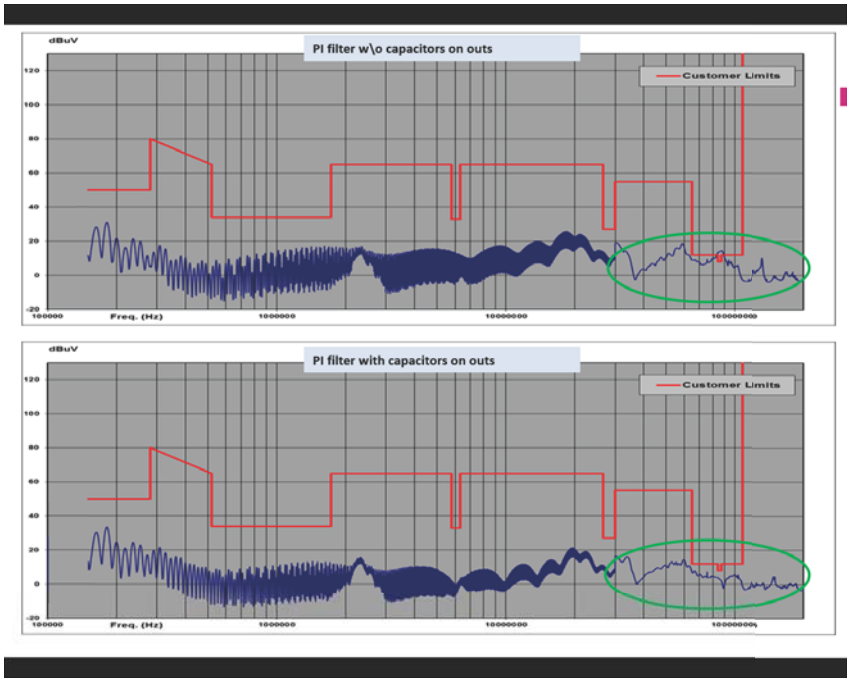
They also smooth falling and rising edges of output waveforms, which benefits emissions at high frequencies (reducing emissions conducted on batt).

Capacitor values between 47 nF and 100 nF are recommended: values below this have little effect and values above don’t provide any further benefits and may negatively affect output waveforms and increase switching losses.

C2(Vcc) values between 47 nF and 100 nF are also recommended for similar reasons.

The following spectra with and without C(OUT) highlights the beneficial effect of the output capacitor at high frequencies.

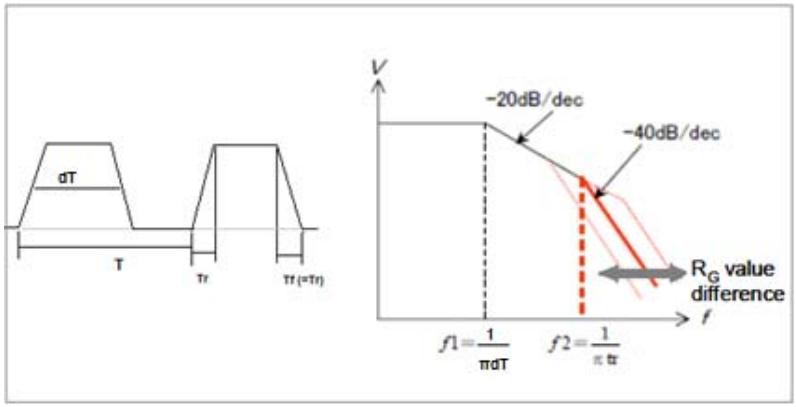
Figure 31. Conducted emission spectra according CISPR25 with and without C(OUT)



7.3 Gate resistor on low side MOS transistors

A repetitive square wave of period T, having a symmetric rise and fall time can be represented by a series of sine waves. The amplitudes of the harmonics, determined in a Fourier analysis, are contained under a logarithmic envelope with two slopes. These slopes intersect at frequencies that are called corner frequencies. The first or lower corner frequency is at f =1/(πdT), where T is the time between zero crossings and d is duty cycle. The amplitude of the harmonics above this frequency decreases of 20 dB per frequency decade. The second or upper corner frequency is at f=1/πTr where Tr is the rise time, for sake of simplicity we assume that Tr =Tf (where Tf is the fall time). Above this upper corner frequency the harmonic amplitudes fall off at 40 dB per decade (please see *Figure 32: waveform and spectrum of a trapezoidal signal*.)

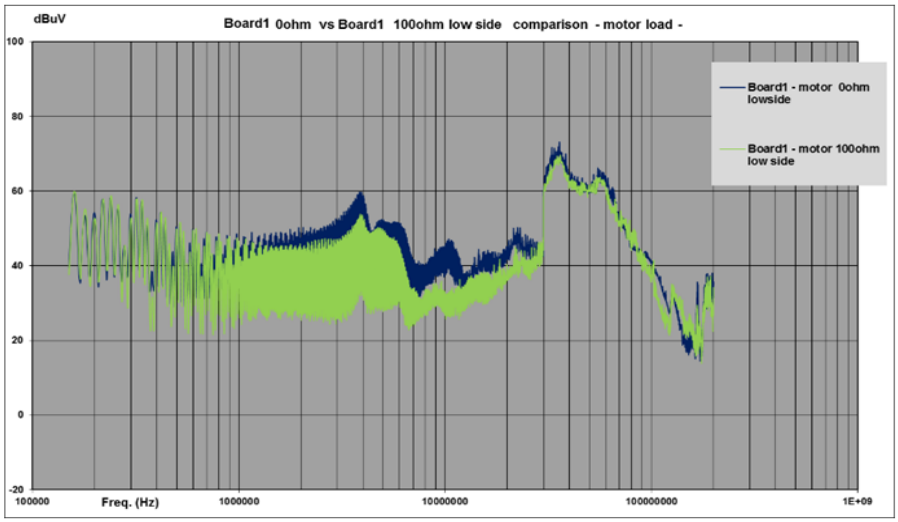
Figure 32. waveform and spectrum of a trapezoidal signal



Considering a PWM signal driving VNHD7xxAY device, being there the option of setting Rg value (gate resistor of LSD external mos transistors), there is the opportunity to improve conducted emission spectrum. According to theory reported above, the higher is R gate, the lower is the frequency at which it is possible to notice benefits due to its introduction. Rg value, however, cannot be too high because this could cause too big switching power loss (with a decreased efficiency and too high heat dissipation). A reasonable gate resistance value could be equal or less than 100 Ω.

In *Figure 36*, a spectrum comparison between a VNHD7008AY board with 0 ohm Rg on both external LSD mos and a VNHD7008 board with 100ohm Rg is shown. It is possible to see emission improvement starting from relatively low frequencies: 1 MHz~2MHz. Measurements are referred to CISPR25 standard and to 20KHz, 80% duty cycle PWM driving signal.

Figure 33. comparison of two spectra with 0 Ohm and 100 Ohm PowerMOS gate resistances



At high frequencies benefits of R_{GATE} are partially attenuated by other phenomena (switching ringing, etc.).

7.4 Ferrite beads for high frequency noise reduction

In the *Chapter 7.1: Pi-filter dimensioning* has been written about LC filter on battery line; starting from some tenths of megahertz this filter begins to lose its filtering capability, mainly due to parasitic capacitance of series inductor. So, generally, this filter is not able to completely reduce high frequency emissions.

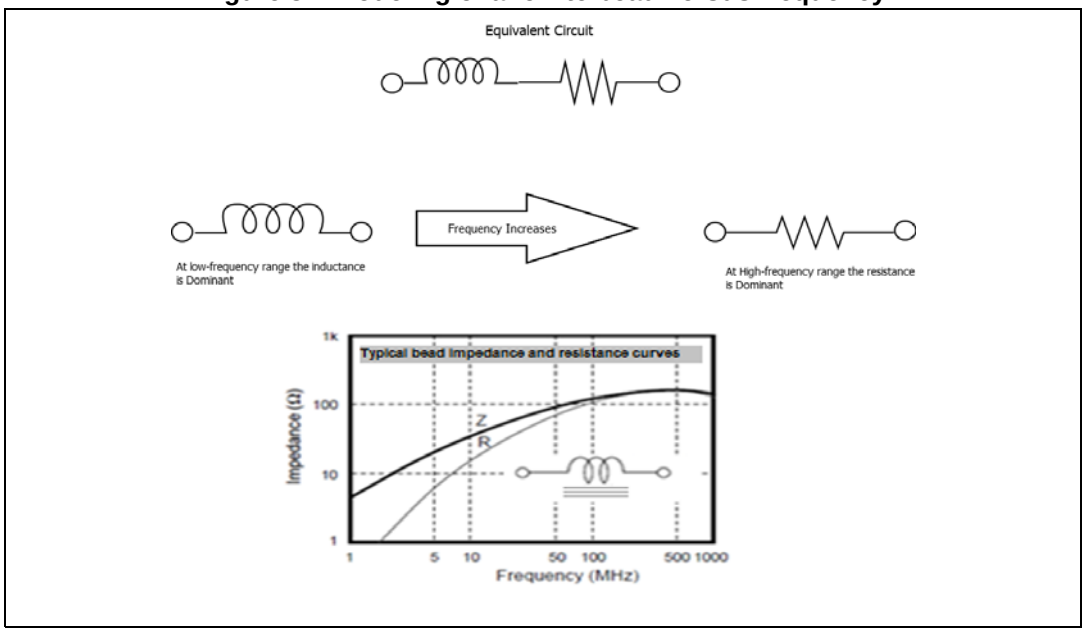
In previous chapters was explained how to select capacitors between outputs and GND to reduce unwanted high frequency noise.

However some series components in battery line, which offer high impedance in the frequency range 30 MHz – 200 MHz, could give extra improvement in EMC performances.

Ferrite beads are suitable for this purpose in fact they are engineered to attenuate higher frequencies, dissipating energy as heat by design, this should be considered in order to choose the right part.

To summarize ferrite bead behavior it is possible to tell at high frequencies they work like resistors instead of inductors.

Figure 34. Modeling of a ferrite bead versus frequency



Due to parasitic capacitive effect, power inductor impedance decreases quickly at high frequencies; this causes PI filter loses its filtering capabilities. Due to its capability to dissipate energy per Joule effect, ferrite beads save their impedance/resistance also at high frequencies.

In order to choose the best part, it is necessary to consider three major parameters:

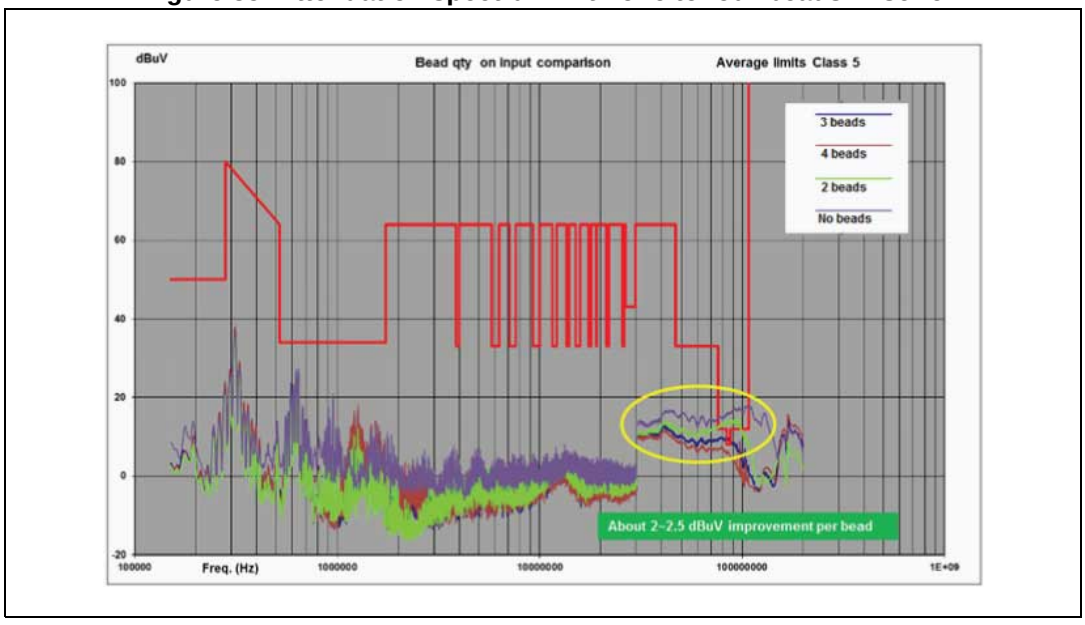
1. **frequency band** where is the highest noise: observing the spectrum of emissions on battery line it is easy to find the frequency band where is the noise to be reduced; generally standard or OEM requirements are critical in frequency range around FM radio band so in most cases a center frequency of 100 MHz is chosen. This

corresponds to the frequency generally reported by ferrite beads manufacturer as the one for which are listed data sheet parameters (especially resistive impedance).

2. **maximum current** that flows in the battery line: the choice of the right ferrite bead for power applications requires careful consideration of the impedance characteristics with respect to DC bias current. In most cases, manufacturers only specify the impedance of the bead at 100 MHz and publish data sheets with frequency response curves at zero DC bias current. However, using ferrite beads for power supply filtering, the load current not only is not zero but it is instead quite high; so ferrite beads parameters may change significantly. Increasing current, the core material begins to saturate and the inductance of the ferrite bead decreases up to 90%. For effective power supply noise filtering, a design guideline is to use ferrite beads at about 20% of their rated DC current.
3. **Attenuation needed** in that frequency band. Attenuation needed to move emission spectrum below standard or OEM required limits: it can be known by measuring the distance, expressed in dBµV, between the most critical value in the spectrum and the allowed limit for the same frequency. Once calculated the attenuation, it is possible to choose one appropriate bead by selecting this according R curves in the datasheet. The higher is the equivalent resistance, the higher will be the dissipated energy at the corresponding attenuation high frequency.

Once selected the bead, if it is not possible to find one that gives the desired noise attenuation, it is also possible to connect two or more of them in series. Below a picture where it is possible to see the effect of each bead; up to four beads have been connected.

Figure 35. Attenuation spectrum with one to four beads in serie



For currents larger than 10 Amps ferrite beads in series with battery line could be too expensive and the use of capacitors on the outputs is preferred in order to attenuate high frequency noise.

7.5 PCB layout considerations form EMI optimization

In an H-bridge driver, high current paths and low current paths are all near each other. Alternating current (ac) paths carry spikes and noise, high direct current (dc) produces significant voltage drops and low current paths are sensitive to noise.

Therefore we can group the signals as follows:

- High frequency and high current (i.e., H-bridge outputs OUT A / OUT B)
- Digital at low frequency (Like INA/INB signals)
- Digital at high frequency (like PWM signals)

A PCB floor plan is important to minimize current loop areas and arrange the power components so that the current flows smoothly, avoiding sharp corners and narrow paths. This helps reduce parasitic capacitance and inductance, therefore, eliminating ground bounce.

The best performance in terms of parasitic inductance and EMC can be reached with a 3- or 4-layer PCB with a dedicated GND plane that improves filtering efficiency.

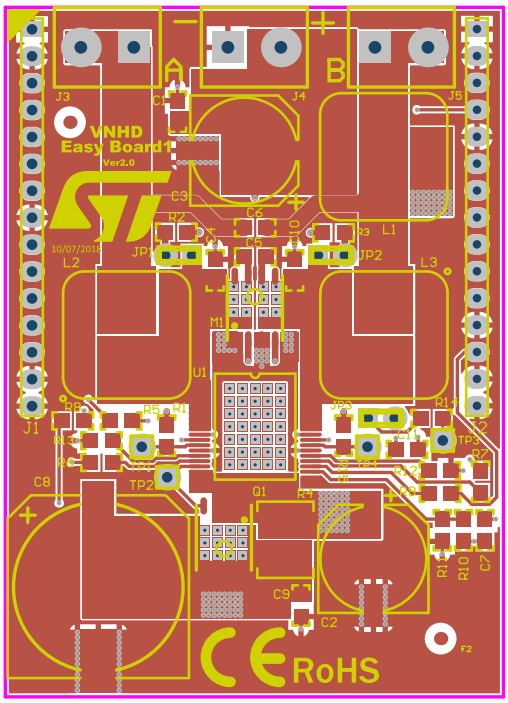
All filtering capacitors, especially those on Device Vbat PIN, must be placed as close as possible to the device terminals to keep the parasitic inductors of the PCB-wires as low as possible.

To keep the RF noise from the DC motor low and reach good immunity from ESD, capacitors on outputs (C9 / C10 / C14 in *Figure 36: PCB top layout with VNHD7008AY with positioning of ESD & filter capacitor*) and on device supply pin (C1 on *Figure 36: PCB top layout with VNHD7008AY with positioning of ESD & filter capacitor* below) must be placed on the board connector and directly soldered to the module GND usually in star connection with all possible ground signals (Digital GND, Analog GND and Power GND).

The best ESD performance can be achieved by putting an ESD filtering component like a transil or ceramic capacitor as close as possible to the connector pin and well-grounded by via to the ground plane.

A multilayer PCB is better than a 2-layer PCB for heat dissipation. For improved thermal and electrical conduction, a 2-ounce-or-higher copper thickness may be used in place of the standard 1 ounce. Several PGND planes connected together with vias also help.

Figure 36. PCB top layout with VNHD7008AY with positioning of ESD & filter capacitor



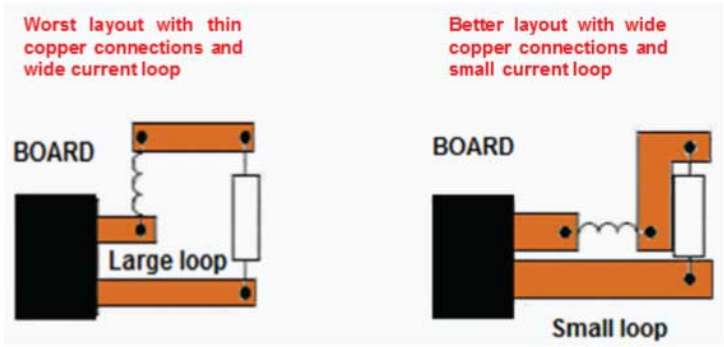
VNHD7008AY Easy board top layer. Optimized symmetrical connections between Drain LS and Source HS (OUTA / OUT B) are visible.

7.6 General considerations about radiated emission reduction

Some basic guidelines for minimizing radiated EMI are reported below:

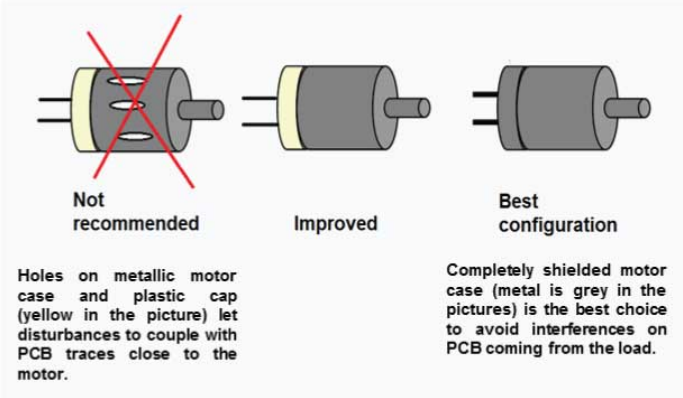
- It is good practice to keep current loops small. The ability of a conductor to couple energy by induction and radiation is lowered with a smaller loop, which acts as an antenna. So, in case of motor load connected to PCB through wires, these have to be twisted and short.
- For pairs of copper printed circuit (PC) board traces, it is useful to design wide (low impedance) traces aligned above and below each other.

Figure 37. Example of pairs of copper printed circuit (PC) board traces



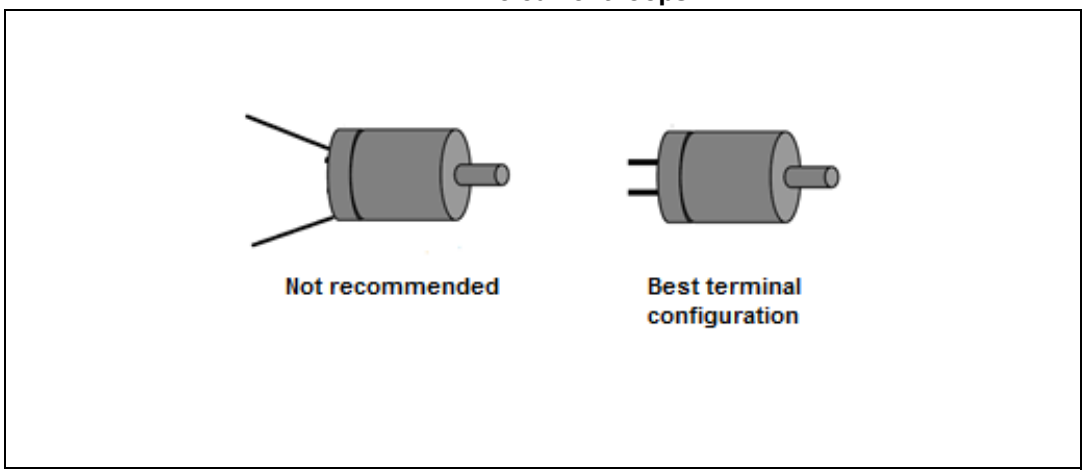
- Location of filters should be as close as possible to the source of interference, basically as close to the power module as possible.
- Bypass capacitor leads should be as short as possible.
- DC motors having motor case completely shielded, with no holes and no plastic cap, have to be chosen in order to avoid noise generated inside the motor is coupled with near PCB traces and/or with measurement system.

Figure 38. Example of DC Motors cases



- Terminals should go out from motor very close each to other (in order to reduce current loops). Suppressing capacitors between metal motor case and terminals should be integrated.

Figure 39. Motor Terminals have to go out as close as possible each other to minimize current loops



8 Revision history

Table 3. Document revision history

Date	Revision	Changes
30-Nov-2018	1	Initial release.
22-Feb-2019	2	Updated *Figure 1* and *Figure 18*. Updated *Chapter 5*. Updated *Equation 21* and *Equation 22*.
02-Sep-2019	3	Updated *Figure 1*.