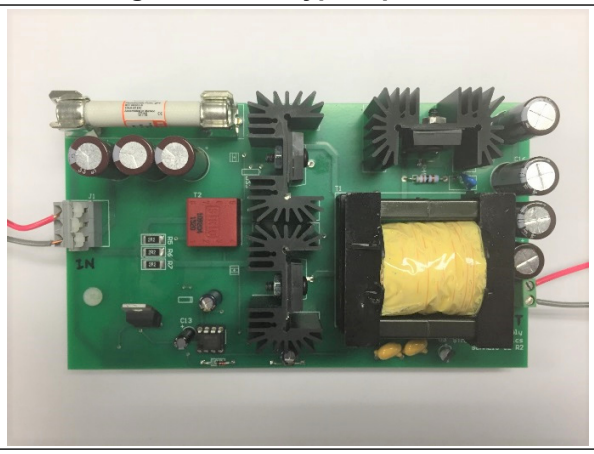
AN5287
Application note

170W high input voltage two switch flyback based on L6565 and 1500V K5 MOSFETs

Introduction

This application note describes a DC-DC converter design based on ST L6565 quasi-resonant controller. The input voltage is from 400 V to 1200 V, but can be scaled to any higher or lower value, as are the output voltage and output power. As an example, the output voltage is 48 V, and the output power is 173 W in this application note. The targeted applications can be power supplies in industrial electrical equipment, wind or photovoltaic systems, or any high-voltage-bus converters in data-center or telecom devices. Design specifications, topology selection, design equations, prototype and experimental results are illustrated in this document.

Figure 1. Prototype top view



Contents

1 Design specifications

Table 1 shows basic design specifications for this DC/DC converter. When applications become more specific, the demo board can be easily trimmed with detailed specific requirements such as the transient response, isolation voltage, lifetime requirement, etc. However, this application note doesn't target any specific product but instead focuses on fundamental technology with basic specifications as in *Table 1*.

There are at least two major challenges for this design: very high voltage stress on switching devices, and associated very high switching loss. These two challenges determine topology selection in the following section.

Table 1. Basic design specifications

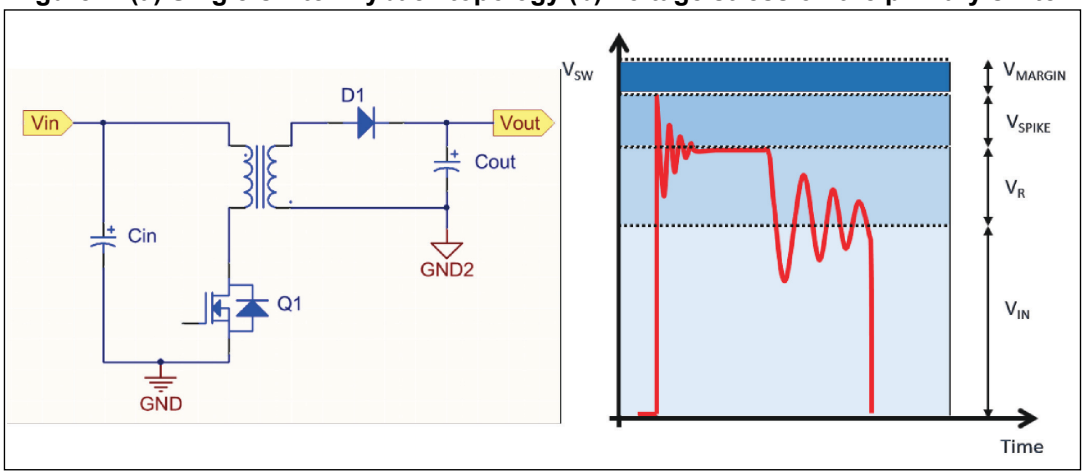
Parameters	Values	Parameters	Values
Input voltage range	400V - 1200V DC	Output voltage	48V DC
Output power	173W (48V @ 3.6A)	Load range	20% to 100%
Efficiency	> 85% Full Load	Regulation accuracy	+/-3%
Output voltage ripple	< 5% PK-PK	Ambient temperature	50 °C
Overcurrent protection	Short-circuit	Overvoltage protection	>60V
Size	17cm x 10cm	Cooling	Natural convection

2 Topology selection

Traditional topologies such as flyback or forward converters can offer a simple power supply solution but have problems such as high switching losses (due to hard switching mechanism) and overvoltages on the primary switch (due to leakage inductance and reflected voltage from the secondary). Overvoltage stresses on the switch are acceptable for low-input-voltage applications but become unrealistic for devices when the input voltage is as high as 1200 V. Resonant converters can reduce switching losses significantly, however, in the meantime, also increase the voltage stress on the primary switch by 2~3 times. In addition, the input voltage of a resonant converter is limited to a narrow range. Compared to power MOSFETs, bipolar devices such as IGBT can stand a higher voltage stress but they can only switch at lower frequencies, typically 10 kHz. As a result, passive components such as the transformer are bigger and the total converter size is thus increased.

Figure 2 shows a single-switch flyback topology and the voltage stress on the primary switch Q1 when the switch is off. The single-switch flyback topology has advantages of the minimum component count, Buck/Boost regulation, and a wide range of input voltage. However, the primary switch suffers very high voltage stress due to the reflected voltage V_R from the secondary side and the spike voltage from transformer leakage inductance. As shown in Fig. 1(b), V_{IN} is the maximum input voltage, V_R is the reflected voltage, V_{SPIKE} is the spike voltage, V_{MARGIN} is the margin voltage, and V_{SW} is the minimum voltage required for the switch equal to the sum of V_{IN}, V_R, V_{SPIKE}, and V_{MARGIN}. If V_{IN} = 1200 V, V_R = 1200 V, V_{SPIKE} = 200 V and V_{MARGIN} = 240 V, V_{SW} is equal to $V_{IN}+V_R+V_{SPIKE}+V_{MARGIN}$ = 2840 V. Even with snubbers, there is still 2640 V breakdown voltage required for the primary switch which is beyond most MOSFET's capability. Moreover, extra snubbers increase the cost, loss and temperature stress of the converter

Figure 2. (a) Single-switch flyback topology (b) Voltage stress on the primary switch



To overcome the problem of a single-switch flyback, a double-switch flyback topology is proposed to implement such a high-voltage power supply. As shown in *Figure 3*, double-switch flyback topology is similar to the traditional one except for one more switch and diode snubber. Two primary switches, Q1 and Q2, are turned on and turned off synchronously. When Q1 and Q2 are off, snubber diodes D3 and D4 clamp peak voltages of Q1 and Q2 to

the input voltage Vin. Energy from the transformer leakage inductance is recycled back to the input through clamping diodes D3 and D4.

Figure 3. Double-switch flyback topology used in this design

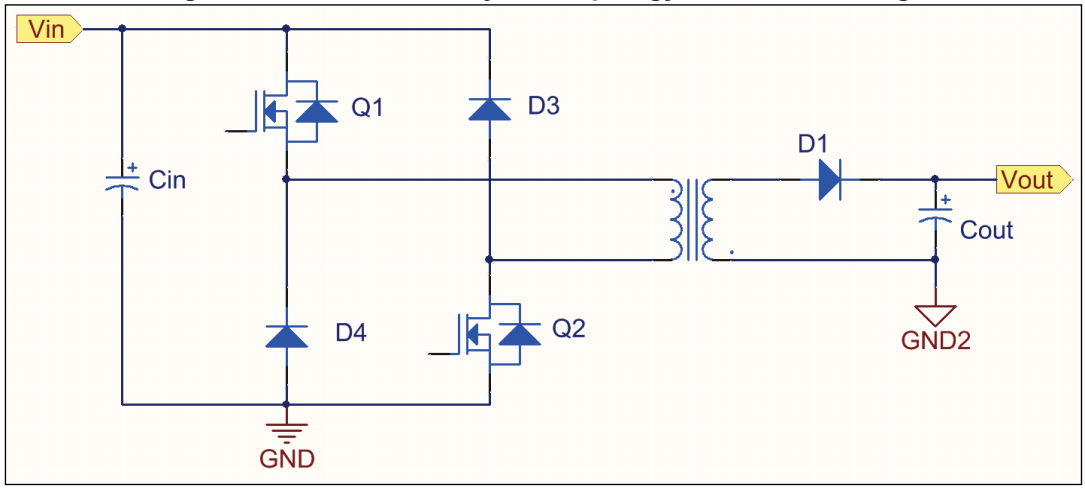
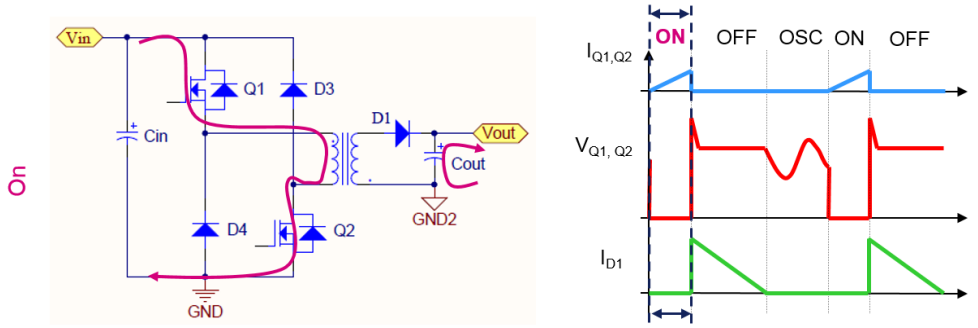
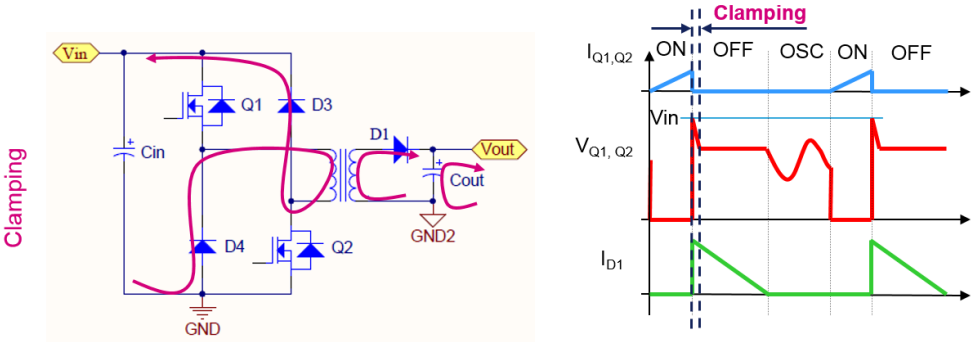


Figure 4 shows four different operational phases for double-switch flyback converter. During Phase I, power switches Q1 and Q2 are both turned on. A current is flowing from the input to the primary side of transformer and increasing linearly. In the meantime, all the clamping and rectifying diodes are off, as shown in *Figure 4*(a). During Phase II, power switches Q1 and Q2 are turned off and the rectifier diode D1 is on. Most of the current accumulated in Phase I is flowing to the output through the rectifier diode and the secondary side of the transformer. However, there is still some residual current at the primary side due to the leakage inductance of the transformer. This leakage current would create overvoltages on Q1 and Q2, if there were no clamping circuits. As shown in *Figure 4*(b), D3 and D4 conduct in Phase II and clamp the peak voltages of Q1 and Q2 at the input voltage Vin. Compared to traditional snubbers such as RCD or Zener diodes, residual energy of the leakage inductance can be recycled through D3 and D4 to the input, boosting the efficiency and reducing the snubber thermal stress. In Phase III, all the switches at the primary side of transformer, including Q1, Q2, D3 and D4 are off, only D1 is rectifying a current to the output. Though there is no current at the primary side, a voltage V_R which is approximately equal to *n* times Vout (*n* is the turns ratio of the transformer primary windings vs. the secondary windings) is reflected to the primary side. Peak voltages of power switches Q1 and Q2 are approximately equal to $0.5(Vin+V_R)$, assuming two switches are sharing voltages equally. During Phase IV, all the switches are off and there is no current in switches. Since there is some residue energy in the drain-to-source capacitance of Q1 and Q2, these capacitance is resonant with the primary inductance of the transformer. This phase is still as important as previous ones. If the switches Q1 and Q2 can be turned on at the valleys of oscillating voltage, the switching loss of the device can be reduced.

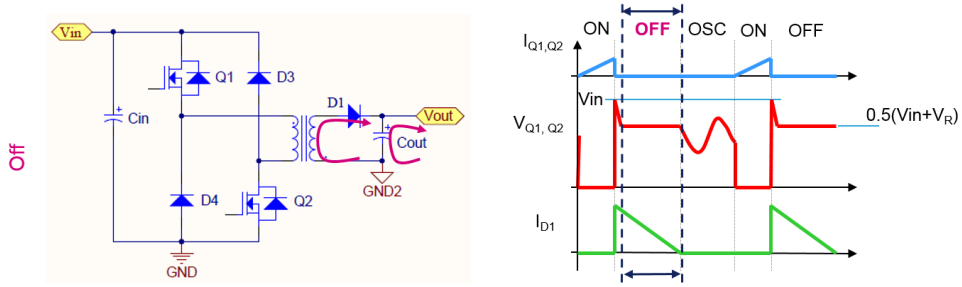
Figure 4. Operational phases for double-switch flyback converter



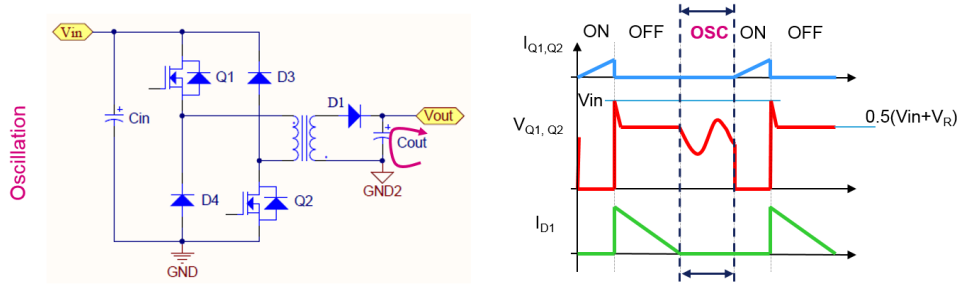
(a) Phase I: Q1 Q2 are on, D1 D3 D4 are off



(b) Phase II: Q1 and Q2 are off, D3 and D4 are on and clamping, D1 is on and rectifying



(c) Phase III: Q1 Q2 D3 D4 are off, D1 is on and rectifying



(d) Phase IV: Q1 Q2 D1 D3 D4 are off, but the primary side inductance of transformer is resonant with the drain-to-source capacitance of primary side switches

Like a traditional single switch flyback converter, double-switch flyback converters can also work in Continuous Conduction Mode (CCM), Discontinues Conduction Mode (DCM) and Transition Mode (TM) which is a boundary mode between CCM and DCM. In DCM and TM, both switches Q1, Q2 and the rectifier diode D1 achieve zero current switching and switching losses are reduced. DCM has the disadvantage of unused time slot of duty cycle and TM has the disadvantage of a variable frequency control. When switches Q1 and Q2 are turned on at the valley of oscillating drain-to-source voltage waveform, a quasi-ZVS (Zero Voltage Switching) is achieved. Quasi-resonant mode is a hybrid mode of DCM and TM and has even smaller switching loss because it can achieve both ZCS and quasi-ZVS at the same time. Similar to TM, the quasi-resonant mode needs a variable frequency to control.

Compared to a traditional single-switch flyback, the duty cycle of a double-switch flyback should never be exceeding 0.5, i.e., 50%. This is because the reflected voltage V_R should be always smaller than the minimum input voltage Vin otherwise clamping diode D3 and D4 are on at Phase III and become kind of full-bridge operation. When Q1 and Q2 are on in Phase I, the voltage on the primary side of the transformer is Vin. When Q1 and Q2 are off in Phase III, this voltage is V_R. Since V_R should be smaller than Vin as explained above, it takes a longer time to reset the transformer. For this reason, duty cycle D must be smaller than 0.5 to avoid transformer saturation.

Because of very high input voltage from design specifications, minimizing switching losses of power switches Q1 and Q2 is the major concern. The quasi-resonant mode is thus adopted and implemented by ST quasi-resonant controller L6565. L6565 is a current-mode primary controller IC, specially designed to build an offline quasi-resonant ZVS flyback converter. L6565 can offer line feed-forward to deliver constant power when the mains change, frequency foldback for optimum standby efficiency, pulse-by-pulse and hiccup-mode overcurrent protection. The details of L6565 and quasi-resonant flyback converter design is illustrated in [*1*] and [*2*].

3 Design equations

There are several pre-design choices based on experience and estimation. An iteration approach can be applied to change these pre-design choices if an optimization is wanted.

- Minimum Switching Frequency Fmin: Fmin is chosen based on design experience. For example, F_{min} is tens of kHz for application specifications in *Table 1*. In general, F_{min} is higher, the transformer is smaller but its loss is also higher.
- Reflected Voltage V_R: $V_R \approx D/(1-D)$ Vin without considering oscillation and D<0.5. V_R is a critical parameter influencing many aspects of the converter. Table 2 in [*1*] summarizes the effect of V_R selection on converter performance.
- Turns Ratio $n=n1/n2=V_R/Vout$, n1 and n2 are turns numbers of primary and secondary windings
- Estimated total drain-to-source capacitance Cd
- Estimated total efficiency η

The predesign choices are summarized in *Table 2*.

Table 2. Predesign choices

Fmin	V_R	n	Cd	η
30 kHz	179 V	3.679	0.15 nF	85%

To begin the design, calculate the input power Pin first:

Equation 1

$$P_{in} = \frac{P_{out}}{\eta}$$

Pin=240 W.

Calculate the maximum primary inductance [1].

Equation 2

$$L_{pmax} = \frac{1}{\left[\sqrt{2 \cdot P_{in\,max} \cdot f_{sw\,min}} \cdot \left(\frac{1}{V_{in\,min}} + \frac{1}{V_R}\right) + \pi \cdot f_{sw\,min} \cdot \sqrt{C_d}\right]^2}$$

Lpmax≈1.675 mH, let Lp=1.55 mH.

The resonance (oscillation) frequency of the drain tank circuit is [1]:

Equation 3

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_p \cdot C_d}}$$

The transition frequency is the frequency the system would work if no oscillation [1]:

Equation 4

$$f_T = \frac{1}{2 \cdot P_{in} \cdot L_p \cdot \left(\frac{1}{V_{in}} + \frac{1}{V_R}\right)^2}$$

The switching frequency is [1]:

Equation 5

$$f_{SW} = \frac{2 \cdot f_T}{1 + \frac{f_T}{f_r} + \sqrt{1 + 2 \cdot \frac{f_T}{f_r}}}$$

From (5), recalculate the new minimum switching frequency fmin: f_{SWmin} = 32.4 kHz when Vin = 400 V and f_{SWmax} = 51.5 kHz when Vin = 1200 V.

Calculate the duty cycle of primary side:

Equation 6

$$D = \frac{1}{V_{in}} \cdot \sqrt{2 \cdot P_{in} \cdot L_p \cdot f_{SW}}$$

Calculate the duty cycle of secondary side:

Equation 7

$$D' = \frac{1}{V_R} \cdot \sqrt{2 \cdot P_{out} \cdot L_p \cdot f_{SW}}$$

From (6) and (7), D = 0.318, D' = 0.616 when Vin = 400 V.

Calculate the peak current of primary side:

Equation 8

$$I_{PKp} = \sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f_{SW}}}$$

Calculate the peak current of secondary side:

Equation 9

$$I_{PKs} = \frac{2 \cdot I_{DCs}}{D'}$$

From (8) and (9), I_{PKp} = 3.14A, I_{PKs} = 11.85A when Vin = 400 V. (Currents are maximized at the minimum Vin).

Calculate the DC current of primary and secondary sides:

Equation 10

$$I_{PKp} = \sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f_{SW}}}$$

Equation 11

$$I_{DCs} = \frac{P_{out}}{V_{out}}$$

From (10) and (11), I_{DCp} = 0.499A, I_{DCs} = 3.646A when Vin = 400 V.

Calculate the total RMS current:

Equation 12

$$I_{RMSp} = I_{PKp} \cdot \sqrt{\frac{D}{3}}$$

Equation 13

$$I_{RMSs} = I_{PKs} \cdot \sqrt{\frac{D'}{3}}$$

From (12) and (13), I_{RMSp} = 1.022A and I_{RMSs} = 5.366A.

Calculate the RMS of the total AC current:

Equation 14

$$I_{ACp} = \sqrt{I_{RMSp}^2 - I_{DCp}^2}$$

Equation 15

$$I_{ACs} = \sqrt{I_{RMSs}^2 - I_{DCs}^2}$$

From (14) and (15), I_{ACp} = 0.892 A and I_{ACs} = 3.937A.

Calculate the peak voltage of primary side switch:

Equation 16

$$V_{PKDS} = V_{in}$$

Calculate the peak voltage of secondary side diode:

Equation 17

$$V_{REV} = V_{out} \cdot \left(1 + \frac{V_{in}}{V_R}\right)$$

From (*16*) and (*17*), V_{PKDS} = 1200 V and V_{REV} = 310 V.

Calculate sensing resistor R_{sense}:

Equation 18

$$Rsense = \frac{Vcs}{I_{PKp}}$$

Vcs = 1.13 V is the maximum signal available on current sense input. From (*18*), R_{sense} = 0.300 Ω.

Calculate the maximum ESRs of the primary and secondary capacitors:

Equation 19

$$ESR_{capp} = \frac{\Delta V_{inp}}{\Delta I_{ACp}}$$

Equation 20

$$ESR_{caps} = \frac{\Delta V_{outmax}}{\Delta I_{ACs}}$$

If there is 5% peak ripple, ΔVinp = 400Vx5% = 20 V and ΔVinp = 48Vx5% = 2.4 V. By (*19*) and (*20*), ESR_{capp} = 15.8 Ω and ESR_{caps} = 0.431 Ω.

Based on the above calculation results, select input and output capacitors from maximum ESRs and input and output voltages, design the transformer, and select power devices.

4 Transformer design

Based on the above equations, the parameters of transformers are calculated in *Table 3*. These parameters are usually sufficient for a manufacturer to customize a transformer. The datasheet of the transformer made for this project is attached in *Appendix A: on page 27*.

Table 3. Transformer parameters

Parameters	Values	Parameters	Values
Primary Inductance Lp	1.18 mH	Turns ratio n	3.864
Switching frequency F_{SW}	32.4 kHz to 51.5 kHz	Ambient temperature	50 °C
Transformer's max. Temperature rise **Δ**T	40 °C	Footprint	33% to 50% of PCB total area
Primary peak voltage V_{PKp}	400 V	Secondary peak voltage VPKs	49.2 V
Primary duty cycle D	0.318	Secondary duty cycle D’	0.616
Primary peak current I_{PKp}	3.14 A	Secondary peak current	11.85 A
Primary DC current I_{DCp}	0.50 A	Secondary DC current I_{DCs}	3.65 A
Primary total RMS current I_{RMSp}	1.02 A	Secondary total RMS current I_{RMSp}	5.37 A
Primary AC RMS current I_{ACp}	0.89 A	Secondary AC RMS current I_{ACs}	3.94 A

Transformer datasheet is attached in *Appendix A*.

5 Device selection

STMDmesh™ K5 series are best in class very high voltage MOSFETs. They have extremely good RDS(on) at very high breakdown voltage BVDSS and also high switching speed with fast body diode, which especially target flyback topologies in the high voltage range with high efficiency and lower design complexity. The STW12N150K5 is selected for this application. *Table 4* shows its basic parameters.

Table 4. : STW12N150K5 basic parameters

BV_{DSS} [V]	R_{DS} [Ω]	I_D [A]	Qg [nC]	Sales type	Main application	Package
1500	1.9	7	47	STx12N150K5	HV SMPS	TO-247

Equation 21 shows how to calculate the loss in the MOSFET.

Equation 21

$$P_{SWmax} \geq \frac{V_{dsmax} \cdot I_{drainmax} \cdot t_{swoff}}{2 \cdot T_s}$$

$$P_{cond\ max} = 1.6 \cdot R_{dson} \cdot I^2_{rms}$$

$$P_{drv} = V_{gs} \cdot Q_g \cdot f_s$$

$$P_{Cd} = 0.5 C_d V^2_{Cd\text{-}turn\text{-}on} f_s \approx 0\ if\ ZVS$$

$$P_{mosfet} = P_{swmax} + P_{condmax} + P_{drv} + P_{Cd}$$

Table 5 shows the loss calculation results and maximum thermal resistance based on (*21*).

Table 5. STW12N150K5 loss calculation results

Parameters	Values	Description
R(ds)on	1.9Ω	On resistance (max. @ 25°C)
Qg	47nC	Total gate charge (max.)
Qgd	32nC	Gate-to-drain charge (typ.)
gfs	4.25S	Forward transconductance (typ.)
Vth	4V	Threshold voltage (typ.)
Coss	0.032nF	Drain-to-source capacitance (typ.)
Rthjc	0.28°C/W	Junction-to-case thermal resistance

Table 5. STW12N150K5 loss calculation results (continued)

Parameters	Values	Description
Rthja	50°C/W	Junction-to-ambient thermal resistance
Rgate	10Ω	External gate resistor
Toff	135ns	Estimated current fall time at turn-off @Vin=Vinmin
Pcond	3.972W	Conduction losses @Vin=Vinminavg, Tj = 125°C
Pcap	0.388W	Capacitive losses at turn-on @Vin=Vinminavg
Psw	1.732W	Switching losses at turn-off @Vin=Vinminavg
Ptot	6.09W	Estimated total MOSFET losses @ Vin=Vinmin
Toff	140ns	Estimated current fall time at turn-off @Vin=Vdcmax
Pcond	0.993W	Conduction losses @Vin=Vdcmax, Tj = 125 °C
Pcap	3.995W	Capacitive losses at turn-on @Vin=Vdcmax
Psw	7.183W	Switching losses at turn-off @Vin=Vdcmax
Ptot	12.172W	Estimated total MOSFET losses @ Vin=Vdcmax
Rth	7°C/W	Maximum total thermal resistance
Rthsink	6°C/W	Maximum heat sink thermal resistance

ST Turboswitch "R" ultra high performance diodes are designed for high frequency applications with hyperfast recovery and size decrease of snubbers and heat sinks. High frequency STTH30R03CW diode in this series is selected for secondary rectifier. *Table 6* summarizes its basic parameters.

Table 6. STTH30R03CW basic parameters

$I_{F(AV)}$	V_{RRM}	I_{RM} (typ.)	Tj (max.)	V_F (typ.)	trr (max)	Package
2 x 15A	300V	4.5A	175°C	1.4V	35ns	TO-247

Equation 22 shows how to calculate the diode loss. Since the diode current is in Discontinuous Conduction Mode (DCM), only conduction loss is considered.

Equation 22

$$P = 1 \times I_{F(AV)} + 0.026\ I_F{}^2\ (RMS)$$

Table 7 shows the rectifier diode loss and thermal resistance requirement.

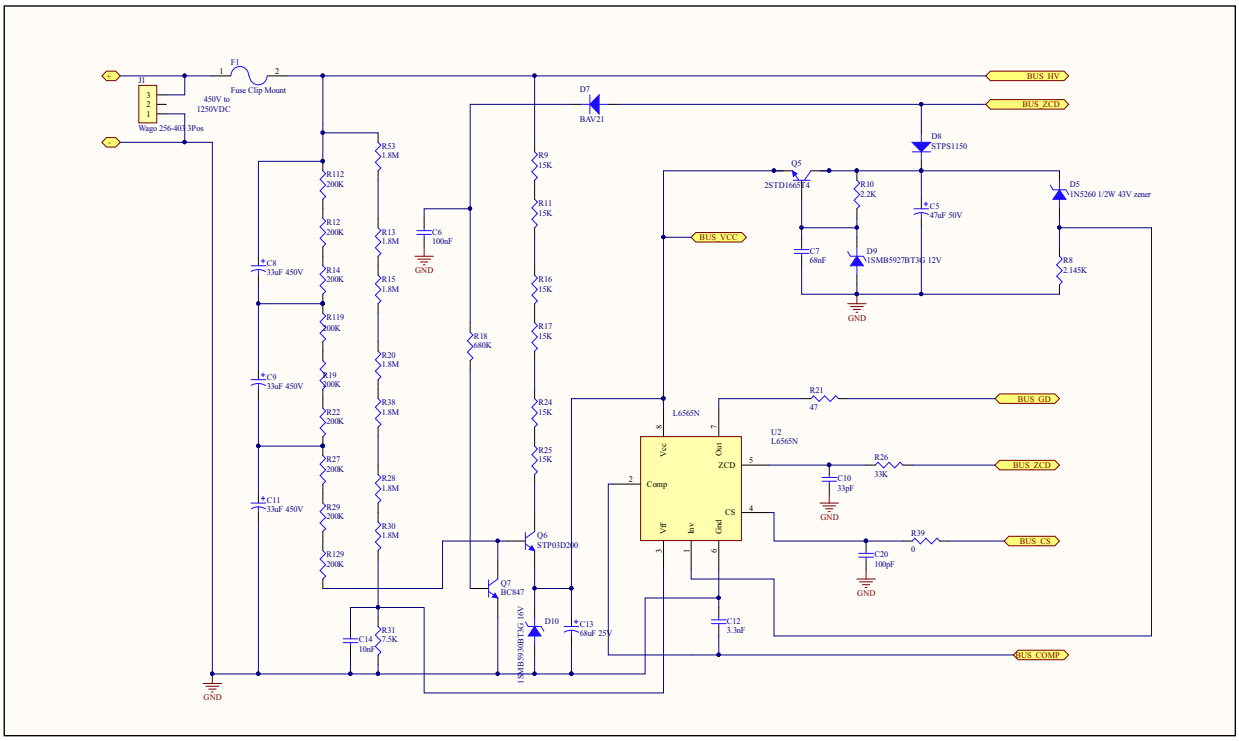
Table 7. STTH30R03CW loss calculation results

Parameters	Values	Units	Description
$I_{F(AV)}$	3.65	A	Averaged Forward Current at Full Load Condition
$I_{F(RMS)}$	5.37	A	Secondary Total RMS Current
Rthjc	1.0	°C/W	Junction-to-Case Thermal Resistance
Pcond	4.40	W	Conduction Loss
Ptot	4.40	W	Only Conduction Loss Considered for DCM
Rthsink	21.5	°C/W	Maximum heat sink Thermal Resistance

6 Schematics and layout

Figure 5, *6*, *7* show the schematics of a double-switch-flyback converter for this application. In *Figure 5*, R9, R11, R16, R17, R24, R25 Q6 are pre-charging L6565N IC when the converter starts. After starting, the pre-charge circuit is turned off by Q7 and the Vcc of L6565N is from Bus ZCD. D5 and R8 is the overvoltage protection of IC [*1*]. The overcurrent protection is through Bus CS.

Figure 5. Double-switch flyback schematic I



In *Figure 6*, U1 is PM8834, a 4 A dual low-side MOSFET driver; T2 is a pulse transformer for isolation. D1 D2 D3 D4 are clamping diodes which are ST STTH112 for high voltage ultrafast rectifier with a peak voltage of 1200 V and an average current of 1 A.

Figure 6. Double-switch flyback schematic II

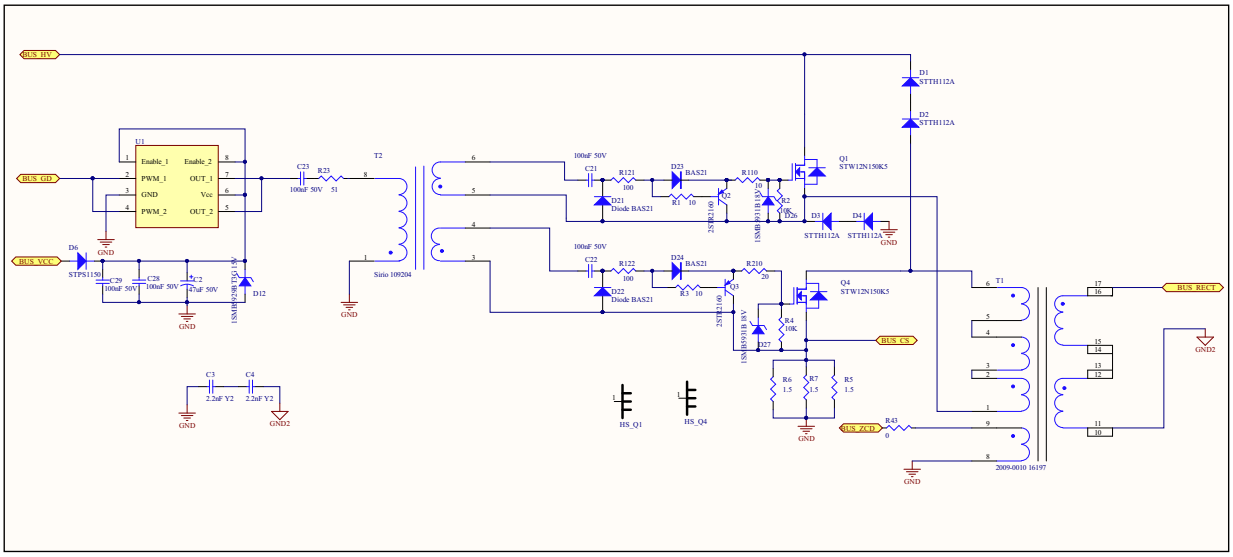


Figure 7. Double-switch flyback schematic III

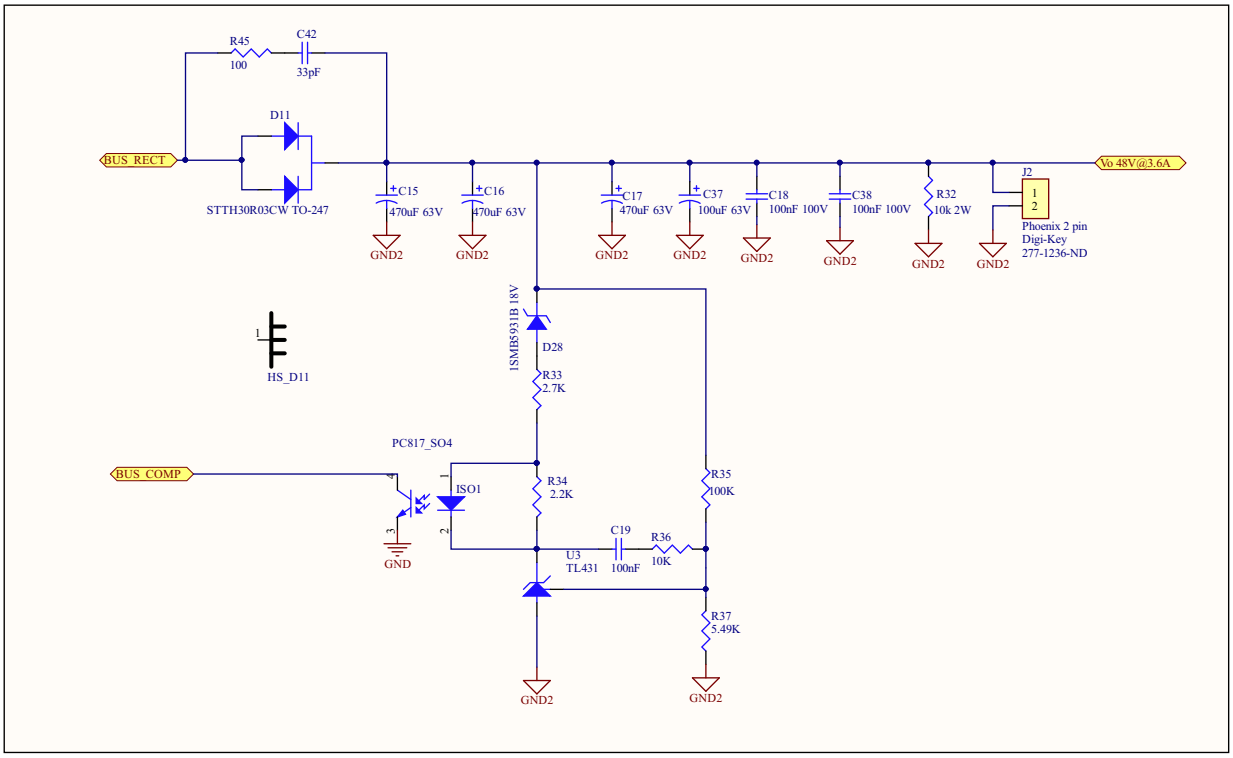


Figure 8 shows the layout of PCB and *Figure 9* shows the prototype.

Figure 8. PCB layout

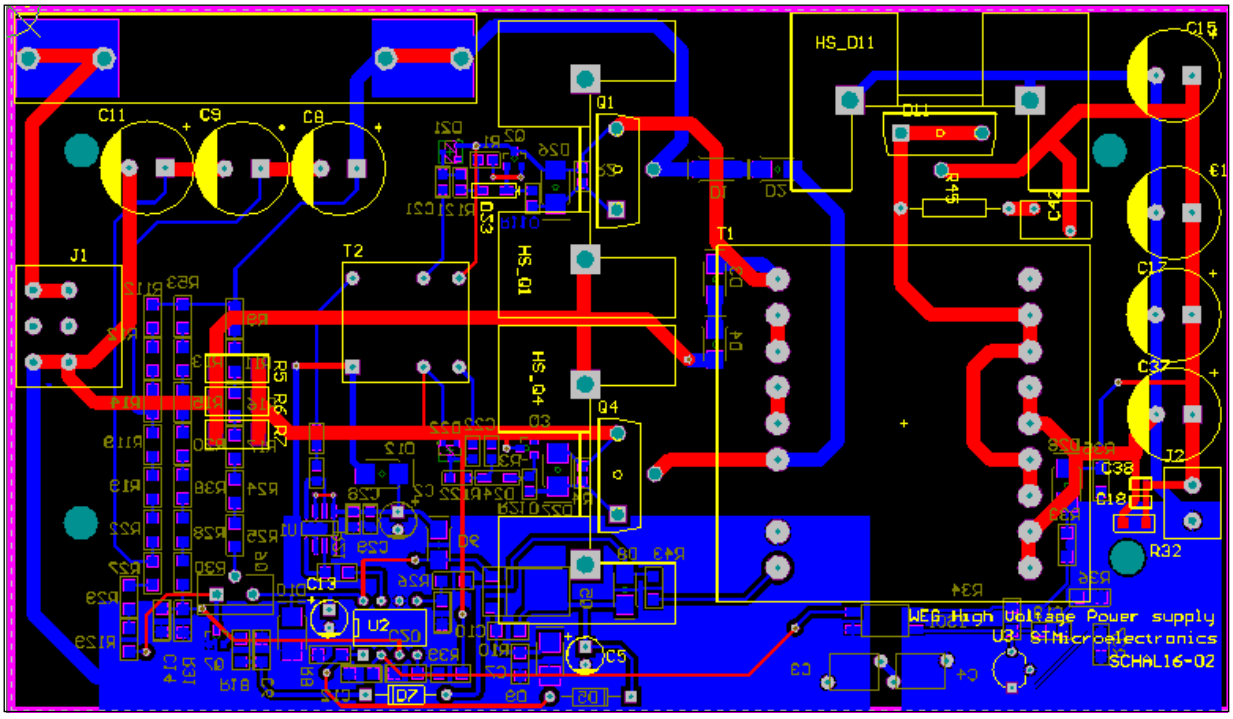
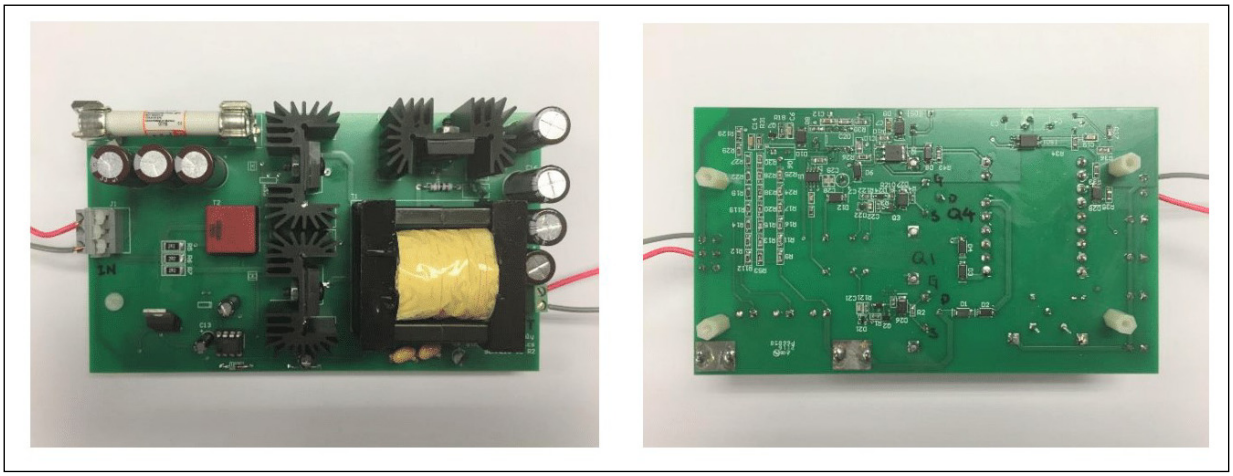


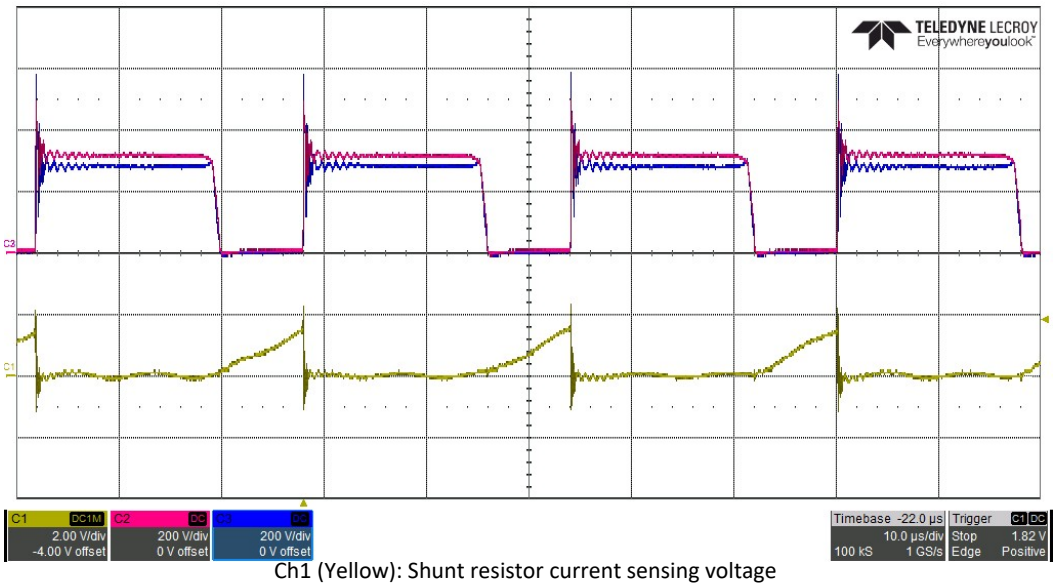
Figure 9. (a) Prototype top view (b) Prototype bottom view



7 Experimental results

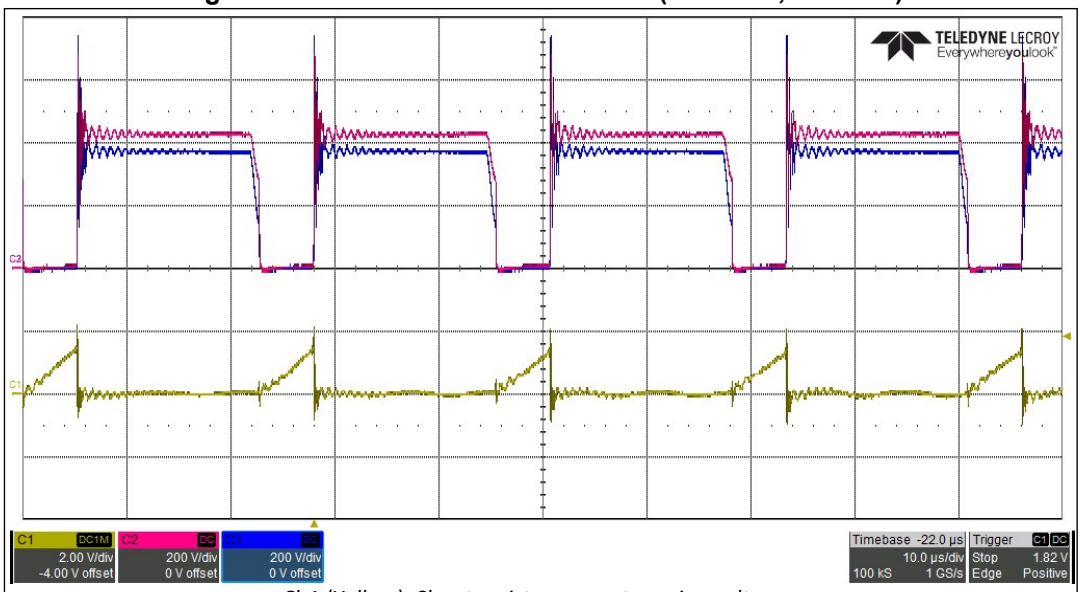
Figure 10~*14* show the waveforms of the prototype under different input voltages.

Figure 10. Waveforms measurements (400V Vin, full load)



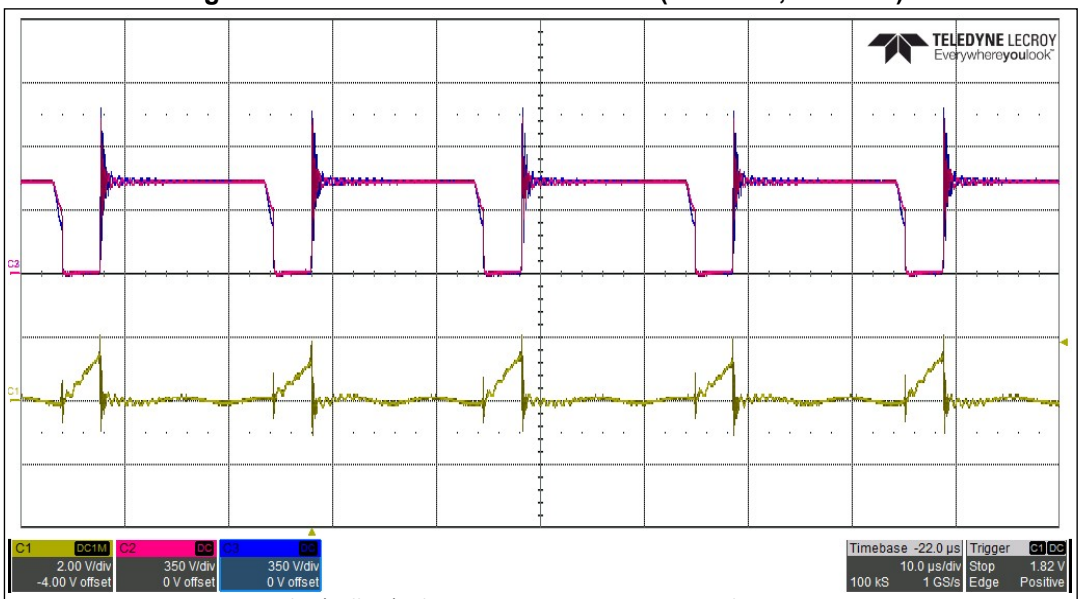
Ch1 (Yellow): Shunt resistor current sensing voltage
Ch2 (Red): Drain to source voltage of the main Mosfet Q1
Ch3 (Blue): Drain to source voltage of the main Mosfet Q4

Figure 11. Waveforms measurements (600V Vin, full load)



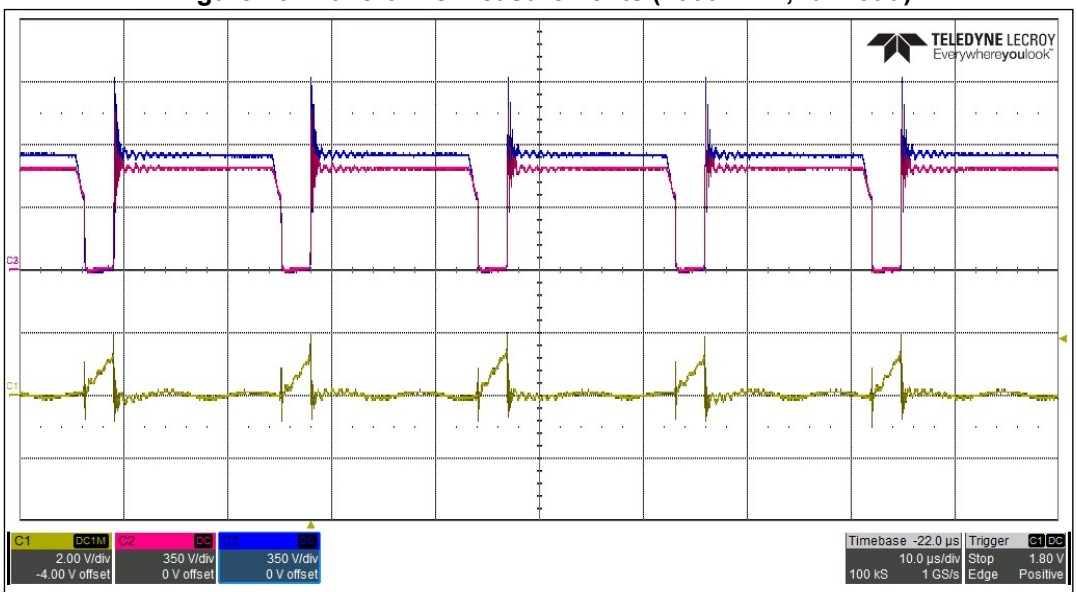
Ch1 (Yellow): Shunt resistor current sensing voltage
Ch2 (Red): Drain to source voltage of the main Mosfet Q1
Ch3 (Blue): Drain to source voltage of the main Mosfet Q4

Figure 12. Waveforms measurements (800V Vin, full load)



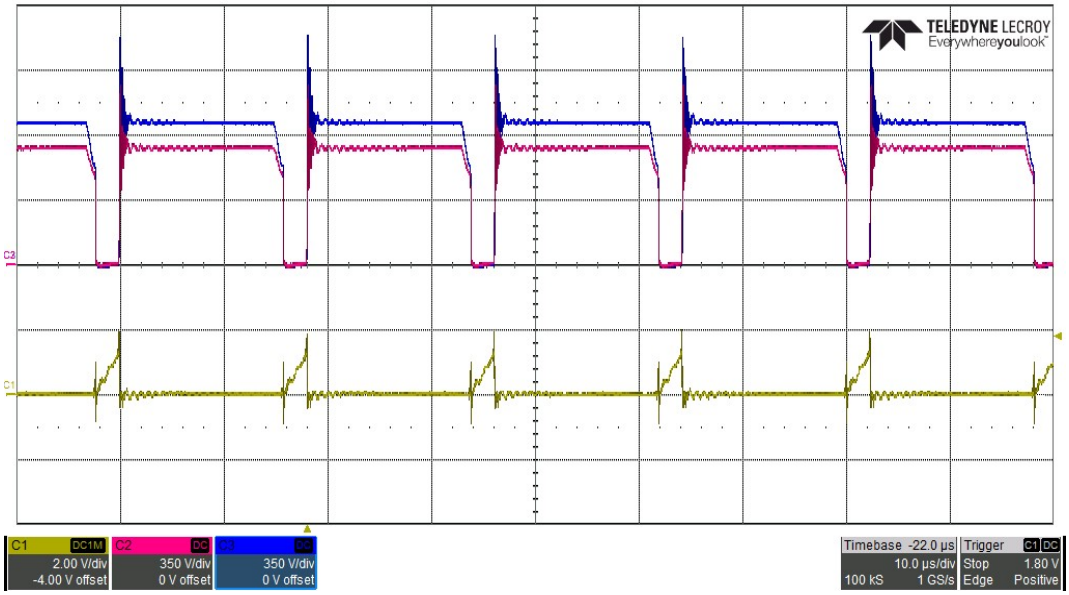
Ch1 (Yellow): Shunt resistor current sensing voltage
Ch2 (Red): Drain to source voltage of the main Mosfet Q1
Ch3 (Blue): Drain to source voltage of the main Mosfet Q4

Figure 13. Waveforms measurements (1000V Vin, full load)



Ch1 (Yellow): Shunt resistor current sensing voltage
Ch2 (Red): Drain to source voltage of the main Mosfet Q1
Ch3 (Blue): Drain to source voltage of the main Mosfet Q4

Figure 14. Waveforms measurements (1200V Vin, full load)



Ch1 (Yellow): Shunt resistor current sensing voltage
Ch2 (Red): Drain to source voltage of the main Mosfet Q1
Ch3 (Blue): Drain to source voltage of the main Mosfet Q4

Measure efficiencies at room temperature and Vin≈400 V, 600 V, 800 V, 1000 V, and 1200 V, and at a load≈20%, 40%, 60%, 80%, and 100%. *Table 8* shows load current and load power for different load percentage. *Table 9* shows efficiencies under different Vin and load.

Table 8. Load percentage and load current

Load percentage	20%	40%	60%	80%	100%
Load current	0.72A	1.44A	2.16A	2.88A	3.60A
Load power	34.6W	69.2W	103.8W	138.4W	173W

Table 9. Efficiency measurement

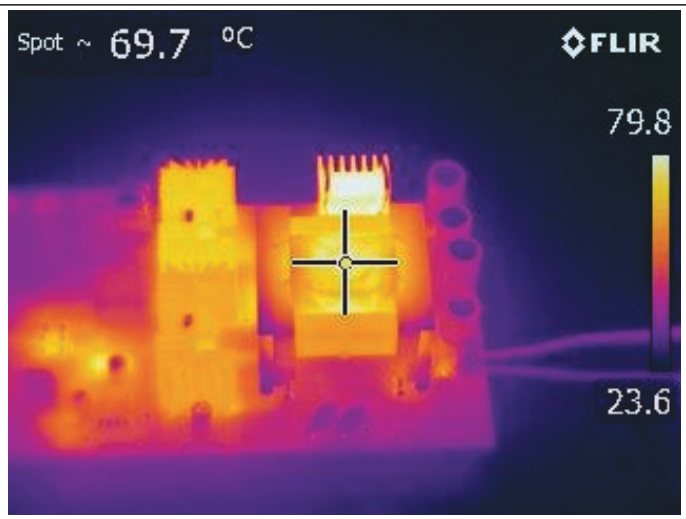
Vin (V)	Iin (A)	Vout (V)	Iout (A)	Load percentage (%)	Efficiency (%)
400	0.105	47.3	0.76	21.1	85.5
400	0.199	47.3	1.47	40.8	87.3
400	0.290	47.3	2.19	60.8	89.2
400	0.384	47.3	2.92	81.1	89.9
400	0.478	47.3	3.62	100	89.6
600	0.071	47.3	0.76	21.1	84.3
600	0.135	47.3	1.47	40.8	85.8
600	0.194	47.3	2.19	60.8	88.9

Table 9. Efficiency measurement (continued)

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Load percentage (%)	Efficiency (%)
600	0.257	47.3	2.92	81.1	89.6
600	0.317	47.3	3.62	100	90.0
800	0.055	47.3	0.76	21.1	81.7
800	0.102	47.3	1.47	40.8	85.2
800	0.148	47.3	2.19	60.8	87.5
800	0.195	47.3	2.92	81.1	88.5
800	0.240	47.3	3.62	100	89.2
1000	0.045	47.3	0.76	21.1	79.9
1000	0.084	47.3	1.47	40.8	82.8
1000	0.121	47.3	2.19	60.8	85.6
1000	0.158	47.3	2.92	81.1	87.4
1000	0.194	47.3	3.62	100	88.2
1200	0.039	47.3	0.76	21.1	76.8
1200	0.071	47.3	1.47	40.8	81.6
1200	0.102	47.3	2.19	60.8	84.6
1200	0.135	47.3	2.92	81.1	85.3
1200	0.164	47.3	3.62	100	87.0

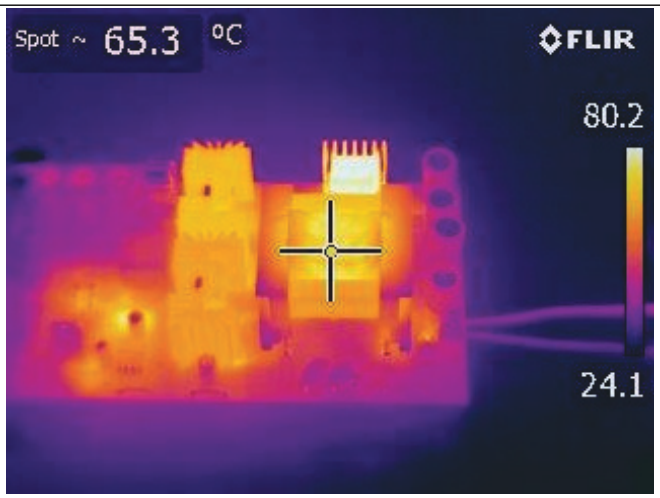
For the thermal measurement setup, the prototype ran for more than 1 hour. ΔT is defined as the measured temperature minus the room temperature (25°C). The temperatures were measured at the full load condition for different input voltages. *Figure 15*-*19* show the results.

Figure 15. Thermal measurement for Vin = 400V and full load



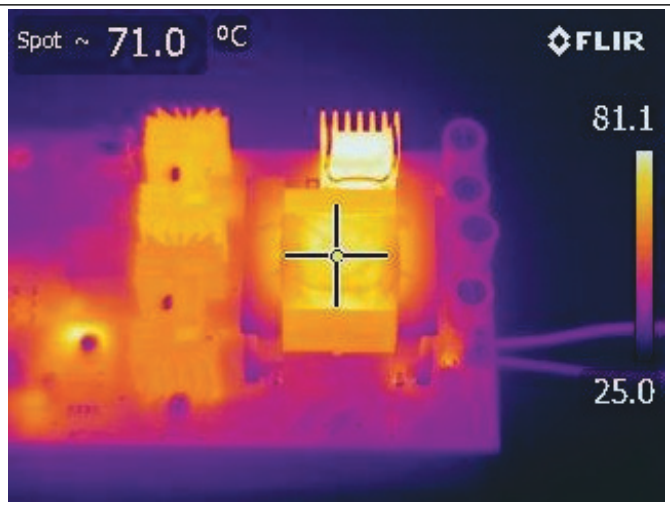
	T	ΔT		T	ΔT
Q1	66.1°C	41.1°C	**D11**	79.8°C	54.8°C
Q4	69.3°C	44.3°C	**T1**	69.7°C	44.7°C

Figure 16. Thermal measurement for Vin = 600V and full load



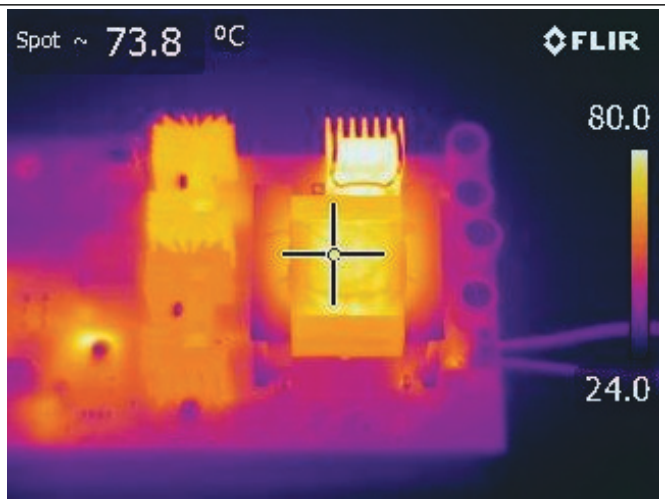
	T	ΔT		T	ΔT
Q1	66.3°C	41.3°C	**D11**	80.2°C	55.2°C
Q4	66.6°C	41.6°C	**T1**	65.3°C	40.3°C

Figure 17. Thermal measurement for Vin = 800V and full load



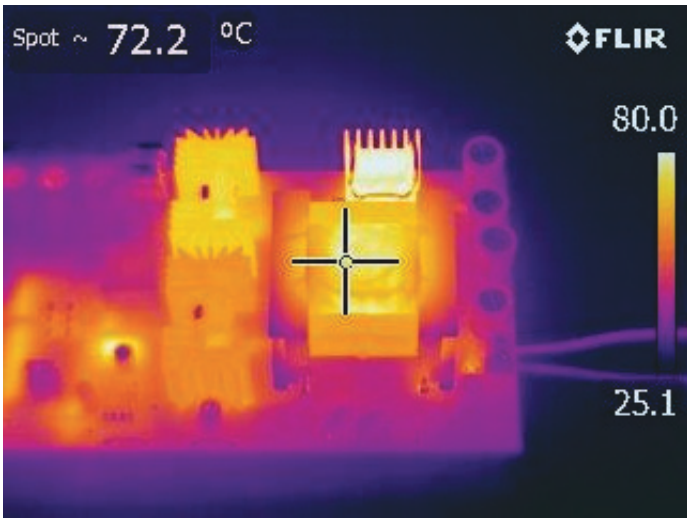
	T	ΔT		T	ΔT
Q1	67.0°C	42.0°C	**D11**	81.1°C	46.0°C
Q4	66.2°C	41.2°C	**T1**	71.0°C	56.1°C

Figure 18. Thermal measurement for Vin = 1000V and full load



	T	ΔT		T	ΔT
Q1	72.8°C	47.8°C	**D11**	80.0°C	55.0°C
Q4	68.6°C	43.6°C	**T1**	73.8°C	48.8°C

Figure 19. Thermal measurement for Vin = 1200V and full load



	T	ΔT		T	ΔT
Q1	77.1°C	52.1°C	**D11**	80.0°C	55.0°C
Q4	70.2°C	45.2°C	**T1**	72.2°C	47.2°C

8 References

1. ST Application Note AN1326 “L6565 Quasi-Resonant Controller” Nov. 2002.
2. ST Datasheet “L6565 Quasi-Resonant SMPS Controller” Jan. 2003.

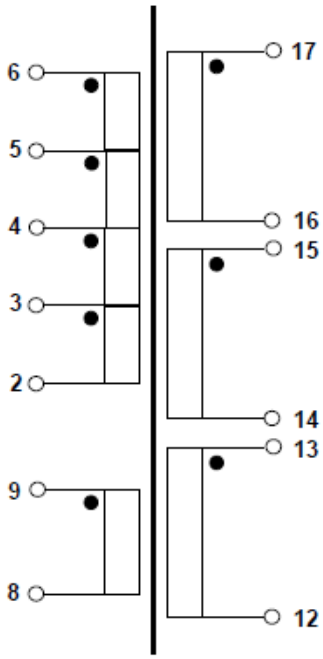
Appendix A

Figure 20. Transformer datasheet

aq Magnetica	Product Technical Specification	Code : 08087
	SMT 175W 26kHz 1.15mH 48V	Class Code : 2009.0010
Date : 07.06.2016	Revision: 01	Page 1 of 2

TYPICAL APPLICATION
TRANSFORMER FOR FLYBACK TOPOLOGY

SCHEMATIC



TECHNICAL DATA

INDUCTANCE (*MEASURE 1KHZ, TA 20°C*)	
PIN 6-2	1.15 mH ±15%
PIN 9-8	12 µH ±15%
PIN 17-16	10 µH ±15%
PIN 15-14	8.5 µH ±15%
PIN 13-12	8.5 µH ±15%
RESISTANCE (*MEASURE D.C, TA 20°C*)	
PIN 6-2	651 mΩ MAX
PIN 9-8	320 mΩ MAX
PIN 17 -16	19.6 mΩ MAX
PIN 15 -14	19.7 mΩ MAX
PIN 13 -12	22 mΩ MAX
TRANSFORMER RATIO (*MEASURE 10KHZ*, WITH TOLERANCE ±0.5, *TA 20°C*)	
PIN 6-2 ⇔ 9-8	10.66 NOM
PIN 6-2 ⇔ 17-16	10.66 NOM
PIN 6-2 ⇔ 15-14	12 NOM
PIN 6-2 ⇔ 13-12	12 NOM
LEAKAGE INDUCTANCE (MEASURE 6-2 (8-9 AND 8÷18 IN S.C., F 10kHz, TA 20°C)	13.5 µH MAX
OPERATING CURRENT (MEASURE 6-2, PMAX 175W ,F 26kHz, TA 20°C)	3.8 A_p MAX
SATURATION CURRENT (MEASURE 6-2, BSAT 0.32T, TA 20°C)	4.6 A_p MAX
OPERATING FREQUENCY (P_{MAX} 175W , TA 20°C)	26 kHz MIN
PARASITIC CAPACITANCE (MEASURE 6-2, F_{Risk} 1.15MHz, TA 20°C)	16 pF NOM
AMBIENT TEMPERATURE RANGE (WITH SELF TRISE 45°C)	-20°C÷+85°C
THERMAL CLASS	B
STORAGE TEMPERATURE RANGE	-20°C÷+85°C
PRIMARY TO SECONDARY INSULATION (F 50HZ,DURATION TEST 2", TA 20°C)	4 kV
MAXIMUM DIMENSIONS	50X52.7 H40 mm
WEIGHT	160 g APPROX

PIN DESCRIPTION

PIN(*)	FUNCTION	PIN(*)	FUNCTION
1	NOT CONNECTED	10	NOT CONNECTED
2	PRIMARY +VB (400-1200VDCMAX)	11	
3	PRIMARY CENTER TAP	12	SECONDARY GROUND
4		13_A	SECONDARY CENTER TAP
5		14_A	
6	PRIMARY DRAIN	15_B	
7	PIN NOT PRESENT	16_B	SECONDARY GROUND
8	AUXILIARY GROUND	17	SECONDARY +48V 3.7A
9	AUXILIARY 15V 10mA	18	NOT CONNECTED

(*)PIN WITH THE SAME SUBSCRIPT MUST BE CONNECTED TOGETHER ON PCB

aq Magnetica Electromagnetic components Switch mode power supply

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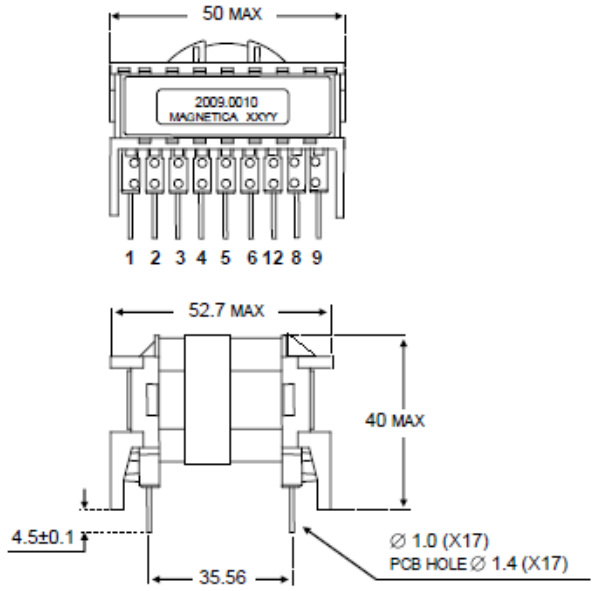
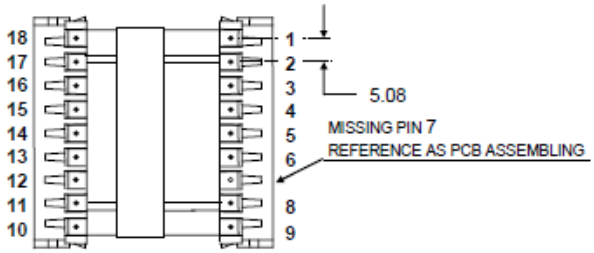
Figure 21. Dimensional drawing

	Product Technical Specification	Code : **08087**
	SMT 175W 26kHz 1.15mH 48V	Class Code : **2009.0010**
Date : 07.06.2016	Revision: 01	Page 2 of 2

DIMENSIONAL DRAWING

RoHS Compliant





BOTTOM VIEW (PIN SIDE)

DIMENSIONS IN MILLIMETERS, DRAWING NOT IN SCALE

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STP21 MOR&D0014 REV02 09/05/16

9 Revision history

Table 10. Document revision history

Date	Revision	Changes
29-Jan-2020	1	Initial release.