Application note

Migration guide from STM32F7 Series and STM32H743/753 line, to STM32H7A3/7B3 and STM32H7B0 Value line devices

Introduction

Designers of STM32 microcontroller applications must be able to easily replace one microcontroller type with another one from the same product family or from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill extended product requirements, extra demands on memory size, or an increased number of I/Os
- To meet cost reduction constraints that require a switch to smaller components and a shrunk PCB area

This application note analyzes the steps required to migrate applications from existing STM32F7 Series or STM32H743/753 line to STM32H7A3/7B3 line and STM32H7B0 Value line devices.

The STM32H743/753 line is named STM32H743/753 devices, and the STM32H7A3/7B3 line and STM32H7B0 Value line are named as STM32H7A3/7B0/7B3 device in this document.

This application note provides a guideline on both hardware and peripheral migration. To fully understand all the information provided by this application note, the user must be familiar with the STM32 microcontroller family.

For additional information, refer to the following documents available on *www.st.com*:

- STM32F75xxx and STM32F74xxx advanced Arm®-based 32-bit MCUs reference manual (RM0385)
- STM32F76xxx and STM32F77xxx advanced Arm®-based 32-bit MCUs reference manual (RM0410)
- STM32H743/753 advanced Arm®-based 32-bit MCUs reference manual (RM0433)
- STM32H7A3/B0/B3 advanced Arm®-based 32-bit MCUs reference manual (RM0455)

1 General information

This document applies to the STM32F7 Series , STM32H743/753 line and STM32H7A3/7B0/7B3 line devices Arm®-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 STM32H7A3/7B0/7B3 device overview

The maximum theoretical performance of the STM32H7A3/7B0/7B3 device Cortex® -M7 core is 1414 CoreMark / 599 DMIPS at 280 MHZ f_{CPU}. STM32H7A3/7B0/7B3 devices deliver this maximum theoretical performance by taking advantage of an L1-cache regardless if the code is executed from the embedded Flash or external memory.

Both STM32H743/753 and STM32H7A3/7B0/7B3 devices offers extra performance versus the STM32F7 Series devices without additional complexity.

STM32H743/753 and STM32H7A3/7B0/7B3 devices, as Cortex® -M7 variants, are compatible with the STM32F7 Series devices (for the common packages). This compatibility allows customers to easily migrate from STM32F7 Series devices towards STM32H7A3/7B0/7B3 devices and to benefit from their significantly higher performance and their advanced peripherals.

STM32H7A3/7B0/7B3 devices are also the entry point of the wider STM32H7 Series devices, which can be seen as an easy stepladder to benefit from the high performance, the rich connectivity and the enhanced features of this advanced platform.

STM32H7A3/7B0/7B3 devices include a larger set of peripherals with advanced features and optimized power consumption compared to STM32F7 Series devices such as:

- Low-power universal asynchronous receiver transmitter (LPUART)
- Single wire protocol master interface (SWPMI)
- FD controller area network (FDCAN)
- Operational amplifiers (OPAMP)
- Comparator (COMP)
- Voltage reference buffer (VREFBUF)
- Switch mode power supply step down converter (SMPS)

When compared to STM32H743/753 devices, STM32H7A3/7B0/7B3 devices offer the following additional features:

- Further optimized power consumption, significant in the low-power modes
- Simplification of the power domains
- Increased internal RAM size, very useful for graphics applications
- DFSDM increased to nine filters with dedicated DMA
- Two OCTOSPI interface, instead of a single QUADSPI
- Possibility to store encrypted code or data on external Octo-SPI memories (for STM32H7B3 devices)
- Graphical oriented memory management unit (GFXXMMU)
- New tampers and active tamper which increases the security level

This migration guide covers the migration from STM32F7 Series devices and STM32H743/753 devices towards STM32H7A3/7B0/7B3 devices.

The new features present on STM32H7A3/7B0/7B3 devices but not already present on STM32F7 Series devices or STM32H743/753 devices are not covered in this document. Refer to the STM32H7A3/7B0/7B3 device reference manual and datasheets for more details).

The migration from STM32F7 Series devices to STM32H743/753 devices is covered in detail in the application note Migration of microcontroller applications from STM32F7 Series devices to STM32H7x3 line microcontrollers (AN4936).

2.1 System architecture differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/H7B0/H7B3 devices

STM32F7 Series devices have one single available domain: an embedded AHB bus matrix.

In STM32H743/753 devices there are three domains: an AXI bus matrix and two AHB bus matrices. Bus bridges permit the interconnection of the bus masters with the bus slaves:

- **D1 domain**: is the high bandwidth / high performance domain with the Cortex-M7 core and acceleration mechanisms. This domain encompasses the high-bandwidth features and the smart management thanks to the AXI bus matrix.
- **D2 domain**: is the "I/O processing" domain. It encompasses most peripherals that are less bandwidth demanding.
- **D3 domain**: it embeds a 64-Kbyte RAM and has a subset of peripherals to run the basic functions while the domains 1 and 2 can be shut-off to save power (autonomous mode).

For the STM32H7A3/7B0/7B3 devices, the D1 and D2 domains are merged in a single domain called CD domain (or CPU domain) and the D3 domain evolved into a domain called SRD domain (or smart-run domain).

- **CD domain**: the CPU domain encompasses the Cortex-M7 core, the AXI bus matrix, an AHB bus matrix and most of the peripherals.
- **SRD domain**: it embeds a 32-Kbyte RAM and some peripherals to run basic functions while the CPU domain is in low-power mode (autonomous mode). For STM32H7A3/7B0/7B3 device the power consumption in autonomous and Stop modes of this domain has been further optimized.

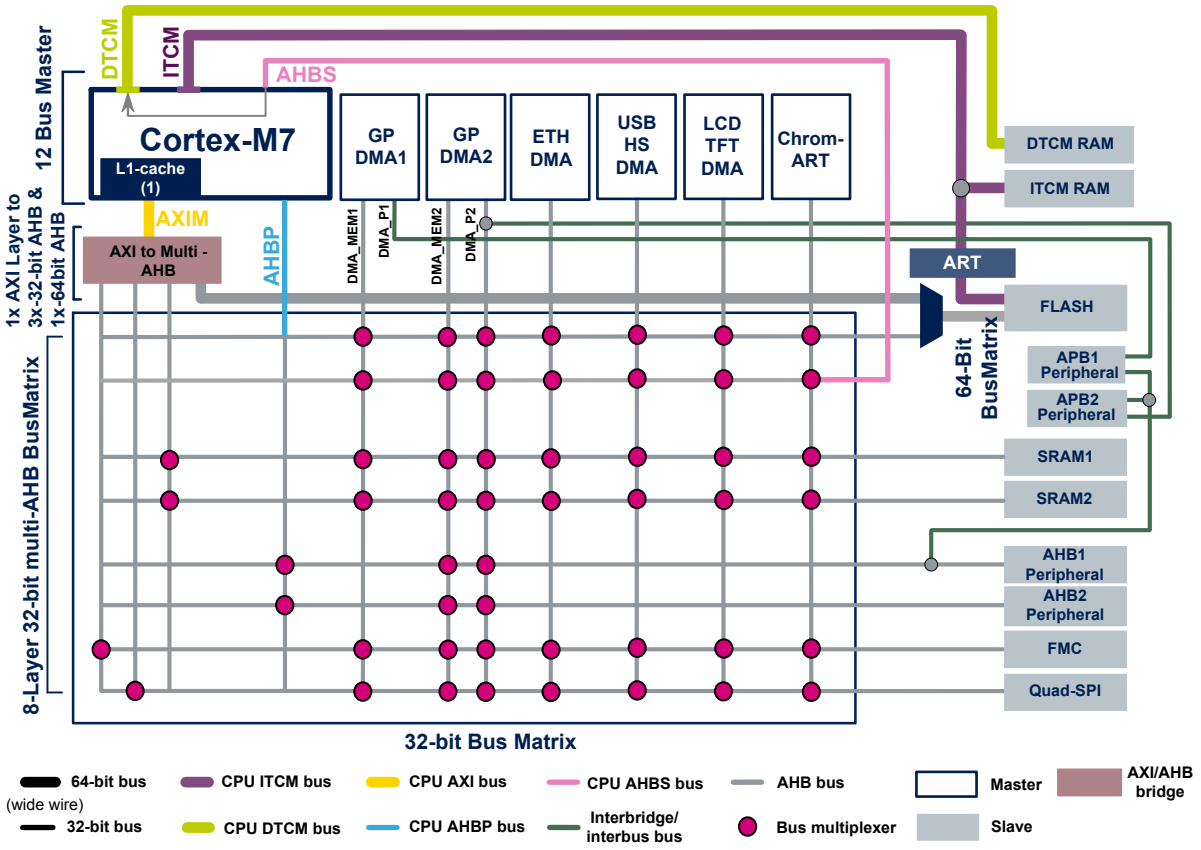
The differences in power modes are addressed on the Power (PWR) section of this application note.

The table below and the two subsequent figures illustrate the system architecture differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 1. Available bus matrix on STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Device	AHB bus matrix	AXI bus matrix
STM32F7 Series devices	1	NA
STM32H743/753 devices	2	1
STM32H7A3/7B0/7B3 devices	2	1

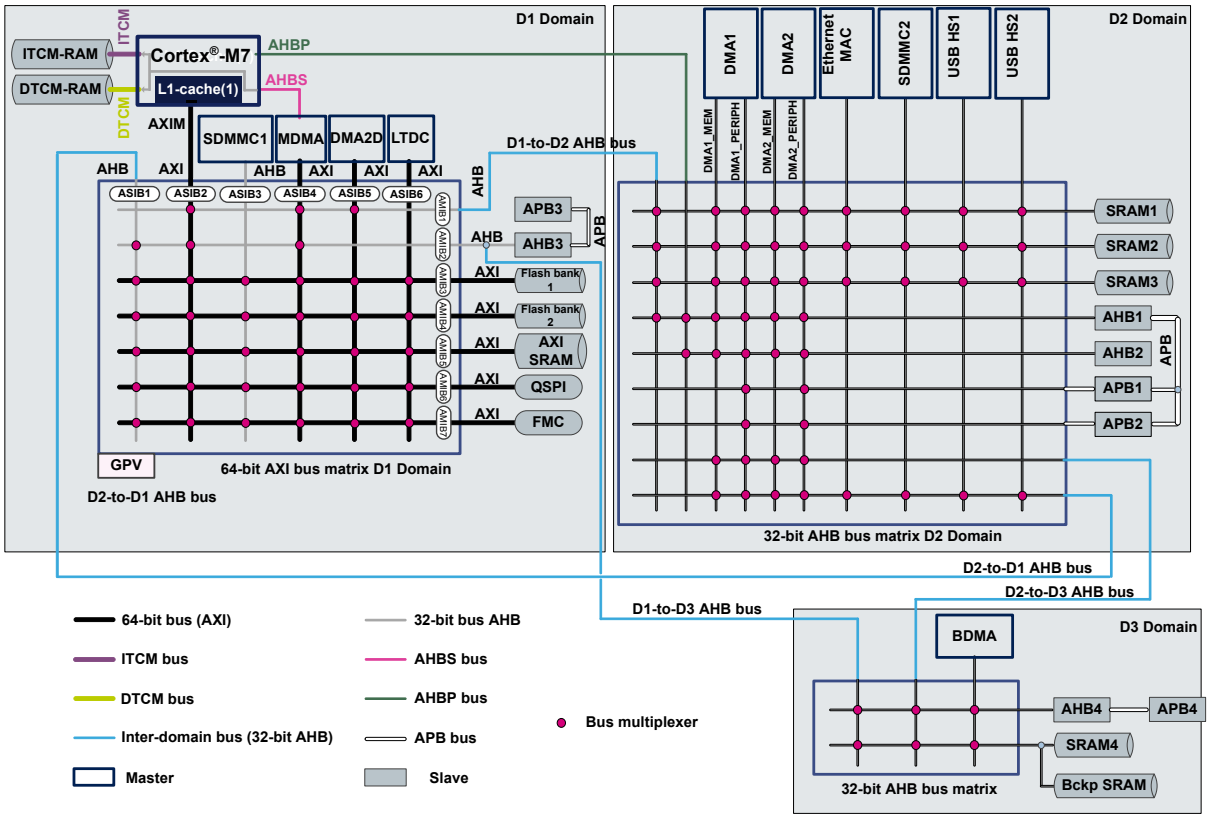
Figure 1. STM32F7 Series devices system architecture



Note: I/D cache size:

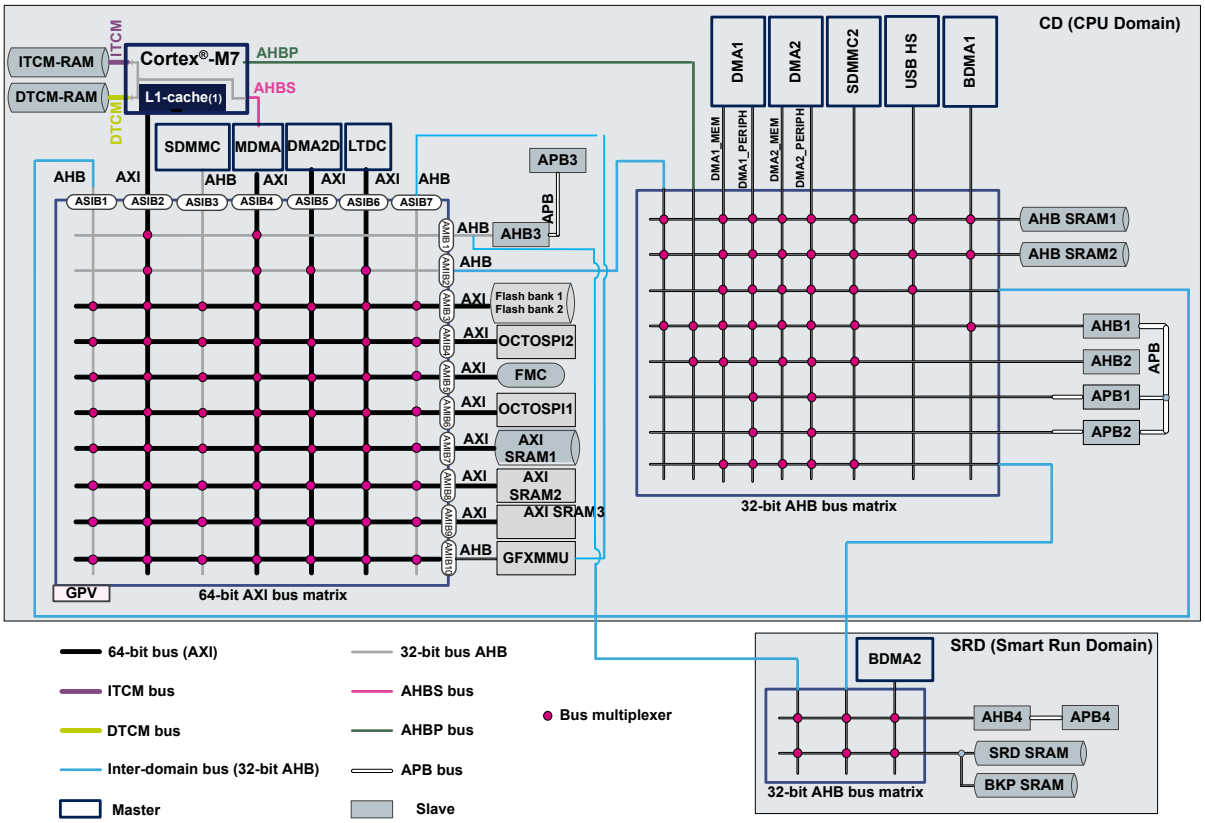
- *For STM32F74xxx and STM32F75xxx devices: 4 Kbytes.*
- *For STM32F72xxx and STM32F73xxx devices: 8 Kbytes.*
- *For STM32F76xxx and STM32F77xxx devices: 16 Kbytes.*

Figure 2. **STM32H743/753 device system architecture**



Note: STM32H743/753 devices supports 16-Kbyte instruction cache and 16-Kbyte data cache.

Figure 3. **STM32H7A3/7B0/7B3 device system architecture**



Note: STM32H7B0 supports a single bank (Flash Bank1 only)

3 Hardware migration

3.1 Available packages

The available packages on STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices are listed in the table below.

STM32H743/753 and STM32H7A3/7B0/7B3 devices support the switched mode power supply (SMPS) step-down converter available in some specific packages which are not compatible with the legacy packages (see table below and refer to Figure 5).

Table 2. Available packages on STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3

Package	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	Regulator
LQFP64	Available	NA	Available	LDO / regulator bypass
LQFP100		Available		
TFBGA100		NA		
WLCSP143			NA	
LQFP144		Available	Available	
UFBGA176+25				
LQFP176				
LQFP208			NA	
TFBGA216		NA	Available	
TFBGA240	NA	Available	NA	LDO / SMPS/ regulator bypass
LQFP100 SMPS		NA	Available	
TFBGA100 SMPS				
WLCSP132 SMPS				
LQFP144 SMPS		Available		
WLCSP156 SMPS			NA	
UFBGA169 SMPS			Available	
UFBGA176+25 SMPS				
LQFP176 SMPS				
LQFP208 SMPS			NA	
TFBGA225 SMPS		NA	Available	

3.2 Pinout compatibility

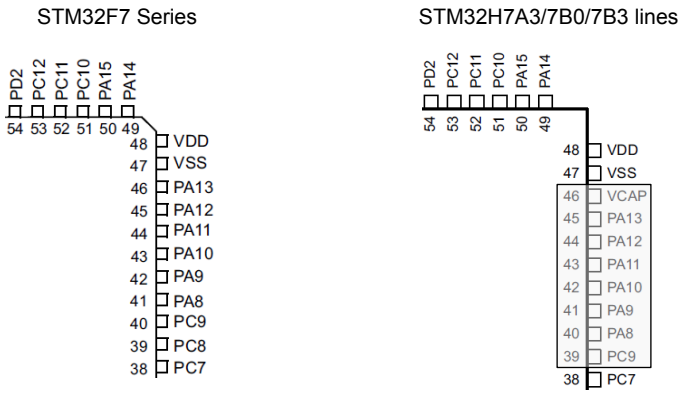
STM32F7 Series devices and STM32H743/753 devices are pin to pin compatible with the STM32H7A3/7B0/7B3 devices (with some restrictions for the LQFP64, TFBGA100, LQFP176, UFBGA176 and TFBGA216 packages).

In STM32H7A3/7B0/7B3 devices, a second VCAP pin is added for the LQFP64 package; in consequence, several GPIOs are no longer compatible with STM32F7 Series devices. See below table and figure for more details.

Table 3. LQFP64 package compatibility between STM32F7 Series devices and STM32H7A3/7B0/7B3 devices

Package	Pin	STM32F7 Series devices	STM32H7A3/7B0/7B3 devices
LQFP64	38	PC7	PC7
	39	PC8	PC9
	40	PC9	PA8
	41	PA8	PA9
	42	PA9	PA10
	43	PA10	PA11
	44	PA11	PA12
	45	PA12	PA13
	46	PA13	VCAP

Figure 4. LQFP64 package compatibility



For the TFBGA100, LQFP176, UFBGA176 and TFBGA216 packages, the BYPASS_REG pin is replaced in the STM32H7 Series with a VSS pin.

For the STM32F7 Series devices, the BYPASS_REG pin connected to VDD permits to select the mode where the internal regulator is switched off and the core supply is externally provided.

For the STM32H7 Series devices, there is no dedicated pin that defines if the regulator is in bypass mode or which regulator(s) is/are used. It is done through software at system startup. Both LDO and SMPS regulators are enabled by default during startup and the user software defines if the LDO or the SMPS or both are switched off (see Figure 5).

Note: Special care has to be taken if an STM32F7 Series device is replaced with an STM32H7A3/7B0/7B3 device on a PCB board where the BYPASS_REG pin is set to VDD (see the table below).

The following table and figure illustrate the BYPASS_REG pin incompatibility in TFBGA100, LQFP176, UFBGA176 and TFBGA216 packages and the system supply configuration on the STM32F7 Series devices and STM32H743/753 devices.

Table 4. BYPASS_REG pin incompatibility

Package	Pin/ball	STM32F7 Series devices	STM32H7A3/7B0/7B3 devices	Comment
TFGA100	Ball E6	BYPASS_REG	VSS	Impacts only the boards designed with STM32F7 Series devices in the regulator bypass mode (BYPASS_REG set to VDD)
LQFP176	Pin 48			
UFBGA176+25	Ball L4			
TFBGA216	Ball L5			

Figure 5. System supply configuration on STM32H743/753 and STM32H7A3/7B0/7B3 devices with SMPS

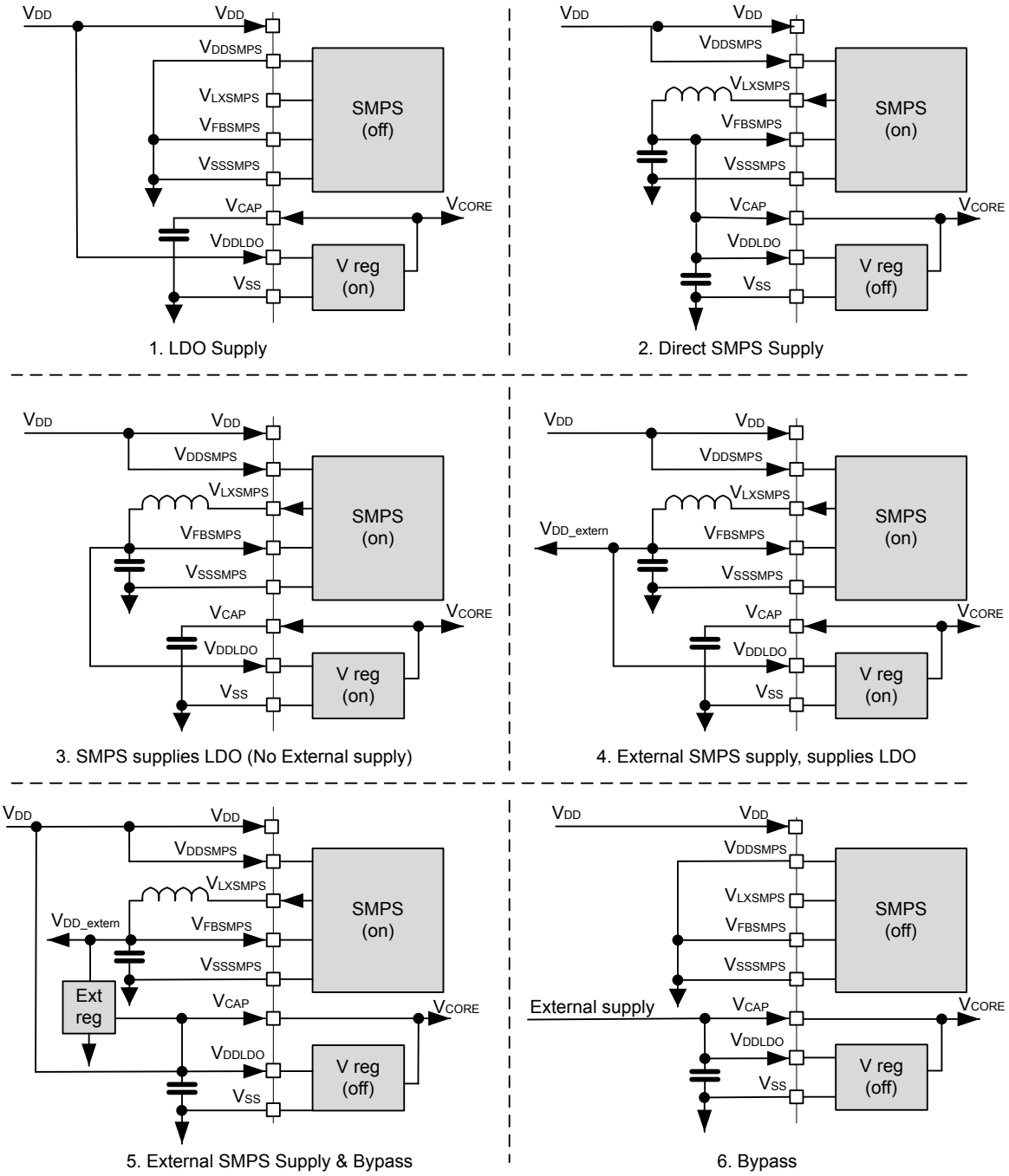
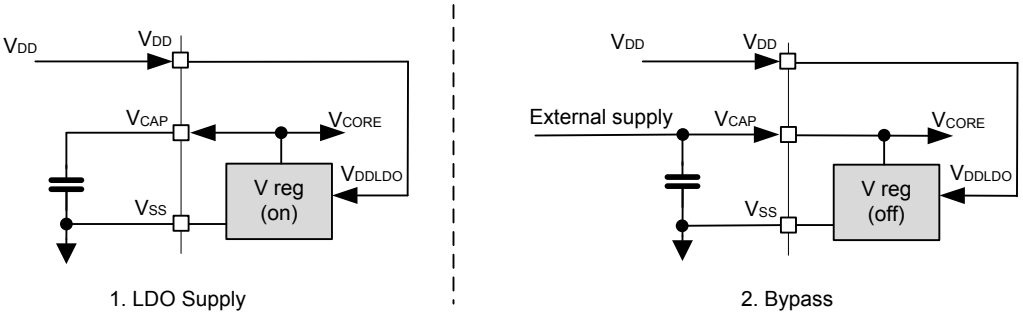


Figure 6. System supply configuration on STM32H743/753 and STM32H7A3/7B3/7B0 devices without SMPS



3.3 System bootloader

The system bootloader is located in the system memory, programmed by ST during production. The system bootloader permits to reprogram the Flash memory using one of the supported serial interfaces. More details are provided in the following table:

Table 5. STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices bootloader communication peripherals

System bootloader peripherals	STM32F7 Series I/O pin	STM32H743/753 I/O pin	STM32H7A3/7B0/7B3 I/O pin
DFU	USB OTG FS (PA11 / PA12) in device mode		
USART1	PA9 / PA10		
USART 2	NA	PA2 / PA3	
USART3	PB10 / PB11 PC10 / PC11	PB10 / PB11	PB10 / PB11 / PD9 / PD8
I2C1	PB6 / PB9		
I2C2	PF0 / PF1		
I2C3	PA8 / PC9		
SPI1	PA7 / PA6 / PA5 / PA4		
SPI2	PI3 / PI2 / PI1 / PI0		
SPI3	NA	PC12 / PC11/ PC10 / PA15	
SPI4	PE14 / PE13 / PE12 / PE11		
FDCAN1	PB5 / PB13(1) PD0 / PD1(2)	-	PH13 / PH14 / PD1 / PD0

1. *Available on the STM32F2xxx/73xxx devices.*
2. *Available on the STM32F74xxx/75xxx and STM32F76xxx/77xxx devices.*

4 Boot mode compatibility

The STM32F7 Series devices, the STM32H743/753 and the STM32H7A3/7B0/7B3 devices boot spaces are based on BOOT0 and boot address option bytes as described in the table below.

For the STM32F7 Series devices, the boot base address supports any address in the range from 0x0000 0000 to 0x3FFF FFFF while in STM32H743/753 and STM32H7A3/7B0/7B3 devices, the boot base address supports any address in the range from 0x0000 0000 to 0x3FFF 0000.

Table 6. Boot mode compatibility between STM32F7 Series devices and STM32H7xx lines

Boot mode selection		STM32F7 Series devices	STM32H743/753 STM32H7A3/7B0/7B3 devices
Boot	Boot address option bytes		
0	BOOT_ADD0[15:0]	Boot address defined by user option byte BOOT_ADD0[15:0] ST programmed value: Flash on ITCM at 0x0020 0000	Boot address defined by user option byte BOOT_ADD0[15:0] ST programmed value: Flash memory at 0x0800 0000
1	BOOT_ADD1[15:0]	Boot address defined by user option byte BOOT_ADD1[15:0] ST programmed value: System bootloader at 0x0010 0000	Boot address defined by user option byte BOOT_ADD1[15:0] ST programmed value: System bootloader at 0x1FF0 0000

5 Peripheral migration

5.1 STM32 product cross-compatibility

The STM32 microcontrollers embed a set of peripherals which can be classed in three categories:

- The first category is for the peripherals which are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals which are shared by all STM32 products but have only minor differences (in general to support new features), so the migration from one product to another is very easy and does not need any significant new development effort.
- The third category is for peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, the migration requires a new development at application level.

This table below shows the STM32 peripheral compatibility between the STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. The software compatibility mentioned in this table refers only to the register description for *low level* drivers. The Cube hardware abstraction layer (HAL) is compatible between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 7. Peripheral summary STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

<table>
<tr><th colspan="2">Peripheral</th><th>STM32F7 Series devices</th><th>STM32H743/753 devices</th><th colspan="2">STM32H7A3/7B0/7B3 devices</th><th>Compatibility/ comments</th></tr>
<tr><td colspan="2">Power supply</td><td>- Power supply for I/Os: 1.71 to 3.6 V
- Internal regulator VDD = 1.7 to 3.6 V</td><td colspan="3">- Power supply for I/Os: 1.62 to 3.6 V
- Internal regulator VDDLDO = 1.62 to 3.6 V
- SMPS step down converter
- VDDSMPS = 1.62 to 3.6 V</td><td>-</td></tr>
<tr><td colspan="2">Maximum frequency</td><td>216 MHz</td><td>480 MHz</td><td colspan="2">280 MHz</td><td>-</td></tr>
<tr><td colspan="2">MPU region number</td><td>8</td><td colspan="3">16</td><td>-</td></tr>
<tr><td colspan="2" rowspan="4">Flash</td><td rowspan="3">2 Mbytes</td><td rowspan="3">Up to 2M to 2Mbytes</td><td>2 Mbytes (2 x 1M)</td><td rowspan="2">Dual bank</td><td>STM32H7B3 / A3xI</td></tr>
<tr><td>1 Mbytes (2 x 512k)</td><td>STM32H7A3xG</td></tr>
<tr><td>128 Kbytes</td><td>Single bank</td><td>STM32H7B0</td></tr>
<tr><td colspan="3">- Single bank
- Dual bank</td><td>• Mapped on AXI bus
• With ECC protection in STM32H743/753 and STM32H7A3/7B0/7B3 devices</td></tr>
<tr><td rowspan="3">SRAM</td><td>System</td><td>512 Kbytes</td><td>~1 Mbyte
(992 Kbytes)</td><td colspan="2">~1.3 Mbytes
(1312 Kbytes)</td><td rowspan="3">With ECC protection in STM32H743/753 devices
ECC protection only on TCM and Cache in STM32H7A3/B0/B3 devices</td></tr>
<tr><td>Instruction</td><td>16 Kbytes</td><td colspan="3">64 Kbytes</td></tr>
<tr><td>Backup</td><td colspan="4">4 Kbytes</td></tr>
<tr><td rowspan="2">Common peripherals</td><td>FMC</td><td colspan="4">1</td><td>Mapped on AXI bus</td></tr>
<tr><td>QUADSPI</td><td colspan="2">1</td><td colspan="2">NA</td><td>Mapped on AXI bus</td></tr>
</table>

Peripheral		STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	Compatibility/ comments
Common peripherals	OCTOSPI	NA		2[1]	Mapped on AXI bus All features of the QUADSPI are covered by the OCTOSPI
	Ethernet	1		NA	Wakeup from Stop capability
Timers	High resolution	NA	1	NA	-
	General purpose	10			-
	PWM	2			-
	Basic	2			-
	Low-power	1	5	3	Wakeup from Stop capability
RNG		Yes			-
Communication interfaces	SPI/I2S	4/3	6/3	6/4	Wakeup from Stop capability in STM32H743/753 devices and STM32H7A3/7B0/7B3 devices
	I2C	4			Wakeup from Stop capability in STM32H743/753 devices and STM32H7A3/7B0/7B3 devices
	USART	4		5	Wakeup from Stop capability in STM32H743/753 devices and STM32H7A3/7B0/7B3 devices
	UART	4		5	Wakeup from Stop capability in STM32H743/753 devices and STM32H7A3/7B0/7B3 devices
	LPUART	NA	1		New feature
	SAI	2	4	2	PDM interface supporting up to eight microphones in STM32H743/753 devices and 4 microphones in STM32H7A3/7B0/7B3 devices
	SPDIFRX	4 inputs			-
	SWPMI	NA	1		New feature
	MDIO	1			Wakeup from Stop capability
	SDMMC	2			• With DMA capability

Peripheral		STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	Compatibility/ comments
Communication interfaces					• Wakeup from Stop • eMMC boot support
	CAN	x3 CANs (2.0B Active)	x2 CAN FD (FDCAN1 supports TTCAN)		New feature
	USB OTG FS	1		NA	With DMA capability
	USB OTG HS	1			• Supports FS and HS with ULPI • With DMA capability
	HDMI-CEC	1			Wakeup from Stop capability
	DFSDM number of filters	1		2	-
		4		8/1	• One DFSDM with 8 filters • One DFSDM with 1 filter
Digital camera interface		1			-
MIPI-DSI host		1	1	NA	Available only for some packages
Graphics	LCD-TFT	1			-
	Chrom-ART Accelerator™ (DMA2D)	1			YCbCr to RGB color space conversion on STM32H743/753 devices and STM32H7A3/7B0/7B3 devices
	JPEG Codec	1			-
	GFXMMU	NA		1	Graphical oriented memory management unit
GPIOs		Up to 159	Up to 168		IO posts with interrupt capability
Analog peripherals	ADC	- Power supply: 1.7 V to 3.6 V - x3 (8- to 12-bit) number of channels: up to 24	Power supply: 1.62 V to 3.6 V - x3 (8- to 12-bit) number of channels: up to 36	Power supply: 1.62 V to 3.6 V - x2 (8- to 12-bit) number of channels: up to 24	VREF+ can be either externally provided or provided through the internal VREFBUF regulator
	12-bit DAC	2 channels		3 channels	
	Operational amplifiers	NA	2		-
	Ultra-low-power comparator	NA	2		-

Peripheral		STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	Compatibility/ comments
DMA		General purpose DMA: 16-stream DMA controller with FIFOs and burst support	4 DMA controllers to unload the CPU - x1 high-speed general-purpose master direct memory access controller (MDMA) - x2 dual-port DMAs with FIFO and request router capabilities for optimal peripheral management - x1 basic DMA with request router capabilities	5 DMA controllers to unload the CPU - x1 high-speed general-purpose master direct memory access controller (MDMA) - x2 dual-port DMAs with FIFO and request router capabilities for optimal peripheral management - x1 basic DMA with request router capabilities - x1 basic DMA dedicated to the DFSDM	• No limitation for peripheral requests thanks to DMAMUX • DMA1 and DMA2 can access to peripherals in APB1/APB2 buses • Peripheral request mapping is no longer managed by the DMA controller but by the DMAMUX controller
Cryptographic acceleration		- AES 128, 192, 256, DES/TDES - HASH (MD5, SHA-1, SHA-2); HMAC - True random number generator			32-bit true random numbers, produced by an analog entropy source conditioned with block cipher AES-CBS
Security	ROP	ROP	ROP, PC-ROP Two secure-only areas (one per Flash bank)		STM32H7B0 devices support only one secure area (single bank device)
	Tamper	NA	Tamper	Active tamper	Active tamper improves the tamper security

1. *OctoSPI is not supported for the LQFP64 and LQFP100-SMPS packages (limited to Quad). OctoSPI2 is not supported on all packages and for some packages only in multiplexed mode (see datasheet)*

5.2 Memory organization

5.2.1 RAM size

The following table illustrates the difference of RAM size between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 8. Comparison of RAM size between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Memory	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	Units
ITCM-RAM	16	64	64	Kbyte
DTCM-RAM	128	128	128	
AXI-SRAM	-	512	1024 (split in 3 SRAMs)	
SRAM1	368	128	64 (AHB_SRAM1)	
SRAM2	16	128	64 (AHB_SRAM2)	
SRAM3	NA	32	NA	
SRAM4	NA	64	32 (SRD_SRAM)	
Backup SRAM	4	4	4	
Total	532	1060	1380	

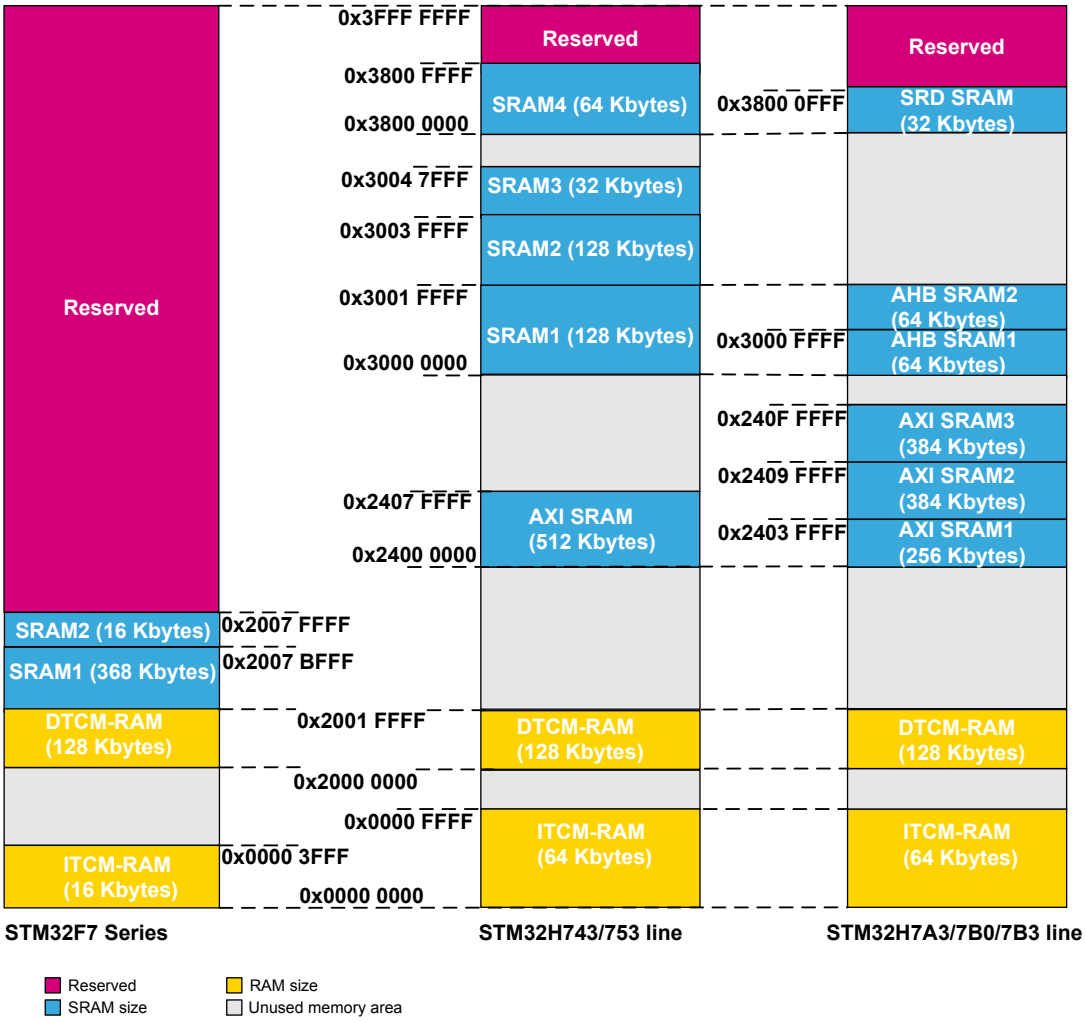
5.2.2 Memory map and peripherals register boundary addresses

The table and figure below illustrate the memory addresses between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 9. Memory organization and compatibility between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

<table>
<tr><th>Memory</th><th>STM32F7 Series devices</th><th>STM32H743/753 devices</th><th>STM32H7A3/7B0/7B3 devices</th><th>Comments</th></tr>
<tr><td>ITCM-RAM</td><td>0x0000 0000 – 0x0000 3FFF</td><td colspan="2">0x0000 0000 – 0x0000 FFFF</td><td>-</td></tr>
<tr><td>DTCM-RAM</td><td colspan="3">0x2000 0000 – 0x2001 FFFF</td><td>-</td></tr>
<tr><td rowspan="9">FLASH</td><td rowspan="8">• Flash bank 1
0x0800 000 - 0x080F FFFF
• Flash bank 2
0x0810 0000 - 0x081F FFFF</td><td colspan="2">Flash bank 1</td><td>-</td></tr>
<tr><td colspan="2">0x0800 0000 – 0x080F FFFF</td><td>STM32H7B3/ H7A3xI</td></tr>
<tr><td colspan="2">0x0800 0000 – 0x0807 FFFF</td><td>STM32H7A3xG</td></tr>
<tr><td colspan="2">0x0800 0000 – 0x0801 FFFF</td><td>STM32H7B0</td></tr>
<tr><td colspan="2">Flash bank 2</td><td>-</td></tr>
<tr><td colspan="2">0x0810 0000 – 0x081F FFFF</td><td>STM32H7B3/ H7A3xI</td></tr>
<tr><td colspan="2">0x0810 0000 – 0x0817 FFFF</td><td>STM32H7A3xG</td></tr>
<tr><td colspan="2">-</td><td>STM32H7B0</td></tr>
<tr><td>Flash - ITCM
0x0020 0000 – 0x002FF FFFF</td><td colspan="2">NA</td><td>-</td></tr>
<tr><td rowspan="2">System memory</td><td>0x1FF0 0000 – 0x1FF0 EDBF</td><td>• Bank 1
0x1FF0 0000 – 0x1FF1 FFFF
• Bank 2
0x1FF4 0000 – 0x1FF5 FFFF</td><td>• Bank 1
0x1FF0 0000 – 0x1FF0 FFFF
• Bank 2
0x1FF1 0000 – 0x1FF1 FFFF</td><td>-</td></tr>
<tr><td>0x0010 0000 – 0x0010 EDBF</td><td colspan="2">NA</td><td>-</td></tr>
</table>

Figure 7. RAM memory organization of STM32F7 Series devices, STM32H743/753 and STM32H7A3/B0/B3 devices



Note: DTCM-RAM size:

- *128 Kbytes STM32F76xxx, STM32F77xxx and STM32H743/753 and STM32H7A3/7B0/7B3 devices*
- *64 Kbytes for the STM32F75xxx and STM32F74xxx devices*

5.2.3 Peripheral register boundary addresses

The peripheral address mapping has been changed for most of peripherals in the STM32H743/753 and STM32H7A3/7B0/7B3 devices versus the STM32F7 Series devices.

For more details about registers boundary addresses differences refer to Memory map and register boundary addresses section of RM0410, RM0385, RM0433 and RM0455 reference manuals.

Table 10 shows the detail of all the peripherals address mapping differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 10. Examples of peripheral address mapping differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Peripheral	STM32F7 Series devices		STM32H743/753 devices		STM32H7A3/7B0/7B3 devices	
	Bus	Base address	Bus	Base address	Bus	Base address
QUADSPI control	AHB3	0xA000 1000 - 0xA000 1FFF	AHB3	0x5200 5000 - 0x5200 5FFF	NA	
GPIOA	AHB1	0x4002 0000 - 0x4002 03FF	AHB4 (D3)	0x5802 0000 - 0x5802 03FF	AHB4 (SRD)	0x5802 0000 - 0x5802 03FF
RCC		0x40023800 - 0x40023BFF		0x58024400 - 0x580247FF		0x5802 4400 - 0x5802 47FF
DFSDM2	NA					0x5800 6C00 - 0x5800 73FF
DTS	NA					0x5800 6800 - 0x5800 6BFF
RTC and Backup reg	AHB1	0x4000 2800 - 0x4000 2BFF	AHB4 (D3)	0x5800 4000 - 0x5800 43FF	NA	
Tamp and Backup reg	NA				AHB4 (SRD)	0x5800 4400 - 0x5800 47FF
RTC3	NA					0x5800 4000 - 0x5800 43FF
DAC2	NA					0x5800 3400 - 0x5800 37FF
GFXMMU	NA				AHB3	0x5200 C000 - 0x5200 EFFF
OTFDEC2	NA					0x5200 BC00 - 0x5200 BFFF
OTFDEC1	NA					0x5200 B800 - 0x5200 BBFF
OTCOSPI I/O manager	NA					0x5200B400 - 0x5200B7FF
Delay block OCTOSPI2	NA					0x5200 B000 - 0x5200 B3FF
OCTOSPI2	NA				AHB3	0x5200 A000 - 0x5200 AFFF
Delay block OCTOSPI1	NA					0x5200 6000 - 0x5200 63FF
OCTOSPI1	NA					0x5200 5000 - 0x5200 5FFF
QUADSPI	AHB3	0xA000 1000 - 0xA000 1FFF	AHB3	0x5200 5000 - 0x5200 5FFF	NA	
BDMA1	NA				AHB2	0x48022C00 - 0x48022FFF
HSEM	NA		AHB4	0x58026400 - 0x580267FF		0x48020800 - 0x4802 0BFF
PSSI	NA					
CRC	AHB1	0x4002 3000 - 0x4002 33FF	AHB4 (D3)	0x5802 4C00 - 0x5802 4FFF	AHB1	0x4002 3000 - 0x4002 33FF
DFSDM1	APB2	0x4001 7400 - 0x4001 77FF	APB2	0x4001 7000 - 0x4001 73FF	APB2	0x4001 7800 - 0x4001 7FFF
USART10	NA					0x4001 1C00 - 0x4001 1FFF
UART9	NA					0x4001 1800 - 0x4001 1BFF

5.3 Flash memory

Table 11 presents the differences of the Flash memory interface between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

The STM32H7 Series devices instantiate a different Flash module both in terms of architecture and interface. For more information on programming, erasing and protection of STM32H743/753 and STM32H7A3/7B0/7B3 Flash memory, refer to STM32H743/753 reference manual (RM0433) and STM32H7A3/7B0/7B3 reference manual (RM0455).

Table 11. Flash memory differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Flash	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Mapping	AHB	AXI	AXI
Flash address	• STM32F76xxx/STM32F77xxx *Flash - AXI* 0x0800 0000 – 0x081F FFFF • STM32F746xx/STM32F756xx *Flash - AXI* 0x0800 0000 – 0x080F FFFF	• Flash bank 1 0x0800 0000 – 0x080F FFFF • Flash bank 2 0x0810 0000 – 0x081F FFF	
	• STM32F76xxx/STM32F77xxx *Flash – ITCM* 0x0020 0000 – 0x003F FFFF • STM32F746xx/STM32F756xx *Flash – ITCM* 0x0020 0000 – 0x002FF FFFF	NA	
Main / program memory	• STM32F76xxx/STM32F77xxx – Up to 2 Mbytes (single/dual bank) – Single bank: up to 256-Kbyte sector size – Dual bank: up to 128-Kbyte sector size • STM32F746xx/STM32F327F56xx – Up to 1 Mbyte (single bank) – Up to 256-Kbyte sector size	Up to 2 Mbytes (dual bank) 128-Kbyte size sector	Up to 2 Mbytes (dual bank) 8-Kbyte size sector
	Programming granularity: 64 bits Flash line width: 256 bits or 128 bits	Programming granularity: 256 bits Flash line width: 256 bits	Programming granularity: 128 bits Flash line width: 128 bits
Wait state	Up to 9 (depending on the supply voltage and frequency)	Up to 4 (depending on the core voltage and frequency)	Up to 6 (depending on the core voltage and frequency)
Option bytes	32 bytes	2 Kbytes	2 Kbytes
OTP	1024 bytes	NA	1024 bytes
Features	STM32F76xxx/STM32F77xxx • Read while write (RWW) • Supports dual boot mode • Sector, mass erase and bank mass erase (only in Dual-bank mode)	• Error code correction (ECC) • Double-word, word, half-word and byte read / write operations • Sector erase, bank erase and mass erase • Dual-bank organization supporting simultaneous operations: two read/program/erase operations can be executed in parallel on the two banks • Bank swapping: the address mapping of the user Flash memory of each bank can be swapped.	
Protection mechanisms	Readout protection (RDP)		
	NA	• 2 PCROP protection area (1 per bank, execute-only memory) • 2 secure area in user Flash memory (1 per bank)	
		Sector write protection 128-Kbyte sectors	Sector write protection 32-Kbyte sectors

5.4 Nested vectored interrupt controllers (NVIC)

The table below presents the interrupt vector differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 12. Interrupt vector differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Position	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
3	RTC_WKP	RTC_TAMP_STAMP_CSS_LSE	
18	ADC	ADC1_2	
19	CAN1_TX	FDCAN1_IT0	
20	CAN1_RX0	FDCAN2_IT0	
21	CAN1_RX1	FDCAN1_IT1	
22	CAN1_SCE	FDCAN2_IT1	
24	TIM1_BRK_TIM9	TIM1_BRK	
25	TIM1_UP_TIM10	TIM1_UP	
26	TIM1_TRG_COM_TIM11	TIM1_TRG_COM	
42	OTG_FS WKUP	Reserved	DFSDM2
61	ETH	ETH	Reserved
62	ETH_WKUP	ETH_WKUP	Reserved
63	CAN2_TX	FDCAN_CAL	
64	CAN2_TX	Reserved	DFSDM1_FLT4 (filter 4)
65	CAN2_RX1	Reserved	DFSDM1_FLT5 (filter 5)
66	CAN2_SCE	Reserved	DFSDM1_FLT6 (filter 6)
67	OTG_FS	Reserved	DFSDM1_FLT7 (filter 7)
81	-	FPU	
92	QUADSPI	QUADSPI	OCTOSPI
97	Reserved	SPDIFRX	
98	DSIHOST	OTG_FS_EP1_OUT	Reserved
99	DFSDM1_FLT1	OTG_FS_EP1_IN	Reserved
100	DFSDM1_FLT2	OTG_FS_WKUP	Reserved
101	DFSDM1_FLT3	OTG_FS	Reserved
102	DFSDM1_FLT4	DMAMUX1_OV	
103	SDMMC2	HRTIM1_MST	Reserved
104	CAN3_TX	HRTIM1_TIMA	Reserved
105	CAN3_RX0	HRTIM_TIMB	Reserved
106	CAN3_RX1	HRTIM1_TIMC	Reserved
107	CAN3_SCE	HRTIM1_TIMD	Reserved
108	JPEG	HRTIM_TIME	Reserved
109	MDIOS	HRTIM1_FLT	Reserved
110	NA	DFSDM1_FLT0 (filter 0)	
111		DFSDM1_FLT1 (filter 1)	

Position	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
112	NA	DFSDM1_FLT2 (filter 2)	
113		DFSDM1_FLT3 (filter 3)	
114	NA	SAI3	Reserved
115	NA	SWPMI1	
116		TIM15	
117		TIM16	
118		TIM17	
119		MDIO_WKUP	
120		MDIO	
121		JPEG	
122		MDMA	
123	NA	DSI/DSI_WKUP	Reserved
124	NA	SDMMC2	
125		HSEM0	
127	NA	ADC3	DAC2
128	NA	DMAMUX2_OVR	
129		BDMA_CH1	
130		BDMA_CH2	
131		BDMA_CH3	
132		BDMA_CH4	
133		BDMA_CH5	
134		BDMA_CH6	
135		BDMA_CH7	
136		BDMA_CH8	
137		COMP	
138		LPTIM2	
139		LPTIM3	
140	NA	LPTIM4	UART9
141		LPTIM5	USART10
142	NA	LPUART1	
143	NA	WWDG1_RST	Reserved
144	NA	CRS	
145		ECC	
146	NA	SAI4	Reserved
147		Reserved	TEMP_IT
148		Reserved	Reserved
149	NA	WKUP	

5.5 Extended interrupt and event controller (EXTI)

5.5.1 EXTI main features in STM32H7A3/7B0/7B3 devices

The extended interrupt and event controller (EXTI) manages wakeup through configurable and direct event inputs. It provides wakeup requests to the power control, it generates interrupt requests to the CPU NVIC and to the SRD domain DMAMUX2. It also generates events to the CPU event input.

The asynchronous event inputs are classified in two groups:

- Configurable events (active edge selection, dedicated pending flag, triggerable by software)
- Direct events (interrupt and wakeup sources from other peripherals, requiring to be cleared in the peripheral) with the following features:
  - Fixed rising edge active trigger
  - No interrupt pending status register bit in the EXTI (the interrupt pending status is provided by the peripheral generating the event)
  - Individual interrupt and event generation mask
  - No SW trigger possibility
  - Direct system SRD domain wakeup events, that have a SRD pending mask and status register and may have a SRD interrupt signal

The table below describes the difference of EXTI event input types between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

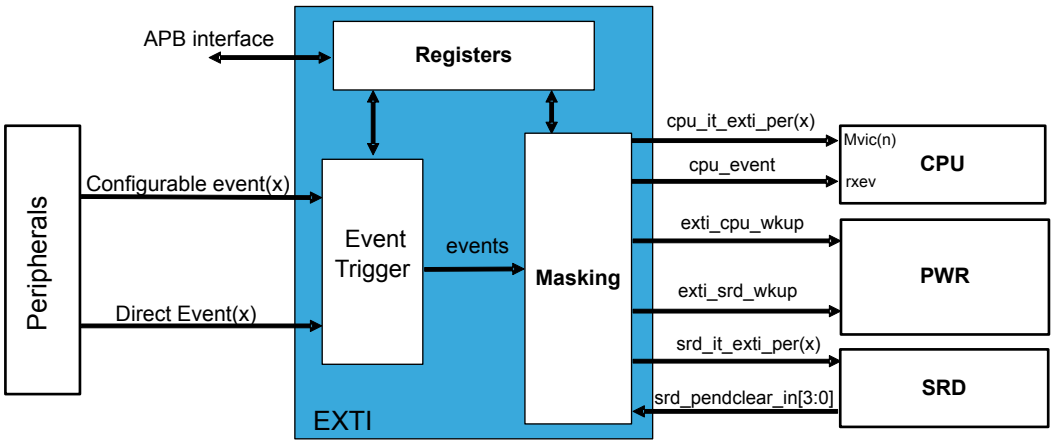
Table 13. EXTI event input types differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Main Features	STM32F7 Series devices	STM32H743/753 and STM32H7A3/7B0/7B3 devices
Configurable events	Available	Available
Direct events	-	Available

5.5.2 EXTI block diagram in STM32H7A3/7B0/7B3 devices

As shown in Figure 8, the EXTI consists of a register block accessed via an APB interface, an event input trigger block, and a masking block. The register block contains all the EXTI registers. The event input trigger block provides an event input edge triggering logic.

Figure 8. EXTI block diagram on STM32H7A3/7B0/7B3 devices



Note: For more details about EXTI functional description and registers description, refer to RM0455.

The table below presents the EXTI line differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 14. EXTI line differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

EXTI line	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	Event input type
		Source	Source	
0 - 15	EXTI[15:0]	EXTI[15:0]		Configurable
16	PVD output	PVD and AVD		Configurable
17	RTC alarm event	RTC alarms		Configurable
18	USB OTG FS wakeup event	RTC tamper, RTC timestamp, RCC LSECSS		Configurable
19	Ethernet wakeup event	RTC wakeup timer		Configurable
20	USB OTG HS (configured in FS) wakeup event	COMP1		Configurable
21	RTC tamper and time stamp events	COMP2		Configurable
22	RTC wakeup event	I2C1 wakeup		Direct
23	LPTIM1 asynchronous event	I2C2 wakeup		Direct
24	MDIO slave asynchronous interrupt	I2C3 wakeup		Direct
25	NA	I2C4 wakeup		Direct
26		USART1 wakeup		Direct
27		USART2 wakeup		Direct
28		USART3 wakeup		Direct
29		USART6 wakeup		Direct
30		UART4 wakeup		Direct
31		UART5 wakeup		Direct
32		UART7 wakeup		Direct
33		UART8 wakeup		Direct
34	NA	LPUART1 RX wakeup		Direct
35		LPUART1 TX wakeup		Direct
36	NA	SPI1 wakeup		Direct
37		SPI2 wakeup		Direct
38		SPI3 wakeup		Direct
39		SPI4 wakeup		Direct
40		SPI5 wakeup		Direct
41		SPI6 wakeup		Direct
42		MDIO wakeup		Direct
43		USB1 wakeup		Direct
44	NA	USB2 wakeup	Reserved	Direct
47	NA	LPTIM1 wakeup		Direct
48		LPTIM2 wakeup		Direct
49		LPTIM2 output		Configurable

EXTI line	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	Event input type
		Source	Source	
50	NA	LPTIM3 wakeup		Direct
51		LPTIM3 output		Configurable
52	NA	LPTIM4 wakeup	UART9 wakeup	Direct
53		LPTIM5 wakeup	USART10 wakeup	Direct
54	NA	SWPMI wakeup		Direct
55		WKUP1		Direct
56		WKUP2		Direct
57		WKUP3		Direct
58		WKUP4		Direct
59		WKUP5		Direct
60		WKUP6		Direct
61		RCC interrupt		Direct
62		I2C4 Event interrupt		Direct
63		I2C4 Error interrupt		Direct
64		LPUART1 global Interrupt		Direct
65		SPI6 interrupt		Direct
66	NA	BDMA CH0 interrupt	BDMA2 CH0 interrupt	Direct
67		BDMA CH1 interrupt	BDMA2 CH1 interrupt	Direct
68		BDMA CH2 interrupt	BDMA2 CH2 interrupt	Direct
69		BDMA CH3 interrupt	BDMA2 CH3 interrupt	Direct
70		BDMA CH4 interrupt	BDMA2 CH4 interrupt	Direct
71		BDMA CH5 interrupt	BDMA2 CH5 interrupt	Direct
72		BDMA CH6 interrupt	BDMA2 CH6 interrupt	Direct
73		BDMA CH7 interrupt	BDMA2 CH7 interrupt	Direct
74	NA	DMAMUX2 interrupt		Direct
75	NA	ADC3 interrupt	Reserved	Direct
76		SAI4 interrupt	Reserved	Direct
85	NA	HDMICEC wakeup		Configurable
86	NA	ETHERNET wakeup	Reserved	Configurable
87	NA	HSECSS interrupt		Direct
88	NA	Reserved	TEMP wakeup	Direct

Note: For more details about EXTI events input mapping, refer to EXTI event input mapping section of RM0433 and RM0455 reference manuals.

5.6 Reset and clock control (RCC)

5.6.1 Clock management

The table below presents the source clock differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 15. Different source clock in STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Source clock		STM32F7 Series devices	STM32H7A3/7B0/7B3 and STM32H743/753 devices
Internal oscillators	HSI	16 MHz	64 MHz
	HSI48	NA	48 MHz
	CSI	NA	4 MHz
	LSI	32 kHz	40 kHz
External oscillators	HSE	4-26 MHz	4-50 MHz
	LSE	32.768 kHz	
PLLs(1)		x3 without fractional mode	x3 with fractional mode (13-bit fractional multiplication factor)

1. *Special care to be taken for the PLL configuration:*
   - *STM32H743/H753: the PLL VCO max frequency is 836 MHz*
   - *STM32H7A3/H7B3: the PLL VCO max frequency is 560 MHz*

5.6.2 Peripheral clock distribution

The peripheral clocks are the clocks provided by the RCC to the peripherals. Two kinds of clocks are available:

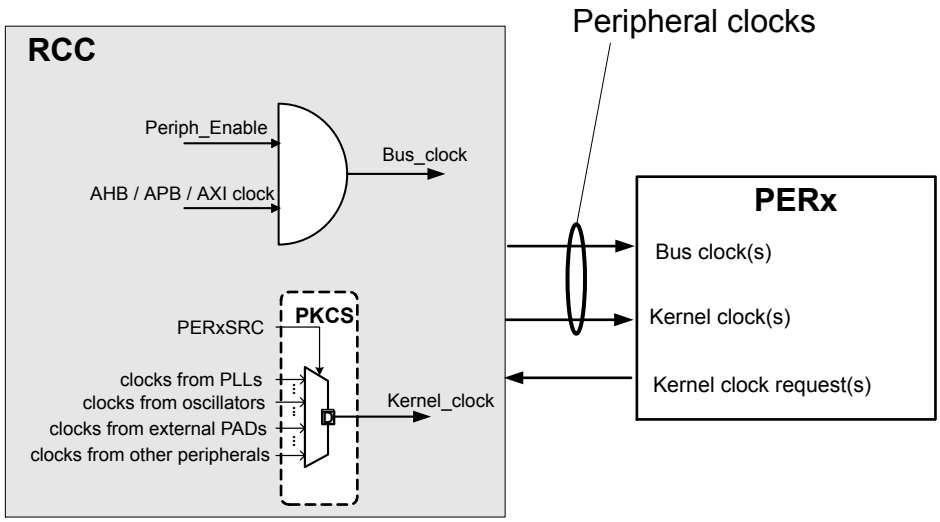
- The bus interface clocks
- The kernel clocks

On STM32H743/753 and STM32H7A3/7B0/7B3 devices, the peripherals generally receive:

- One or several bus clocks.
- One or several kernel clocks.

Figure 9 describes the peripheral clock distribution on the STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Figure 9. Peripheral clock distribution STM32H743/753 and STM32H7A3/7B0/7B3 devices



The following table describes an example of peripheral clock distribution for STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

For more details about the kernel peripheral clock distribution, refer to Kernel clock distribution overview table of RM0455 and RM0433 reference manuals

Table 16. Peripheral clock distribution example

Peripheral	STM32F7 Series devices	STM32H743/753 devices STM32H7A3/7B0/7B3 devices
SPI1	**APB2_Clock**	• Bus clock APB2_Clock • Kernel clock Pll1_q_ck/Pll2_p_ck/Pll3_p_ck/I2S_CKIN/ Per_ck
USART1	• Bus clock APB2_Clock • Kernel clock – LSE – HSI – SYSCLK – PCLK2	• Bus clock APB2_Clock • Kernel clock Pll2_q_ck/pll3_q_ck/hsi_ker_ck/csi_ker_ck/lse_ck

5.7 Operating conditions

The table below illustrates the maximum operating frequency of STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 17. General operating conditions for STM32F7 Series devices, STM32H7A3/7B0/7B3 and STM32H743/753 devices

Scale	STM32F7 Series devices maximum frequency	STM32H743/753 devices maximum frequency		STM32H74A3/7B0/7B3 devices maximum frequency		Unit
		Max CPU	Max D1/D2/D3	Max CPU	Max CD/SRD	
Scale 0	NA	480	240	280	280	MHz
Scale 1	216	400	200	225	225	
Scale 2	180	300	160	160	160	
Scale 3	144	200	88	88	88	

6 Power (PWR)

The table below presents the PWR controller differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. Both dynamic and static power-consumption had been optimized for the STM32H7A3/7B0/7B3 devices.

Table 18. PWR differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

PWR		STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Low-power modes	Autonomous mode (basic operation with inactive CPU domain(s) in low-power mode)	NA	D3 in Run mode	SRD in Run mode
			D1/D2 in DStop	CD in DStop
			NA	CD in DStop with RAM Shut-off(1)
			D1/D2 in DStandby	NA
			NA	CD in DStop2 (retention mode) with/without RAM Shuf-off(1)
	Stop	Stop	D3 in DStop	SRD in DStop
			D1/D2 in DStop	CD in DStop
		NA	NA	CD in DStop with RAM Shut-off(1)
			D1/D2 in DStandby	NA
			NA	CD in DStop2 (retention mode) with/without RAM Shuf-off(1)
Power supplies	External power supply for I/Os	VDD = 1.7 to 3.6 V	VDD = 1.62 to 3.6 V	
	Internal regulator (LDO) supplying VCORE	VDD = 1.7 to 3.6 V	VDDLDO = 1.62 to 3.6 V	
	Step-down converter (SMPS) supplying VCORE	NA	VDDSMPS = 1.62 to 3.6 V	
	External analog power supply	VDDA = 1.7 to 3.6 V VREF-	VDDA = 1.8 to 3.6 V VREF-	
		VREF+: a separate reference voltage, available on VREF+ pin for ADC and DAC	VREF+: a separate reference voltage, available on VREF+ pin for ADC and DAC When enabled by ENVR bit in the VREFBUF control status and status register(2), VREF+ is provided from the internal voltage reference buffer	
	USB power supply	VDD33USB = 3.0 to 3.6 V	VDD33USB = 3.0 to 3.6 V VDD50USB = 4.0 to 5.5 V	
	Backup domain	VBAT = 1.65 to 3.6 V	VBAT = 1.2 to 3.6 V	
	Independent power supply	VDDSDMMC = 1.7 to 3.6 V VDDDSI = 1.7 to 3.6 V	NA NA	VDDMMC = 1.62 to 3.6 V NA

PWR			STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Power supplies	VCORE supplies		1.08 V ≤ VCAP_1 and VCAP_2 ≤ 1.40 V	0.7 V ≤ VCAP ≤ 1.35 V	1.0 V ≤ VCAP ≤ 1.3V
	Reg bypass: must be supplied from external regulator on VCAP pins	VOS0	NA	1.35 V	1.3 V
		VOS1	1.32 V	1.2 V	
		VOS2	1.26 V	1.1 V	
		VOS3	1.14 V	1.00 V	
Peripheral supply regulation			DSI voltage regulator	USB regulator	
Power supply supervision			POR/PDR monitor BOR monitor PVD monitor		
			NA	AVD monitor(3) VBAT thresholds(4) Temperature thresholds(5)	

1. *To further optimize the power consumption, the unused RAMs can be Shut-off with the consequence of their content being lost (refer to RM0455).*
2. *For more details about VREFBUF see Voltage reference buffer (VREFBUF) section of RM0433 and RM0455 reference manuals.*
3. *Analog voltage detector (AVD): to monitor the VDDA supply by comparing it to a threshold selected by the ALS[1:0] bits in the PWR_CR1 register. The AVD is enabled by setting the AVDEN bit in the PWR_CR1 register.*
4. *Battery voltage thresholds (VBAT thresholds): indicate if VBAT is higher or lower than the threshold. The VBAT supply monitoring (available only in VBAT mode) can be enabled/disabled via MONEN bit in the PWR_CR2 register.*
5. *Temperature thresholds: the temperature monitoring can be enabled/disabled via MONEN bit in the PWR_CR2 register. It indicates whether the device temperature is higher or lower than the threshold.*

7 System configuration controller (SYSCFG)

The table below illustrates the SYSCFG main differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 19. SYSCFG main features differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

-	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
SYSCFG	Remap the memory areas Manage Class B feature	-	-
	Select the Ethernet PHY interface		-
	Manage the external interrupt line connection to the GPIOs Manage I/O compensation cell feature I2C Fast mode + configuration		
	-	Analog switch configuration management	
	-	Get readout protection and Flash memory bank swap informations Management of boot sequences and boot addresses Get BOR reset level Get Flash memory secured and protected sector status Get Flash memory write protections status Get DTCM secured section status Get independent watchdog behavior (hardware or software / freeze) Reset generation in Stop and Standby mode Get secure mode enabling/disabling	Not part of the system controller Features are part of the Flash registers

Note: For more details, refer to the SYSCFG register description section of RM0433 and RM0455 reference manuals.

8 Secure digital input/output and MultiMediaCard interface (SDMMC)

The following table presents the differences between the SDMMC interface of STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 20. SDMMC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

SDMMC	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Features	Full compliance with MultiMediaCard system specification version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	Full compliance with MultiMediaCard system specification version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	
	Full compliance with SD memory card specifications version 2.0	Full compliance with SD memory card specifications version 4.1.	
	Full compliance with SD I/O card specification version 2.0. Card support for two different databus modes: 1-bit (default) and 4-bit	Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit.	
	Data transfer up to 200 Mbyte/s for the 8-bit mode.	Data transfer up to 208 Mbyte/s for the 8-bit mode.(1)	
	NA	SDMMC IDMA: is used to provide high speed transfer between the SDMMC FIFO and the memory. The AHB master optimizes the bandwidth of the system bus. The SDMMC internal DMA (IDMA) provides one channel to be used either for transmit or receive.	
	Independent power supply for SDMMC2	NA	Independent power supply for SDMMC2

1. *Depending of the maximum allowed IO speed. for more details refer to datasheets.*

9 Universal (synchronous) asynchronous receiver-transmitter (U(S)ART)

The STM32H743/753 and STM32H7A3/7B0/7B3 devices implement several new features on the U(S)ART compared to the STM32F7 Series devices. The following table shows the U(S)ART differences.

Table 21. U(S)ART differences between STM32F7 Series devices, STM32H743/753, and STM32H7A3/7B0/7B3 devices

U(S)ART	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Instances	x4 USART x4 UART	x4 USART x4 UART x1 LPUART	x5 USART x5 UART x1 LPUART
Clock	Dual clock domain with dedicated kernel clock for peripherals independent from PCLK		
Wakeup	NA	Wakeup from low-power mode	
Features		SPI slave transmission, underrun flag Two internal FIFOs for transmit and receive data Each FIFO can be enabled/disabled by software and come with a status flag.	

10 Serial peripheral interface (SPI)

The STM32H743/753 and STM32H7A3/7B0/7B3 devices implement some enhanced SPI compared to the STM32F7 Series devices. See the table below for the SPI differences.

Table 22. SPI differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

SPI	STM32F7 Series devices	STM32H743/753 and STM32H7A3/7B0/7B3 devices
Instances	x4	x6
Clock	Single clock domain	Dual clock domain with dedicated kernel and serial interface clock independent from PCLK with transmission and reception capability at low-power stop
Wakeup	NA	Wakeup from low-power mode
Features	• Full-duplex synchronous transfers on three lines (with two separated data lines) • Half-duplex synchronous transfer on two lines (with single bidirectional data line) • Simplex synchronous transfers on two lines (with unidirectional data line) • 8 master mode baud rate prescalers up to fPCLK/2 • Slave mode frequency up to fPCLK/2 • NSS management by hardware or software for both master and slave • Master and slave capability, multi-master multi-slave support • Programmable clock polarity and phase • Programmable data order with MSB-first or LSB-first shifting • Dedicated transmission, reception and error flags with interrupt capability • SPI Motorola and TI formats support • Hardware CRC feature for reliable communication (at the end of transaction): – Configurable size and polynomial – Autommatic CRC upend in Tx mode – Automatic CRC check in Rx mode – Configurable RxFIFO threshold, data packeting support • Configurable data size (4-32 bit)	
	• Two 32-bit embedded Rx and Tx FIFOs with DMA capability • CRC pattern size 8 or 16 bit • RxFIFO threshold 8 or 16 bit	• Protection of configuration and setting • Adjustable minimum delays between data and between SS and data flow at master Configurable SS signal polarity and timing, MISO x MOSI swap capability • Programmable number of data within a transaction to control SS and CRC Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability • Programmable number of data in transaction Configurable behavior at slave underrun condition (support of cascaded circular buffers) • Master automatic suspend at receive mode Master start/suspend control • Alternate function control of associated GPIOs Selected status and error flags with wake up capability • CRC pattern size configurable from 4 to 32 bit Configurable CRC polynomial length • RxFIFO threshold from 1 to 16 data

11 Inter-integrated circuit interface (I^2S)

The table below presents the I^2S differences between the STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 23. I2S differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

I2S	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Features	x3	x3	x4
	Full duplex only when the extension module is implemented	Full duplex native	
	Minimum allowed value = 4	More flexible clock generator (division by 1,2 are possible)	
	Sampling edge is not programmable	Programmable sampling edge for the bit clock	
	Frame sync polarity cannot be selected	Programmable frame sync polarity	
	Receive buffer accessible in half-word	Receive buffer accessible in half-word and words	
	Data are right aligned into the receive buffer	Various data arrangement available into the receive buffer	
	Error flags signaling for underrun, overrun and frame error	Error flags signaling for underrun, overrun and frame error	
	NA	Improved reliability: automatic resynchronization to the frame sync in case of frame error	
		Improved reliability: re-alignement of left and right samples in case of underrun or overrun situation	
		MSb/LSb possible in the serial data interface	
	16 or 32 bits channel length in master	16 or 32 bits channel length in master	
	16 or 32 bits channel length in slave	Any channel length in slave	
	NA	Embedded RX and TX FIFOs	
	DMA capabilities (16-bit wide)	DMA capabilities (16-bit and 32-bit wide)	

12 Flexible memory controller (FMC)

The table below presents the FMC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 24. FMC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

FMC	STM32F7 Series devices	STM32H743/753 and STM32H7A3/7B0/7B3 devices
Mapping	AHB	AXI
Clock	Single clock domain	Dual clock domain with dedicated kernel clock for peripherals independent from AXI clock
Bank remap	SYSCFG_MEMRMP register FMC bank mapping can be configured by software through the SWP_FMC[1:0] bits.	FMC_BCR1 register FMC bank mapping can be configured by software through the BMAP[1:0] bits. See Figure 10 and Figure 11.
Features	NA	FMCEN bit: FMC controller Enable bit added in the FMC_BCR1 register. To modify some parameters while FMC is enabled follow the below sequence: 1. First disable the FMC controller to prevent any further accesses to any memory controller during register modification. 2. Update all required configurations. 3. Enable the FMC controller again. When the SDRAM controller is used, if the SDCLK clock ratio or refresh rate has to be modified after initialization phase, the following procedure must be followed. 1. Put the SDRAM device in Self-refresh mode. 2. Disable the FMC controller by resetting the FMCEN bit in the FMC_BCR1 register. 3. Update the required parameters. 4. Enable the FMC controller once all parameters are updated. 5. Then, send the clock configuration enable command to exit Self-fresh mode.

Figure 10. FMC bank address mapping on STM32H7A3/7B0/7B3 devices

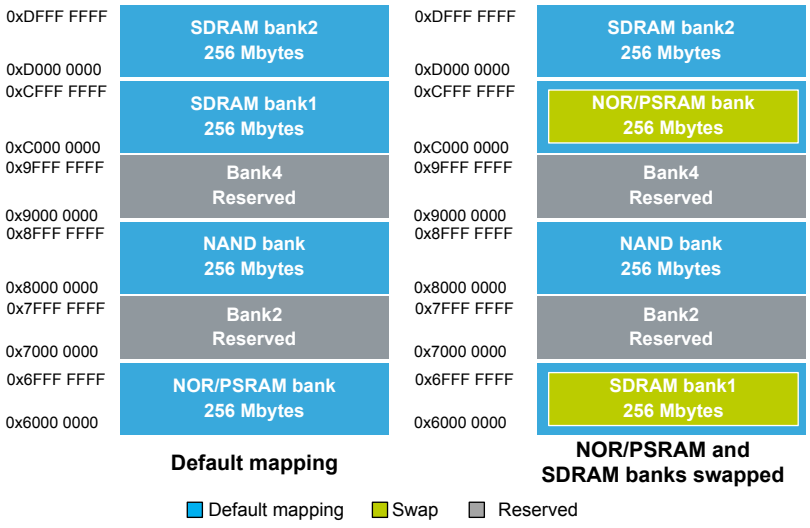
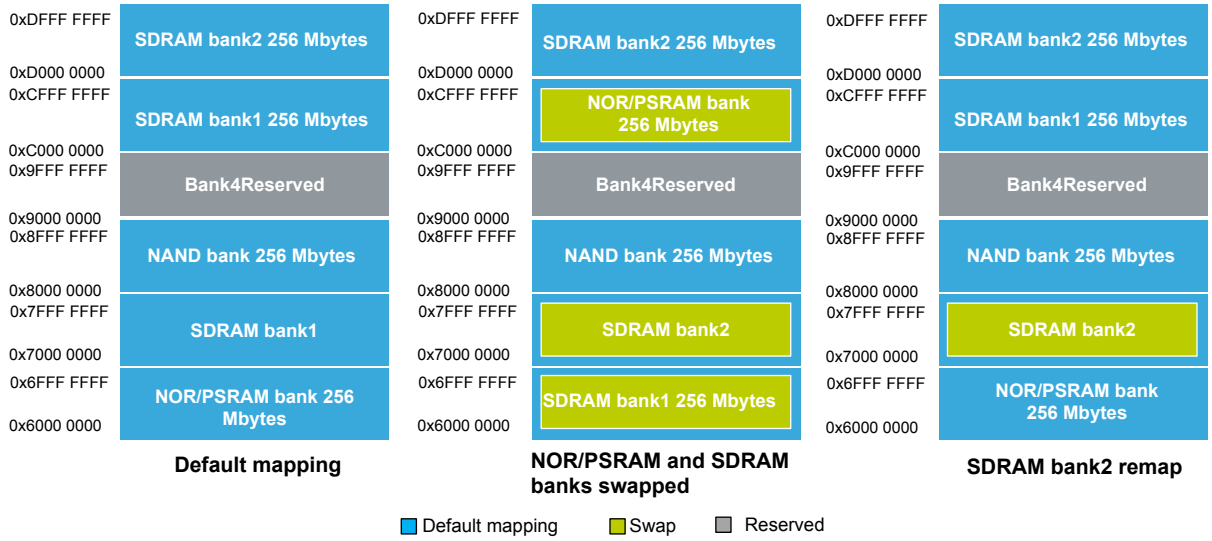


Figure 11. FMC bank address mapping on STM32H743/753 devices



13 Analog-to-digital converters (ADC)

The following table presents the differences between the ADC peripheral of the STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 25. ADC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

ADC	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Instances	x3	x3	x2
Clock	Single clock domain	Dual clock domain with dedicated kernel clock for peripherals independent from CLK or HCLK	
Number of channels	Up to 24 channels	Up to 20 channels	
Resolution	12, 10, 8 or 6-bit	16, 14, 12, 10 or 8-bit	
Conversion modes	• Single • Continuous • Scan • Discontinuous • Dual and triple mode		
DMA	Yes		
New features	NA	Input voltage reference from VREF+ pin or internal VREFBUF reference ADC conversion time is independent from the AHB bus clock frequency Self-calibration (both offset and the linearity) Low-power features Three analog watchdogs per ADC Internal dedicated channels: the internal DAC1 channel 1 and channel 2 are connected to ADC2 Oversampler: • 32-bit data register • Oversampling ratio adjustable from 2 to 1024 • Programmable data right and left shift Data can be routed to DFSDM for post processing	
	NA	All the internal references (VBAT, VREFINT, VSENSE) are connected to ADC3	All the internal references (VBAT, VREFINT, VSENSE) are connected to ADC2 The internal DAC2 channel 1 is connected to ADC2 One additional DAC for STM32H7A3/7B0/7B3 devices

The following two tables present the differences of external trigger for regular channels and injected channels between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 26. External trigger for regular channel differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Type	EXTSEL[3:0] STM32F7 Series devices	EXTSEL[4:0] STM32H7A3/7B0/7B3 STM32H743/753	ADC		
			STM32F7 Series devices	STM32H743/753	STM32H7A3/7B0/7B3
Internal signal from on-chip timers	0000	00000	TIM1_CC1 event		
	0001	00001	TIM1_CC2 event		
	0010	00010	TIM1_CC3 event		
	0011	00011	TIM2_CC2 event		
	0100	00100	TIM5_TRGO event	TIM3_TRGO event	
	0101	00101	TIM4_CC4 event		
	0110	00110	TIM3_CC4	EXTI line 11	
	0111	00111	TIM8_TRGO event		
	1000	01000	TIM8_TRGO(2) event		
	1001	01001	TIM1_TRGO event		
	1010	01010	TIM1_TRGO(2) event		
	1011	01011	TIM2_TRGO event		
	1100	01100	TIM4_TRGO event		
	1101	01101	TIM6_TRGO event		
	NA	01110	EXTI line11	TIM15_TRGO event	
	1111	01111	NA	TIM3_CC4 event	
	NA	10000		HRTIM1_ADCTRG1 event	Reserved
		10001		HRTIM1_ADCTRG3 event	Reserved
		10010		LPTIM1_OUT event	
		10011		LPTIM2_OUT event	
		10100		LPTIM3_OUT event	

Table 27. External trigger for injected channel differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Type	JEXTSEL[3:0] STM32F7 Series devices	JEXTSEL[4:0] STM32H7A3/7B0/7B3 STM32H743/753 devices	ADC		
			STM32F7 Series devices	STM32H743/753	STM32H7A3/7B0/7B3
Internal signal from on-chip timers	0000	00000	TIM1_TRGO event		
	0001	00001	TIM1_CC4 event		
	0010	00010	TIM2_TRGO event		
	0011	00011	TIM2_CC1 event		
	0100	00100	TIM3_CC4 event		
	0101	00101	TIM4_TRGO event		
	NA	00110	NA	EXTI line 15	
	0111	00111	TIM8_CC4 event		
	1000	01000	TIM1_TRGO(2) event		
	1001	01001	TIM8_TRGO event		
	1010	01010	TIM8_TRGO(2) event		
	1011	01011	TIM3_CC3 event		
	1100	01100	TIM5_TRGO event		
	1101	01101	TIM3_CC1 event		
	1110	01110	TIM6_TRGO event		
	NA	01111	NA	TIM15_TRGO event	
		10000		HRTIM1_ADCTRG2 event	Reserved
		10001		HRTIM1_ADCTRG4 event	Reserved
		10010		LPTIM1_OUT event	
		10011		LPTIM2_OUT event	
		10100		LPTIM3_OUT event	

14 Digital-to-analog converter (DAC)

TheSTM32H7A3/7B0/7B3 and STM32H743/753 devices implement some enhanced DAC compared to the STM32F7 Series devices devices. Refer to the table below for the main DAC differences between them.

Table 28. DAC differences between STM32F7 Series devices, STM32H7A3/7B0/7B3 and STM32H743/753 devices

DAC	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Instance	1x One dual channel	1x One dual channel	2x One dual channel One single channel
Clock	Single clock domain	Single clock domain (APB) LSI is used for sample and hold mode	
Features	Input voltage reference, VREF+	Input voltage reference from VREF+ pin or internal VREFBUF reference	
	NA	Buffer offset calibration DAC output connection to on chip peripherals Sample and hold mode for low power operation in Stop mode	

Table 29. DAC1 trigger selection differences between STM32F7 Series devices, STM32H7A3/7B0/7B3 and STM32H743/753 devices

Type	TSEL[2:0] STM32F7 Series devices	TSEL[3:0] STM32H7A3/7B0/7B3 STM32H743/753 devices	DAC1		
			STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Internal signal from on-chip timers	000	0000	TIM6_TRGO	SWTRIG	
	001	0001	TIM8_TRGO	TIM1_TRGO	
	010	0010	TIM7_TRGO	TIM2_TRGO	
	011	0011	TIM5_TRGO	TIM4_TRGO	
	100	0100	TIM2_TRGO	TIM5_TRGO	TIM3_TRGO event
	101	0101	TIM4_TRGO	TIM6_TRGO	
	110	0110	EXTI9	TIM7_TRGO	EXTI line 11
	111	0111	SWTRIG	TIM8_TRGO	
	NA	1000	NA	TIM15_TRGO	
		1001		HRTIM1_DACTRG1	Reserved
		1010		HRTIM1_DACTRG2	Reserved
		1011		LPTIM1_OUT	
		1100		LPTIM2_OUT	
		1101		EXTI9	
		1110		Reserved	LPTIM2_OUT
		1111		Reserved	

Table 30. DAC2 trigger selection new for STM32H7A3/7B0/7B3 devices

Type	TSEL[3:0]	DAC2
		STM32H7A3/7B0/7B3 devices
Internal signal from on-chip timers	0000	SWTRIG
	0001	TIM1_TRGO
	0010	TIM2_TRGO
	0011	TIM4_TRGO
	0100	TIM5_TRGO
	0101	TIM6_TRGO
	0110	TIM7_TRGO
	0111	TIM8_TRGO
	1000	TIM15_TRGO
	1001	Reserved
	1010	Reserved
	1011	LPTIM1_OUT
	1100	LPTIM2_OUT
	1101	EXTI9
	1110	LPTIM3_OUT
	1111	Reserved

15 USB on-the-go (USB OTG)

The STM32H7A3/7B0/7B3 devices embed one USB OTG HS/FS instance while the STM32H743/753 devices and STM32F7 Series devices embed one USB OTG HS/FS instance and one USB OTG FS instance.

The table below summarizes the difference of USB OTG between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 31. USB OTG differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

USB OTG	STM32F7 Series devices		STM32H743/753 devices	STM32H7A3/7B0/7B3 devices
Instance	FS	HS	x2 HS(1)	HS
Device bidirectional endpoints (including EP0)	6	9	9	
Host mode channels	12	16	16	
Size of dedicated SRAM	1.2 Kbytes	4 Kbytes	4 Kbytes	
USB 2.0 link power management (LPM) support	Yes			
OTG revision supported	1.3, 2.0		2.0	
Attach detection protocol (ADP) support	Not supported			
Battery Charging Detection (BCD) support	No		Yes	
ULPI available to primary IOs via, muxing	-	x1	x1	x1
Integrated PHY	x1 FS	x1 FS	x1 FS	x1 FS
DMA availability	Yes			

1. *Both OTG_HS1 and OTG_HS2 can potentially be programmed for HS operation, only one has an accessible ULPI interface which will allow a High Speed operation using an external HS transceiver.*

16 Ethernet (ETH)

The STM32H743/753 devices implement several new features on the Ethernet compared to the STM32F7 Series devices.

There is no Ethernet embedded in STM32H7A3/7B0/7B3 devices.

17 Digital filter for sigma delta modulators (DFSDM)

The STM32H7A3/7B0/7B3 devices implement several new features on the DFSDM compared to STM32H743/753 devices and to the STM32F7 Series devices with a DFSDM.

For STM32H7A3/7B0/7B3 devices, an additional single filter DFSDM has been included in the APB4 that can run in autonomous mode The following table shows the DFSDM differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 32. DFSDM differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

DFSDM	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM2
Number of channels	8		8	2
Number of filters	4		8	1
Input from ADC	NA	Yes	Yes	NA
Supported trigger sources	12	16		7

The table below presents the DFSDM internal signals differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 33. DFSDM internal signal differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Name	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM2
Internal/ external trigger signal	Refer to the following tables for DFSDM triggers signals connections			
break signal output	Refer to the following tables for DFSDM break signal connections			
DMA request signal	x4 DMA request from DFSDM_FLTx (x =0..3)		x8 DMA request from DFSDM_FLTx (x =0..7)	x1 DMA request
Interrupt request signal	x4 interrupt request from each DFSDM_FLTx (x=0..3)		x8 interrupt request from each DFSDM_FLTx (x=0..7)	x1 interrupt request
ADC input data	NA	dfsdm_dat_adc[15:0]		NA

This table describes the DFSDM triggers connection differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 34. DFSDM trigger connection differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Trigger name	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM2
DFSDM_JTRG[0]	TIM1_TRGO			Reserved
DFSDM_JTRG[1]	TIM1_TRGO2			
DFSDM_JTRG[2]	TIM8_TRGO			
DFSDM_JTRG[3]	TIM8_TRGO2			
DFSDM_JTRG[4]	TIM3_TRGO			
DFSDM_JTRG[5]	TIM4_TRGO			
DFSDM_JTRG[6]	TIM10_OC1	TIM16_OC1		
DFSDM_JTRG[7]	TIM6_TRGO			
DFSDM_JTRG[8]	TIM7_TRGO			
DFSDM_JTRG[9]	Reserved	HRTIM1_ADCTRG1	Reserved	
DFSDM_JTRG[10]	Reserved	HRTIM1_ADCTRG3	Reserved	
DFSDM_JTRG[23 :11]	Reserved			
DFSDM_JTRG[24]	EXTI11			
DFSDM_JTRG[25]	EXTI15			
DFSDM_JTRG[26]	LPTIMER1			
DFSDM_JTRG[27]	Reserved	LPTIMER2		
DFSDM_JTRG[28]	Reserved	LPTIMER3		
DFSDM_JTRG[29]	Reserved		COMP1_OUT	
DFSDM_JTRG[30]	Reserved		COMP2_OUT	
DFSDM_JTRG[31]	Reserved			

This table presents the DFSDM break connections differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices.

Table 35. DFSDM break connection differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices

Break name	STM32F7 Series devices	STM32H743/753 devices	STM32H7A3/7B0/7B3 devices	
Instance	DFSDM1	DFSDM1	DFSDM1	DFSDM2
DFSDM_BREAK[0]	TIM1 break	TIM15 break	TIM1/TIM15 break	LPTIM3 ETR
DFSDM_BREAK[1]	TIM1 break2	TIM16 break2	TIM1_break2 /TIM16 break	-
DFSDM_BREAK[2]	TIM8 break	TIM1/TIM17/TIM8 break	TIM17/TIM8 break	-
DFSDM_BREAK[3]	TIM8 break2	TIM1/TIM8 break2	TIM8 break2	-

Revision history

Table 36. **Document revision history**

Date	Version	Changes
27-Feb-2019	1	Initial release.
15-Mar-2019	2	Updated: • Section 2 STM32H7A3/7B0/7B3 device overview • Section 2.1 System architecture differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/H7B0/H7B3 devices • Table 7. Peripheral summary STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices • Section 6 Power (PWR) • Table 9. Memory organization and compatibility between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices • Table 25. ADC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices
31-Jan-2020	3	Changed document classification to public.
25-May-2020	4	Updated: • Added support for the STM32H7B0 Value line devices • Section 2 STM32H7A3/7B0/7B3 device overview • Figure 2. STM32H743/753 device system architecture • Figure 3. STM32H7A3/7B0/7B3 device system architecture • Figure 5. System supply configuration on STM32H743/753 and STM32H7A3/7B0/7B3 devices with SMPS • Table 7. Peripheral summary STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices • Table 9. Memory organization and compatibility between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices • Table 11. Flash memory differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices • Table 15. Different source clock in STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices • Table 17. General operating conditions for STM32F7 Series devices, STM32H7A3/7B0/7B3 and STM32H743/753 devices Added: • Section 1 General information • Figure 6. System supply configuration on STM32H743/753 and STM32H7A3/7B3/7B0 devices without SMPS
12-Oct-2020	5	Updated Table 5. STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices bootloader communication peripherals

Contents

1 General information 2
2 STM32H7A3/7B0/7B3 device overview 3
2.1 System architecture differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/H7B0/H7B3 devices 4
3 Hardware migration 8
3.1 Available packages 8
3.2 Pinout compatibility 9
3.3 System bootloader 13
4 Boot mode compatibility 14
5 Peripheral migration 15
5.1 STM32 product cross-compatibility 15
5.2 Memory organization 19
5.2.1 RAM size 19
5.2.2 Memory map and peripherals register boundary addresses 20
5.2.3 Peripheral register boundary addresses 22
5.3 Flash memory 24
5.4 Nested vectored interrupt controllers (NVIC) 26
5.5 Extended interrupt and event controller (EXTI) 28
5.5.1 EXTI main features in STM32H7A3/7B0/7B3 devices 28
5.5.2 EXTI block diagram in STM32H7A3/7B0/7B3 devices 28
5.6 Reset and clock control (RCC) 31
5.6.1 Clock management 31
5.6.2 Peripheral clock distribution 32
5.7 Operating conditions 33
6 Power (PWR) 34
7 System configuration controller (SYSCFG) 36
8 Secure digital input/output and MultiMediaCard interface (SDMMC) 37
9 Universal (synchronous) asynchronous receiver-transmitter (U(S)ART) 38
10 Serial peripheral interface (SPI) 39

11 Inter-integrated circuit interface (I^2S) 41
12 Flexible memory controller (FMC) 42
13 Analog-to-digital converters (ADC) 44
14 Digital-to-analog converter (DAC) 47
15 USB on-the-go (USB OTG) 49
16 Ethernet (ETH) 50
17 Digital filter for sigma delta modulators (DFSDM) 51
Revision history 53
Contents 54
List of tables 56
List of figures 57

List of tables

Table 1. Available bus matrix on STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 4
Table 2. Available packages on STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 8
Table 3. LQFP64 package compatibility between STM32F7 Series devices and STM32H7A3/7B0/7B3 devices 9
Table 4. BYPASS_REG pin incompatibility 10
Table 5. STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices bootloader communication peripherals 13
Table 6. Boot mode compatibility between STM32F7 Series devices and STM32H7xx lines. 14
Table 7. Peripheral summary STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 15
Table 8. Comparison of RAM size between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 19
Table 9. Memory organization and compatibility between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 20
Table 10. Examples of peripheral address mapping differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 23
Table 11. Flash memory differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 25
Table 12. Interrupt vector differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 26
Table 13. EXTI event input types differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 28
Table 14. EXTI line differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices . . 29
Table 15. Different source clock in STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 31
Table 16. Peripheral clock distribution example 32
Table 17. General operating conditions for STM32F7 Series devices, STM32H7A3/7B0/7B3 and STM32H743/753 devices 33
Table 18. PWR differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 34
Table 19. SYSCFG main features differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 36
Table 20. SDMMC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices . . 37
Table 21. U(S)ART differences between STM32F7 Series devices, STM32H743/753, and STM32H7A3/7B0/7B3 devices . 38
Table 22. SPI differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 40
Table 23. I2S differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 41
Table 24. FMC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 42
Table 25. ADC differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices 44
Table 26. External trigger for regular channel differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 45
Table 27. External trigger for injected channel differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 46
Table 28. DAC differences between STM32F7 Series devices, STM32H7A3/7B0/7B3 and STM32H743/753 devices 47
Table 29. DAC1 trigger selection differences between STM32F7 Series devices, STM32H7A3/7B0/7B3 and STM32H743/753 devices. 47
Table 30. DAC2 trigger selection new for STM32H7A3/7B0/7B3 devices. 48
Table 31. USB OTG differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices . 49
Table 32. DFSDM differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. . . 51
Table 33. DFSDM internal signal differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 51
Table 34. DFSDM trigger connection differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 52
Table 35. DFSDM break connection differences between STM32F7 Series devices, STM32H743/753 and STM32H7A3/7B0/7B3 devices. 52
Table 36. Document revision history 53

List of figures

Figure 1. STM32F7 Series devices system architecture . . . 5
Figure 2. STM32H743/753 device system architecture . . . 6
Figure 3. STM32H7A3/7B0/7B3 device system architecture . . . 7
Figure 4. LQFP64 package compatibility . . . 9
Figure 5. System supply configuration on STM32H743/753 and STM32H7A3/7B0/7B3 devices with SMPS . . . 11
Figure 6. System supply configuration on STM32H743/753 and STM32H7A3/7B3/7B0 devices without SMPS . . . 12
Figure 7. RAM memory organization of STM32F7 Series devices, STM32H743/753 and STM32H7A3/B0/B3 devices . . . 21
Figure 8. EXTI block diagram on STM32H7A3/7B0/7B3 devices . . . 28
Figure 9. Peripheral clock distribution STM32H743/753 and STM32H7A3/7B0/7B3 devices . . . 32
Figure 10. FMC bank address mapping on STM32H7A3/7B0/7B3 devices . . . 42
Figure 11. FMC bank address mapping on STM32H743/753 devices . . . 43