ST25R3911B to ST25R3916 and ST25R3920 migration guide

Introduction

The ST25R3916 and ST25R3920, high performance NFC universal devices and EMVCo™ readers, are an evolution of the ST25R3911B, NFC / HF RFID reader IC. It comprises several enhancements such as improved receiver sensitivity and noise immunity, more robust driver stage with improved radiated emission characteristics, two host interfaces, a larger FIFO, CE support, hardware EMD suppression, undershoot and overshoot protection, among many others.

1 Terms and acronyms

Table 1. Terms definition

Acronym	Definition
AAT	Automatic antenna tuning
ADC	Analog to digital converter
AP2P	Active P2P
CSO	Capacitance sense output
CSI	Capacitance sense input
EMC	Electromagnetic compatibility
HW	Hardware
I^2C	Inter-integrated circuit
IRQ	Interrupt request
MCU	Microcontroller
P2P	Peer to peer
PSRR	Power supply rejection ratio
PCB	Printed circuit board
RC	Resistive capacitive
RF	Radio frequency
RFAL	RF abstraction layer
SPI	Serial peripheral interface
SW	Software

2 Pinout comparison

All three chips have a similar footprint. Additional features introduced on the ST25R3916 and ST25R3920 silicon require a pinout change, which brakes the chip pin-to-pin compatibility. As a reference, use the ST25R3916-DISCO schematic and layout. Table 2 below details the pin layout difference between the ST25R3911B, and the ST25R3916 and ST25R3920 with the signal description in Table 3.

Table 2. Signal layout comparison

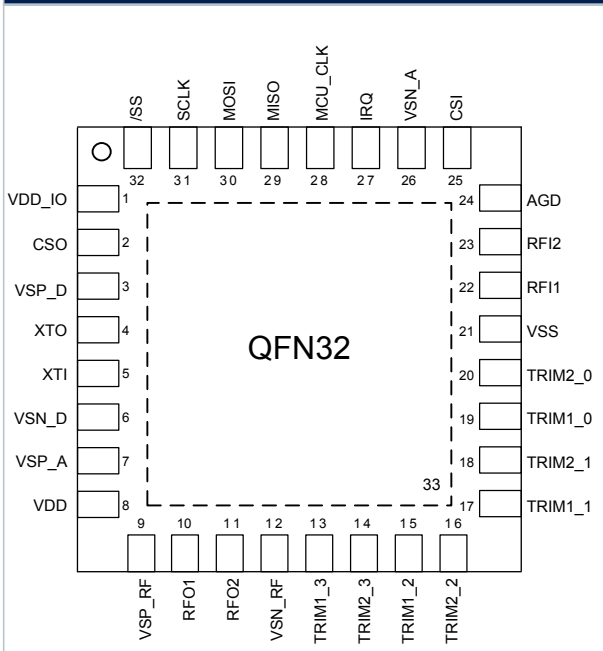
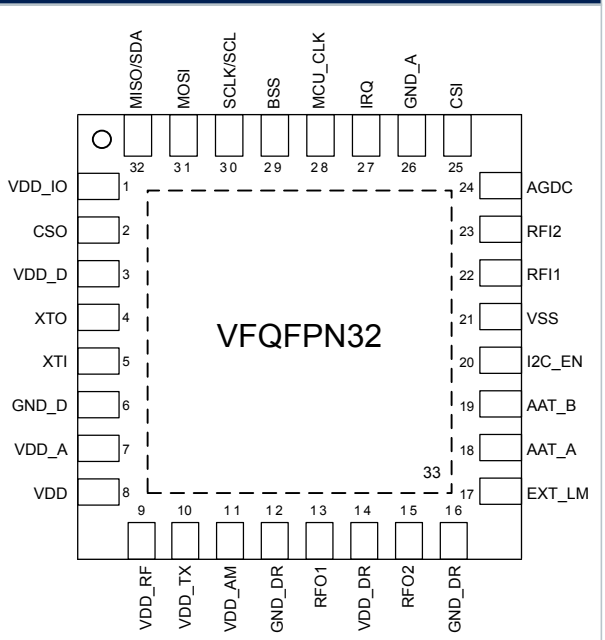
ST25R3911B	ST25R3916 and ST25R3920
	

Table 3. Signal description comparison

		ST25R3911B		ST25R3916 and ST25R3920	
change	PIN	Name	Description	Name	Description
Same	1	VDD_IO	Positive supply for peripheral communication	VDD_IO	Positive supply for peripheral communication
Same	2	CSO	Capacitor sensor output	CSO	Capacitor sensor output
Same	3	VSP_D	Regulator output	VDD_D	Regulator output
Same	4	XTO	Xtal oscillator output	XTO	Xtal oscillator output
Same	5	XTI	Xtal oscillator input	XTI	Xtal oscillator input
Same	6	VSN_D	Digital ground	GND_D	Digital ground
Same	7	VSP_A	Analog supply regulator output	VDD_A	Analog supply regulator output
Same	8	VDD	External positive supply	VDD	External positive supply
Same	9	VSP_RF	Supply regulator output for antenna drivers	VDD_RF	Supply regulator output for antenna drivers
Different	10	RFO1	Antenna driver output	VDD_TX	External positive supply for the TX part

		ST25R3911B		ST25R3916 and ST25R3920	
change	PIN	Name	Description	Name	Description
Different	11	RFO2	Antenna driver output	VDD_AM	Regulated driver supply for AM modulation
Different	12	VSN_RF	Ground of antenna drivers	GND_DR	Antenna driver ground, including driver VSS
Different	13	TRIM1_3	Analog I/O input to trim antenna resonant circuit	RFO1	Antenna driver output
Different	14	TRIM2_3	Analog I/O input to trim antenna resonant circuit	VDD_DR	Antenna driver positive supply input
Different	15	TRIM1_2	Analog I/O input to trim antenna resonant circuit	RFO2	Antenna driver output
Different	16	TRIM2_2	Analog I/O input to trim antenna resonant circuit	GND_DR	Antenna driver ground, including driver VSS
Different	17	TRIM1_1	Analog I/O input to trim antenna resonant circuit	EXT_LM	External load modulation MOS gate driver
Different	18	TRIM2_1	Analog I/O input to trim antenna resonant circuit	AAT_A	AAT tune voltage for variable capacitor AAT_A
Different	19	TRIM1_0	Analog I/O input to trim antenna resonant circuit	AAT_B	AAT tune voltage for variable capacitor AAT_B
Different	20	TRIM2_0	Analog I/O input to trim antenna resonant circuit	I2C_EN	I2C interface enable
Same	21	VSS	Ground, die substrate potential	VSS	Ground, die substrate potential
Same	22	RFI1	Analog input receiver input	RFI1	Analog input receiver input
Same	23	RFI2	Analog input receiver input	RFI2	Analog input receiver input
Same	24	AGD	Analog reference voltage	AGDC	Analog reference voltage
Same	25	CSI	Capacitor sensor input	CSI	Capacitor sensor input
Same	26	VSN_A	Analog ground	GND_A	Analog ground
Same	27	IRQ	Interrupt request output	IRQ	Interrupt request output
Same	28	MCU_CLK	Microcontroller clock output	MCU_CLK	Microcontroller clock output
Different	29	MISO	Serial peripheral Interface data output	BSS	Serial peripheral interface enable (active low)
Different	30	MOSI	Serial peripheral interface data input	SCLK/SCL	Serial peripheral interface clock / I2C clock
Different	31	SCLK	Serial peripheral interface clock	MOSI	Serial peripheral interface data input
Different	32	/SS	Serial peripheral interface enable (active low)	MISO/SDA	Serial peripheral interface data output / I2C data line
Same	33	VSS	Die substrate potential, connected to VSS on PCB	VSS	Die substrate potential, connected to VSS on PCB

3 Feature description

This section describes differences between the above-mentioned pinout and features.

3.1 Power management and AM modulation

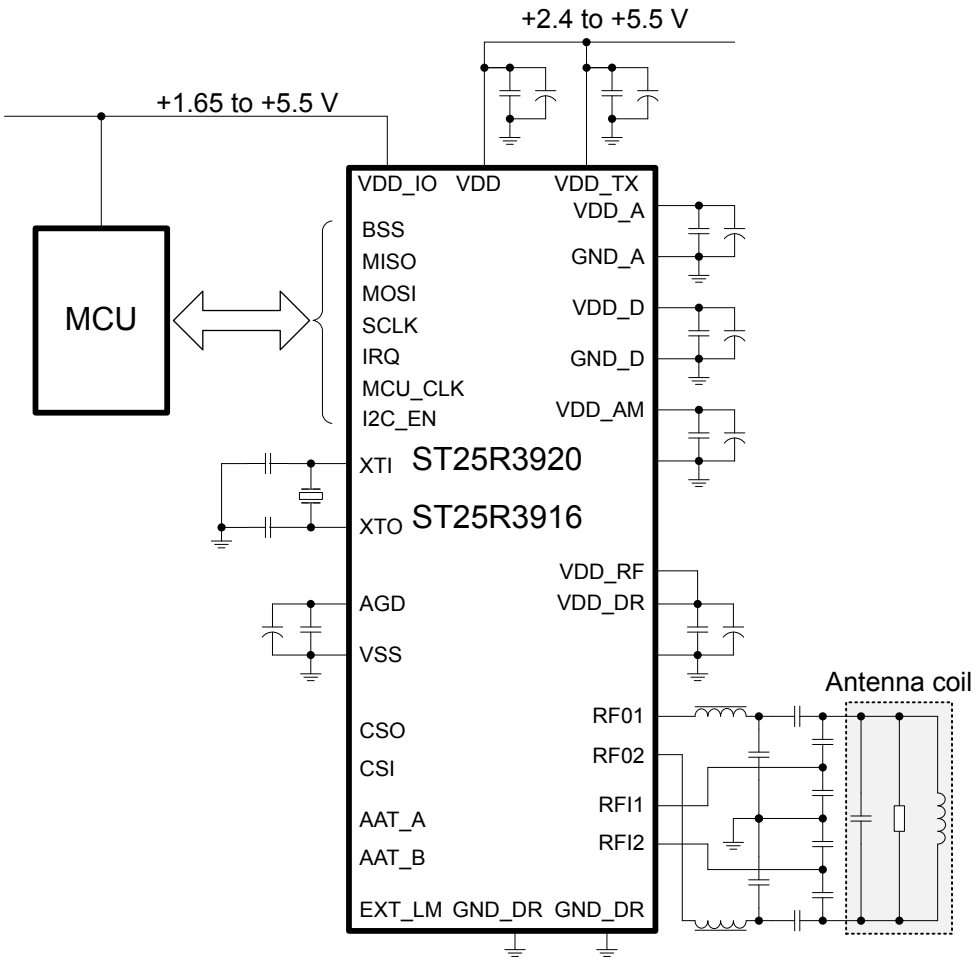
The ST25R3916 and ST25R3920 feature three positive supply pins, VDD, VDD_TX and VDD_IO. The details of the power and antenna circuit is illustrated in Figure 1

VDD is the main power supply pin. It supplies power to the analog and digital blocks through two regulators (VDD_A, VDD_D). VDD_TX is the transmitter power supply pin. It supplies power to the transmitter via two regulators (VDD_RF, VDD_AM). The supported VDD and VDD_TX supplies range between 2.4 V to 3.6 V and 3.6 V to 5.5 V respectively. The VDD and VDD_TX pins must be connected to the same power source.

VDD_A and VDD_D blocks should be connected to 3.6 V max. The use of VDD_A and VDD_D regulators is mandatory at 5 V power supply (range 3.6 V to 5.5 V).

The regulated voltage is automatically adjusted to have the highest possible regulated voltage while still providing good PSRR. All regulator pins also have corresponding negative supply pins, externally connected to the ground plain (VSS). All regulator pins and AGDC voltage are buffered with a pair of ceramic capacitors. For VDD, VDD_TX, VDD_RF, VDD_AM and VDD_DR pins, the recommended blocking capacitors are 2.2 µF in parallel with 10 nF, for pin AGDC the recommended capacitance value is 1 µF in parallel with 10 nF.

Figure 1. Power and antenna circuit schematic



The AM modulation transmitter uses the VDD_AM regulator as power source. The transmitter supply uses the VDD_AM regulator output voltage during the modulation phase. In the case of modulation, the transmitter is switched to the internal supply. This allows the correct modulation index for a supply voltage between 2.4 and 5.5 V.

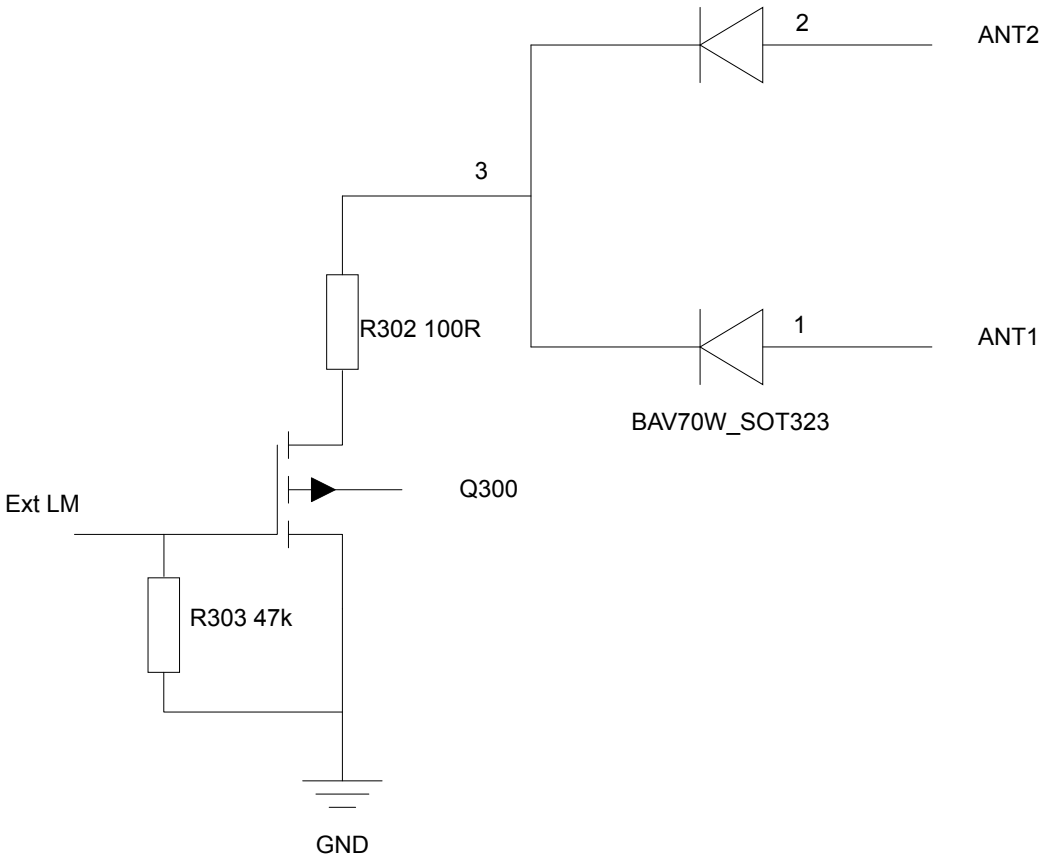
The output voltage and modulation index settings are controlled by AM_MOD<3:0> option bits in the TX driver register in a range of 5-40%. As an alternative, set the resistive AM modulation as is done for the ST25R3911B by setting the DIS_REG_AM bit in the Auxiliary modulation setting register to high. No further settings are needed for proper software modulation depth. The voltage based AM modulation level generation is linear against detuning by PICC and environment.

3.2 Card mode / EXT_LM

The ST25R3916 and ST25R3920 add the passive target mode as a new feature, which supports ISO14443-A and FeliCatm protocols. The ST25R3916 and ST25R3920 generate the load modulation in passive target mode by switching between two RFO driver resistance values. The bits PT_RES<3:0> and PTM_RES<3:0> in the Passive target modulation register represents the RFO driver resistance in demodulated (PT_RES) and modulated (PTM_RES) state respectively.

Additionally, the transmitter can also drive an external MOS transistor via the EXT_LM pin to generate the load modulation signal. Figure 2 illustrates the implementation circuit implementing an external MOS transistor, containing the resistors and diodes necessary for correct operation. The component choice must be adapted to the final application specification.

Figure 2. External load modulation circuit



Refer to the ST25R3916 and ST25R3920 datasheets for detailed operating conditions.

3.3 Automatic antenna tuning (AAT)

The ST25R3916 and ST25R3920 feature two 8-bit DAC outputs (AAT_A and AAT_B) to control variable capacitors for the antenna tuning. The AAT feature is an optional feature. The DAC output ranges from 150 mV to VDD_A-150 mV when VDD_A = 3.4 V. The load resistance must not be rated below 60 kΩ per DAC output. The variable capacitors are four pin devices, which change their capacitance between two pins, when applying a DC control voltage.

The variable capacitors can be put into the antenna matching circuit in addition to the series and parallel matching capacitance. The typical tuning range from 50% (control voltage = 3 V) to 100% (control voltage = 0 V). Further details are in the automatic antenna tuning application note for the ST25R3911B, ST25R3916, and ST25R3920 devices on www.st.com.

3.4 SPI / I²C interface

Both the ST25R3916 and the ST25R3920 feature two host interfaces. The SPI interface, similar to the ST25R3911B SPI interface implementation and a newly integrated I²C interface. Table 4. Host interface signal lines below details of the shared signal interface pins.

Table 4. Host interface signal lines

Name	Signal	Description
I2C_EN	Digital input	Interface selection (I2C_EN = low for SPI interface)
BSS	Digital input	SPI chip enable (active low)
MOSI	Digital input	SPI data input
MISO / SDA	Digital output	SPI data output / I²C data line
SCLK / SCL	Digital input	SPI clock / I²C clock
IRQ	Digital output	Interrupt output (active high)

The interface selection is done by either connecting the I2C_EN pin to GND or VDD_D level. If the I²C interface is selected, (I2C_EN = VDD_D) additional pull up resistors are needed on the SDA and SCL line and the host interface has to be correctly connected to the MCU. Table 5. SPI and I²C interface communication speed details the maximum communication speed of each interface.

Table 5. SPI and I²C interface communication speed

Interface	ST25R3911B	ST25R3916 and ST25R3920
SPI	Up to 6 Mbit/s	Up to 10 Mbit/s
I²C	-	Up to 3.4 Mbit/s

4 Interface

Although the ST25R3911B, and ST25R3916 and ST25R3920 have similar operation and interface, they are not identical. Features are either added or removed, and some behavior may differ from one device to the other.

This document details the changes from the host point of view.

To ensure maximum functional coverage, use the ST NFC library (RFAL) freely available from www.st.com.

If RFAL is already used on the ST25R3911 project, migrating is as simple as switching the drivers to compile from ST25R3911B to either the ST25R3916 or ST25R3920. The migration process is outlined below.

4.1 Communication with host

As with the ST25R3911B, the ST25R3916 and ST25R3920 can be controlled via mostly the same mechanisms: read/write registers, execute direct commands, read/write FIFO.

Additionally, the ST25R3916 and ST25R3920 contain a passive target memory area that can be accessed in a similar way as the FIFO.

SPI is available on both devices and these transactions (apart from the command codes themselves) are mostly the same. An existing SPI driver does not to require further modifications, although increase of the SPI speed would be beneficial (up to 10 Mbit/s).

4.2 Commands

Although some commands do share the same code, a number of new commands and features are added while others are removed. Table 6 below summarizes these changes.

Table 6. ST25R3911B, ST25R3916 and ST25R3920 command differences

Command	ST25R3911B	ST25R3916 and ST25R3920
C0	-	Set default
C1	Set default	
C2	Clear	Stop all activities
C3	Clear	Stop all activities
C4	Transmit with CRC	
C5	Transmit without CRC	
C6	Transmit REQA	
C7	Transmit WUPA	
C8	NFC initial field ON	
C9	NFC response field ON	
CA	NFC response field ON with n=0	-
CB	Go to normal NFC mode	-
CC	Analog preset	-
CD	-	Go to sense (idle)
CE	-	Go to sleep (halt)
D0	Mask receive data	
D1	Unmask receive data	
D2	-	Change AM modulation state
D3	Measure amplitude	
D4	Squelch	-

Command	ST25R3911B	ST25R3916 and ST25R3920
D5	Reset Rx gain	
D6	Adjust regulators	
D7	Calibrate modulation depth	-
D8	Calibrate antenna	Calibrate driver timing
D9	Measure phase	
DA	Clear RSSI	
DB	-	Clear FIFO
DC	Enter transparent mode	
DD	Calibrate capacitive sensor	
DE	Measure capacitance	
DF	Measure power supply	
E0	Start general purpose timer	
E1	Start wake-up timer	
E2	Start mask-receive timer	
E3	Start No-response timer	
E4	-	Start PPON2 timer
E8	-	Stop No-response timer
FB	-	Register Space-B access

4.2.1 Analog preset

Unlike ST25R3911B, the ST25R3916 and ST25R3920 do not provide a direct command to load predefined settings to neither the receiver, nor the transmitter. Instead the host is responsible for loading the appropriate mode and bit rate settings according to the devices required performance.

Refer to the analog configuration table in the latest ST25R3916 and ST25R3920 RFAL driver packages for the recommended settings, available on www.st.com

In the RFAL, these settings are referred to as analog configs/settings and the library applies them as needed. These settings are conveniently grouped in a table that can be easily customized and generated using available tools.

4.2.2 Calibrate modulation depth

With the ST25R3916 and ST25R3920, modulation depth calibration is no longer necessary. Instead the ASK modulation is ensured via an additional regulated supply providing stable and accurate modulation depth.

4.2.3 Calibrate antenna

On ST25R3916 and ST25R3920, the antenna calibration is no longer performed internally by a direct command. The calibration is performed by driving the outputs on two 8-bit DACs which are meant to control variable capacitors. Refer to the Section 3.3 above for further information.

4.3 Registers

Several new registers are added to accommodate the new features and some configuration bits that exist on both devices are moved.

No exhaustive list of the changes is made in this document. Only 4 out of the 79 registers keep the same address and content between devices.

A portion of these new registers is added in a new area called Space-B. Access to these registers is done using an additional command called Register Space-B Access.

In the official ST RFAL drivers, the registers are flagged (40h) on the address to indicate Space-B register.

4.4 FIFO

While ST25R3911B provides a FIFO with 96 bytes, the ST25R3916 and ST25R3920 have larger FIFOs of 512 bytes.

Depending on the device, the FIFO water level interrupts occur at different moments of the transmission/reception process.

Unlike on the ST25R3911B, the ST25R3916 and ST25R3920 FIFO water level interrupts are fixed to 200 bytes on transmission and 300 bytes during reception and cannot be changed.

Also, the FIFO read command is changed. On the ST25R3916 and ST25R3920, the command code is 9Fh.

4.5 Interrupts

All three devices use an equivalent interrupt mechanism. The same IRQ pin notifies the host that one or more interrupts have occurred if not masked out, and the host must retrieve the interrupt status as soon as possible.

New interrupts added to the ST25R3916 and ST25R3920 are contained in 4 registers instead of 3 on the ST25R3911B.

Similarly to the ST25R3911B, all these registers must be read in a single SPI / I^2C operation.

Table 7 summarizing the interrupt differences.

Table 7. Interrupt differences

Bit	ST25R3911	ST25R3916 and ST25R3920
1	I_osc	
2	I_wl	
3	I_rxs	
4	I_rxe	
5	I_txe	
6	I_col	
7	I_tim	I_rx_rest
8	I_err	RFU
9	I_dct	
10	I_nre	
11	I_gpe	
12	I_eon	
13	I_eof	
14	I_cac	
15	I_cat	
16	I_nfct	
17	I_crc	
18	I_par	
19	I_err2	
20	I_err1	
21	I_wt	
22	I_wam	
23	I_wph	
24	I_wcap	
25	-	I_ppon2
26	-	I_sl_wl
27	-	I_apon
28	-	I_rxe_pta
29	-	I_wu_f
30	-	RFU
31	-	I_wu_a*
32	-	I_wu_a

These new interrupts are related to introduced features and new handlings that differ between the two devices.

4.6 Timers

All timers that exist on ST25R3911B are also available on the ST25R3916 and ST25R3920.

Some of these are enhanced with less jitter and additional control on the step size.

For example, the mask receive timer is now controlled by the mrt_step bit in the Timer and EMV control register which specifies which step size is to be used.

An additional timer (PPON2) is introduced for improved AP2P support.

4.7 Bit rate detection mode

As ST25R3916 and ST25R3920 also support the passive listen mode, the bit rate detection mode is different from the one previously available on the ST25R3911B. The host needs to configure the ST25R3916 and ST25R3920 properly and set the protocols which are expected to be activated on (passive listen and/or AP2P).

Specific handling for supporting listen mode activation is required.

5 Migrating existing software projects

As stated above, it is advised to use of the STMicroelectronics NFC library (RFAL) which provides support for all required technologies and protocols, while encapsulating all existing ST25Rxxxx devices (ST25R3911, ST25R3916, ST25R3920, ST25R95).

This library is periodically updated to introduce new features, wider support of NFC devices, as well as fixes, and its compliancy to the latest versions of the relevant standards is continuously ensured.

Patching and tweaking of existing non-RFAL ST25R3911B drivers require considerable effort and possibly lead to an incomplete driver, that is neither able to receive official updates nor be easily supported. It is therefore not recommended.

5.1 Project using RFAL

The RFAL is structured so that the ST25Rxxxx device underneath is encapsulated. Therefore, to migrate an existing ST25R3911B project to a ST25R3916 or ST25R3920 project, only requires the modification of the RFAL HAL (hardware abstraction layer) to ST25R3916 or ST25R3920.

On the project compilation list or makefile, replace the include folder from `rfal/source/st25r3911` to `rfal/source/st25r3916`, and switch the following modules:

Table 8. Makefile definitions

ST25R3911B	ST25R3916 and ST25R3920
rfal_rfst25r3911	rfal_rfst25r3916
st25r3911	st25r3916
st25r3911_com	st25r3916_com
st25r3911_interrupt	st25r3916_irq
-	st25r3916_led

5.2 Project not using RFAL

The recommended procedure is to make use of the RFAL. Refer to the existing documentation and reference designs available on www.st.com to adapt your project accordingly.

Revision history

Table 9. Document revision history

Date	Version	Changes
10-Apr-2019	1	Initial release.
03-Nov-2020	2	Document updated to support the ST25R3920. Updated: • Introduction • Section 2 Pinout comparison • Section 3.1 Power management and AM modulation • Figure 1. Power and antenna circuit schematic • Section 3.2 Card mode / EXT_LM • Section 3.3 Automatic antenna tuning (AAT) • Section 3.4 SPI / I2C interface • Section 4 Interface • Section 4.1 Communication with host • Section 4.2 Commands • Section 4.2.1 Analog preset • Section 4.2.2 Calibrate modulation depth • Section 4.2.3 Calibrate antenna • Section 4.4 FIFO • Section 4.5 Interrupts • Section 4.6 Timers • Section 4.7 Bit rate detection mode • Section 5 Migrating existing software projects • Section 5.1 Project using RFAL

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