AN5311
Application note

L9945 in H-bridge configuration

Introduction

The aim of this application note is to provide criteria for proper configuration and correct driving of L9945 in H-bridge configuration.

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1 HW configuration

The device can handle up to two H-bridges. There are two possible configurations which can co-exist:

- H-bridge 1: it involves channels 1 (HS), 2 (HS), 3 (LS) and 4 (LS)
- H-bridge 2: it involves channels 5 (HS), 6 (HS), 7 (LS) and 8 (LS)

While high-side channels can be populated either with NMOS FETs or with PMOS FETs, low-side channels must be populated only with NMOS type transistors. *Figure 1* shows an example of H-bridge 1 configuration with NMOS transistors on high-side channels. In case of PMOS on high-side channels, refer to the example illustrated in *Figure 2*.

Figure 1. Example of H-bridge configuration with NMOS as HS transistors (channel 1-4)

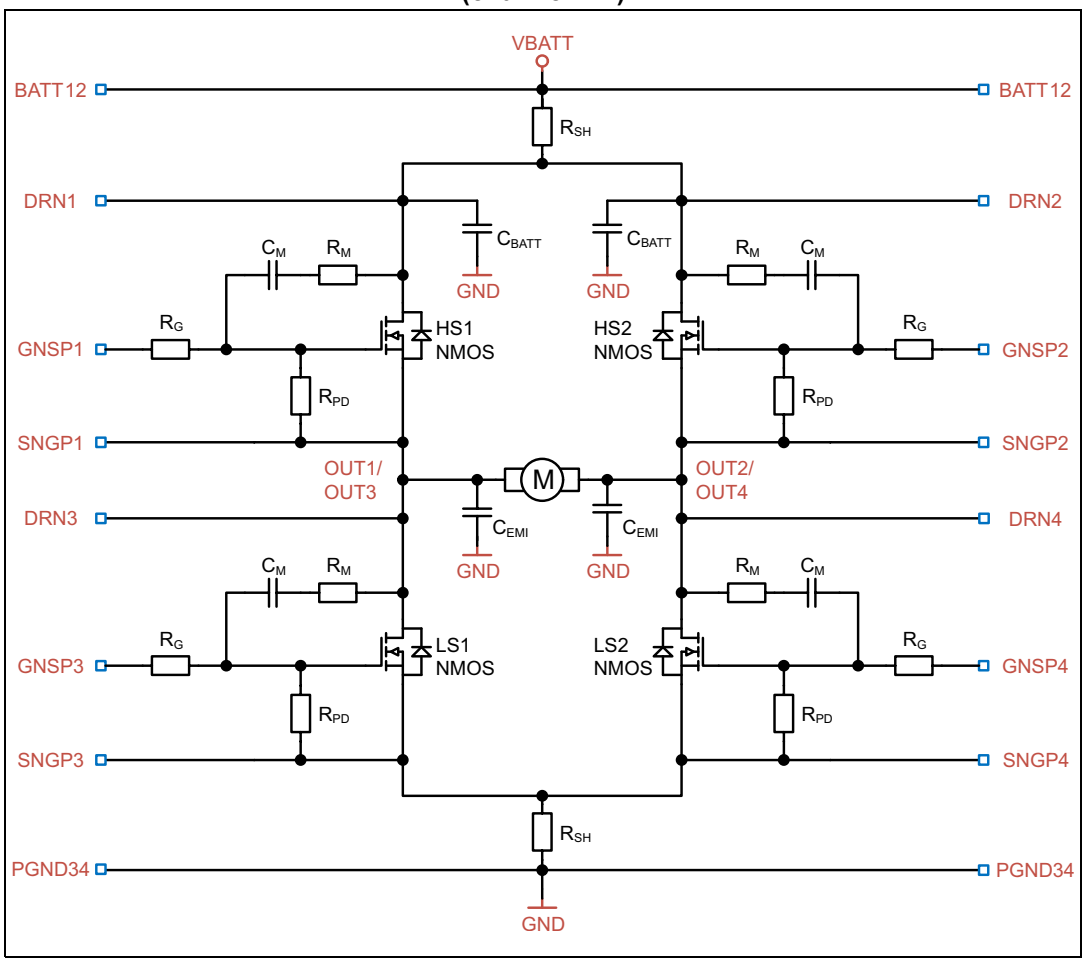
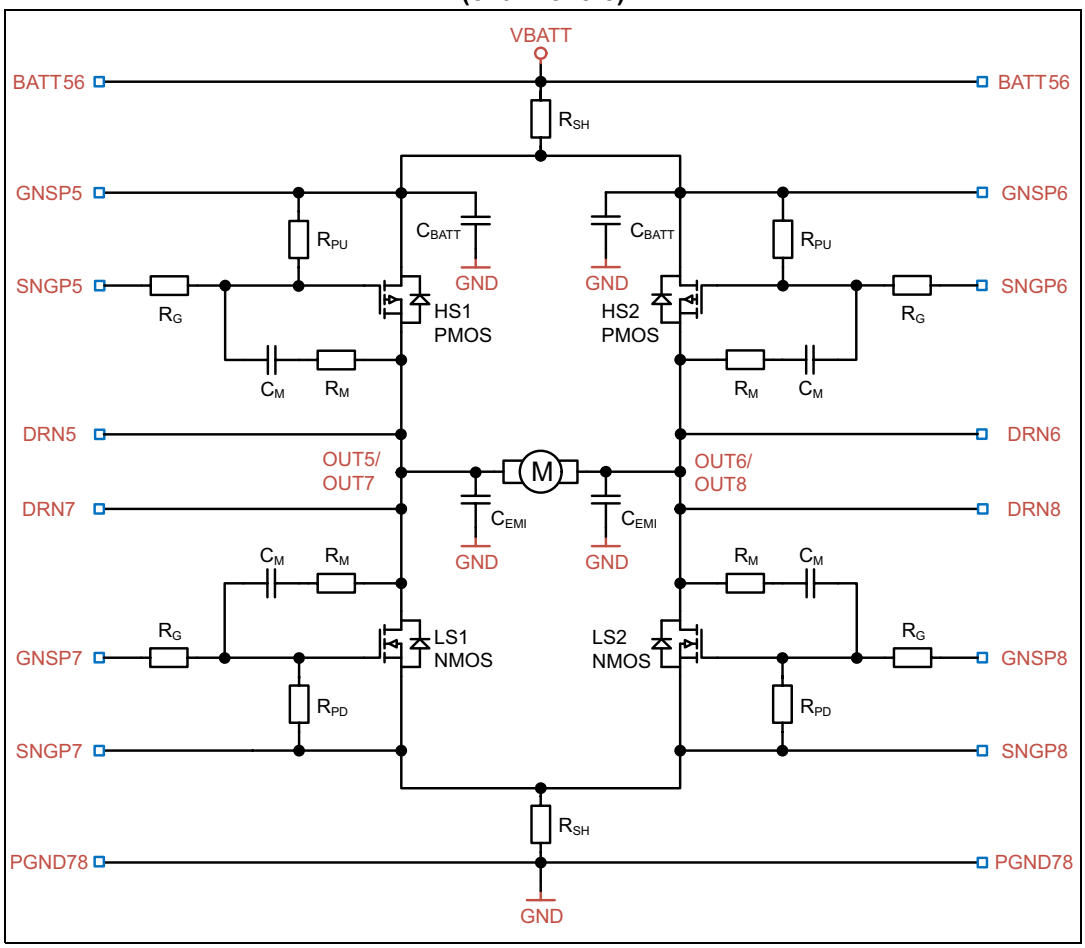


Figure 2. Example of H-bridge configuration with PMOS as HS transistors (channel 5-8)



- Resistor RG is used for limiting the gate charge/discharge current in case the corresponding option is selected via the GCC_CONFIG_XX bit
- Pull-down resistors RPD are used to keep the NMOS transistors reliably OFF in case of output three-state
- Pull-up resistors RPU are used to keep the PMOS transistors reliably OFF in case of output three-state
- Miller capacitors CM and resistors RM are mounted between transistor gate and drain to improve EMI behavior

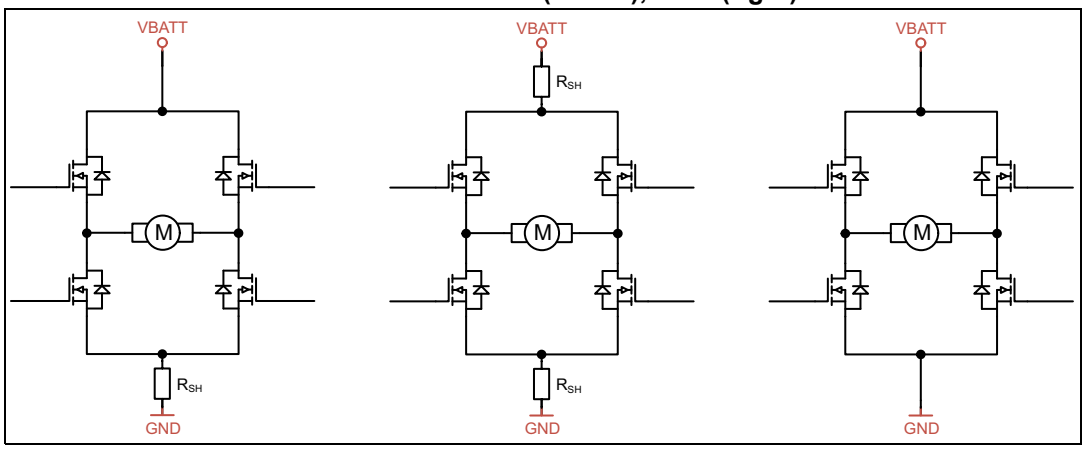
The over current detection (OC) can be performed either by measuring the voltage drop on shunt resistors or through a Drain to Source Measurement (DSM). Different scenarios for OC detection are possible (see *Figure 3*):

- OC detection through one shunt resistor RSH mounted on the low-side (between SNGPx and PGNDxx pins) and DSM used for OC detection on high-side transistors
- OC detection through two shunt resistors RSH. The first mounted on the low-side (between SNGPx and PGNDxx pins) and the second mounted on the high-side (between GNSPx and BATTxx pins for PMOS transistors or between DRNx and

BATTxx pins for NMOS transistors). These two shunt resistors must be equal to avoid inhomogeneous OC threshold for the H-bridge (*Figure 1* and *Figure 2*)

- OC detection through DSM on both low-side and high-side

Figure 3. OC detection strategies: shunt resistor for LS and DSM for HS (left), two shunt resistors (center), DSM (right)



2 L9945 configuration

To allow valid operation of the L9945 in H-bridge mode, the device must be configured in proper way. The configuration is operated via SPI commands. It is always mandatory to:

- Select HS configuration (PMOS/NMOS) via the N_P_CONFIG_XX bit
- Enable all used channels via the EN_OUT_XX bit
- Enable H-bridge via the HBX_CONFIG

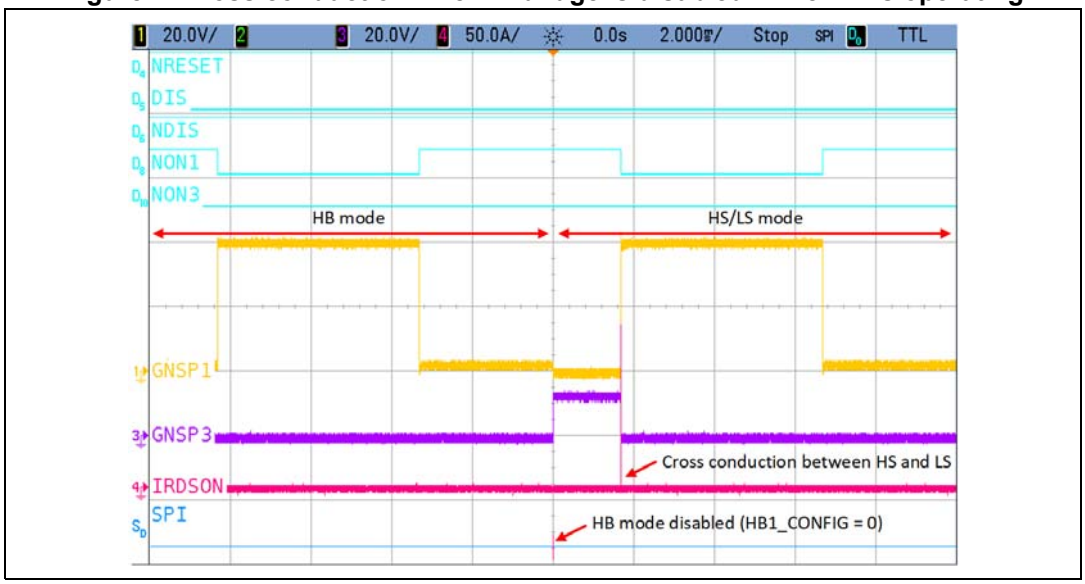
To guarantee safe and correct functionality of the output pre-drivers, the L9945 offers a wide range of possibilities which can be configured:

- ON state / OFF state diagnostic filter times, programmable via TBLANK_OC_XX / TDIAG_CONFIG_XX bit
  - The HBX_TDIAG_EXT_CONFIG extends the CH1/CH5 OFF state diagnostic filter time to other channels involved in the same H-Bridge
- Current limitation feature, activated via HBX_ILIM_EN and selectable through OC_CONFIG_03 (HB1) or OC_CONFIG_07 (HB2) bit
- "Several switching parameters
  - The dead time between FETs on the same branch can be programmed via the HBX_DEAD_TIME bit
  - The gate charge/discharge currents can be selected via the GCC_CONFIG_XX bit

2.1 Enabling of H-bridge

The H-bridge configuration is enabled by setting HBx_CONFIG bit to 1. The H-bridge mode shouldn't be disabled (HBx_CONFIG = 0), while H-bridge is operating, to avoid potential cross-conduction between HS and LS channels (see Figure 4).

Figure 4. Cross conduction when H-bridge is disabled while HB is operating



2.2 HW configuration

It is necessary to configure the device to be in line with mounted HW configuration. When H-bridge mode is selected (HBx_CONFIG = 1), MOSFET side of corresponding output channels is automatically configured as described in *Chapter 1*. The value in LS_HS_CONFIG_XX is therefore fixed and any attempt to modify it via SPI is ignored.

The MOSFET type (N_P_CONFIG_XX bit) of LS channels is also fixed and locked to NMOS. The only HW configuration which is necessary to perform is selection of MOSFET type for HS channels (NMOS / PMOS).

Outputs are in three-state until they are configured and enabled. All involved output channels must be therefore enabled prior to use by setting EN_OUT_XX bit to 1.

2.3 H-bridge diagnostic

The device performs two types of diagnostic: OFF state and ON state diagnostic. H-bridge status can be then monitored by reading each channel diagnostic as if they operated independently. Diagnostic report for all channels is readable via SPI frame 0x9AAA0001 if diagnostic is enabled by ENABLE_DIAGNOSTIC bit. If ENABLE_DIAGNOSTIC = 0, diagnostic for all outputs is read as "No diagnostic done".

Channel diagnostics are mainly performed as they operated independently, and they are described in detail in a dedicated application note [2] (see *Table 12*). However, some additional features have been implemented for H-bridge configuration.

2.3.1 OFF state diagnostic

The device performs OFF state diagnostic during OFF phase of the dedicated channel. OFF state diagnostic is used for monitoring if the output node is floating (open load) or if the output node is shorted to ground (for LS configuration) or to battery (for HS configuration).

The device offers the possibility to select an OFF state diagnostic filter time tDIAG and current capability of an internal regulator that regulates voltage of an output node VOUT. Selection of proper values of these parameters is crucial for a correct function of the OFF state diagnostic (refer to [2] see *Table 12*).

There are two different strategies for selection of OFF state diagnostic filter time. They are selectable via HBX_TDIAG_EXT_CONFIG bit. When HBX_TDIAG_EXT_CONFIG = 0, the diagnostic filter time tDIAG selected for CH1 (CH5) is automatically extended to all channel member of the bridge. When HBX_TDIAG_EXT_CONFIG = 1, the diagnostic filter time tDIAG must be set individually for each channel. Regardless of the selected strategy, the tDIAG filter time can be programmed via TDIAG_CONFIG_XX bit (see *Table 1*). Current capability of the internal regulator is selectable via DIAG_I_CONFIG_XX (see *Table 2*).

Table 1. OFF state diagnostic timings for H-bridge

HBX_TDIAG_EXT_CONFIG	TDIAG_CONFIG_0X [1:0]	Dead time [µs]			Comment
		min	typ	max	
0	00	10	11.2	12.4	All channels of HB1 set as CH1 All channel of HB2 set as CH5
	01	26	28.9	31.8	
	10	36	40	44	
	11	46	51.2	56.4	
1	00	23	25.6	28.2	Channels to be set individually
	01	55	61.2	67.4	
	10	95	105.6	116.2	
	11	135	150	165	

Table 2. Selection of current capability of Vout regulator

DIAG_I_CONFIG_0X	Current capability Idiag [mA]	
	Min	Max
0	0.06	0.1
1	0.6	1

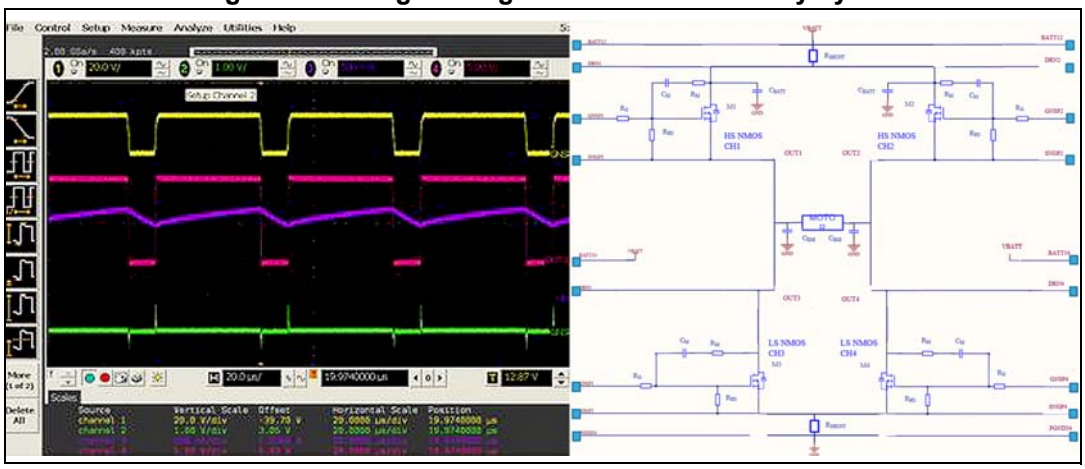
OFF state diagnostics are performed and reported only if the driving PWM signal applied on the NON1 (NON5) input guarantees an OFF time interval smaller than the programmed t_{DIAG}. Consider *Figure 5* as an example where the motor is being driven at high speed (high duty cycle value, 85%):

- The yellow curve plots CH1 gate signal. The OFF time is less than the smallest t_{DIAG} (11.2 us). Hence, CH1 diagnostic latches will always hold the value determined by ON state diagnostics (No OC)
- The pink curve plots node 1 signal (CH3 drain DRN3). Every time DRN3 falls below the OL threshold V_{OL}, the t_{DIAG} is triggered and restarted on CH3 in order to verify the presence of a STG. However, since the OFF period is too small, diagnostics are not accomplished and CH3 diagnostic latches will hold the last valid value determined in OFF state (most probably NO OL/STG/STB in a Normal condition)

Following these two recommendations will guarantee a safe operation also for high duty-cycle values:

- Always read OFF state diagnostics before starting the motor, to guarantee that H-Bridge output nodes are correctly connected to the load
- When reaching critical duty-cycle values, determining an OFF period smaller than t_{DIAG}, a periodical OFF diagnostic pulse (via SPI COMMAND 9) on the HS FET is recommended to verify the presence of short-to-battery failures on the H-Bridge outputs

Figure 5. Driving H-bridge at 20kH and 80% duty-cycle



2.3.2 ON state diagnostic

The device performs ON state diagnostic during ON phase of the dedicated channel. ON state diagnostic is used for detection of over current (OC).

Different scenarios for OC detection are possible (refer to *Chapter 1*). The over current detection can be performed either by measuring the voltage drop on external shunt resistors or through the Drain to Source Measurement of each transistor. Regardless of the selected strategy, OC sensing strategy must be set individually for each channel via OC_DS_SHUNT_XX bit.

The device offers the possibility to select an ON state diagnostic blanking time t_{BLANK_OC}. Selection of the proper value of the filter blanking time is a crucial for a correct function of the ON state diagnostic. When t_{BLANK_OC} is not correctly set, wrong diagnostics will be reported. For instance, a t_{BLANK_OC} smaller than the VDS settling time can cause false detection of OC in DSM mode. In order to understand how to program t_{BLANK_OC} filter time refer to [2] (see *Table 12*). The t_{BLANK_OC} filter time can be programmed via TBLANK_OC_XX bit (see *Table 3*).

Table 3. OC detection timings

TBLANK_OC_XX [0:0]	No OC blanking time [µs]		
	min	typ	max
000	10	11.1	12.2
001	14	15.6	17.1
010	18	20	22
011	28	31.1	34.2
100	39	42.2	46.5
101	48	53.3	58.7
110	88	97.8	107.6
111	128	142.2	156.5

OC threshold is programmable for each channel via OC_CONFIG_XX bit (see *Table 4*). It must be selected according to the *Equation 1*

Equation 1- Programming of the OC threshold

$$V_{OC} = R_{OC} * I_{OC}$$

Where:

- I_{OC} is the maximum current for the given application
- R_{OC} is either resistance of the shunt resistor RSH or drain-source on-resistance of the external MOSFET R_{DSon} (depending on the selected OC sensing strategy)

Table 4. OC threshold selection

OC_CONFIG_XX [5-0]	Min.	Max.	Min.	Max.	Unit
	LS		HS		
0	53	67	53	69	mV
1	68	82	68	85	mV
2	83	97	83	101	mV
3	97	113	99	117	mV
4	113	128	113	133	mV
5	128	143	129	150	mV
6	142	158	144	166	mV
7	157	173	159	182	mV
8	172	188	172	198	mV
9	186	204	189	214	mV
10	201	220	204	231	mV
11	216	235	219	247	mV
12	231	250	234	263	mV
13	246	266	248	279	mV
14	261	281	264	295	mV
15	275	296	278	311	mV
16	290	311	290	326	mV
17	305	327	305	341	mV
18	320	343	320	356	mV
19	334	358	338	375	mV
20	349	374	351	391	mV
21	364	389	367	407	mV
22	379	405	382	423	mV
23	393	420	397	439	mV
24	408	436	412	455	mV

Table 4. OC threshold selection (continued)

OC_CONFIG_XX [5-0]	Min.	Max.	Min.	Max.	Unit
	LS		HS		
25	423	451	427	471	mV
26	438	467	442	488	mV
27	453	482	456	504	mV
28	467	498	472	520	mV
29	482	513	486	536	mV
30	497	529	501	552	mV
31	512	544	515	568	mV
32	526	559	525	579	mV
33	541	575	545	595	mV
34	556	590	560	612	mV
35	570	606	575	628	mV
36	585	621	590	644	mV
37	600	637	604	660	mV
38	614	653	619	676	mV
39	629	668	634	693	mV
40	644	684	649	708	mV
41	658	699	663	724	mV
42	673	715	679	740	mV
43	688	730	693	756	mV
44	702	746	708	772	mV
45	717	761	723	788	mV
46	732	777	738	804	mV
47	746	792	753	821	mV
48	761	808	767	836	mV
49	776	823	782	852	mV
50	791	839	797	868	mV
51	806	854	812	885	mV
52	820	870	827	900	mV
53	835	885	842	916	mV
54	849	900	856	933	mV
55	864	916	871	949	mV
56	878	931	886	964	mV
57	893	947	900	981	mV

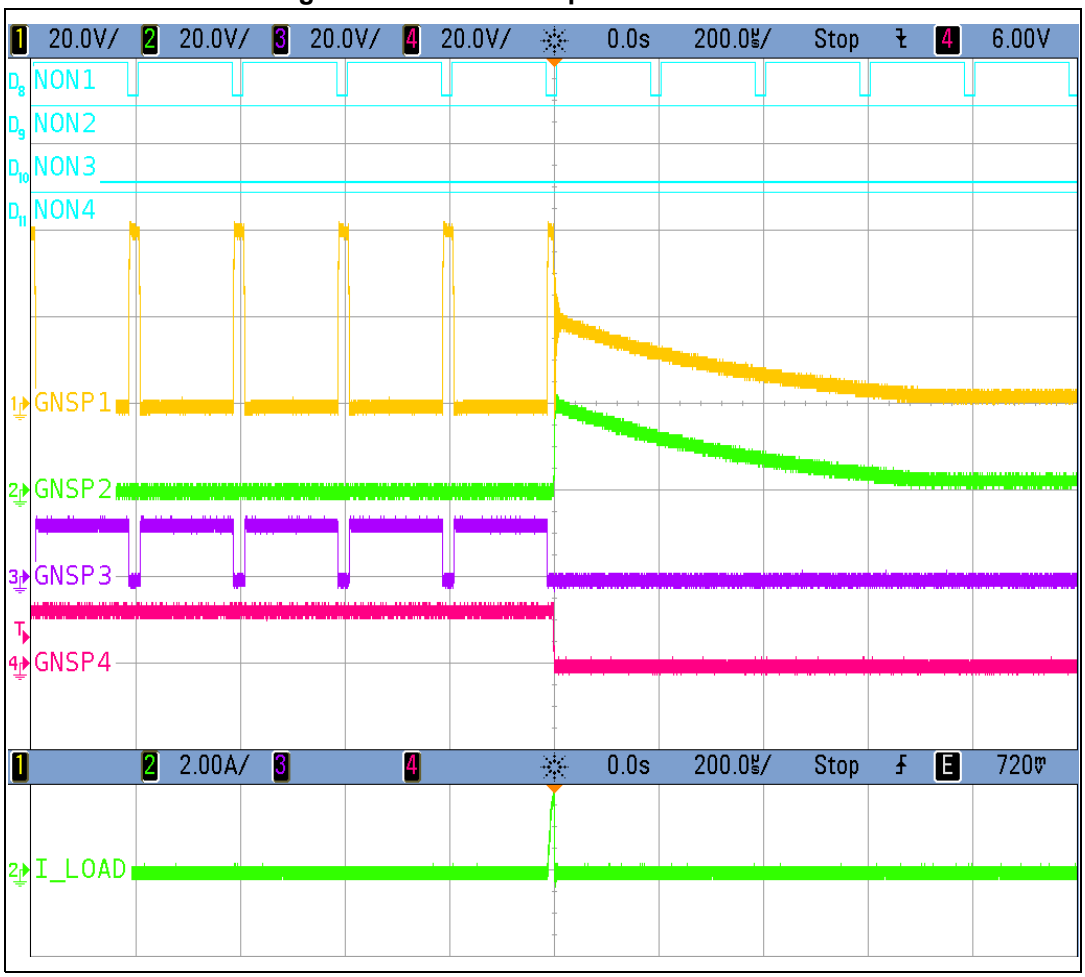
Table 4. OC threshold selection (continued)

OC_CONFIG_XX [5-0]	Min.	Max.	Min.	Max.	Unit
	LS		HS		
58	908	962	916	997	mV
59	922	977	930	1013	mV
60	937	992	946	1029	mV
61	951	1008	960	1045	mV
62	967	1023	975	1061	mV
63	982	1038	987	1078	mV

Programmed OC threshold can be compensated against battery and temperature variations on each channel. Compensation against battery variations is enabled / disabled via OC_BATT_COMP_XX bit. Two compensation factors, respectively for Passenger Vehicle (PV, 12 V) and Commercial Vehicles (CV, 24 V) are available and selectable via BATT_FACT_CONFIG. Compensation against temperature variations can be set via OC_TEMP_COMP_XX bit. The OC_READ_XX bit selects whether reading the original threshold or the compensated one. For more information about the compensation against battery and temperature variations please refer to [1] (see *Table 12*)

If an OC event occurs on the channel, while current limitation feature is disabled, all channels of the H-bridge will be actively shut-off and the H-bridge outputs will be three-stated (see *Figure 6*).

Figure 6. Shutoff of outputs after OC event



To prevent MOSFET damage, the device implements a configuration override that allows an ultra-fast shutdown in case of overcurrent. In fact, a higher shut-off current will be used in respect to the one programmed in the GCC_CONFIG_XX. It is possible to select the entity of current increase in case of OC by programming the GCC_OVERRIDE_CONFIG bit, as shown in *Table 5*. The settings is common between all channels

Table 5. Gate charge / discharge currents strategy

GCC_override_config	GCC in normal operation [mA]	Shut-off current [mA]
0	1	5
	5	20
1	1	20
	5	20

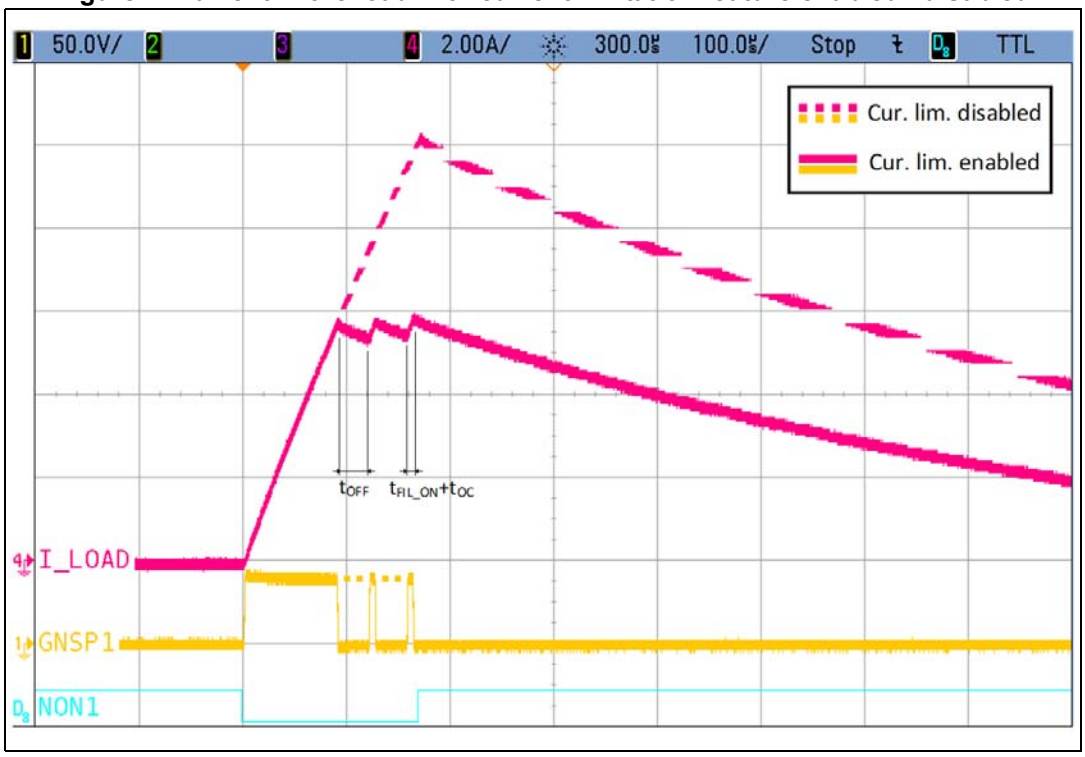
After an OC event, the H-bridge must be manually re-enabled. Outputs are re-engaged after diagnostic readout via SPI. Configuration of PROT_CONFIG_XX bit and

DIAGNOSTIC_ENABLE bit has no influence on the re-engagement strategy in H-bridge mode.

2.4 Current limitation feature

A current limitation feature allows limiting the maximum current in the load modulating NPWM signal, as shown in *Figure 7*. It can be activated by setting HBX_ILIM_EN = 1. This feature is available only if over current detection is performed via shunt resistors.

Figure 7. Current in the load with current limitation feature enabled / disabled



Current limitation threshold (I_LIM_th) is set by OC_CONFIG_03 [5-0] bit for H-bridge 1 and OC_CONFIG_07 [5-0] bit for H-Bridge 2. Hence, channel 3 (7) is no longer used for OC detection, but it activates the current limitation.

If the current stays above the programmed threshold (ILIM_th) longer than tOC, the H-bridge is driven into freewheeling phase for a programmable OFF time (tOFF). The tOFF is selectable via SPI according to HBX_TOFF bit (see *Table 6*). Once tOFF expires, load current is compared against ILIM_th threshold:

- In case load current is below ILIM_th, normal operation can continue
- In case current is not below ILIM_th, the high-side channel is turned on for a tFIL_ON + tOC period and then turned off for another tOFF time. Such operation continues until either the current decreases below ILIM_th or the current reaches the overcurrent threshold. If the overcurrent threshold is reached, H-Bridge is three-stated (refer to *Figure 8*)

Figure 8. OC threshold reached when current limitation is enabled

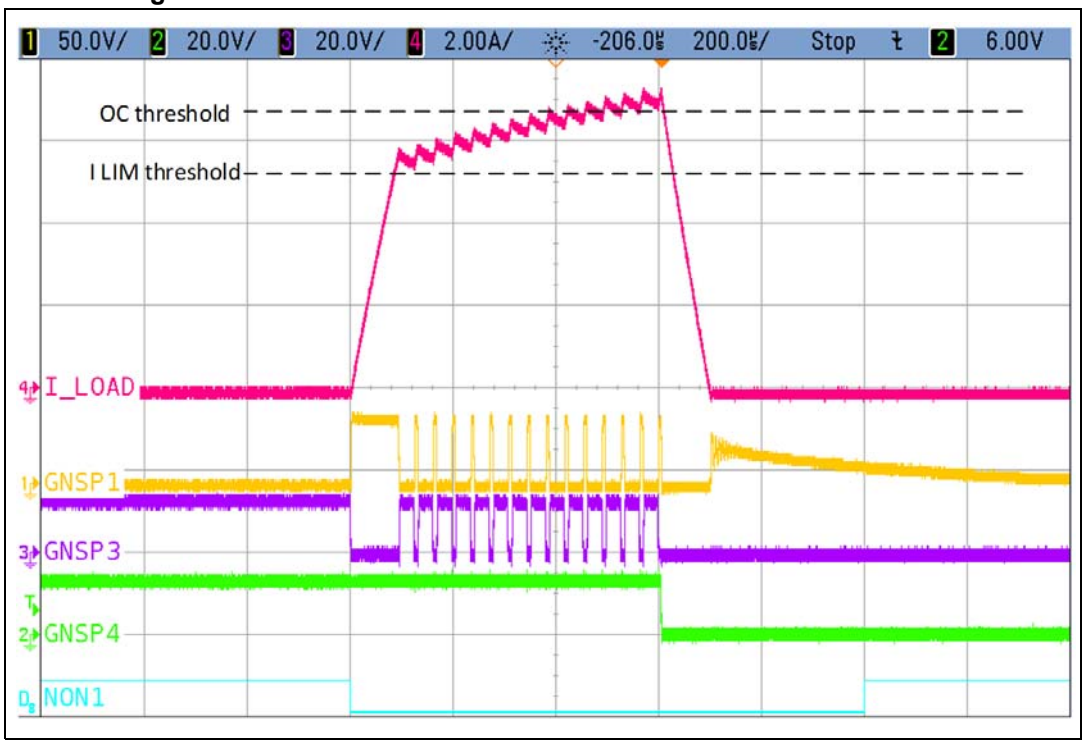


Table 6. tOFF selection

HBX_TOFF [1:0]	OFF time [µs]		
	min	typ	max
00	28	31	34
01	42	48	52
10	56	62.5	70
11	110	125	140

2.5 Switching parameters

It's possible to choose different dead time values for both H-bridges independently to prevent cross-conduction between HS and LS channels. Such parameters are selectable via SPI through the HBX_DEAD_TIME bit according to the following *Table 7*.

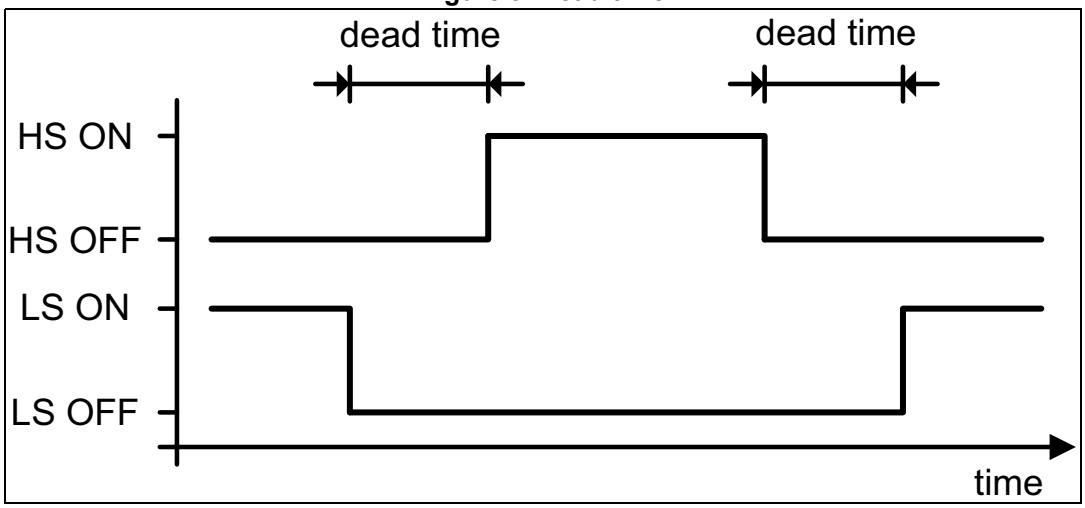
Table 7. Dead time values

HBX_DEAD_TIME [1:0]	Dead time [us]		
	min	typ	max
00	0.5	1	1.5
01	1	2	3

Table 7. Dead time values (continued)

HBX_DEAD_TIME [1:0]	Dead time [us]		
	min	typ	max
10	3	4	5
11	7	8	9

Figure 9. Dead time

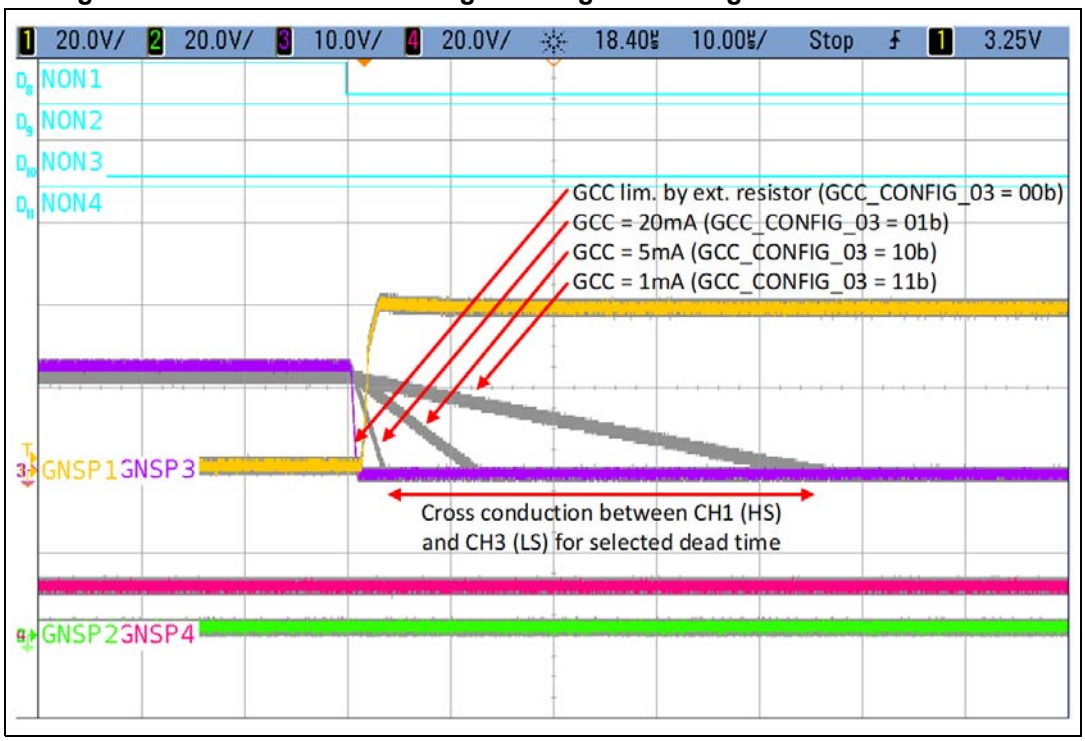


It's possible to choose different gate charge / discharge currents for every channel via SPI through GCC_CONGIG_XX bit according *Table 8*. Gate charge/discharge currents can be either constant (with specific value) or limited by external resistor (see *Figure 10*). They should be selected with respect to the selected dead time to avoid cross-conduction between HS and LS channels. If strategy with limitation of gate charge / discharge current by external resistor is selected, an external resistor must be mounted between gate of the transistor and the output of the L9945.

Table 8. Gate charge / discharge currents strategy

GCC_config_0x [1:0]	GCC strategy
00	Current limited by external resistor
01	20 mA
10	5 mA
11	1 mA

Figure 10. Selection of different gate charge / discharge currents of channel 3



The freewheeling is performed on low side. Two different freewheeling strategies can be selected with the SPI bit HB_X_AFW (see *Figure 11*). If HB_X_AFW = 0, passive freewheeling through MOSFET body-drain diode is performed. If HB_X_AFW = 1, active freewheeling through MOSFET channel is performed.

3 L9945 control by external microcontroller

3.1 Correct handling of disable sources

There are several disable sources implemented in order to guarantee safety and correct functionality of the output pre-drivers. Correct handling of these disable sources is a prerequisite for valid operation of the H-bridge.

It is necessary to drive correctly external disable pins DIS and NDIS, control pin EN6 and reset pin NRES by external microcontroller. After power-on microcontroller should:

- Set high NRES signal
- Set low DIS signal
- Set high NDIS signal
- Set high EN6 to enable channel 6 for driving H-bridge 2

Next prerequisite for the correct functionality of the output pre-drivers is proper service of Communication Check (CC) (for more info refer to [1] see *Table 12*). The Communication Check monitors the SPI communication and in case of no valid communication or continuous communication failures, a CC_LATCH bit is set and all related outputs are disabled. The Communication Check is active by default, but it can be deactivated with SPI command CONFIG_CC = 10b.

Before driving output pre-drivers, it's recommended to check

- If outputs are not being disabled by any disable source. It is recommended to perform two consecutive SPI read via Command 10 in order to verify that all relevant faults (latches) are cleared. Summary of all disable sources and fault events with effects on outputs is shown in *Table 9*
- If H-Bridge output nodes are not shorted to GND/VBATT, by enabling output drivers and reading OFF state diagnostics

Table 9. Summary of disable sources and faults

Event	Effect on CH1-CH5, CH7 – CH8	Effect on CH6
DIS assertion	Actively OFF(1)	Actively OFF(1)
NDIS assertion	Actively OFF(1)	Actively OFF(1)
EN6 set low	No effect	Actively OFF(1)
NRES assertion	Actively OFF(2)	Actively OFF(2)
VPS undervoltage	Actively OFF(1)	Actively OFF(1)
Charge pump undervoltage	Actively OFF(1)	Actively OFF(1)
VDD5 overvoltage	Actively OFF(2)	Actively OFF(2)
VDD5 undervoltage	Actively OFF(1)	Actively OFF(1)
BIST ongoing	Three-state	Three-state
BIST failed	Actively OFF(2)	Actively OFF(2)
HWSC ongoing	Actively OFF	Actively OFF
HWSC failed	Actively OFF(2)	Actively OFF(2)
Disable via SPI (En_OUT_xx)	Three-state(2)	Three-state(2)

Table 9. Summary of disable sources and faults (continued)

Event	Effect on CH1-CH5, CH7 – CH8	Effect on CH6
Disable via SPI (Prot_disable_xx)	Actively OFF(2)	Actively OFF(2)
CC failed	Actively OFF(2)	Actively OFF(2)
OC failure	Actively OFF(2)	Actively OFF(2)
STG / STB failure	No effect	No effect
OL failure	No effect	No effect
ON pulse request	Actively ON(1)	Actively ON(1)
OFF pulse request	Actively OFF(1)	Actively OFF(1)

1. automatic re-engagement
2. manual re-engagement

3.2 Driving of H-bridge

The device in H-bridge configuration must be controlled via external NONx pins. Any attempt to control channels via SPI is ignored while H-bridge mode is active.

If the device is configured in H-bridge mode, alternative functions are assigned to NONx inputs. The assignment of these alternative functions to NONx inputs is listed in *Table 10*. The motor direction can be chosen with the Direction input (DIR), the duty cycle and frequency with the NPWM input. All MOSFET's can be actively switched-off with the High impedance input (HiZ).

Table 10. Assignment of alternative functions to NONx inputs in H-bridge configuration

HB1	HB2	Alternative function of NONx inputs in H-bridge mode
NON1	NON5	NPWM (Negative asserted Pulse Width Modulation signal)
NON2	NON6	DIR (Direction signal)
NON3	NON7	HiZ (High impedance)
NON4	NON8	Not used

Driving combinations of H-bridge are shown on *Figure 11* and in *Table 11*.

Table 11. H-bridge control truth table

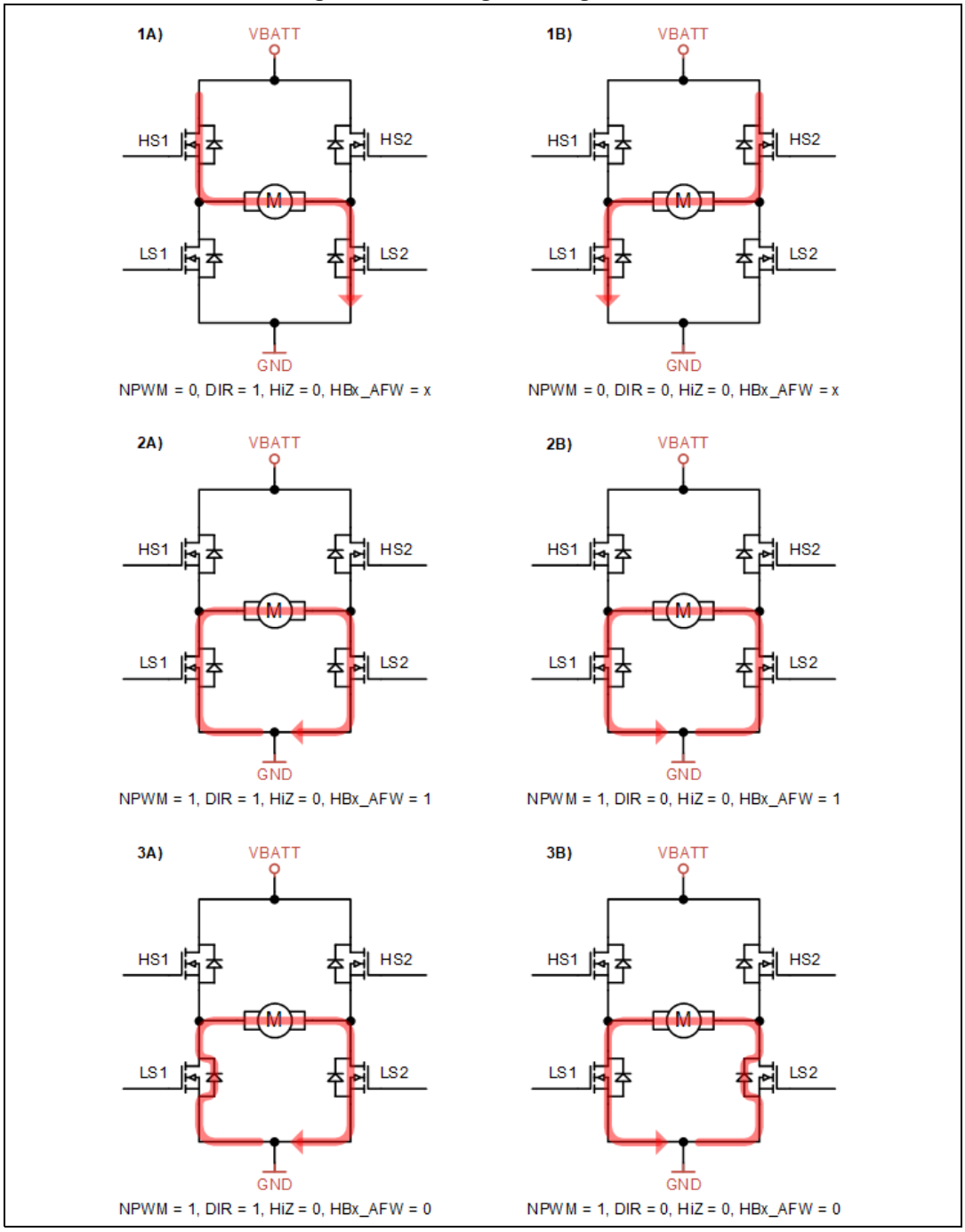
HiZ	DIR	NPWM	HBx_AFW	HS1	HS2	LS1	LS2	Load's driving mode
0	0	0	X(1)	OFF	ON	ON	OFF	Reverse
0	0	1	0	OFF	OFF	ON	OFF	Freewheeling (reverse)
0	0	1	1	OFF	OFF	ON	ON	Active freewheeling (reverse)
0	1	0	X(1)	ON	OFF	OFF	ON	Forward
0	1	1	0	OFF	OFF	OFF	ON	Freewheeling (forward)

Table 11. H-bridge control truth table (continued)

HiZ	DIR	NPWM	HBx_AFW	HS1	HS2	LS1	LS2	Load's driving mode
0	1	1	1	OFF	OFF	ON	ON	Active freewheeling (forward)
1	X(1)	X(1)	X(1)	OFF	OFF	OFF	OFF	High Impedance

1. don't care

Figure 11. H-bridge driving modes



4 Reference documents

Table 12. Reference documents

Ref	Document name	Document type
1	L9945	Datasheet
2	Criteria for configuring L9945 diagnostic parameters in automotive switching applications	Application note (AN5078)

5 Revision history

Table 13. Document revision history

Date	Revision	List of changes
22-Mar-2019	1	Initial release.