Using the STM32F334 microcontroller embedded high resolution timer to implement a 1MHz, LLC topology, digital MPPT solar converter

Introduction

This application note describes how to implement a digital solar converter using the STM32F334 microcontrollers and the high resolution timer (HRTIM1).

Effective solar power energy production requires an adaptive close-loop system. There is a fine balance to be targeted to reach the optimum result delivering the maximum power throughput. Sunshine and cloud cover vary substantially during the day leading to a large variation in the usable energy and the optimum production conditions constantly need monitoring. Other factors need to be taken into consideration such as heat dissipation issues coming from a high temperature environment and poor ventilation conditions which impact the capability of the system.

The aim of this digital MPPT solar converter (solar converter) is to address all of these requirements with one board, by providing a compact form factor demonstrator capable of reaching a high operating frequency. It implements a 1MHz LLC topology for PV DC-DC conversion. For this purpose, the design makes use of the high resolution timer (HRTIM1) embedded in the STM32F334 microcontroller, together with its analog features such as the embedded operational amplifiers and the high speed analog to digital converters.

1 General information

This document applies to the STM32F334 Arm®-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 General precautions

During assembly and operation, the digital MPPT solar converter poses several potential hazards, including bare wires and hot surfaces which may lead to serious personal injury and damage to property if the solar converter or its components are not used or installed correctly.

All transport, installation, running and maintenance operations must be performed by skilled technical personnel able to understand and implement national accident prevention regulations. For the purpose of these basic safety instructions, skilled technical personnel are suitably qualified people who are familiar with the installation, use and maintenance of power electronic systems.

1.2 Acronyms

This is a list of acronyms used in this document.

Table 1. Document acronyms

Acronym	Definition
LLC	Inductor / capacitor resonant half bridge topology
PV	Photovoltaic or in other words photoelectric
MPPT	Maximum power point tracking
CV	Power converter
DC-DC	Direct current to direct current

1.3 Digital MPPT solar converter characteristics

The system characteristics are as follows:

- Maximum input voltage: 50 V
- Minimum input voltage: 30 V
- Input voltage detection: 20 V
- Nominal input voltage: 37 V
- Nominal output voltage: 400 V
- Absolute maximum output voltage: 440 V
- Absolute maximum input current: 1.5 A
- Maximum output power: 50 W
- Minimum output power: 10 W
- Maximum output current: 125 mA
- Minimum efficiency at full load: 92%
- Maximum power point tracking (MPPT) input
- Current source output to allow parallel connections
- Effective converter size: 20 cm².

2 Solar converter operating modes and results

This section describes the solar converter operating modes, starting with the inputs, the outputs, the power switching modes and finally some operating recommendations.

2.1 Input characteristics

The input definition of the solar converter is the electric power coming from the solar panels. Power variations result in both current and voltage changes.

The objective of this converter is to extract the maximum amount of energy from solar panels, so the converter is constantly looking for the maximum power output for any given condition. As the amount of sunshine varies throughout the day, the system has to constantly adjust to these conditions. The power tracking operation is done by continuously monitoring and adjusting the input current and acquiring the corresponding input voltage. When a power drop occurs, a cloud passes by for example, the direction of the current is reversed to allow the converter to recalculate the optimum power throughput.

The optimum power setting is not determined instantly but uses a looping algorithm. This is illustrated when a DC power supply with a constant voltage is connected to the converter, the input current increases steadily as the input power increases. When the input power changes, both voltage and current change, then the input current is readjusted inline with the resulting voltage to obtain the optimum power balance.

When running at full power, the input current is clamped to 1.5 A for the selected input voltage. In these conditions, 37 V input corresponds to about 50 W output. The converter does not reach full power immediately, it takes about 45 s to reach this point from start up (jumper JP201 closed). In order to start correctly, the converter must not be supplied with any power. This means that in real life, the solar panels have to be covered up prior to the converter being started up.

The actual start up behavior is summarized in the following code:

```
P1 += Vin * Iin;
V1 += Vin;
if(--MPPT_cnt == 0)
{
   MPPT_cnt = 1000;
   if(P2 > 0)
   {
      if(P1<P2) P_dir = -P_dir;
      Icons += 2 * P_dir;
      if(Icons > 3000) Icons = 3000;
      else if(Icons < 5) Icons = 5;
   }
   else Icons += 2;
   P2 = P1;
   P1 = 0;
   V1 = 0;
}
```

Despite the fact that the input voltage is stable, the power input is not immediately determined, it has to be determined through a series of refinement loops defined by the above procedure. This procedure is run every 32 µs:

- Each cycle adds its own (Vin x Iin) product value to P1.
- When 1000 cycles are run, the value of P1 and V1, the new input power P1 is compared to the old power P2.
- The direction P_dir is inverted (i.e. becomes -1 if it was +1, and vice verse)
- Twice the P_dir value is summed to Icons which corresponds to the target input current.
- P1 then becomes P2, P1 is reset to 0 together with V1 and the cycle is repeated
- The scale factor of this variable is about 2 LSB / mA, which means that steps of +/-1 mA are applied to the input current in order to search for the point of maximum power.

The jumper JP201 allows operational control:

- When closed, the converter is operating as described above

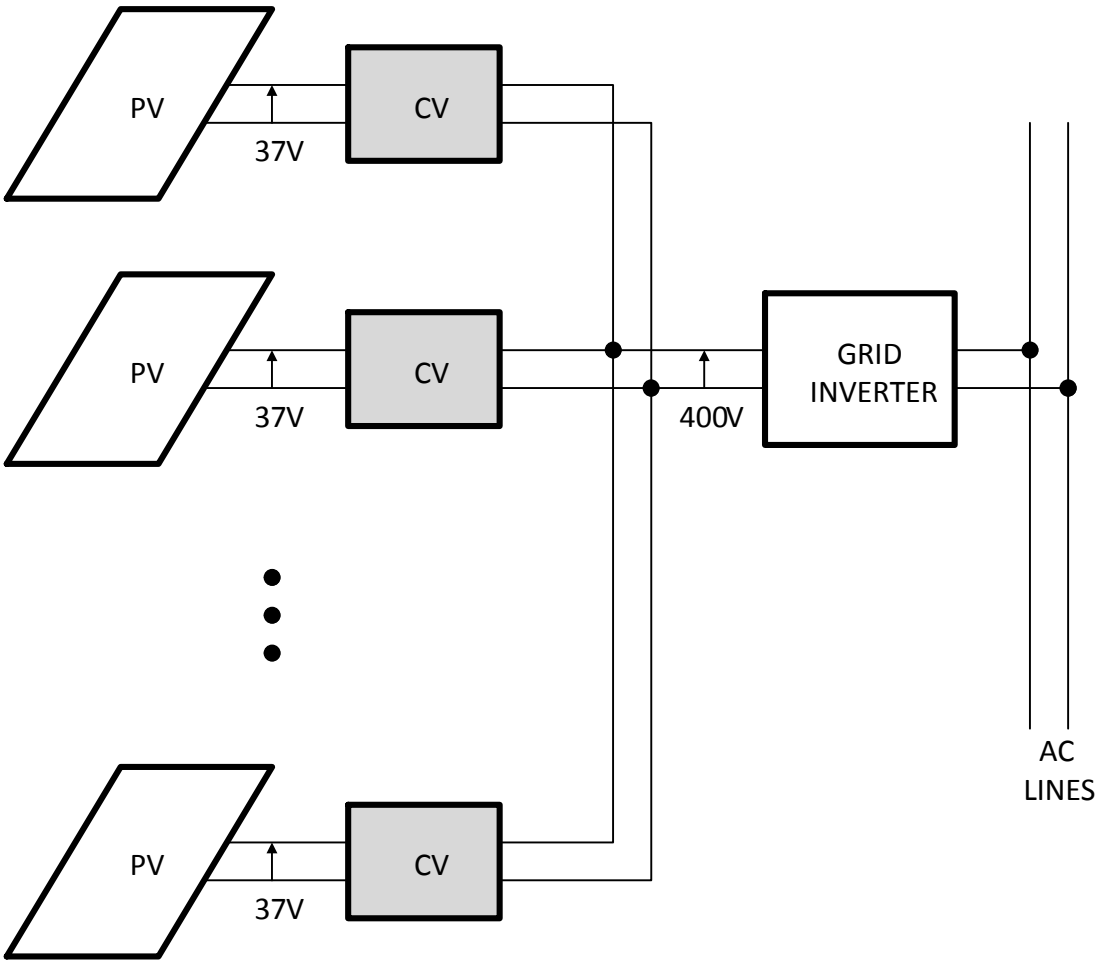
- When open, the conversion is stopped and is reset to the lowest input current value, which is approximately 20 mA.

Note: The converter does not start if the jumper JP201 is already closed when an input voltage is applied.

2.2 Output characteristics

The output is the resulting power conversion from the input discussed in Section 2.1 . One power converter (CV) manages one solar panel in the solar farm array. All the power converters are connected to a common grid inverter which sets the converter output voltage and collects the current supplied by all the power converters in the array, as illustrated in Figure 1.

Figure 1. Grid converter layout



The nominal grid converter voltage is set to 400 V and if an electronic load is used in place of the grid inverter, it has to be set at a constant voltage mode to this value.

In case the output is disconnected from the load, the voltage surge protection is triggered (see Section 3.1.5) and the converter shuts down.

It is also possible to operate the converter with a standard 440 V output supply if the load is current limited. This is done by using a resistance or an electronic load set in constant current mode. For this purpose, the code below presents two thresholds on the PA3 pin which is connected to the output of the optocoupler U101 (described in Section 3.1.1 and Section 3.1.2):

```
if(FB_temp < 0x1000) Power_off();
if(FB_temp < 0x7000) FB_mode = 1;
else if(FB_temp > 0x7200) FB_mode = 0;
if(FB_mode
{
   err = ((int32_t)FB_temp - 0x4000) >> 3;
   FB_int += err << 3;
   if(FB_int < 0) FB_int = 0;
   else if(FB_int > (3000 << 16)) FB_int = (3000 << 16);
   Icons = (FB_int >> 16) + (err >> 5);
   if(Icons < 5) Icons = 5;
}
else FB_int = ((Icons - 48) << 16);
```

FB_temp contains the sum of 8 measured samples acquired every 4µs.

- When `FB_temp` is lower than 0x1000 which corresponds to a voltage of about 0.41 V on PA3, the converter is shutdown.
- When `FB_temp` is between 0x1000 and 0x7000 (which corresponds to about 2.9 V), the converter enters voltage regulation mode by setting `FB_mode` to 1.
- The reference voltage on PA3 is set to 0x4000, that is to say half the VDDA voltage (1.65 V).

The regulation scheme is a classical proportional-integral configuration. When out of the voltage regulation mode, the `FB_int` integrator variable is maintained at the exact value which produces a seamless operation when entering this mode, as described in the last line of the code. The 48 constant value is computed as the initial value of the `err` variable, in order to keep an equivalent Icons at the start of the regulation:

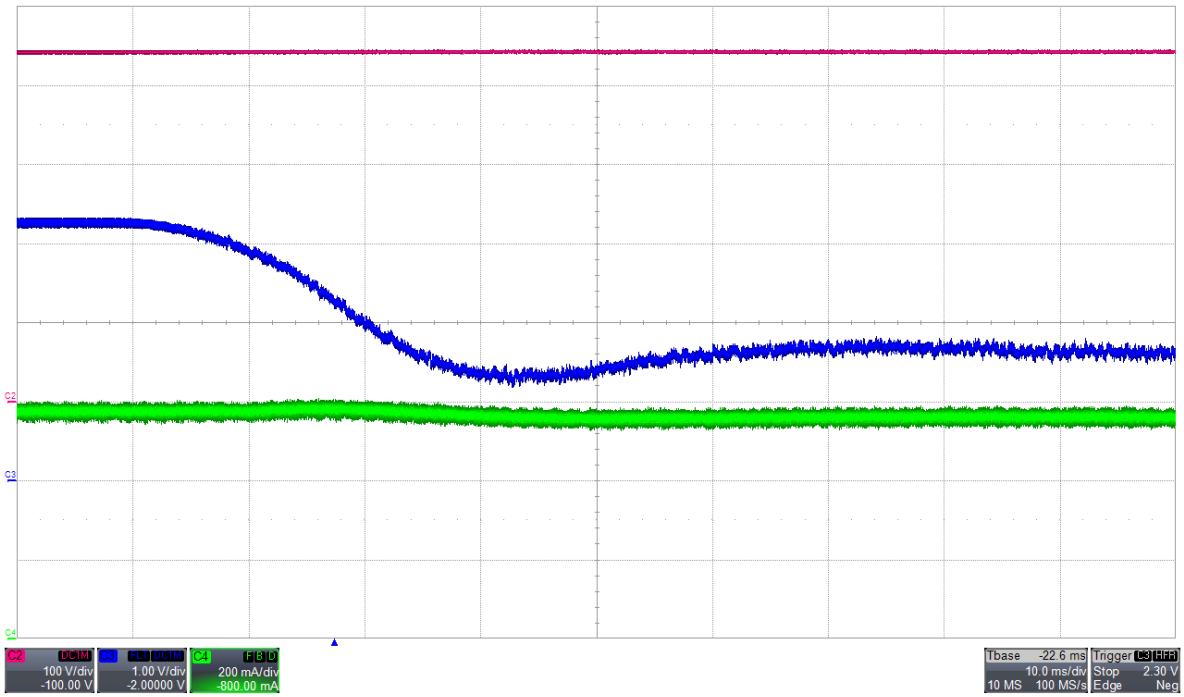
48 = (((0x7000 – 0x4000) >> 3) >>5).

The two operative modes of the output voltage surge protection are illustrated in Figure 2 and Figure 3.

The color coding for all the illustrations are:

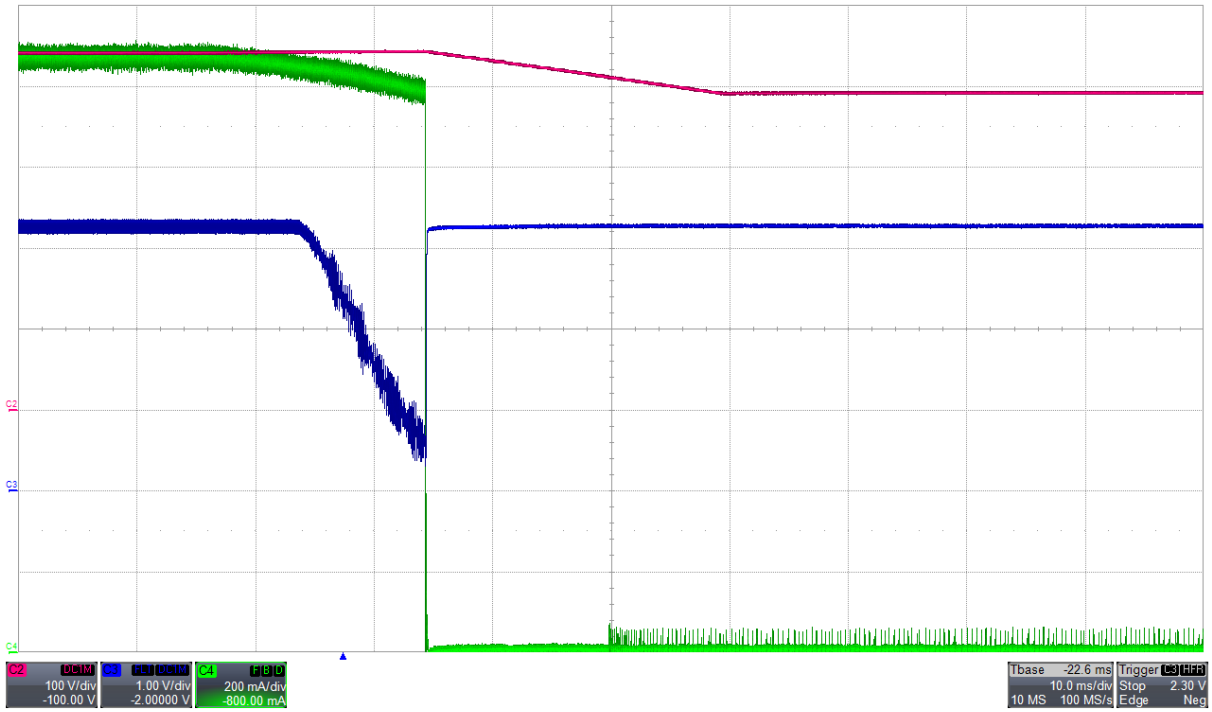
- blue: PA3 – output of optocoupler U101
- red: output voltage
- green: input current.

Figure 2. Output voltage surge protection



The CV enters constant output voltage regulation at 440 V / 40 mA as illustrated in Figure 3.

Figure 3. Constant output voltage regulation



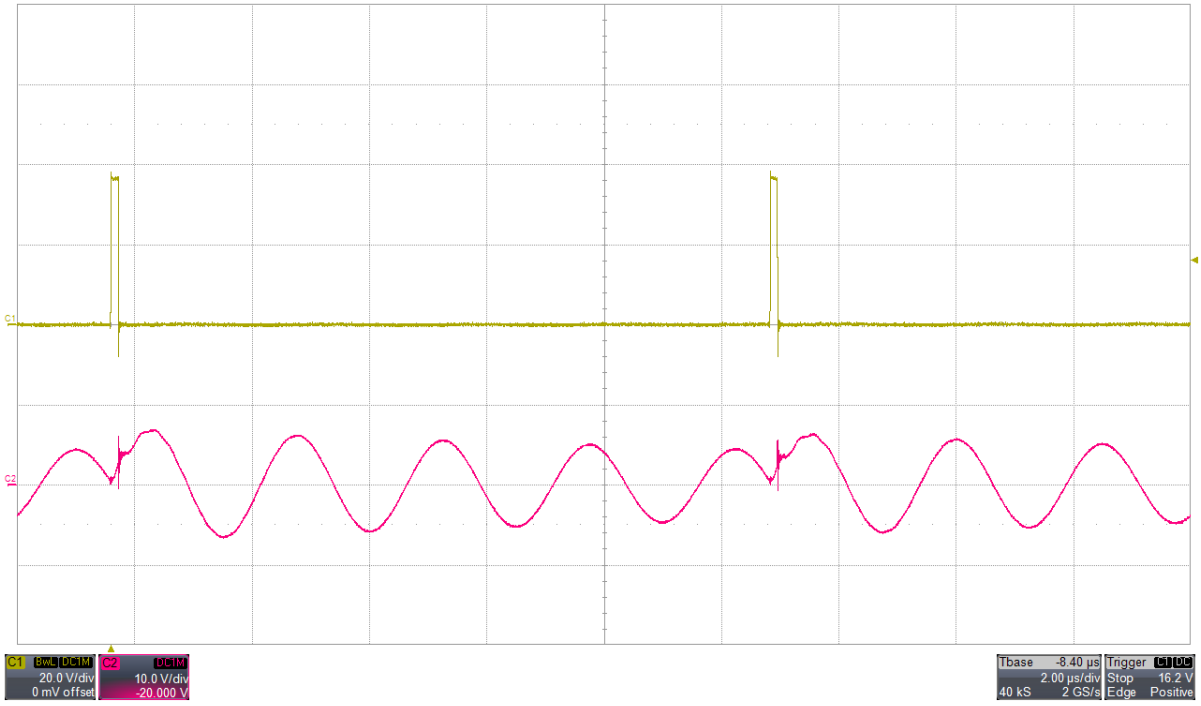
When there is a brutal load reduction, the converter switches off.

2.3 Power switching modes and efficiency

An LLC converter generally provides most efficient output at full load and performs poorly at low load where a higher operating frequency is needed to control the output power and voltage. This behavior is dramatically impacted when a large input voltage range has to be accommodated.

A special reduced power operation mode has been implemented to overcome this issue. Instead of increasing the frequency, the duty cycle is set to a very low value with an asymmetric operation. In order to keep a zero voltage switching (ZVS) characteristic, the period is set to match the LLC network resonating events for which the current in the low side switch Q102 leads to natural rising of the voltage at switch off. This is illustrated in Figure 4 waveform.

Figure 4. Reduced power operation switch mode



The trace color definition is:

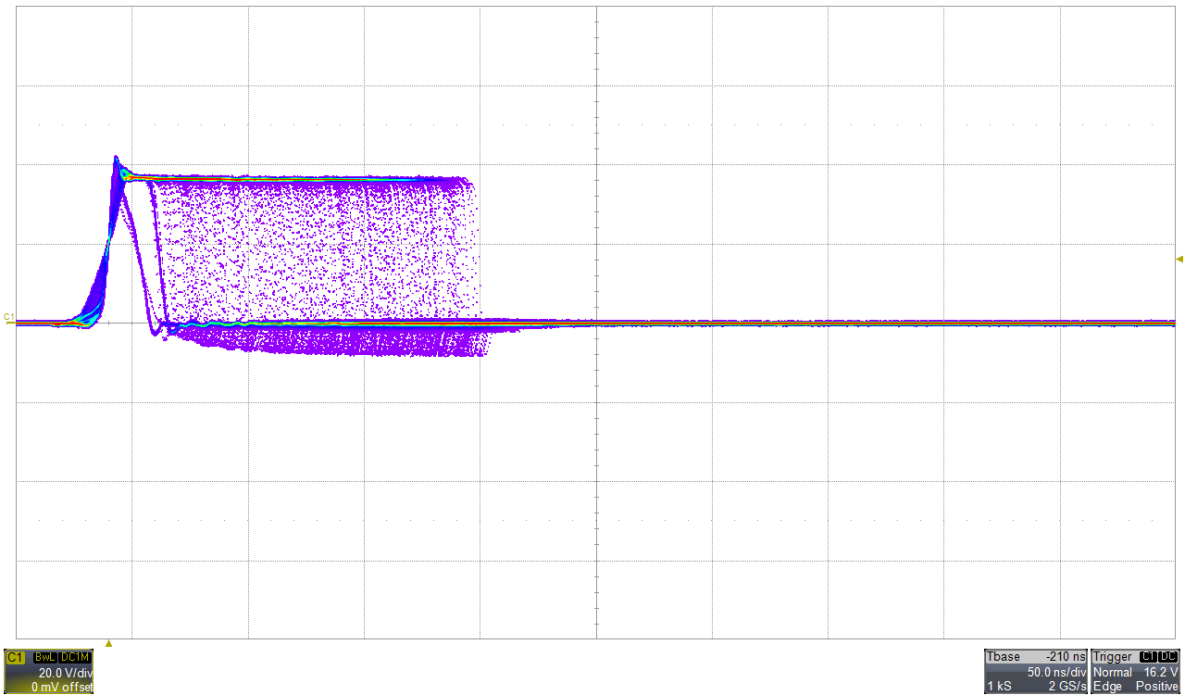
- brown: mid point of Q101-Q102 half bridge
- red: mid point of C105-C106.

When the converter starts up, the inrush current is limited by the controller. This is done by using an asymmetric mode (duty cycle in the range of a few percent), which guarantees a low input current. The turn-off of the low-side transistor Q102 is done when the C105-C106 middle point voltage is positively reaching 0V. This corresponds to maximum negative current in the primary winding of the transformer and thus maximum positive current on the Q102 drain. This ensures ZVS operation for Q102. The same applies for the high side Q101, but this is done naturally as the current increases and reverts to the opposite direction very quickly during the conduction of this switch.

Note: Refer to An introduction to LLC resonant half-bridge converter (AN2644) for more details on operating principle.

The pulse duration has to be set very accurately to ensure a correct regulation of the input current, and consequently a correct operation of the MPPT feature (see Section 2.1). Figure 5 illustrates the infinite persistence mode which shows the number of conduction periods needed during this phase.

Figure 5. Scope waveform in infinite persistence mode



With a timescale set to 50 ns/div, a resolution greater than 1 ns is needed. This is achieved using the high resolution timer embedded in the STM32F334 microcontrollers, with its base frequency set to run at the right frequency.

When the power is increased further, the converter operates in a second and then a third period as shown in the Figure 6 and Figure 7.

Figure 6. Second stage period scope plot

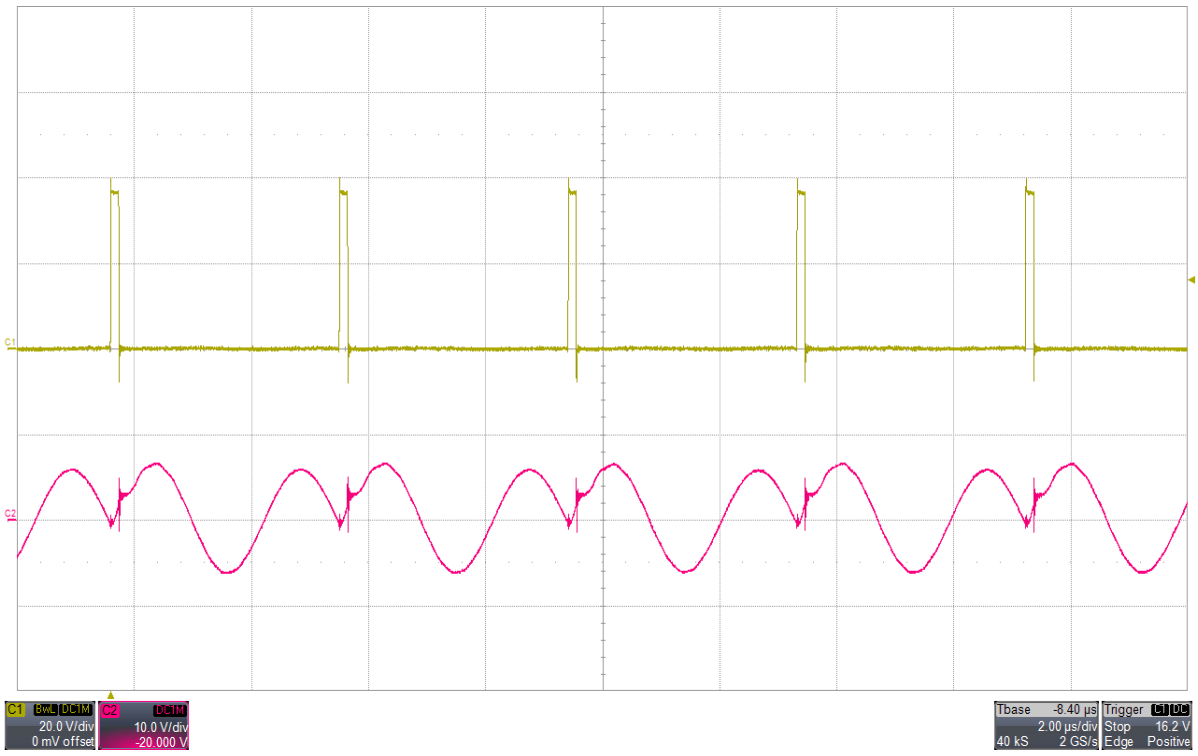
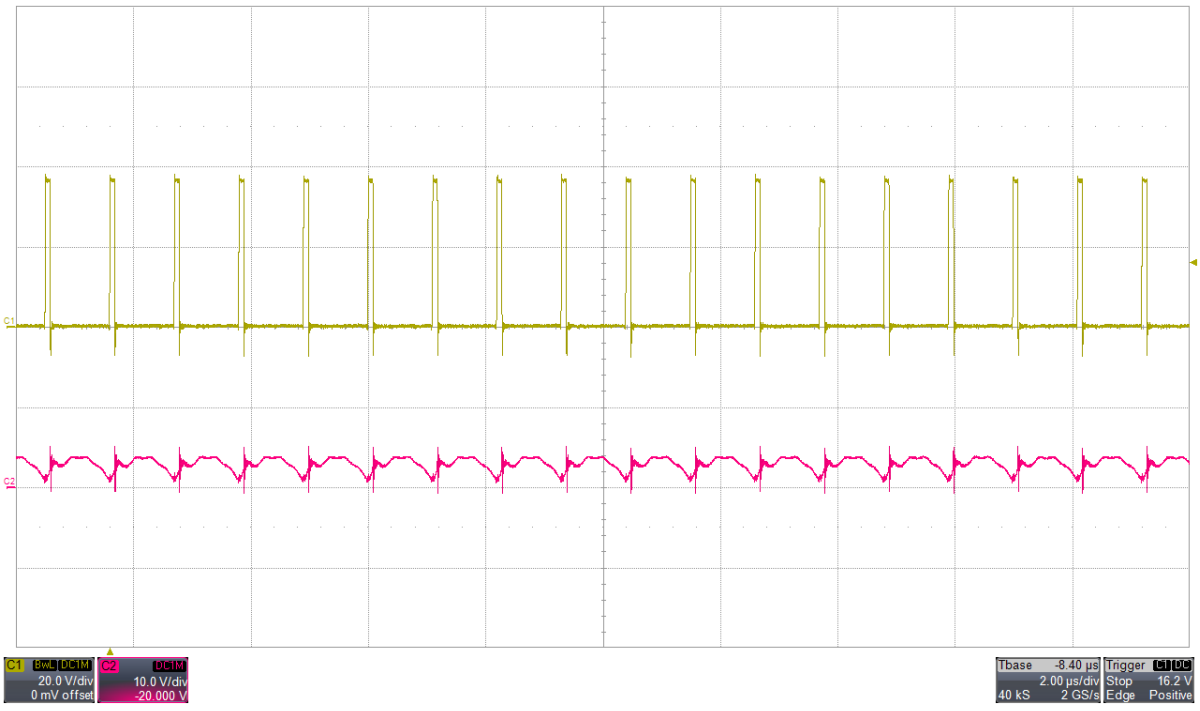


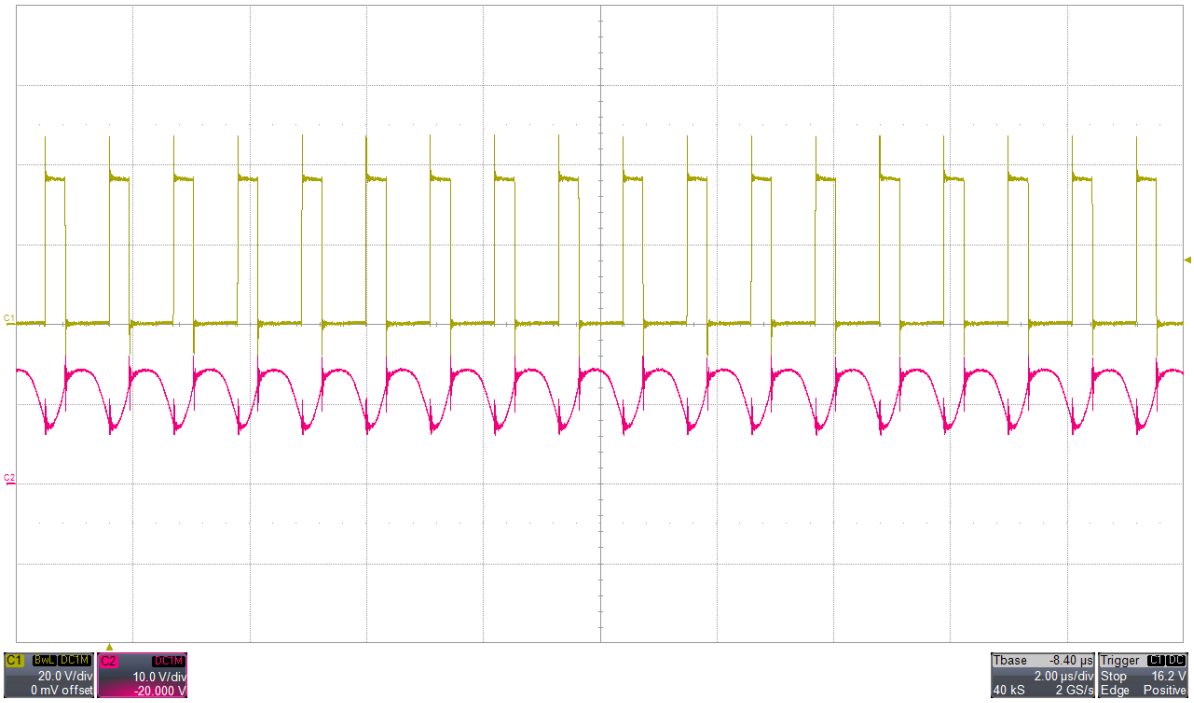
Figure 7. Third stage period scope plot



The third period corresponds to a switching frequency of about 1 MHz.

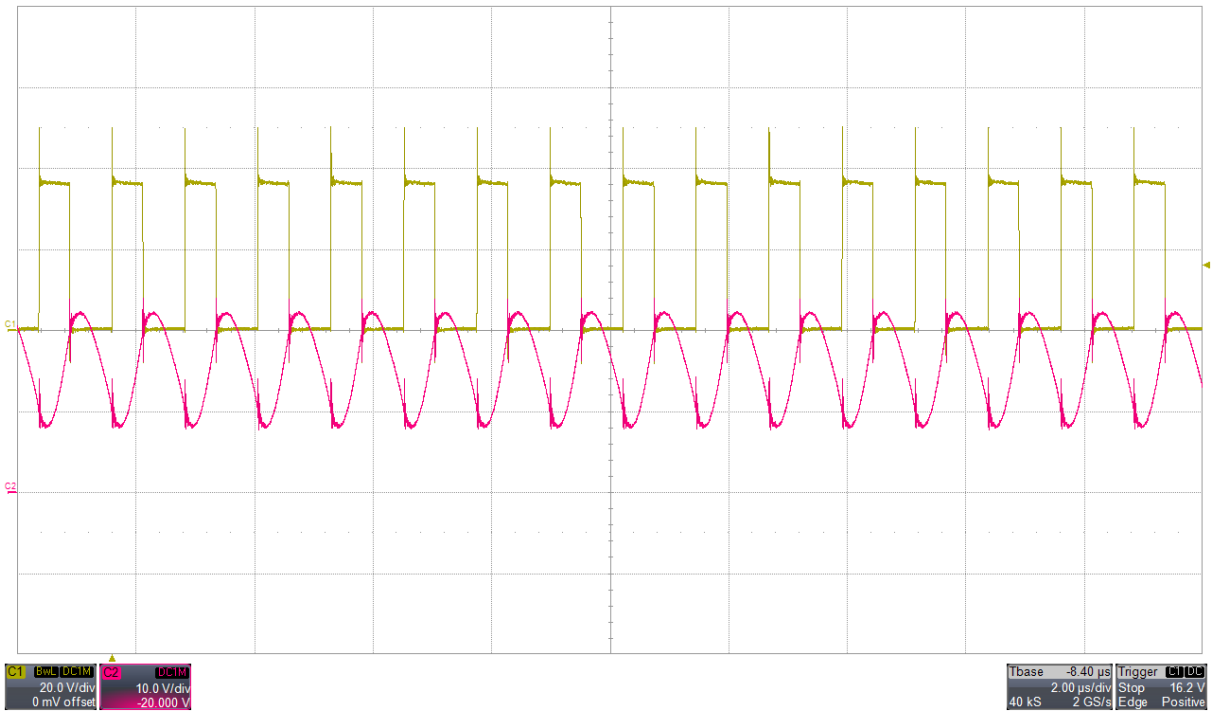
Once the third period is reached, the duty cycle is set to 42%. At this point, an LLC type control takes place, with a variable frequency illustrated in Figure 8.

Figure 8. Variable LLC control plot



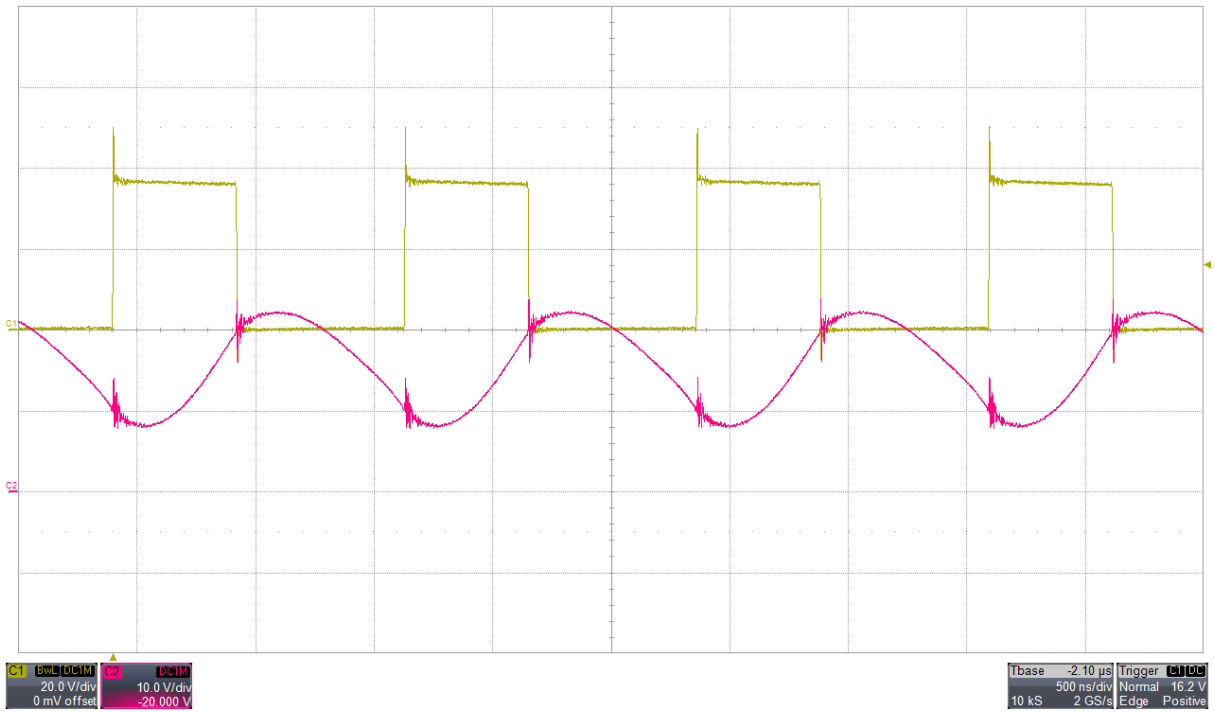
Period 3 with a high duty cycle is illustrated in Figure 9.

Figure 9. Period 3 high duty cycle operation



LLC operation at full power is illustrated in Figure 10.

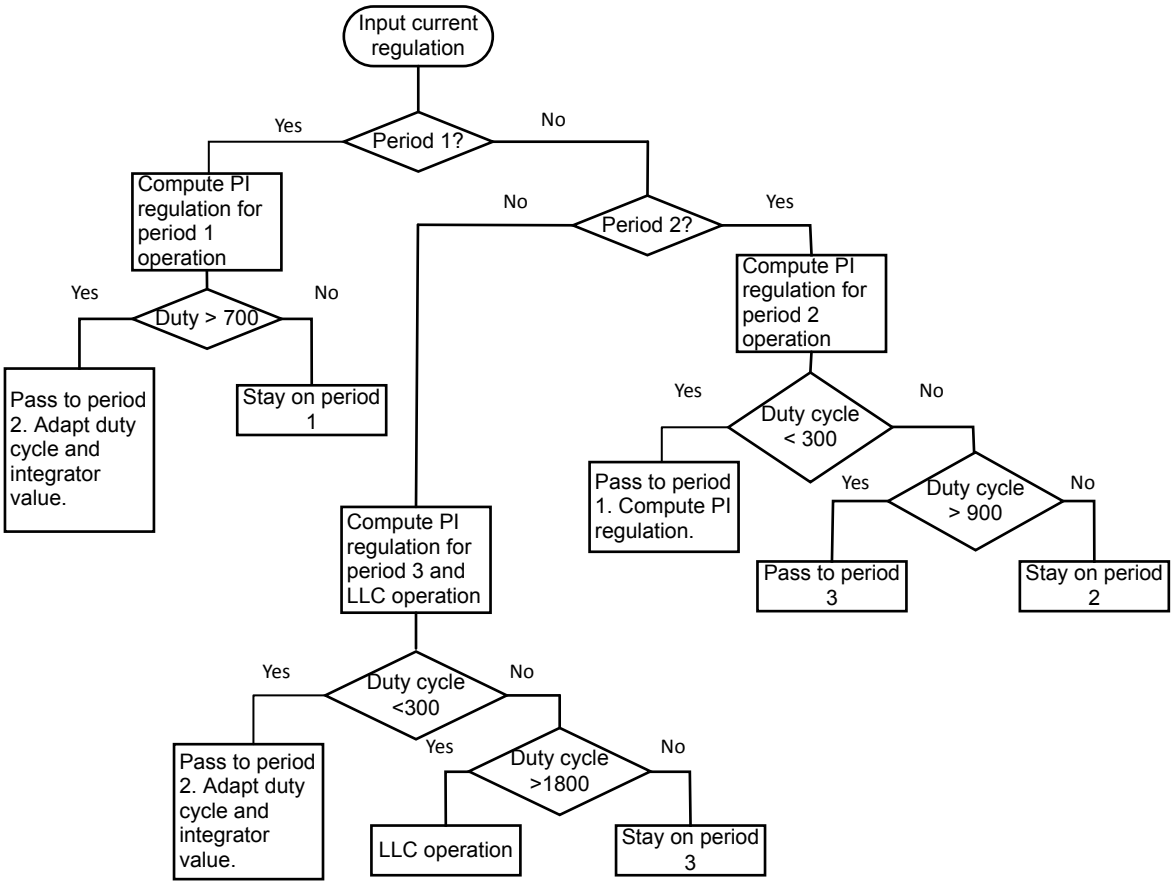
Figure 10. Full power LLC Operation



Magnification of the LLC operation at full power, switching frequency is about 800 kHz.

The three periods correspond to 4.5, 1.5 and 0.5 of the LLC network natural resonance respectively. They are all in a ratio of 3 between each period. The code managing the different transfers from one period to the next is represented in Figure 11 and is called every 32 µs.

Figure 11. Input current logic chart

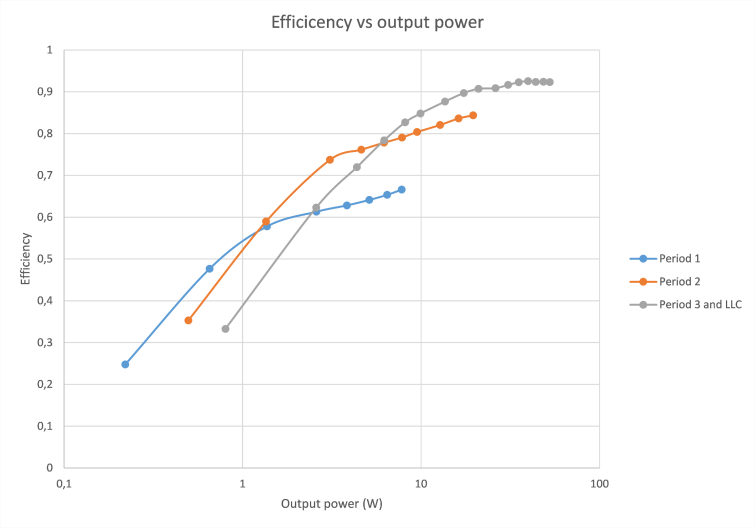


Each period manages its regulation with its own proportional and integral component gains. The third period is managed as any value below period 2 because the LLC operation takes place at this point, with a variable value that is always lower than period 2. The duty cycle is kept below 50% during the LLC operation, to avoid any discontinuity with the fixed frequency operation in period 3 which is designed for a duty cycle of 42%. Instead, the duty cycle is slightly increased from this value according to the formula:

$$d = \frac{\text{Duty cycle}}{\text{Duty cycle} + 740} \quad \text{for any duty cycle} > 1880$$

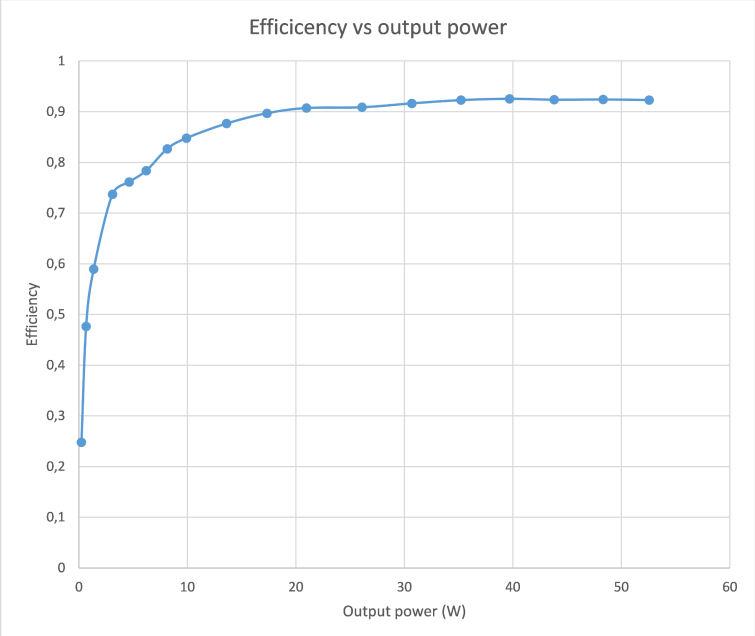
The efficiency for the three periods has been measured with the forced operation in order to select the best power range for each of them. The result is presented in Figure 12.

Figure 12. Periodic output power efficiency chart



Each period has its own optimum power range and the code sample presented previously implements the corresponding limits with a slight hysteresis. The overall efficiency is illustrated in Figure 13.

Figure 13. Overall output power efficiency



2.4 Solar converter board operating hints

When designing and manufacturing a product, the following suggestions must be considered.

2.4.1 Solar converter board operation

The solar converter board can be operated in several ways:

- with a photoelectric panel and a grid inverter
- with a photoelectric panel emulator and an electronic load
- with a DC power supply and a resistive load (for instance 5 x 15 kΩ / 25 W resistors in parallel, mounted on a heatsink).

The solar converter board must not be operated without any load as the converter requires a minimum of 10 W to operate properly.

Note: With some electronic loads, a 47 µF/ 450 V electrolytic capacitor may be needed on the output to damp any potential oscillations.

In this case, special attention must be taken as there may be residual high voltage remaining in this capacitor after the converter is switched off as it is only discharged through high value resistances.

Here is the recommended sequence to operate a board based on the reference design:

1. Connect a minimum load on the output (resistive or with an electronic load enabled)
2. Remove the jumper JP201
3. Apply V_{in} between 30 V and 50 V
4. Fit the JP201 jumper
5. Vary load or V_{in} if needed
6. Remove the jumper to disable the converter (optional)
7. Remove V_{in}.

2.4.2 STM32F334 microcontroller firmware reprogramming

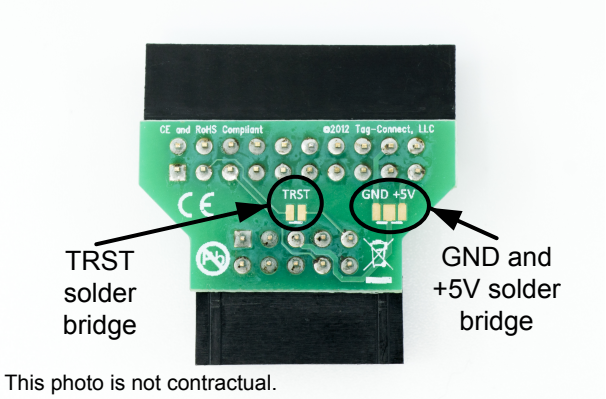
The board must be designed to allow the update of the STM32F334 microcontroller firmware. To update the firmware, the converter must be turned off, in other words the JP201 jumper must be left open to prevent the converter from unexpectedly starting up.

2.4.3 ST-LINK/V2 connection adapter

The reference design includes a programming interface to connect to an ST-LINK/V2 programer. An example of a suitable adapter is provided by a Tag-Connect 20 to 10 adapter used with 10 pin ribbon, 0.1" headers. A specimen of this adapter is shown in Figure 14 below. Tag-Connect part number is "TC2050-ARM2010 ARM 20-pin to TC2050 adapter". The adapter also needs to be configured with the two solder bridges left open:

- TRST line solder bridge not selected
- GND and +5V solder bridge (this line is tied to 3.3V on the converter side).

Figure 14. TC2050 adapter



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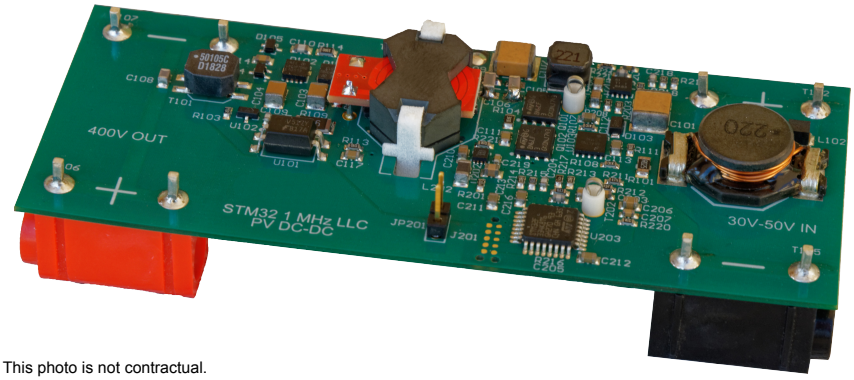
3 Solar converter demonstrator reference design

The demonstrator board is divided into 2 main functional parts:

- the power section that addresses the power management and LLC topology (see Section 3.1)
- the microcontoller section that addresses the board control (see Section 3.2).

Figure 15 illustrates an example of a specimen digital MPPT solar converter board design.

Figure 15. Digital MPPT solar converter demonstrator board illustration



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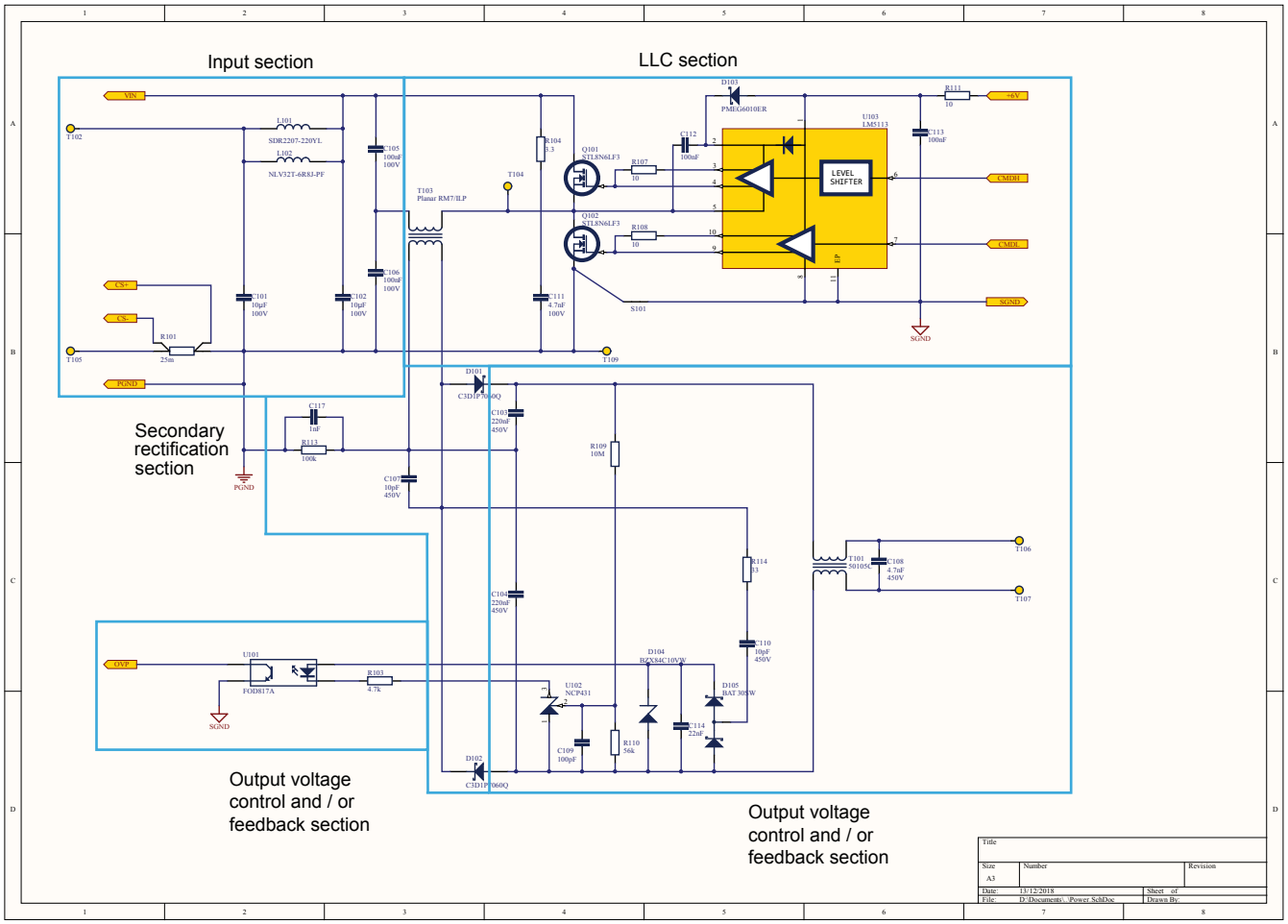
3.1 Solar converter power section reference design

This section outlines the reference design power schematics and description.

3.1.1 Solar converter demonstrator board power schematics

Figure 16. Solar converter demonstrator board electrical power schematics



3.1.2 Input section

The solar panel is connected to the banana sockets T102 (+) and T105 (-). A current sensing resistor (Kelvin resistor) R101 provides input current information before the input filter built around L101 and L102, C101 and C102. L101 has a low ESR resistance, whereas L102 is much smaller in size and is a more resistive element. Its purpose is to damp the LC network composed of the L101 and associated capacitors. This L101 and L102 combination provides improved high frequency filtering compared to a plain resistor.

3.1.3 LLC section

The heart of the LLC conversion resides in the half bridge made up of Q101 and Q102, the primary coil of the transformer T103 and the two capacitors C105 and C106. In practice, these two capacitors can be considered as a single one with a value equal to the sum of them both. The main reason of this choice, compared to mounting the usual single series capacitor with the transformer primary winding, is to lower the observed ripple current in C102, leading to improved EMC characteristics with lower losses. R104 and C111 dampen the oscillation of the C105-C106-Q101-Q102 loop during the switching events.

The transformer characteristics are as follows:

- primary inductance: 1.5 µH
- secondary inductance: 150 µH
- secondary to primary voltage ratio 10
- coupling factor: 0.9.

The transformer is built with a RM7/ILP 3F46 core type planar windings set made of multilayer printed circuit boards. The primary coil is integrated in the 4 lower layers of the board and composed of 3 turns, the secondary coil composes an additional 10 layers of the board totaling 30 turns. As each of these two coils are located in different parts of the core assembly, a poor coupling factor is obtained with a significant leakage inductance which is a desired characteristic for an LLC topology.

The main resonance frequency of the C105 and C106 capacitor assembly occurs around 300 kHz and the working frequency at full load therefore needs to be higher than this value in order to guaranty a ZVS operation, as in any normal LLC design. For reduced power operation, a highly asymmetrical operation with a much lower switching frequency takes place, by maintaining a ZVS behavior described in Section 2.3 .

Q101 and Q102 are driven by the low voltage driver LM5113. As the circuit is supposed to operate at high frequency, it is essential to minimize the driver losses when switching the circuit on and off. Two key parameters are to be observed:

- The gate input capacitance (C_{iss}) at 0 V drain to source voltage is the value to take into account in ZVS operation, instead of the total gate voltage for a hard switching commutation.
- The gate threshold voltage (V_{Gth}) must be as low as possible to reduce the driver supply voltage. This is especially important as the dissipated power is proportional to the square of this value.

Therefore, considering the product of C_{iss} x V_{Gth}^2 for a given R_{on}, this has led to the choice of the 60 V/30 mΩ STL8N6LF3 device. Its input capacitance of 1 nF and gate voltage threshold ranging from 1 V and 2.5 V is compatible with an 5 V peak driving voltage operation, with an estimated driving loss of 50 mW for both switches. The driver U103 is supplied with a voltage slightly higher than 5 V in order to provide a correct value for the high side section which runs in bootstrap mode through D103.

3.1.4 Secondary rectification

The output rectification provides a voltage doubler configuration (aka Delon circuit topology) through the two SiC diodes D101 and D102 and the capacitors C103 and C104. This is not exactly a doubling operation, as the duty cycle on the primary side can be highly asymmetrical. But the output is connected to the extreme points of C103-C104, and is not affected by the real voltage lying on their middle point.

Another advantage of this configuration is the presence of a so called cold point on one edge of the transformer secondary winding, minimizing the common mode current generation between primary and secondary windings. Nevertheless, a common mode output choke has been implemented together with a C117 Y capacitor between primary and secondary windings in order to get rid of any residual high frequency interference.

R113 provides a DC path for maintaining the solar panel at a reasonable voltage versus output.

3.1.5 Output voltage surge control and/or feedback

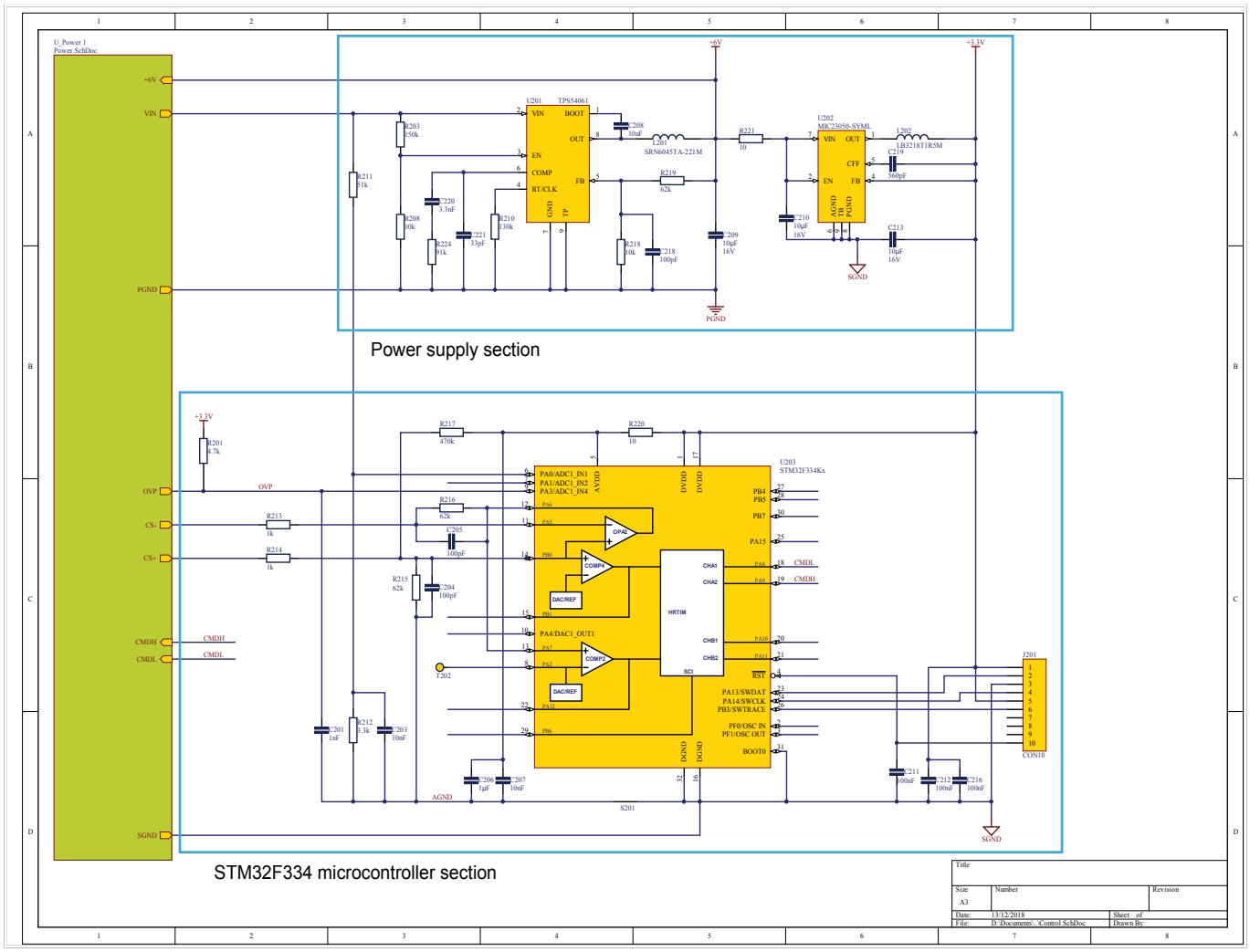
The output voltage is controlled by the resistive divider R109 and R110 connected on the reference pin of a low bias current NCP431. The maximum voltage threshold is set at about 440 V. When this limit is reached, the optocoupler U101 is triggered. See Section 2.2 for a detailed functional description.

This circuit's power supply is provided by a charge pump composed of the capacitor C110 and diode D105. A few picofarads are sufficient to collect 1 or 2 mA when the converter is running at 1 MHz, with an output voltage of 400 V or 440 V. The voltage is clamped to 10 V with the Zener diode D104.

3.2 Solar converter board control section

3.2.1 Solar converter board schematics

Figure 17. Control section control schematics



The green block represents the power section described in Section 3.1 .

3.2.2 Power supply

A first step-down circuit U201 delivers a 6 V supply from V_{IN} provided from the solar panel through the input filter (See Section 3.1.2). This value is needed by the power switch driver (See Section 3.1.3). It also supplies a second step-down U202 to provide the 3.3 V power supply for the microcontroller U203.

3.2.3 Microcontroller section

U203 is the main circuit receiving all the information and controlling the converter. It is based on a STM32F334K microcontroller in a 32 pins LQFP package, of which the following functions are activated:

- Analog to digital converter for digitizing the input voltage (resistive divider R211-R212), the voltage surge signal (pull-up resistance R201) and the input current at the level of the internal operational amplifier OPA2.
- The operational amplifier OPA2 used to amplify the sense voltage delivered from R101 (See Section 3.1.2) in a differential way:
  - The gain is set to 62 through R213 to R215, setting a maximum input voltage of 3.3 V/62 = 53 mV. Together with the 25 mΩ value of the current sensing resistor R101, this configuration ensures a measuring capability of about 2 A for the input current.
  - A bias resistance R217 has been implemented in order to overcome the offset of the operational amplifier which may be negative.
  - A calibration is run every time the converter is inactive.
- A test point is connected on PA2, gives access to the internal output of USART2 as an alternate function. This is especially useful to monitor the internal program execution without disturbing its execution, and to correlate the internal events and associated memory content of the converter behavior. USART2 is configured by software as:
  - 8 bit
  - no parity
  - 1 stop and 1 start bit
  - idle high
  - 8 Mbits/s serial communication.

  The USART2 bus width is not able to handle a 16 bit data transfer, if a test function similar to the test(uint16_t data) function is used, then the data is sent in two consecutive bytes on PA2 as per the example below:
  1. MSByte data first
  2. LSByte data next.

  This function does not lead to any significant delay in the application as the two bytes are immediately absorbed by the USART2 hardware implementation (DATA register and internal shift register).
- JP201 jumper starts (closed) or stops (open) the converter (See Section 2.4.1).
- The high resolution timer HRTIM1 generates the PWM signal to activate the half bridge Q101 and Q102 through the driver U103 (See Section 3.1.3). Its base frequency of 4.096 GHz which allows the accurate duty cycle adjustment, even with a switching frequency as high as 1MHz.
- The program can be loaded and modified through the connector J201 which is a set of 10 pads on the printed circuit board. A dedicated Tag-connect cable with pogo pins must be used for this purpose. A TC2050-IDC-NL connector with a TC2050-ARM2010 adapter (see Section 2.4.3 for more adapter details) fits the ST-LINK/V2 programmer.

The left side of the microcontroller associated circuit and components are dedicated to analog functions. They are connected to a local AGND ground and supplied by the AVDD voltage. Both of these lines are separated from other digital signals by means of a decoupling resistance R220 and a special "net tie" component S201. This component connects both AGND and SGND nets to the PCB through a footprint consisting of two touching pads. This component represents what is usually called a "star point" and is located below the microcontroller footprint. When routing the PCB, it is not possible to connect to AGND components on the SGND or PGND (The same principle applies to PGND and SGND, see Section 3.1.1 with component S101).

4 Conclusion

This application note describes how to implement a demonstrator based on the compact digital MPPT solar converter using the STM32F334 microcontrollers. It makes use of the internal high resolution timer (HRTIM1) with base frequency of up to 4.6 GHz. The converter includes the following characteristics:

- LLC operation at full load with switching frequency of up to 1 MHz.
- Better power density (design using planar transformer and low-profile ceramic capacitors).
- Electrolytic capacitor-free design: higher reliability and extended operating lifetime.
- Two lower switching frequency modes with ZVS operation for reduced power levels.
- Optimized overall efficiency at any power level.
- Output voltage surge protection with either regulation or shut down.
- Input MPPT for solar panel.

The STM32F334 microcontrollers offer additional resources and free pins which allow the implementation and support of complementary functions such as grid inverter communication.

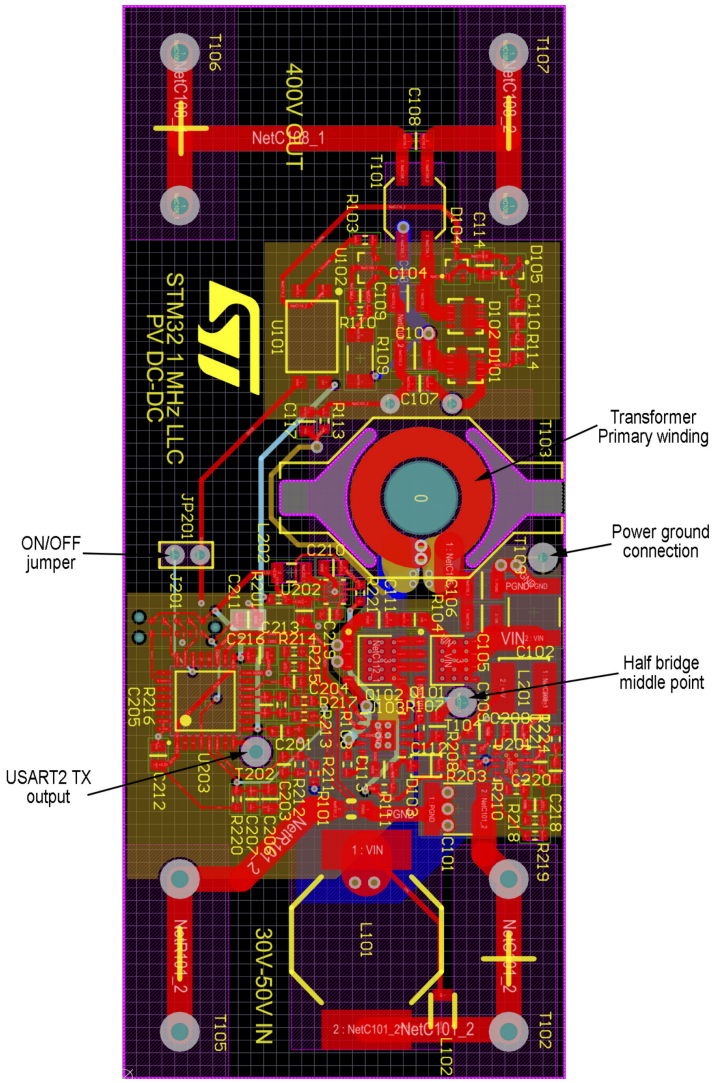
Appendix A Solar converter reference design details

Here are some details of a possible implementation of a digital MPPT solar converter reference design. It is composed of suggested printed circuit board and bill of materials.

A.1 Solar converter demonstrator printed circuit board

This is a potential board layout that can be used as guideline in the event of an actual implementation.

Figure 18. Printed circuit board demonstrator sample picture



This picture is not contractual.

A.2 Bill of material

The following bill of materials is the suggested list based on the reference design schematics that are described in Section 3.1.1 and Section 3.2.1 . The exact list is defined on a case by case basis and varies with the implementation design.

Table 2. Bill of material

Comment	Description	Voltage	Designator	Quantity	Footprint
10 µF	X7R or equivalent ceramic capacitor	100 V	C101, C102	2	CAPC5750N
220 nF	X7R or equivalent ceramic capacitor	450 V	C103, C104	2	CAPC3225
100 nF	COG ceramic capacitor	100 V	C105, C106	2	CAPC3225
10 pF	COG ceramic capacitor	450 V	C107, C110	2	CAPC2012
4.7 nF	X7R or equivalent ceramic capacitor	450 V	C108	1	CAPC2012
100 pF	COG ceramic capacitor	-	C109, C204, C205, C218	4	CAPC1608
4.7 nF	X7R or equivalent ceramic capacitor	100 V	C111	1	CAPC2012
100 nF	X7R or equivalent ceramic capacitor	-	C112, C113, C211, C212, C216	5	CAPC2012
22 nF	X7R or equivalent ceramic capacitor	-	C114	1	CAPC2012
1 nF	X7R or equivalent ceramic capacitor	-	C117	1	CAPC2012
1 nF	X7R or equivalent ceramic capacitor	-	C201	1	CAPC1608
10 nF	X7R or equivalent ceramic capacitor	-	C203, C207	2	CAPC1608
1 µF	X7R or equivalent ceramic capacitor	-	C206	1	CAPC2012
10 nF	X7R or equivalent ceramic capacitor	-	C208	1	CAPC2012
10 µF	X7R or equivalent ceramic capacitor	16 V	C209, C210, C213	3	CAPC2012
560 pF	COG ceramic capacitor	-	C219	1	CAPC1608
3.3 nF	X7R or equivalent ceramic capacitor	-	C220	1	CAPC1608
33 pF	COG ceramic capacitor	-	C221	1	CAPC1608
C3D1P7060Q	SiC diode	-	D101, D102	2	-
PMEG6010ER	Schottky diode	-	D103	1	SOD123W
BZX84C10 VW	Zener diode	-	D104	1	SOT323
BAT30SW	Double Schottky diode	-	D105	1	SOT323
2.54 mm 2pins header	SAMTEC TSW-102-07-G-S	-	JP201	1	-
22 µH	Bourns inductor SDR2207-220YL	-	L101	1	-
6,8 µH	TDK inductor NLV32T-6R8J-PF	-	L102	1	-
220 µH	Bourns inductor SRN6045TA-221M	-	L201	1	-
1,5 µH	TAIYO YUDEN inductor LB3218T1R5M	-	L202	1	-
STL8N6LF3	STMicroelectronics 60 V/30m□ N mosfet	-	Q101, Q102	2	POWERSO8
25 mΩ	Ohmite current sense resistor LVM12FTR025E-TR	-	R101	1	-
4.7 kΩ	Resistor	-	R103, R201	2	RESC1608N
3.3 Ω	Resistor	-	R104	1	RESC2012N

Comment	Description	Voltage	Designator	Quantity	Footprint
10 Ω	Resistor	-	R107, R108, R111, R220, R221	5	RESC1608N
10 MΩ	High voltage resistor Vishay CRCW201010M0JNEF	-	R109	1	RESC5025N
56 kΩ	Resistor	-	R110	1	RESC1608N
100 kΩ	Resistor	-	R113	1	RESC1608N
33 Ω	Resistor	-	R114	1	RESC2012N
150k	Resistor	-	R203	1	RESC1608N
10 kΩ	Resistor	-	R208, R218	2	RESC1608N
130 kΩ	Resistor	-	R210	1	RESC1608N
51 kΩ	Resistor	-	R211	1	RESC1608N
3.3 kΩ	Resistor	-	R212	1	RESC1608N
1 kΩ	Resistor	-	R213, R214	2	RESC1608N
62 kΩ	Resistor	-	R215, R216, R219	3	RESC1608N
470 kΩ	Resistor	-	R217	1	RESC1608N
91 kΩ	Resistor	-	R224	1	RESC1608N
Common mode filter	Murata 50105C	-	T101	1	-
Horizontal banana plug black	DELTRON 571-0100	-	T105, T107	2	-
Horizontal banana plug red	DELTRON 571-0500	-	T102, T106	2	-
Test point	Vero - 20-313143 - Terminal, PCB, blanc, PK100	-	T104, T202	2	-
FOD817A3S	Optoisolator	-	U101	1	SMT-4
NCP431ACSNT1G	Programmable zener	-	U102	1	SOT23
LM5113QDPRRQ1	High frequency half bridge driver	-	U103	1	WSON10
TPS54061DRBR	Step down regulator	-	U201	1	SON8
MIC23050-SYML	Step down regulator	-	U202	1	2x2 ML
STM32F334K8T6	STMicroelectronics 32 bits Arm® power dedicated processor	-	-	1	LQFP32

Revision history

Table 3. **Document revision history**

Date	Version	Changes
19-Jul-2019	1	Initial release.

Contents

List of figures

List of tables