Getting started with the STM32H7 Series MCU 16-bit ADC

Introduction

STM32H7 Series MCUs embed three successive-approximation-register (SAR) ADCs with 16-bit resolution targetting applications requiring high accuracy measurements and high data rates.

This application note describes the new features and performance figures of the 16-bit ADC.

It explains how the ADC performance varies under various conditions, and provides guidelines to exploit the full potential of the STM32 16-bit ADC.

This document applies to the STM32H7 Series product lines listed in Table 1.

Table 1. Applicable products

Type	Product lines
Microcontrollers	STM32H742 STM32H743 STM32H745 STM32H747 STM32H750 Value line STM32H753 STM32H755 STM32H757

1 General information

This document applies to STM32H7 Series Arm®Cortex®-M7-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Reference documents

Table 2. Document references

Reference	Documents
[1]	• STM32H745/755 and STM32H747/757, reference manual (RM0399) • STM32H742, STM32H743/753 and STM32H750 Value line, reference manual (RM0433)
[2]	• STM32H742/43 datasheet (DS12110) • STM32H745 datasheet (DS12923) • STM32H747 datasheet (DS12930) • STM32H750 Value line datasheet (DS12556) • STM32H753 datasheet (DS12117) • STM32H755 datasheet (DS12919) • STM32H757 datasheet (DS12931)
[3]	How to get the best ADC accuracy in STM32 microcontrollers, application note (AN2834)

1.2 Acronyms and abbreviations

Table 3. Definition of terms

Term	Definition
AUTDLY	Auto-delayed conversion mode
DIFF	Differential
DFSDM	Digital filter for sigma delta modulators
DNL	Differential non-linearity
ENOB	Effective number of bits
GE	Gain error
INL	Integral non-linearity
OE	Offset error
SE	Single-ended
SAR	Successive-approximation-register
SNR	Signal-to-noise ratio
THD	Total harmonic distortion
TUE	Total unajusted error

2 STM32 16-bit ADC features

This section presents the main features of the STM32H7 ADC, focusing on enhancements with respect to the STM32F7 Series 12-bit ADC.

2.1 STM32H7 ADC with 16-bit resolution

The resolution of the ADC defines the number of bits it uses to digitize an input signal. For the STM32H7 16-bit ADC, the total voltage range is represented by 2^{16} (65536) discrete digital values.

The absolute minimum level that a system can measure is called the least-significant-bit (LSB) and is defined as:

1 LSB = VREF / 2^N where VREF is the reference voltage and N is the resolution of the ADC in bits.

For 3.3 V VREF, the STM32H7 16-bit ADC can resolve measurements up to 3.3 V / 65536 = 50 µV.

The new STM32H7 16-bit ADCs allow better accuracy and less noise compared with previous STM32 ADCs with 12-bit resolution.

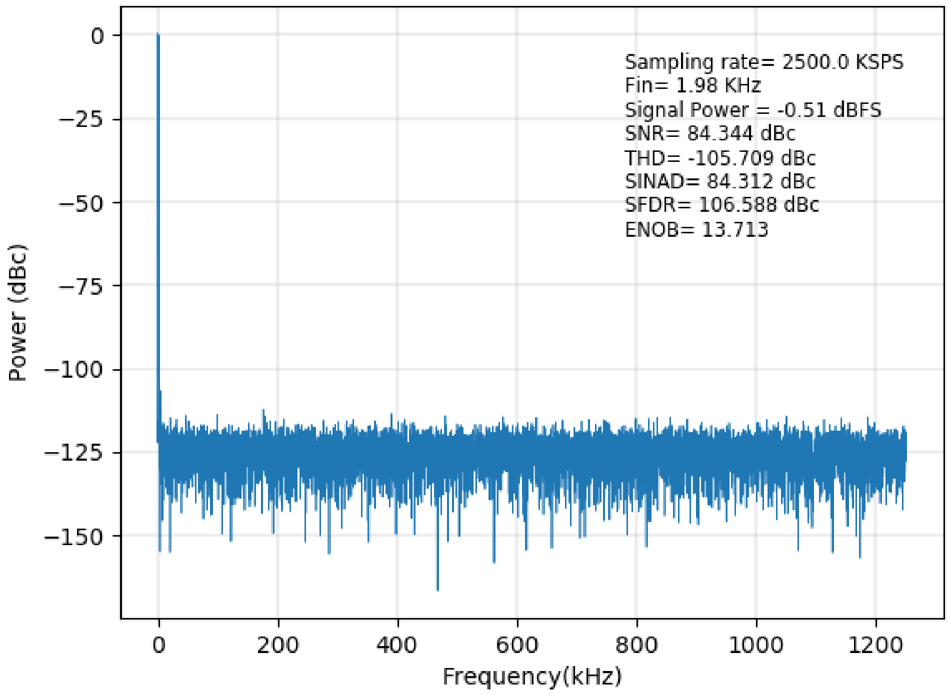
2.1.1 Reduced noise and distortion levels

The STM32H7 16-bit ADC provides very good dynamic figures including lower noise levels and reduced distortion.

Figure 1 shows an FFT plot measured on a board populated with an STM32H747 in a TFBGA240 package. An RC filter, comprising a 50-ohm resistor and a 150 pF capacitor, is placed at the ADC inputs.

The input signal is a 2 kHz low-noise and low-distortion sine wave with an input amplitude of -0.5 dB below full scale.

Figure 1. FFT plot for STM32 16-bit ADC in differential mode @2.5 Msps



Note: All dynamic figures presented in this application note have not been extrapolated to full scale. To derive the parameters in full-scale, 0.5 dB needs to be added to the signal power.

For example, SNR [dBFS] = SNR [dBc] + 0.5 dB = 84.34 + 0.5 = 84.84 dBFS. After extrapolation to full scale, the ENOB is 13.8 bits.

Table 4 shows dynamic parameters at VREF = 3.3 V and temperature = 25 °C in single-ended and differential mode.

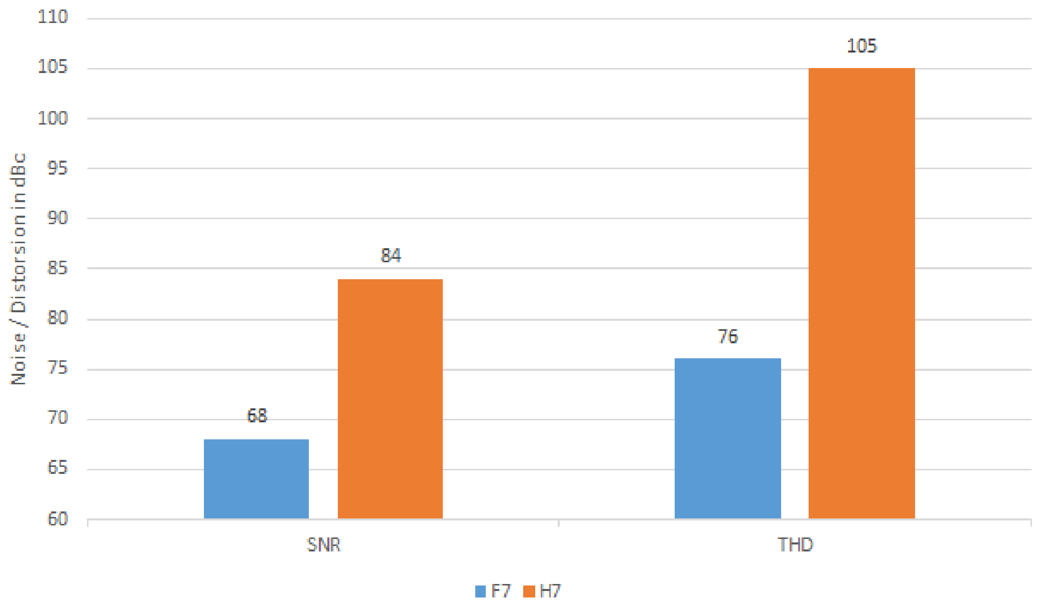
Table 4. STM32H7 ADC dynamic parameters

Symbol	Input signal mode[1]	Typical
ENOB (bits)	SE	12.8
	DIFF	13.7
SNR (dBc)	SE	79.24
	DIFF	84.3
THD (dBc)	SE	-96.5
	DIFF	-105

1. *Conditions: direct channel, Fadc = 25 MHz, Ts = 1.5 cycles.*

Figure 2 shows a comparison between STM32H7 16-bit ADC and STM32F7 12-bit ADC noise and distortion levels. STM32H7 16-bit ADC provides a 16 dB improvement in SNR, meaning that it is 6.3 times less noisy.

Figure 2. Noise and distortion levels comparison between STM32H7 16-bit and STM32F7 12-bit ADCs



Note: THD is provided in absolute format.

In terms of distortion levels, the STM32H7's ADC has a total harmonic distortion of -105 dBc, which is more than 30 dB better than that of the STM32F7.

2.1.2 Improved accuracy

The STM32H7 16-bit ADC has improved static parameters allowing high accuracy measurements.

Table 5 shows static parameters of the STM32H7 ADC in typical conditions.

Table 5. STM32H7 ADC 16-bit static accuracy

Symbol	Input signal mode(1)	Typical
TUE (LSB)	SE	+/-16
	DIFF	+/-10
OE (LSB)	SE	+/-2
	DIFF	+/-6
GE (LSB)	SE	+/-7
	DIFF	+/-13
DNL (LSB)	SE	+1.7/-1
	DIFF	+1.2/-1
INL (LSB)	SE	+/-8
	DIFF	+/-4

1. *Conditions: fast channel, Fadc = 25 MHz, Ts = 2.5 cycles.*

When comparing ADC static parameters defined in LSB units, such as DNL, INL and TUE, the fact that the size of the LSB depends on the resolution must be considered.

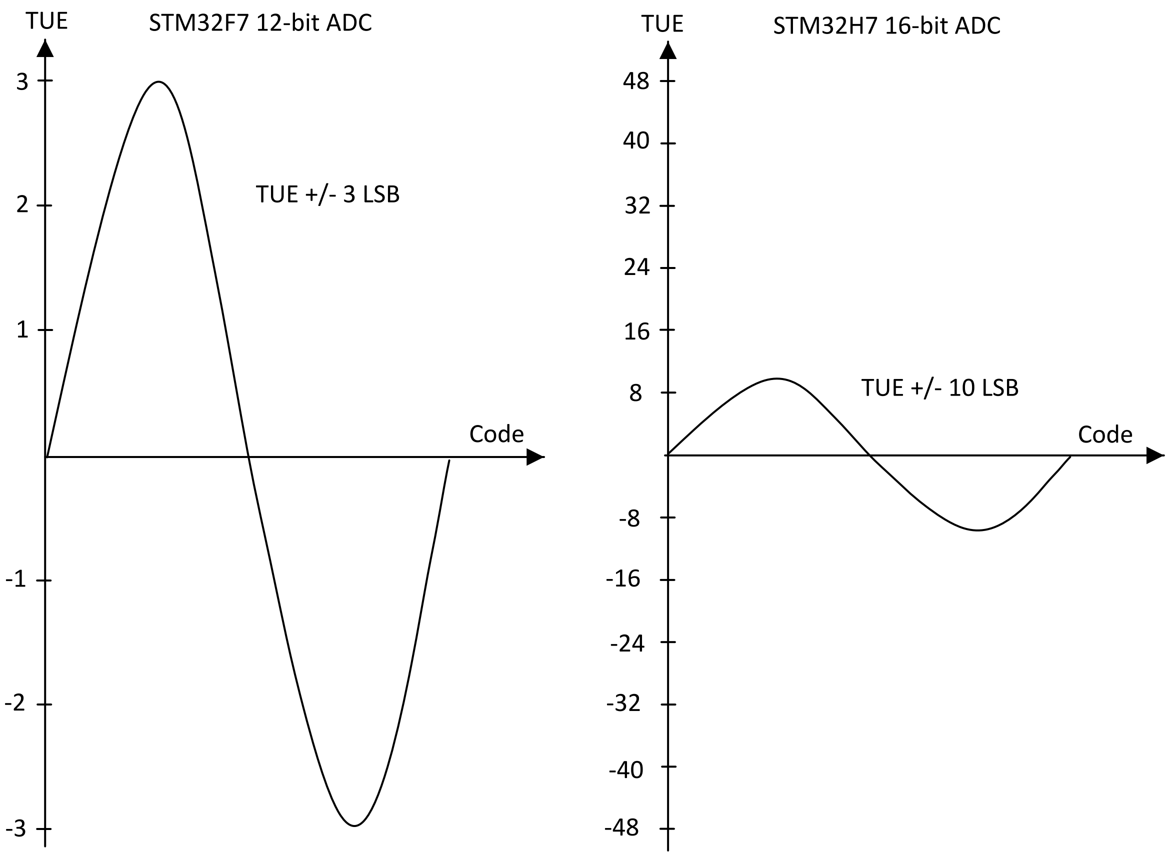
For a 3.3 V voltage reference, the size of an LSB in 16-bit mode is about 50 µV, while the size of an LSB in a 12-bit ADC is about 800 µV.

1 LSB (12 bit mode) = 16 x 1 LSB (16 bit mode)

For example, a 12 bit ADC with a 3-LSB TUE (total unadjusted error) is equivalent to a 48-LSB TUE in 16 mode.

Figure 3. Accuracy comparison between STM32H7 16-bit ADC and STM32F7 12-bit ADC compares an STM32H7 16-bit ADC and an STM32F7 with a 12-bit ADC in terms of TUE. It shows that the STM32H7 16-bit ADC is approximately 5 times more accurate.

Figure 3. Accuracy comparison between STM32H7 16-bit ADC and STM32F7 12-bit ADC



2.2 Increasing ADC resolution with hardware oversampling

The STM32H7 embeds a hardware oversampling engine with a ratio adjustable from 2x to 1024x.

It allows increased SNR by performing data averaging. The averaging is done in hardware, freeing the CPU and allowing lower power consumption compared to the software-based implementation.

For further details, refer to the applicable STM32H7 reference manual [1]and AN4629 [3].

Using the lowest oversampling ratio (x2) the SNR can be improved to reach 86.7 dB, and an ENOB of 14.1 bits.

With 4x oversampling ratio, an SNR of 89 dB and an ENOB of 14.5 bits can be achieved. With a 16x oversampling ratio, ENOB increases to 15.1 bits.

Table 6 provides dynamic parameters for different oversampling ratios. Measurements are performed in differential mode with fADC = 25 MHz and Ts = 1.5 cycles.

Table 6. STM32H7 dynamic figures versus oversampling ratio

OVS ratio	X1	X2	X4	X8	X16	X32
SNR (dBc)	84.3	86.7	89.15	91.3	92.8	94.1
THD (dBc)	-105	-106	-106	-106	-106	-105
ENOB (bits)	13.7	14.1	14.5	14.85	15.09	15.3

2.3 Increasing throughput with multiple ADC operation

STM32H7 embeds 3 ADCs that can operate independently or in dual mode (ADC1 and ADC2). The maximum ADC sampling rate is 3.6 Msps in 16-bit mode.

When 3 ADCs are sampling simultaneously, the system throughput can reach up to 10.5 Msps.

Higher data rates per channel can be obtained when a single channel is converted by two ADCs in dual-interleaved mode. The data rate can reach up to 7 Msps in 16-bit mode and 10 Msps in 14-bit mode.

See Section 4 Maximum data rate for further details.

2.4 STM32H7 ADC channel descriptions

This section presents the different types of ADC channels available in the STM32H7.

2.4.1 ADC direct, fast and slow channels

STM32H7 ADCs have three different types of channels: direct, fast and slow.

Channel performance depends on the resistance present in the path between the input pin and the ADC sampling capacitor. Channels with low input resistance require less time to charge the sampling capacitor, and hence allow higher sampling rates.

This section describes the difference between ADC channels in terms of input resistance.

There are two basic contributors to the total channel resistance that can differ between channels:

- **ADC input multiplexer**: The ADC has an input multiplexer that selects one of 20 channels to sample. There are 6 fast channels characterized with low input resistance. The other 14 channels have higher input resistances that require longer sampling times. These are hence referred to as slow channels.
- **IO analog switch**: Connection between an IO pin and ADC is made through an analog switch, which increases the total ADC channel input resistance. Direct channels are essentially fast channels on the ADC input multiplexer side, but specifically bypass the analog switch on IO side.

Table 7 summarizes the difference between ADC channels in terms of total resistance.

Table 7. ADC channel type versus input resistance

Channel type	IO analog switch resistance	ADC multiplexer resistance
Slow	Yes	High
Fast	Yes	Low
Direct	Bypassed	Low

Figure 4. Paths for different ADC channel types illustrates the different paths of ADC channels.

2.4.2 ADC channel availability across packages

Table 8 shows the available channels, depending on the package type and product line.

Table 8. ADC channel availability across STM32H7 packages

Channel type	STM32H745					STM32H747					STM32H743/STM32H742							
	LQFP144	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25	WLCSP156	UFBGA169	LQFP176	LQFP208	TFBGA240 +25	LQFP100	TFBGA100	LQFP144	UFBGA169	UFBGA176+25	LQFP176	LQFP208	TFBGA240 +25
Direct	2	4	2	2	4	2	2	2	2	4	2	2	2	2	2	2	2	4
Fast	6	9	9	9	9	7	9	9	9	9	3	3	9	9	9	9	9	9
Slow	15	23	17	21	23	14	17	17	21	23	11	11	17	21	21	21	21	23
Total channels	23	36	28	32	36	23	28	28	32	36	16	16	28	32	32	32	32	36

2.4.3 Converting slow channels to fast channels

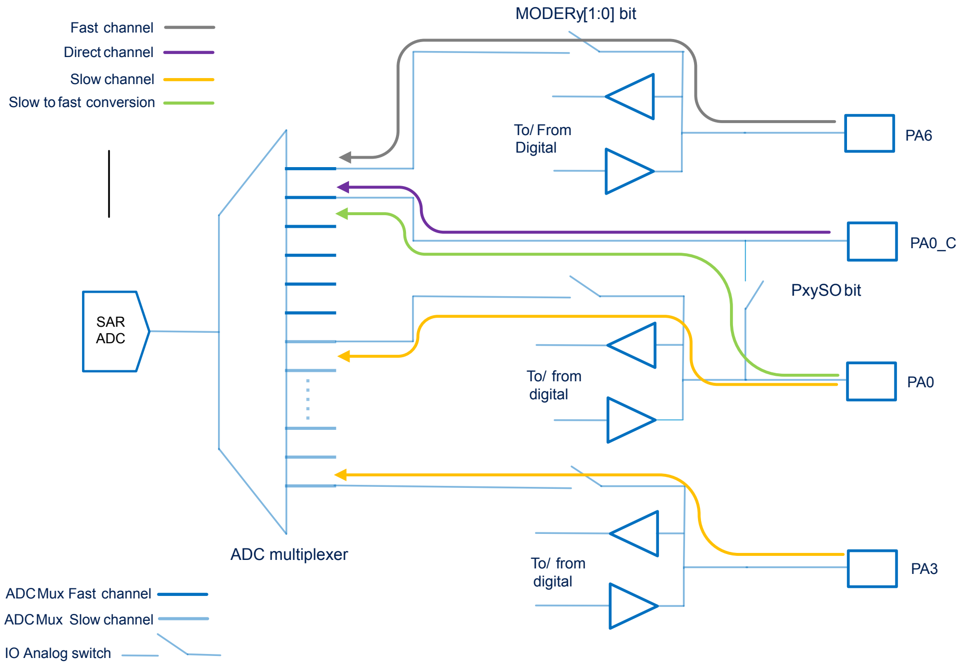
Pxy_C pins are considered direct channels, since they are connected to ADC fast channels without going through the IO analog switch. Pxy pins on the other hand are considered slow channels.

In packages where Pxy_C are not available at package level, the user can use the path connection between Pxy and Pxy_C pins to convert a slow channel to a fast channel.

The user can inject the signals on the Pxy pins and close the analog switch between the Pxy and Pxy_C pads, by setting the PxySO bit to connect to ADC fast channels.

Refer to the green arrow in Figure 4 for the path used to convert a slow channel to a fast channel.

Figure 4. Paths for different ADC channel types



2.4.4 ADC internal channels

The STM32H7 ADCs allow the conversion of internal channels connected to internal peripherals such as the DAC, VREFINT (bandgap reference), VBAT and temperature sensor.

Table 9. **STM32H7 internal ADC channels**

Peripheral	ADC1	ADC2	ADC3
VREFINT	-	-	Yes
VBAT/4	-	-	Yes
VSENSE	-	-	Yes
DAC	-	DAC_OUT1, DAC_OUT2	-

2.4.5 Single-ended and differential operation

STM32H7 allows to convert both single-ended and differential signals.

In single ended mode the input signal is applied on ADCx_INP pin and is converted with respect to VREF-.

In differential mode the input signal is a fully differential signal applied to ADCx_INP (positive input) and ADCx_INN (negative input) pins.

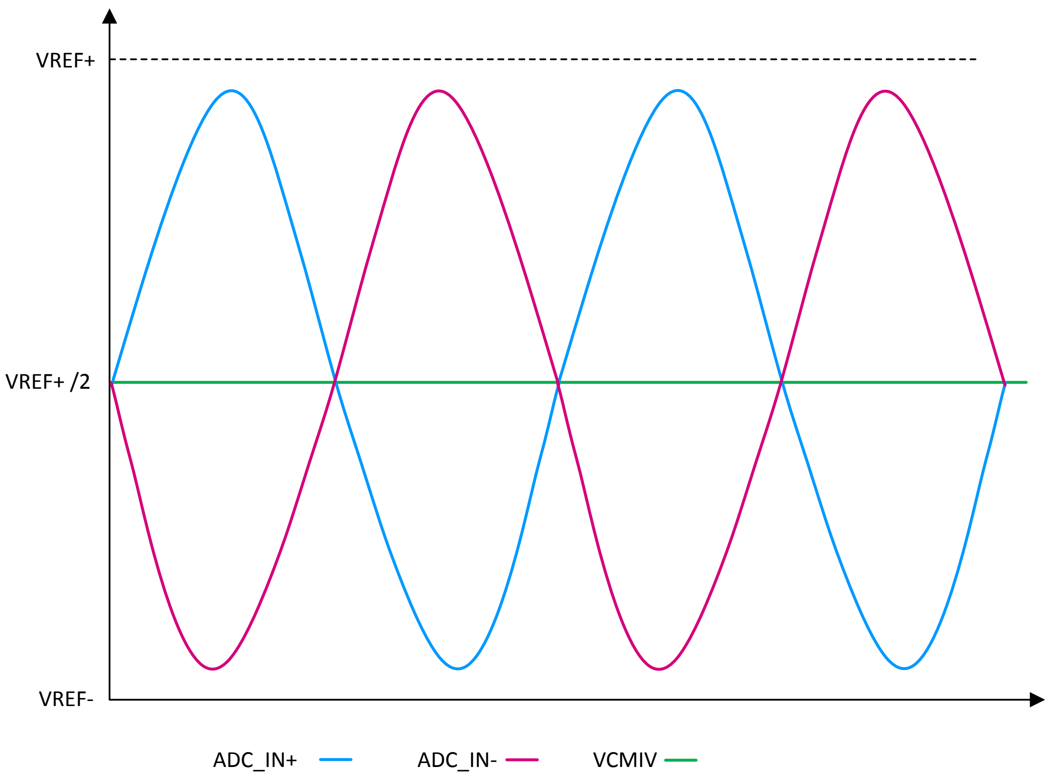
Fully differential conversions have the benefit of common-mode noise rejection and increased dynamic range allowing 6 dB increase in SNR and 1 bit in resolution.

Input signals must be 180° out of phase and the common mode input voltage set to VREF/2. Refer to the applicable STM32H7 datasheet [2] for more details.

The input common mode voltage is calculated as follows:

$$VCMIV = (ADC\_INP + ADC\_INN)/2$$

Figure 5. **Fully differential input signal**



2.5 ADC calibration

The STM32H7 ADC implements a digital calibration algorithm to measure and correct offset and non-linearity errors.

2.5.1 Offset calibration

The STM32H7 ADC embeds an offset calibration feature allowing offset-error cancelling. The user must run an offset calibration after power-up.

Furthermore, it is recommended to re-run the offset calibration whenever the VREF voltage changes by more than 10%.

It is also recommended to run an offset calibration after changes of VDDA or temperature.

2.5.2 Linearity calibration

The STM32H7 embeds a linearity calibration engine to enhance the ADC linearity. It allows compensation of capacitance mismatch during production.

Linearity calibration is purely process dependent and only needs to be run once. It is done in the manufacturing facility under specific conditions, and linearity codes are stored in Flash memory.

After power up, linearity calibration codes must be loaded from Flash memory before the ADC is used. The user can however run a linearity calibration. It should preferably be done under the following conditions: (fADC = 10 MHz, VREF <= 2 V).

2.6 IO voltage booster

The IO analog switch AC performance is degraded when VDDA decreases, causing distortion of the input signal. An IO voltage booster therefore supplies the analog switches embedded in IOs in order to maintain a good distortion level at low supply voltages. By default, the analog switch is supplied by VDDA.

When VDDA is below 2.7 V, switching to VDD is recommended if VDD is greater than 2.7 V.

In cases where both VDDA and VDD are below 2.7 V, the booster should be enabled to supply the analog switch.

Table 10 summarizes recommended settings depending on VDD and VDDA supply levels.

Table 10. IO voltage booster settings versus VDDA and VDD

VDD	VDDA	BOOSTE	BOOSTVDDSEL	Analog switch supply
-	>2.7 V	0	0	VDDA (default)
>2.7 V	<2.7 V	0	1	VDD
<2.7 V	<2.7 V	1	0	Voltage booster

2.7 Voltage reference buffer VREFBUF

The STM32H7 embeds an internal reference buffer that can be used by the ADC and the DAC. It provides a stable voltage based on the internal reference voltage, VREFINT.

Four programmable output voltage levels are available: 2.5 V, 2.048 V, 1.8 V and 1.5 V.

Refer to the applicable STM32H7 datasheet [2] for further information on the VREFBUF characteristics.

2.8 STM32H7 Series versus STM32F7 Series ADC comparison

Table 11 summarizes the main differences between STM32H7 series ADC and STM32F7 series ADC.
For more information about STM32H7 ADC features, refer to the applicable STM32H7 reference manual [1].

Table 11. STM32H7 / STM32F7 ADC comparison

ADC parameter	STM32H7 Series	STM32F7 Series
Maximum resolution	16 bit	12 bit
ADC units	3	3
Interleaved mode	Dual	Dual/triple
tsampling (cycles)	1.5 to 810.5	3 to 480
tconversion (cycles)	tsampling + N/2 + 0,5	tsampling + N
Sampling rate	16-bit 3.6 Msamples/s	-
	14-bit 5 Msamples/s	-
	12-bit 5.6 Msamples/s	2.4 Msamples/s
Input channels per ADC	20	16
Total external input channels (1)	36	24
Differential input mode	Yes	-
External triggers	21	16
Calibration	Linearity + offset	Offset
Hardware oversmapling	Yes	-
Analog watchdogs per ADC	3	1
IO voltage booster	Yes	-
Internal reference VREFBUF	Yes (1.5 V, 1.8 V, 2.048 V, 2.5 V)	-
DFSDM	Yes	-
AUTDLY conversion	Yes	-

1. *Depends on package*

3 Maximum ADC frequency across resolutions, packages and number of ADCs

In the SAR ADC architecture, the reference input pin, VREF, needs to respond to large amplitude and fast current spikes. These transient currents happen during the conversion phase in which the VREF pin is connected / disconnected to / from the capacitive DAC during bit evaluation. (Refer to AN2834[3] for further details about the SAR ADC internal structure.)

The VREF pin is subject to a current-induced voltage drop. Therefore, in order to avoid conversion errors, enough time is needed for the voltage reference level to resettle to +/-0.5 LSB of the final value . This is critical to guarantee resolution consistency, and to ensure that there are no missing codes.

The maximum ADC frequency decreases when the time needed for VREF to settle increases. The following sections present the main parameters that have an impact on the maximum achievable ADC frequency. Maximum ADC frequencies for different packages, resolutions and number of ADCs are also presented.

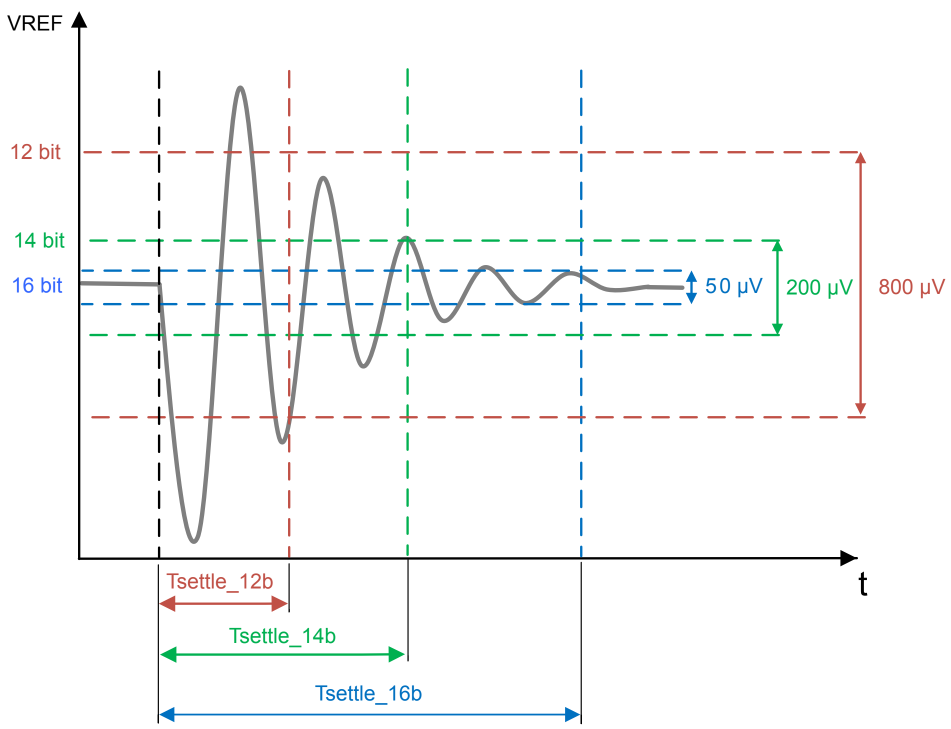
3.1 Resolution impact

Higher resolutions put more constraints on the voltage reference settling time because when the ADC resolution increases, VREF needs to settle to a lower voltage level.

Figure 6 shows the time required for VREF to settle to +/-0.5 LSB of the final value for different resolutions.

For 16-bit mode resolution, VREF needs to settle to +/-25 µV of the final value and therefore needs more time to settle than lower resolutions. This causes the maximum frequency to decrease with increasing resolutions.

Figure 6. Voltage reference settling time for different resolutions



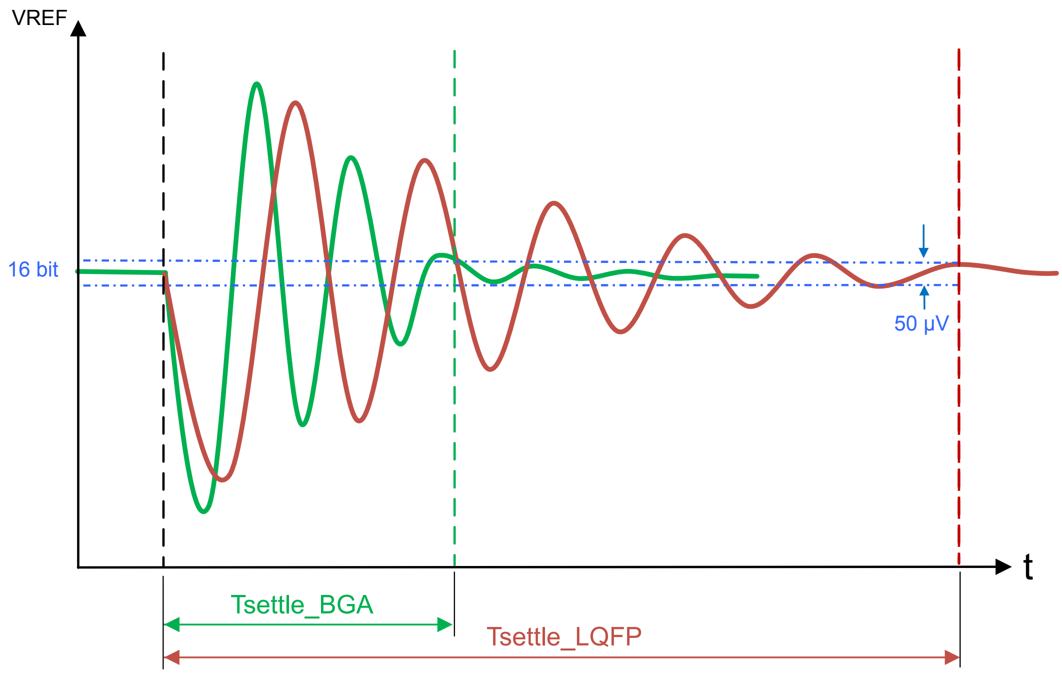
3.2 Package impact

The reference voltage settling time can be degraded by the inductance of the package bonding. The package adds a parasitic inductance on the VREF pin, increasing the VREF settling time. This limits the maximum achievable ADC frequency.

Hence the choice of package is crucial for ADC performance and must be considered at an early stage of the design. BGA packages generally perform better in this respect than LQFP packages, since they have a lower package pin inductance.

Figure 7 gives a generic indication of how the package influences the VREF recovery time.

Figure 7. Voltage reference settling time in 16-bit mode versus package



3.3 Number of ADCs

When multiple ADCs convert simultaneously, the transient currents on the VREF pin increase causing the VREF settling time to increase. This degrades the maximum ADC frequency.

3.4 Maximum ADC frequency

Based on the parameters presented previously which affect the VREF settling time, maximum ADC frequency can be defined to ensure the VREF is correctly settled during bit evaluation and hence guarantee an ADC transfer function with no missing codes.

Table 12 provides maximum ADC frequency in MHz for each package, resolution and number of overlapping ADCs under typical conditions.

Table 12. Maximum ADC frequency versus package type (VREF=VDDA=3 V, T=25°C)

Number of ADCs	Resolution	BGA100	BGA169	BGA176	BGA240	LQFP100	LQFP144	LQFP176	LQFP208
1	8	50	50	50	50	50	50	50	50
	10	50	50	50	47	47	36	32	39
	12	50	50	50	38	38	29	20	19
	14	49	49	49	31	24	16	15	15
	16	33	38	39	25	19	12	10	10
2	8	50	50	50	50	50	50	48	50
	10	50	50	50	43	38	31	28	25
	12	50	50	50	34	35	17	16	15
	14	40	49	49	29	21	15	12	13
	16	26	37	38	22	19	10	7	10
3	8	50	50	50	50	50	38	33	50
	10	50	50	50	42	38	30	28	20
	12	50	50	50	34	25	16	15	15
	14	32	49	49	25	20	12	10	12
	16	25	35	37	19	18	7	7	7

4 Maximum data rate

This section provides further details of the ADC performance including maximum data rates across packages, resolutions, number of ovelapping ADC conversions, and the channel type. This allows the user to select the best package to achieve the targeted performance.

The defined maximum sampling rate takes into account the maximum ADC frequency defined in Section 3 Maximum ADC frequency across resolutions, packages and number of ADCs to guarantee no missing codes.

The data presented in this section is only valid for revision V silicon, and is based on simulations in typical conditions: temperature = 25°C, VDDA = VREF = 3 V.

4.1 Single ADC operation

In 16-bit mode, the STM32H7 can reach sampling rates as high as 3.6 Msamples/s using a UFBGA176 package. Performance is degraded with an LQFP package, but stays in the order of 1.9 Msamples/s for LQFP100 package, and 1 Msamples/s for an LQFP208 package.

In 14-bit mode, sampling rates up to 5 Msamples/s can be reached.

Applications requiring low resolution and a high sampling rate can benefit from low resolution modes such as the 8-bit mode, which can reach 8.33 Msamples/s.

In 12-bit mode sampling rates can reach up to 5.6 Msamples/s.

Table 13 shows the maximum data rate (in Msamples/s) for BGA packages.

Table 13. Maximum data rate (Msamples/s) versus resolution for BGA packages - single ADC operation

Resolution	TFBGA100		UFBGA169		UFBGA176		TFBGA240	
	Direct	Fast	Direct	Fast	Direct	Fast	Direct	Fast
8	8.33	7.14	8.33	7.14	8.33	7.14	8.33	7.14
10	7.14	6.25	7.14	6.25	7.14	6.25	7.14	6.25
12	5.63	4.67	5.63	4.67	5.63	4.67	5.13	4.56
14	5	3.6	5	3.6	5	3.6	3.44	3.1
16	3.3	2.73	3.5	2.73	3.6	2.73	2.5	2.27

Table 14 presents maximum data rates in Msamples/s for LQFP packages.

Table 14. Maximum data rate (Msamples/s) versus resolution for LQFP packages - single ADC operation

Resolution	LQFP100		LQFP144		LQFP176		LQFP208	
	Direct	Fast	Direct	Fast	Direct	Fast	Direct	Fast
8	8.33	7.14	8.33	7.14	8.33	7.14	8.33	7.14
10	7.14	6.25	5.14	4.86	4.57	4.57	5.57	4.88
12	4.88	4.33	3.63	3.5	2.5	2.5	2.38	2.38
14	2.67	2.67	1.78	1.78	1.67	1.67	1.67	1.67
16	1.9	1.9	1.2	1.2	1	1	1	1

4.2 Dual ADC operation

A slight degradation in performance is observed when 2 ADC conversions overlap. There is almost no degradation on UFBGA176 and UFBGA169 packages. Degradation is more visible on large LQFP packages.

In 16-bit mode, UFBGA176 the sampling rate can reach up to 3.5 Msamples/s per ADC, meaning that system throughput using 2 ADCs can reach 7 Msamples/s. The user can also convert one channel using dual-interleaved mode with a sampling rate of 7 Msamples/s.

In 14-bit mode, data rates can reach 10Msamples/s on direct channels in dual-interleaved mode.

Table 15 presents maximum data rate in MSPS for BGA packages when two ADCs are converting.

Table 15. Maximum data rate (Msamples/s) versus resolution for BGA packages - double ADC operation

Resolution	TFBGA100		UFBGA169		UFBGA176		TFBGA240	
	Direct	Fast	Direct	Fast	Direct	Fast	Direct	Fast
8	8.33	7.14	8.33	7.14	8.33	7.14	8.33	7.14
10	7.14	6.25	7.14	6.25	7.14	6.25	6.29	5.5
12	5.63	4.67	5.63	4.67	5.63	4.67	4.38	3.89
14	4.44	3.6	5	3.6	5	3.6	3.22	2.9
16	2.6	2.36	3.5	2.73	3.5	2.73	2.2	2

Table 16 presents maximum data rate in MSPS for LQFP packages when two ADCs are converting.

Table 16. Maximum data rate (Msamples/s) versus resolution for LQFP packages - double ADC operation

Resolution	LQFP100		LQFP144		LQFP176		LQFP208	
	Direct	Fast	Direct	Fast	Direct	Fast	Direct	Fast
8	8.33	7.14	8.33	7.14	8	7	8.33	7.14
10	5.86	5.13	4.57	4.57	4.29	4.29	3.57	3.57
12	4.38	3.89	2.13	2.13	2	2	1.88	1.88
14	2.33	2.33	1.67	1.67	1.33	1.33	1.44	1.44
16	1.8	1.8	1	1	0.7	0.7	0.9	0.9

4.3 Triple ADC operation

This section presents maximum data rates when 3 ADCs conversions overlap.

- in 16-bit mode, system throughput can reach up to 10.5 Msamples/s on UFBGA176 and UFBGA169 packages
- in 14-bit mode, system throughput can reach up to 15 Msamples/s.

Table 17 presents maximum data rate in Msamples/s for BGA packages when three ADCs are converting.

Table 17. Maximum data rate (Msamples/s) versus resolution for BGA packages - triple ADC operation

Resolution	TFBGA100		UFBGA169		UFBGA 176		TFBGA240	
	Direct	Fast	Direct	Fast	Direct	Fast	Direct	Fast
8	8.33	7.14	8.33	7.14	8.33	7.14	8.33	7.14
10	7.14	6.25	7.14	6.25	7.14	6.25	6	5.25
12	5.63	4.67	5.63	4.67	5.63	4.67	4.25	3.78
14	3.89	3.5	5	3.6	5	3.6	2.89	2.67
16	2.5	2.27	3.5	2.73	3.5	2.73	1.9	1.9

Table 18 presents maximum data rate in MSPS for LQFP packages when three ADCs are converting.

Table 18. Maximum data rate (Msamples/s) versus resolution for LQFP packages - triple ADC operation

Resolution	LQFP100		LQFP144		LQFP176		LQFP208	
	Direct	Fast	Direct	Fast	Direct	Fast	Direct	Fast
8	8.33	7.14	6.33	6.33	5.5	5.5	8.33	7.14
10	5.57	4.88	4.29	4.29	4	4	2.86	2.86
12	3.13	3.13	2	2	1.88	1.88	1.88	1.88
14	2.22	2.22	1.33	1.33	1.11	1.11	1.33	1.33
16	1.8	1.8	0.7	0.7	0.7	0.7	0.7	0.7

5 STM32H7 ADC parameters across resolutions

STM32H7 supports several resolutions providing flexible configuration depending on the required precision and power budget. This section provides typical ADC static and dynamic parameters for 14-, 12-, 10-, and 8-bit resolutions.

The measurement conditions are T = 25°C, VDDA/VREF = 3.3 V.

Note: 14-bit and 12-bit resolutions each have two modes: standard mode and optimized mode.

The optimized modes have better power consumption figures. The standard modes have better parameters, but power consumption is not optimized and is comparable to 16-bit mode. The optimized modes are only available in revision V.

For power consumption figures for different resolutions, refer to the applicable STM32H7 datasheet [2].

Note: For static parameters listed below, gain error and offset error can be improved, with longer sampling times.

5.1 14-bit mode

This section presents the ADC static and dynamic parameters in 14-bit mode.

5.1.1 Static parameters

Table 19 shows the STM32H7 ADC static parameters for 14-bit optimized and standard modes.

Table 19. STM32H7 ADC static parameters in 14-bit mode

Symbol	Input signal mode(1)	Typical value
TUE (LSB)	SE	+/-2.5
	DIFF	+/-2
OE (LSB)	SE and DIFF	+/-3
GE (LSB)	SE and DIFF	+/-3
DNL (LSB)	SE	+/-0.8
	DIFF	+/-0.5
INL (LSB)	SE	+/-2.5
	DIFF	+/-1.5

1. *Conditions: fast channel, Fadc = 30 MHz, Ts = 2.5 cycles.*

5.1.2 Dynamic parameters

Table 20 presents the STM32H7 ADC dynamic parameters in 14-bit optimized mode.

Table 20. STM32H7 ADC dynamic parameters in 14-bit optimzed mode @ 3.4 Msps

Symbol	Input signal mode (1)	Typical value
ENOB (bits)	SE	11.76
	DIFF	12.48
SNR (dBc)	SE	72.7
	DIFF	77.48
THD (dBc)	SE	-90
	DIFF	-91

1. *Conditions: direct channel, Fadc = 31 MHz, Ts = 1.5 cycles.*

Table 21 presents the STM32H7 ADC dynamic parameters in 14-bit standard mode.

Table 21. STM32H7 ADC dynamic parameters in 14-bit standard mode @3.4 Msps

Symbol	Input signal mode [1]	Typical value
ENOB (bits)	SE	12.56
	DIFF	13.24
SNR (dBc)	SE	77.49
	DIFF	81.5
THD (dBc)	SE	-94
	DIFF	-102

1. *Conditions: direct channel, Fadc = 31 MHz, Ts = 1.5 cycles.*

5.2 12-bit mode

This section presents the ADC static and dynamic parameters in 12-bit mode.

5.2.1 Static parameters

Table 22 shows the STM32H7 ADC static parameters for 12-bit optimized and standard modes.

Table 22. STM32H7 ADC static parameters in 12-bit mode

Symbol	Input signal mode[1]	Typical value
TUE (LSB)	SE	+/-3.5
	DIFF	+/-2.5
OE (LSB)	SE	+/-0.5
	DIFF	+/-1.5
GE (LSB)	SE	+/-3.1
	DIFF	+/-3.6
DNL (LSB)	SE and DIFF	+/-0.5
INL (LSB)	SE and DIFF	+/-0.5

1. *Conditions: fast channel, Fadc = 40 MHz, Ts = 2.5 cycles.*

5.2.2 Dynamic parameters

Table 23 presents the STM32H7 ADC dynamic parameters in 12-bit optimized mode.

Table 23. STM32H7 ADC dynamic parameters in 12-bit optimized mode @ 5 Msps

Symbol	Input signal mode[1]	Typical value
ENOB (bits)	SE	11.19
	DIFF	11.65
SNR (dBc)	SE	69.23
	DIFF	72
THD (dBc)	SE	-85.7
	DIFF	-88

1. *Conditions: direct channel, Fadc = 40 MHz, Ts = 1.5 cycles.*

Table 24 presents the STM32H7 ADC dynamic parameters in 12-bit standard mode.

Table 24. STM32H7 ADC dynamic parameters in 12-bit standard mode @5 Msps

Symbol	Input signal mode(1)	Typical value
ENOB (bits)	SE	11.58
	DIFF	11.84
SNR (dBc)	SE	71.7
	DIFF	73.05
THD (dBc)	SE	-85
	DIFF	-96

1. *Conditions: direct channel, Fadc = 40 MHz, Ts = 1.5 cycles.*

5.3 10-bit mode

This section presents the ADC static and dynamic parameters in 10-bit mode.

5.3.1 Static parameters

Table 25 shows the STM32H7 ADC static parameters in 10-bit mode

Table 25. STM32H7 ADC static parameters in 10-bit mode

Symbol	Typical value(1)
TUE (LSB)	+/-2
OE (LSB)	+/-0.5
GE (LSB)	+/-1.5
DNL (LSB)	+/-0.2
INL (LSB)	+/-0.2

1. *Conditions: fast channel, Fadc= 45 MHz, Ts = 2.5cycles, VDDA = 3.3 V.*

5.3.2 Dynamic parameters

Table 26 presents the STM32H7 ADC dynamic parameters in 10-bit mode.

Table 26. STM32H7 ADC dynamic parameters in 10-bit mode @ 7.14 Msps

Symbol	Input signal mode(1)	Typical value
ENOB (bits)	SE	9.78
	DIFF	9.89
SNR (dBc)	SE	60.7
	DIFF	61.33
THD (dBc)	SE	-81
	DIFF	-90

1. *Conditions: direct channel, FADC = 50 MHz, Ts = 1.5 cycles, VDDA = 3.3 V.*

5.4 8-bit mode

This section presents the ADC static and dynamic parameters in 8-bit mode.

5.4.1 Static parameters

Table 27 presents static parameters of STM32H7 in 8-bit mode

Table 27. STM32H7 ADC static parameters in 8-bit mode

Symbol	Typical value(1)
TUE (LSB)	+/-1
OE (LSB)	+/-0.5
GE (LSB)	+/-0.4
DNL (LSB)	+0.1
INL (LSB)	+/-0.5

1. *Conditions: fast channel, Fadc = 50 MHz, Ts = 2.5 cycles, VDDA = 3.3 V.*

5.4.2 Dynamic parameters

Table 28 presents the STM32H7 ADC dynamic parameters in 8-bit mode.

Table 28. STM32H7 ADC dynamic parameters in 8-bit mode @ 8.3 Msps

Symbol	Input signal mode(1)	Typical value
ENOB (bits)	SE	7.9
	DIFF	7.93
SNR (dBc)	SE	49.38
	DIFF	49.53
THD (dBc)	SE	-80
	DIFF	-83

1. *Conditions: direct channel, Fadc = 50 MHz, Ts = 1.5 cycles.*

6 PCB design considerations

6.1 Board partitioning

For a mixed-signal board, component placement and partitioning are critical to good layout.

Separating analog and digital sections is recommended, so that noisy digital signals do not interfere with sensitive analog parts.

The digital signals and their corresponding return current paths must remain in the digital section of the board, and must not interfere with analog signals.

6.2 Ground plane

Use of a single, solid, ground plane common to analog and digital sections is recommended. The ground plane must have a very low impedance. Cuts into the ground plane must be minimized to avoid return current path diversion.

The VSS/VSSA/VREF- MCU pins must be connected to the ground plane with shortest distance possible.

6.3 ADC input

6.3.1 ADC input filter

Placing a capacitor very close to the ADC input pin is recommended (47 pF is a good starting point). This capacitor acts as a charge reservoir to respond quickly to the high dynamic current demand when the sampling switch is closed. This capacitor ensures a good settling time of the sampling capacitor to the desired input voltage level.

It is possible to increase the value of the input capacitor when, for instance, the voltage source impedance is not low enough. The user can add a series resistor for anti-aliasing or low-pass filtering. The value depends on the application, however the sampling time must be adjusted accordingly.

6.3.2 ADC input routing

The ADC voltage source must be placed close to the MCU, and the ADC input tracks must be kept as straight and as short as possible. They must have a ground plane on an adjacent layer.

Adding ground shielding around ADC traces is also recommended, with sufficient vias between the shielding and the ground plane.

6.4 Voltage reference

The SAR ADC principle is based on the comparison of an input voltage to fractions of a reference voltage. The voltage reference therfore has a direct impact on the accuracy of the results.

Connecting the VREF pin to a low offset, low drift, and low-noise voltage source is recommended. The reference voltage must have a low impedance and sufficient bandwidth to respond to the transient current demand of the ADC.

6.5 Decoupling capacitors

A pair of decoupling capacitors should be added between VDDA/VSSA and VREF+/VREF- :

- a 1 µF X7R dielectric ceramic capacitor in 0603 or 0402 package
- a 10 nF X7R dielectric ceramic capacitor in 0402 package

These capacitors must be placed very close to the MCU and connected directly to a ground plane.

Each VDD/VSS power supply pair should be decoupled with ceramic filtering capacitors (100 nF), and a single ceramic capacitor (minimum 4.7 µF) connected in parallel.

These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB.

7 Conclusion

The main conclusions of this application note are lised below:

- The STM32H7 series 16-bit ADC provides high accuracy with no missing codes at high data rates
- The maximum sampling rate per channel is 3.6 Msamples/s, and 7 Msamples/s in Dual-interleaved mode
- System throughput reaches 10.5 M Msamples/s using 3 ADCs
- The ADC precision can be improved to reach more than 15 bits by use of the hardware oversampler
- Following the package selection and hardware guidelines is essential in order to attain the best performance figures.

Revision history

Table 29. **Document revision history**

Date	Version	Changes
19-Mar-2020	1	Initial version.

Contents

List of tables

List of figures